Evaluation and simulation of High Voltage-CMOS chips for high radiation environments

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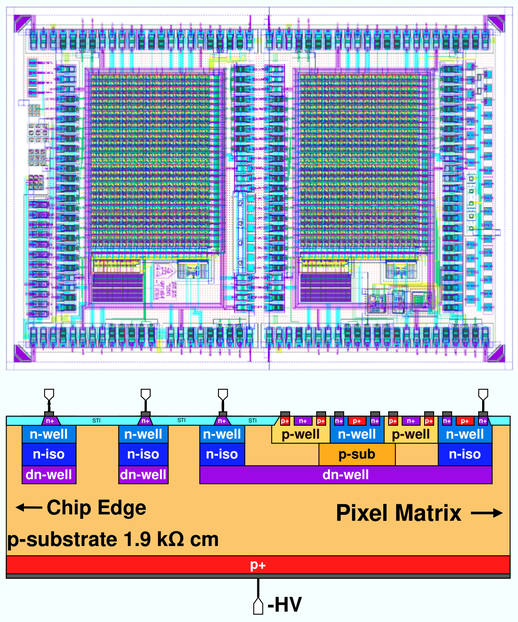
As collider experiments probe to higher energies the radiation tolerance, granularity and timing of silicon trackers is going to have to improve far beyond the high demands already placed on the technology. High Voltage-CMOS is shaping up to be an excellent candidate for the next generation of trackers. The high substrate biasing voltages makes the technology radiation tolerant, where as the Integrated Circuitry (IC) means the sensors can achieve a smaller pixel granularity with reduced material budget, all while being an industrial manufacturing process. Combining the benefits of both Hybrids and conventional CMOS technology. Although it is building steam in the community, further development is needed to reach targets put forth by experiments such as the High Luminosity-LHC (HL-LHC).

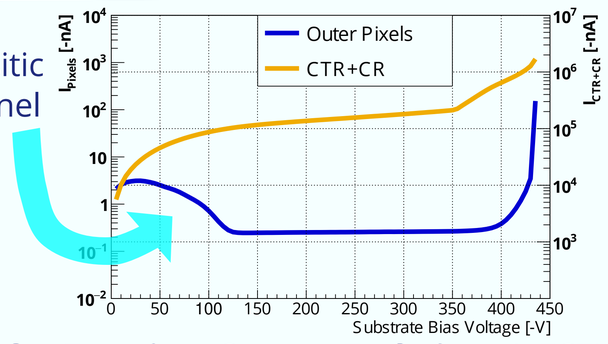


UKRI-MPW0

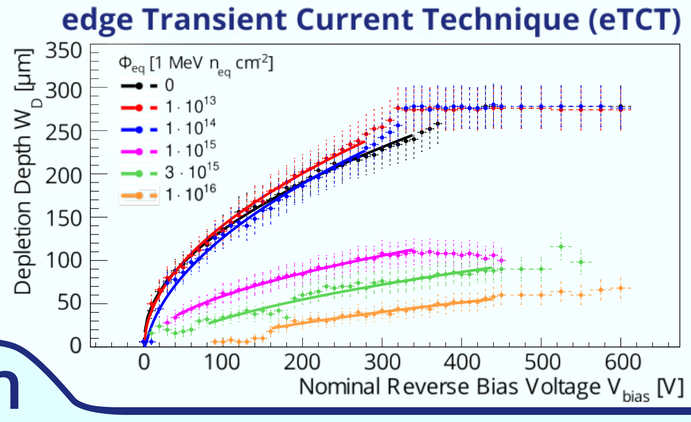
5.0 x 3.5 mm^2 -
280 µm thickness -
Backside biased -
P-type substrate -
1.9 kΩ cm nominal resistivity **-**
Current Terminating Scheme -
(CTS) ring structure
2 Active matrices **-**
60 x 60 µm^2 Pixel Pitch **-**
3 sets of passive test pixels **-**
(one for eTCT)
No topside p-wells -
[1]

MPW0 is a chip designed to prove backside biasing as a radiation tolerant scheme. The chip achieves a high breakdown voltage, but has a 4 mA leakage current at breakdown. Also, a parasitic transistor channel forms between pixels due to charge on the Shallow Trench Isolation (STI). However, the chip can reach a 50 µm depletion after neutron fluences of 1 x10^{16} 1 MeV n_{eq} cm^{-2} [2].

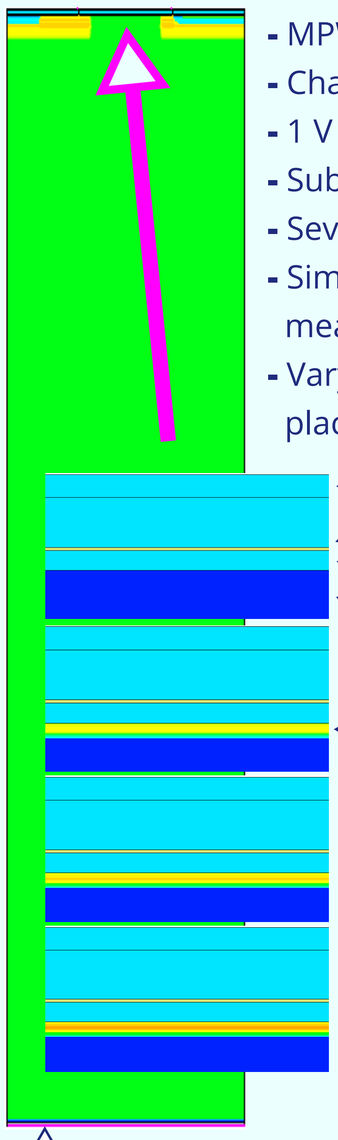
Current-Voltage (IV)



edge Transient Current Technique (eTCT)



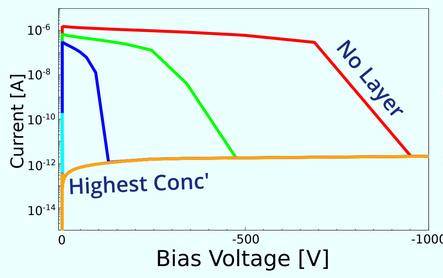
Channel Leakage



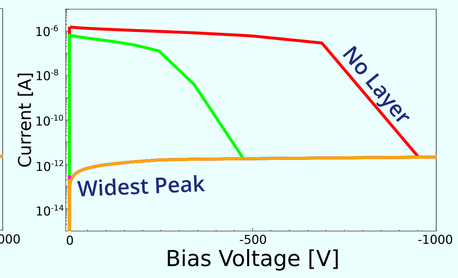
- MPW0 inter-pixel Cross-section generated
- Charge placed on the STI/silicon Interface (STI/Si)
- 1 V potential placed between pixels to simulate the channel
- Substrate Biased transiently until the channel closes
- Several STI/Si charges trialled
- Simulation matched to measurements (Overestimated)
- Varying p-profiles placed along STI/Si interface

By increasing the concentration of the p-layer, with the width and peak position fixed, the parasitic channel can be closed. The shallow layer has little effect on breakdown voltage of the chip (in simulation). Alternatively, concentration and depth can be fixed, and the width of the Gaussian varied. More effective at closing the channel, but results in a drastic reduction in breakdown.

Concentration

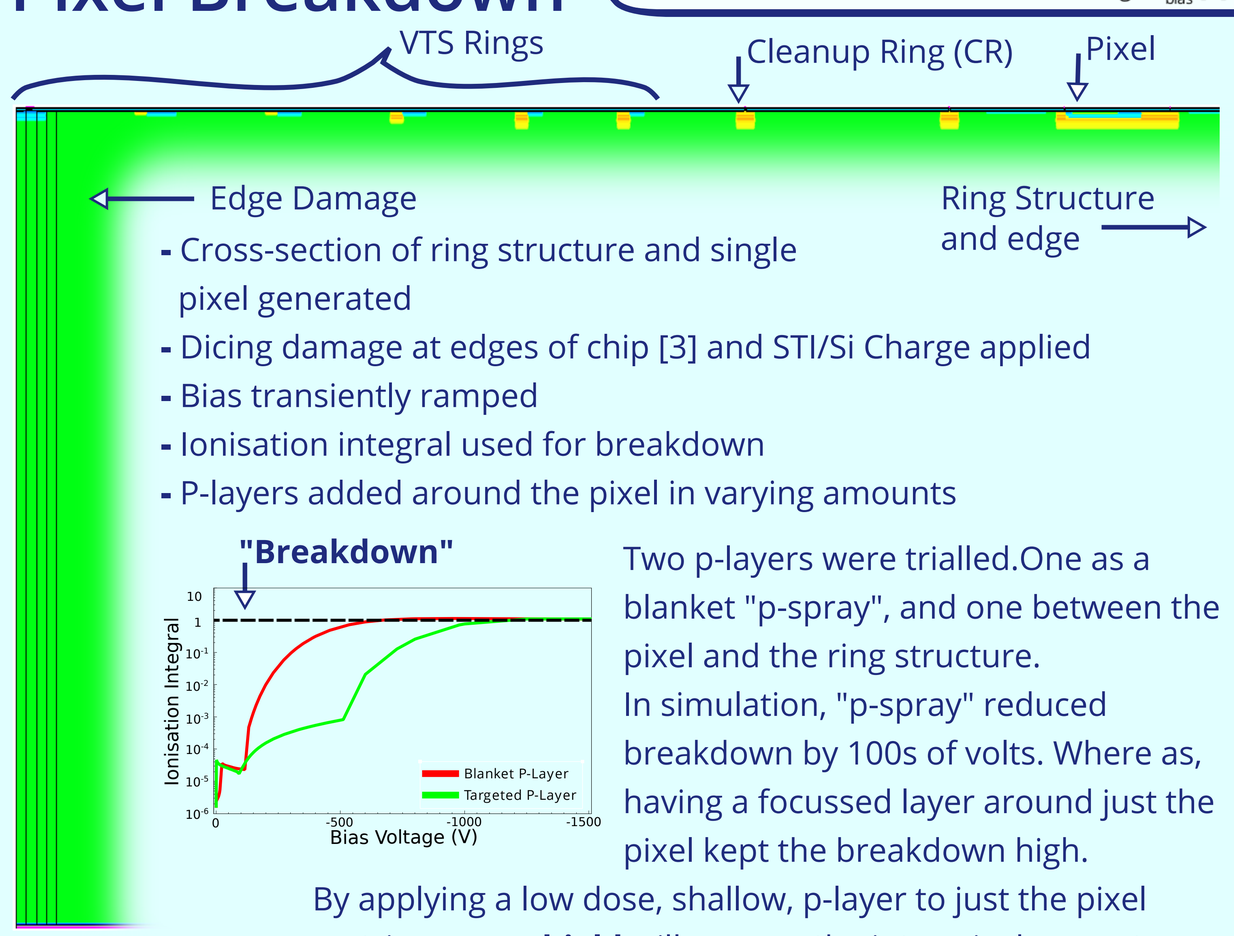


Peak Width



The parasitic channel becomes overexaggerated in the small pixel to pixel simulation. This is due to a number of factors, but the principle is correct.

Pixel Breakdown



- Cross-section of ring structure and single pixel generated
- Dicing damage at edges of chip [3] and STI/Si Charge applied
- Bias transiently ramped
- Ionisation integral used for breakdown
- P-layers added around the pixel in varying amounts

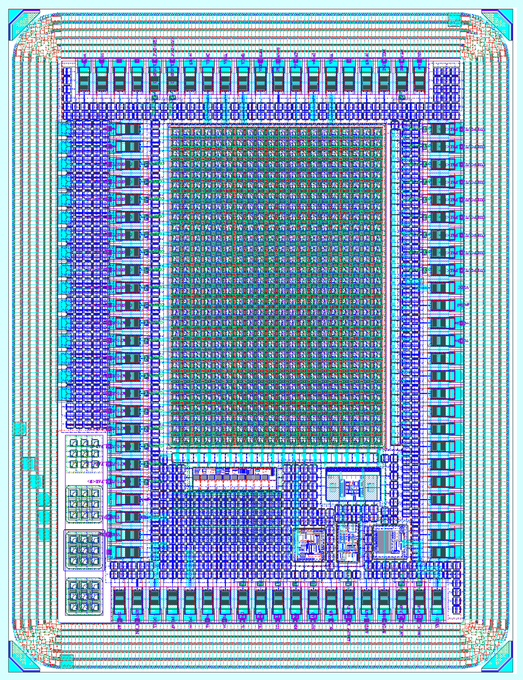
"Breakdown"

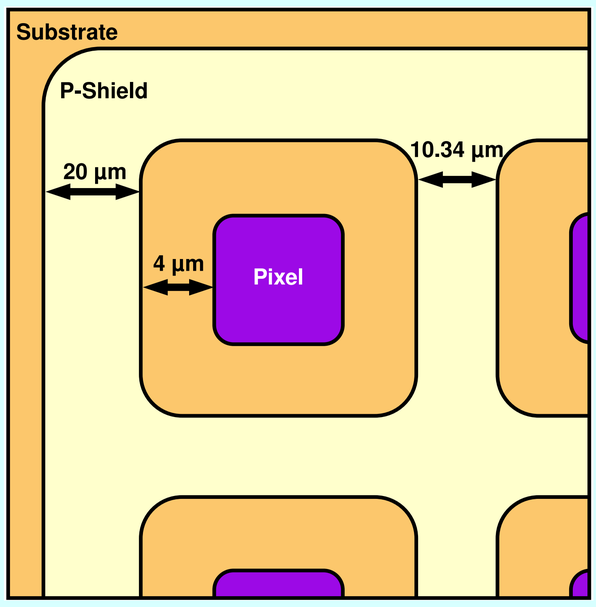
Two p-layers were trialled.One as a blanket "p-spray", and one between the pixel and the ring structure.
In simulation, "p-spray" reduced breakdown by 100s of volts. Where as, having a focussed layer around just the pixel kept the breakdown high.

By applying a low dose, shallow, p-layer to just the pixel matrix, as a **p-shield** will remove the inter-pixel current while maintaining a breakdown greater than 1000 V (in simulation).

UKRI-MPW1

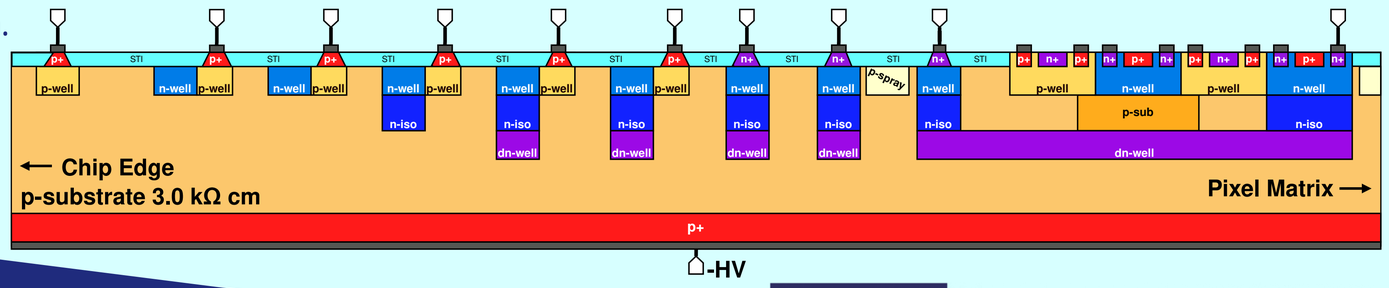
- 3.8 x 2.7 mm^2
- 280 µm thickness Backside biased
- P-type substrate
- 3.0 kΩ cm nominal resistivity
- Voltage Terminating Scheme (VTS)
- 1 Active matrix
- P-shield
- 60 x 60 µm^2 pixel pitch
- 1 sets of passive eTCT test pixels





MPW1 is the next iteration of the design. The **p-shield** designed with LFoundry seeks to correct the issues seen in the previous chip. The **p-shield** will be placed around and in-between the pixels and matrix to close any potential channels while maintaining the high breakdown voltage and radiation tolerance. The **p-shield** is a combination of concentration and peak methods, discussed above. There will be 3 different concentrations trialled on the chip to fine tune the design.

The chip will be delivered January 2024



References

[1] C. Zhang, et al., Design and evaluation of UKRI-MPW0: an HV-CMOS prototype for high radiation tolerance, Nucl. Instrum. Meth. A 1040 (2022) 167214.
[2] **B. Wade**, et al., Edge-tct evaluation of high voltage-cmos test structures with unprecedented breakdown voltage for high radiation tolerance, 2022, 23rd International Workshop on Radiation Imaging Detectors, (2022) JINST 17 C12017.
[3] E. Noschis, et al., Simulations of planar edgeless silicon detectors with a current terminating structure, Nucl. Instrum. Meth. A 574 (2007) 420.

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