First results from the ATLAS ITkPixV2 Readout Chip

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PSD13

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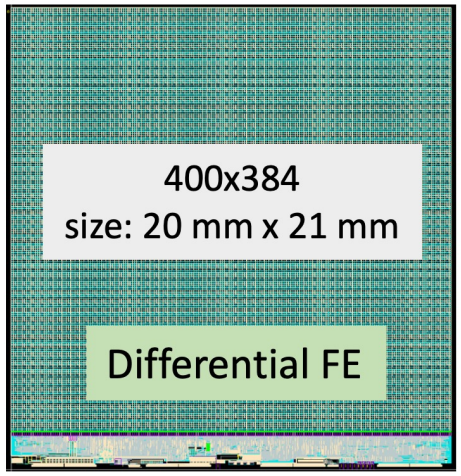
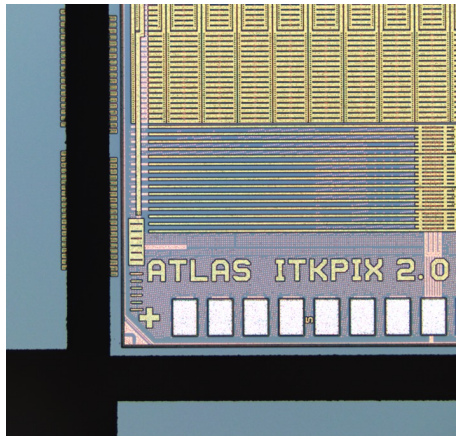
BERKELEY LAB

Introduction

ITkPixV2



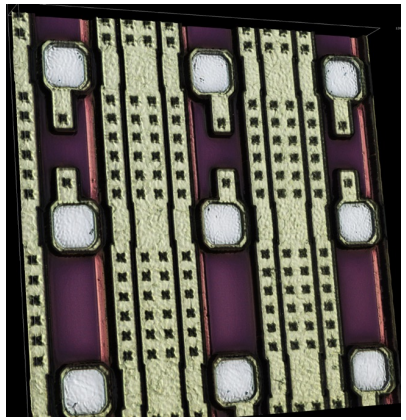


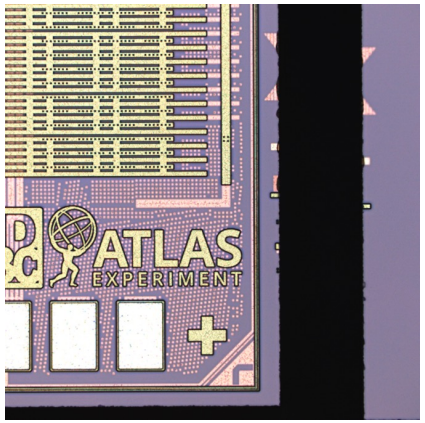
- Pixel chips for the HL-LHC upgrade for ATLAS and CMS have been jointly developed by the RD53 collaboration to cope with the harsh requirements for HL-LHC
- Result of ~10 years of ASIC development, with several intermediate chips
- **ATLAS ITkPixV2** chip submitted in April 2023 → expected to be the final production chip
- Many changes to improve:
  - Proper fix to the ToT memory bug in ITkPixV1
  - Stability against single-event transients
  - Startup and powering stability
  - Improvements and additional monitoring sensors for temperature and radiation
- Received back engineering run wafers → now running tests to validate the performance of the chip, before ordering the main batch of wafers

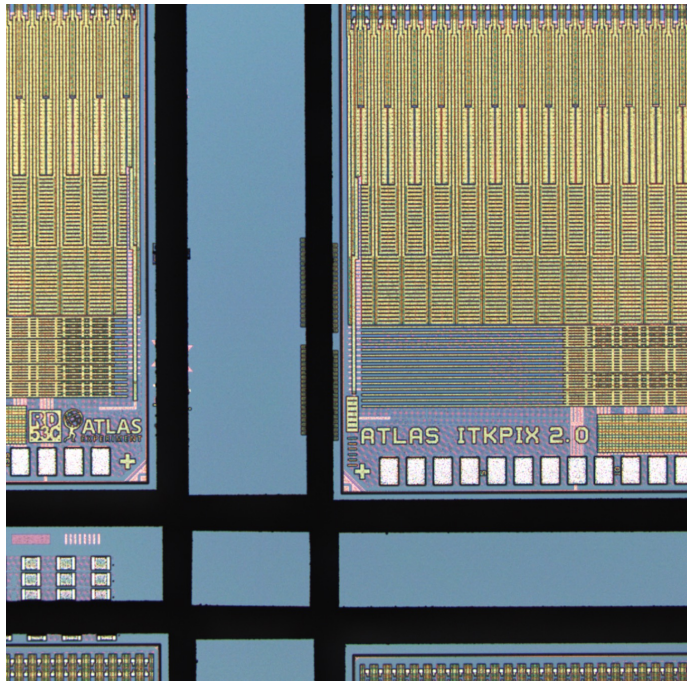
First Start-Up of ITkPixV2

- Received first ITkPixV2 **diced wafer** at the end of July 2023
- Diced chips look good as expected
- Assembled chips on single-chip testing boards (SCCs)
- First power-up was successful and chip currents are within 10% of expectation

Diced ITkPixV2 wafer







Assembled single chip testing board

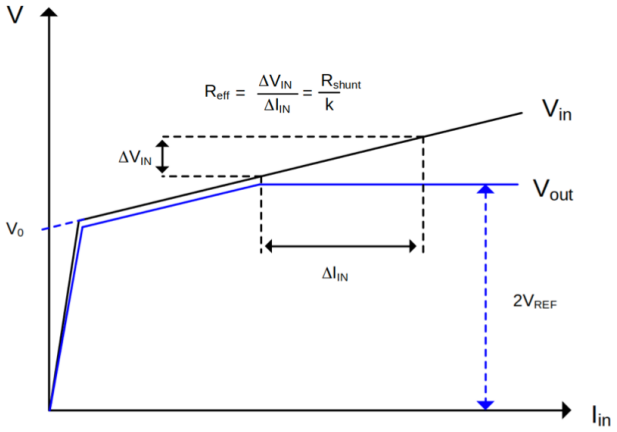
SLDO performance

- ITk modules will be operated in serial powering using a shunt-LDO circuit in the readout chip
- Use **SLDO start-up curves** to characterise chip start-up behaviour

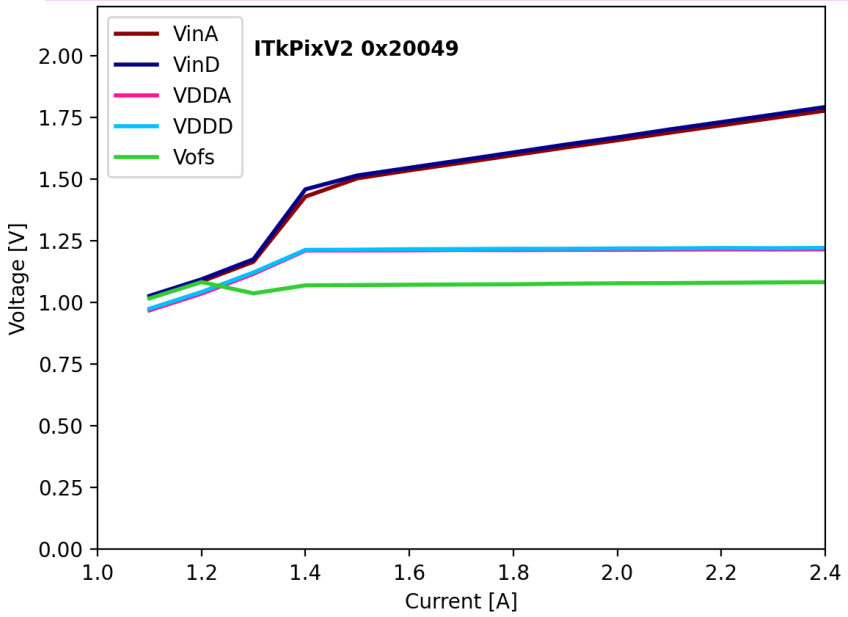
→ Results look as expected for ITkPixV2 and match what was observed for ITkPixV1

- No start-up issues observed down to temperatures of -50 C

Schematic of SLDO VI curve

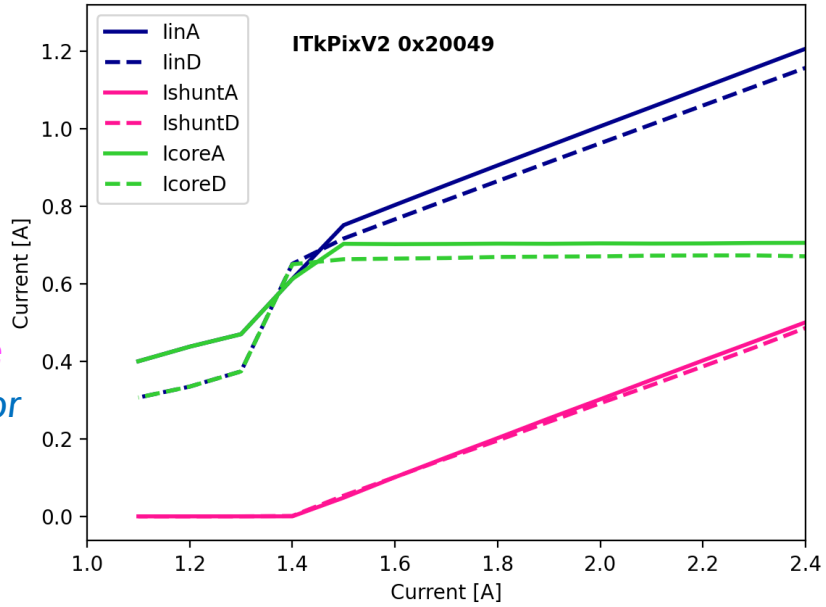


SLDO voltages



VinA – analog input voltage
VinA – digital input voltage
VDDA – analog regulator output voltage
VDDD – digital regulator output voltage
Vofs – offset voltage

SLDO currents



Iin – chip input current
Icore – current consumed by chip
Ishunt – current consumed shunt element

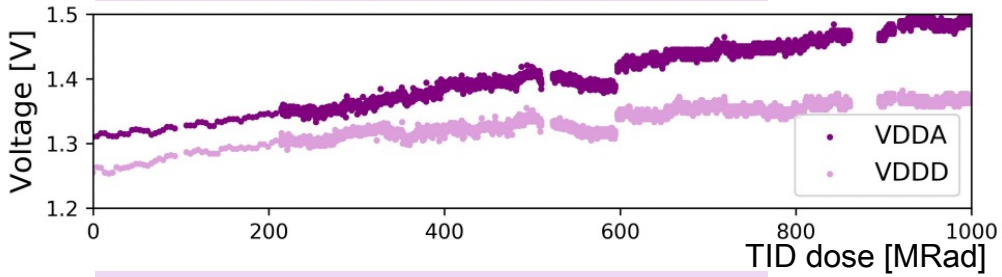
VDD voltages

- SLDO regulator output voltages supplied to analog (VDDA) and digital (VDDD) domain
- VDDA/VDDD voltage level can be controlled by chip configuration setting (”trim bits”)
- Operational setting should be **as close as possible to 1.2 V**
- Saw in irradiations of ITkPixV1 that **VDDA/VDDD voltage increases** due to change in bandgap voltages with irradiation
- VDDA increased significantly more than VDDD (+14% for VDDA, +9% for VDDD after 1 Grad)

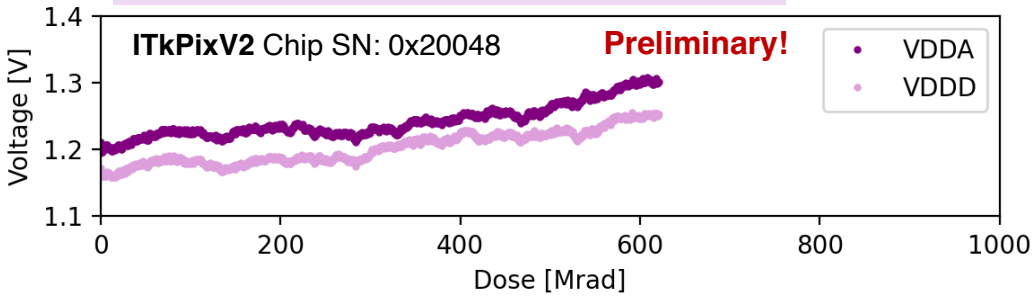
→ likely caused by increased mismatch of current mirrors caused by non-uniform chip metallisation layers

- Included two related modificiations in ITkPixV2 design:
  - More uniform metallisation layers → first irradiation results look promising
  - Larger trim bit size → Larger range of VDDA/VDDD possible, effect as expected

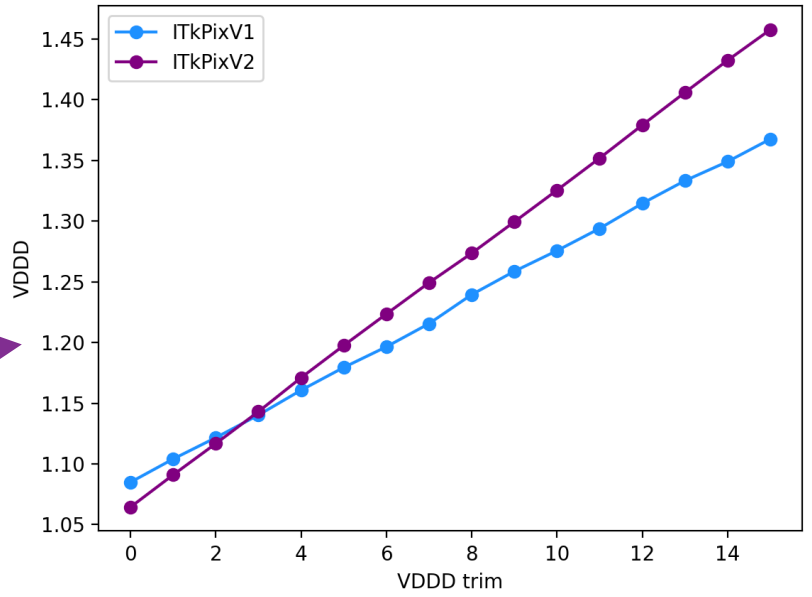
VDD with irradiation on ITkPixV1



VDD with irradiation on ITkPixV2



VDDD as a function of trim bit



Chip currents

- **Analog input current:** Preamplifier consumes most of the analog current

→ Verified linear behaviour with DAC

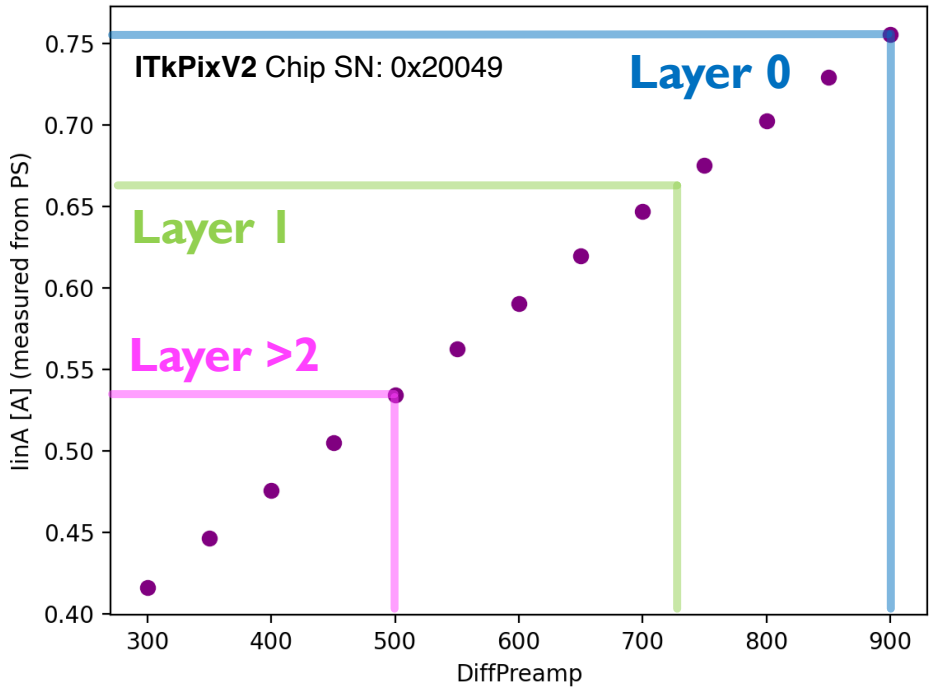
→ Different settings intended for different ITk detector layers

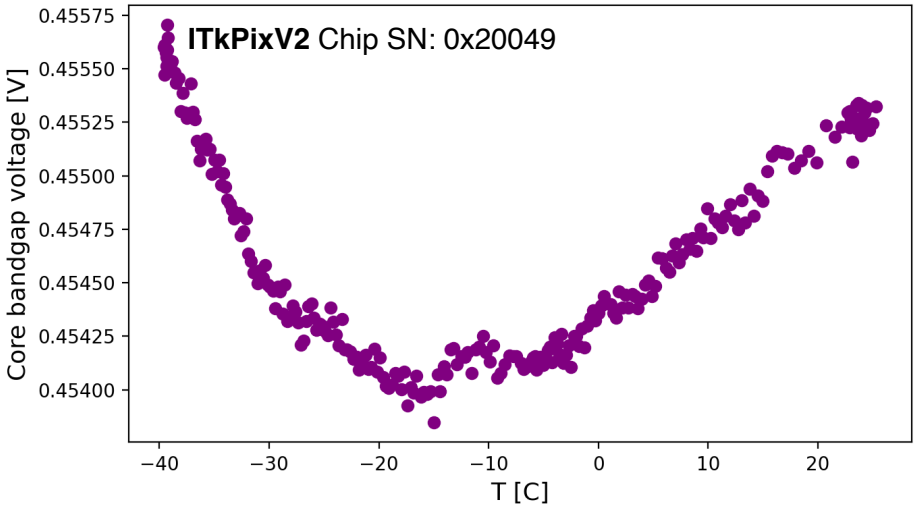
→ Lower values in the outer layers of the detector to reduce power consumption (at the expense of more noise & time-walk)

- **Bias network** based on bandgap reference circuits
- Generates reference voltage/currents for analog front-end etc
- Designed with low sensitivity to temperature variations (4% over a 70 °C) range

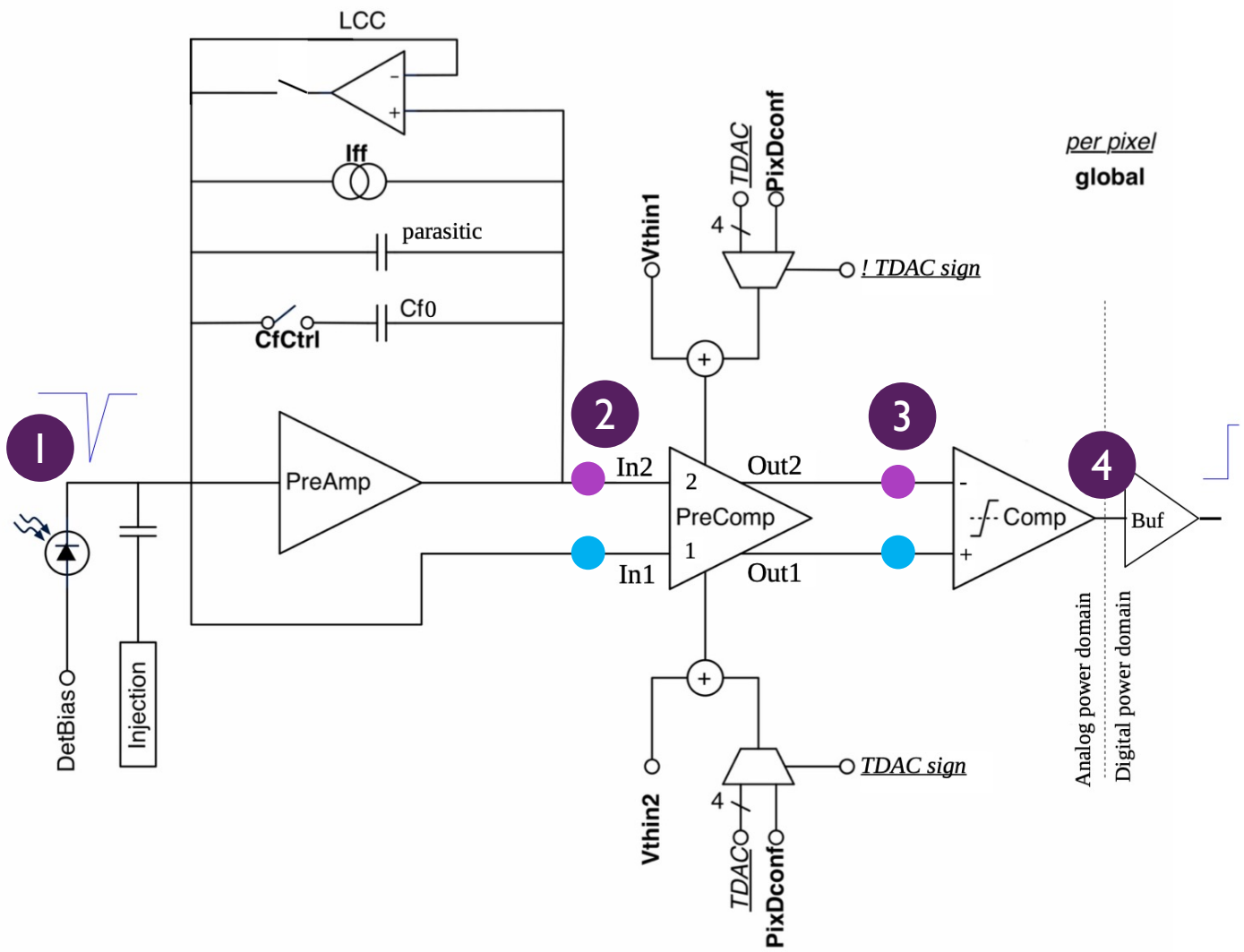
Temperature dependence of core bandgap voltage

Analog current vs preamplifier setting

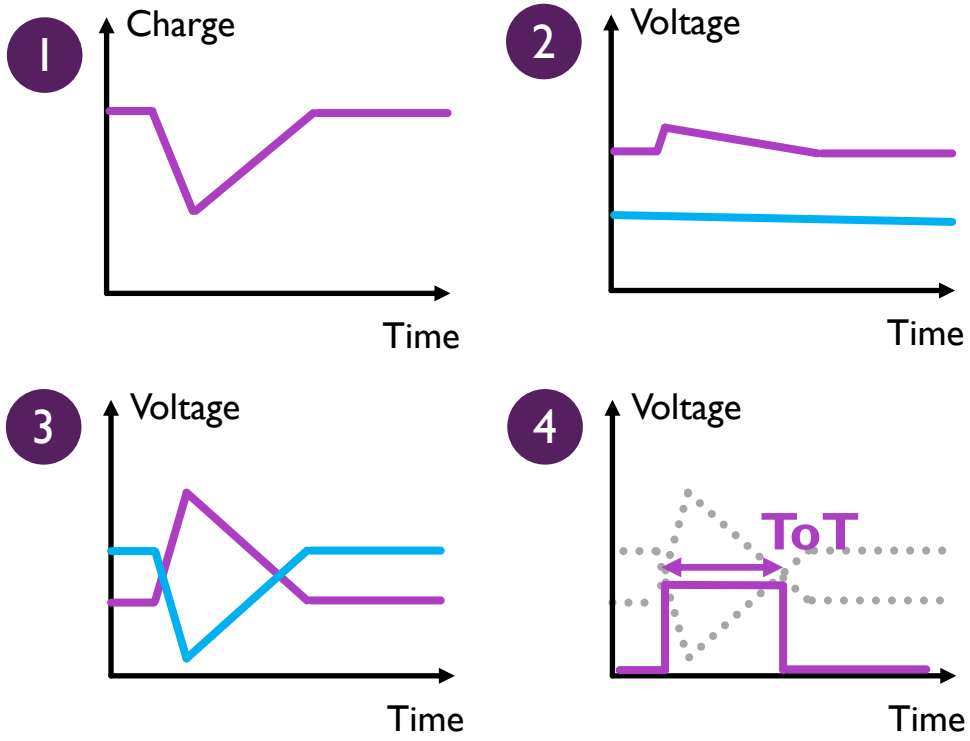




ITkPixV2 Differential Front-End



- ITkPixV2 uses a differential front-end to determine ToT information

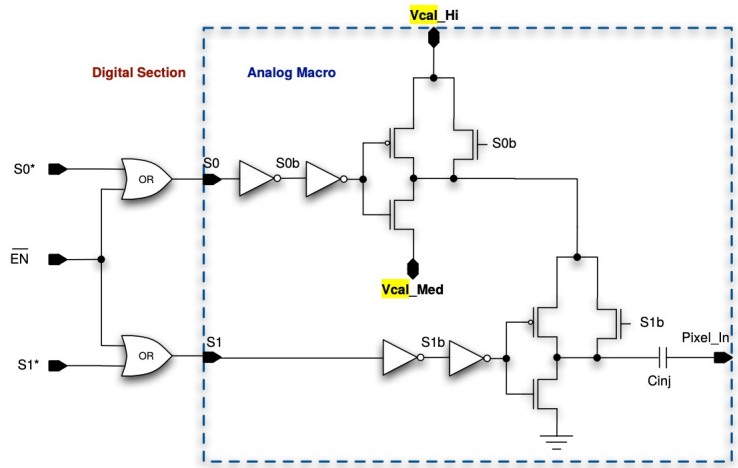


Injection calibrations

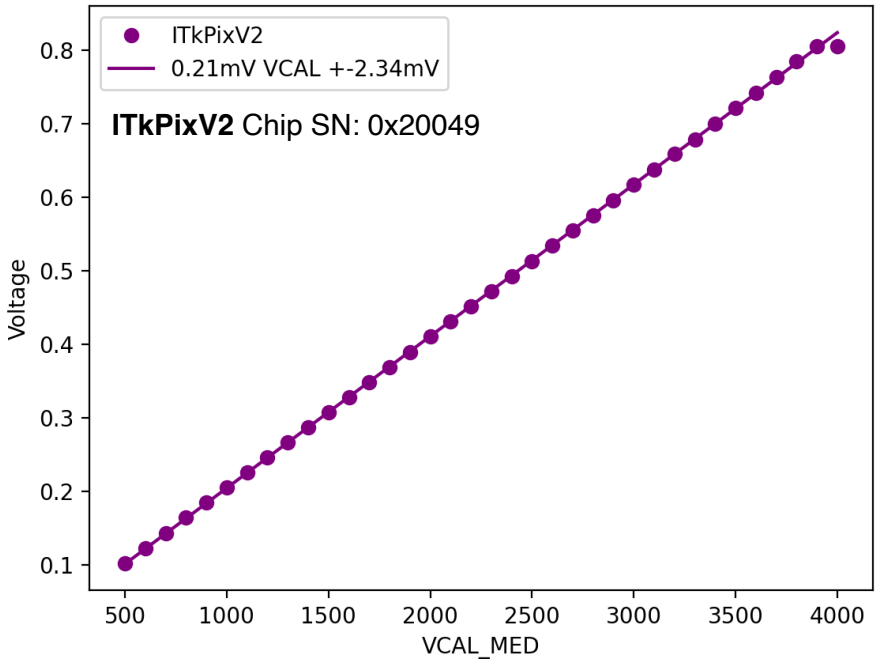
- Charge injection circuit implemented in each pixel for characterisation measurements
- Circuit needs to be calibrated to get conversion from DAC setting to voltage
- Slope measured to be **~0.2 mV/DAC, consistent with ITkPixV1**
- Charge injected using **injection capacitor**
- Injection capacitance can be measured precisely using dedicated circuit in the chip
- Observe injection capacitance of **7.7 fF**

→ Good agreement with expectations (design value 8 fF)

Charge injection circuit



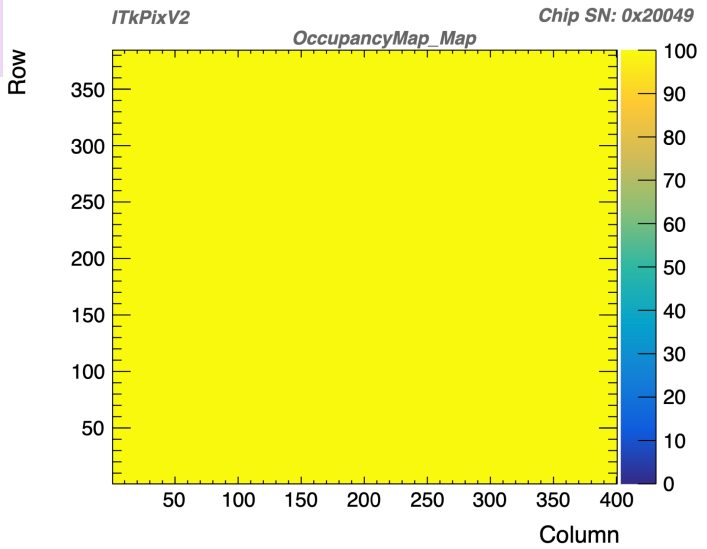
Injection circuit calibration

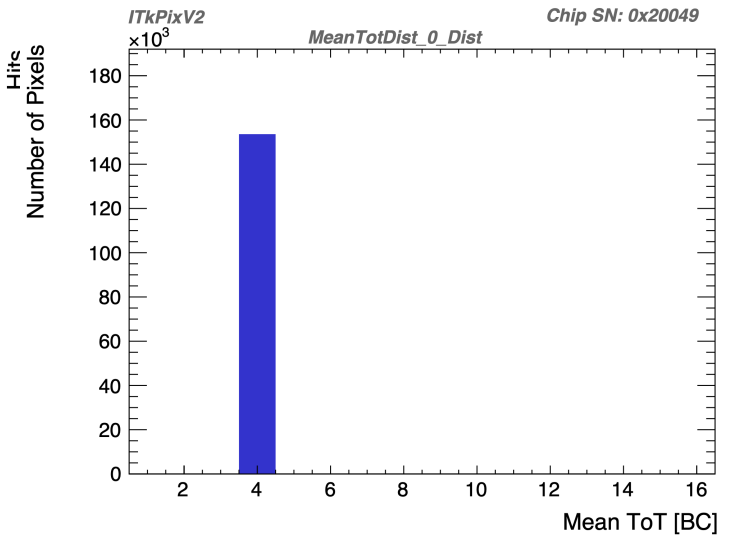


Digital and analog injection tests

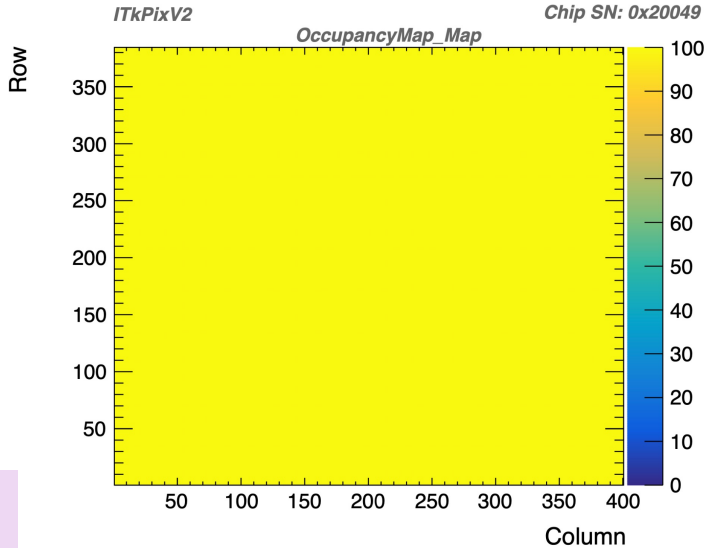
Digital scan

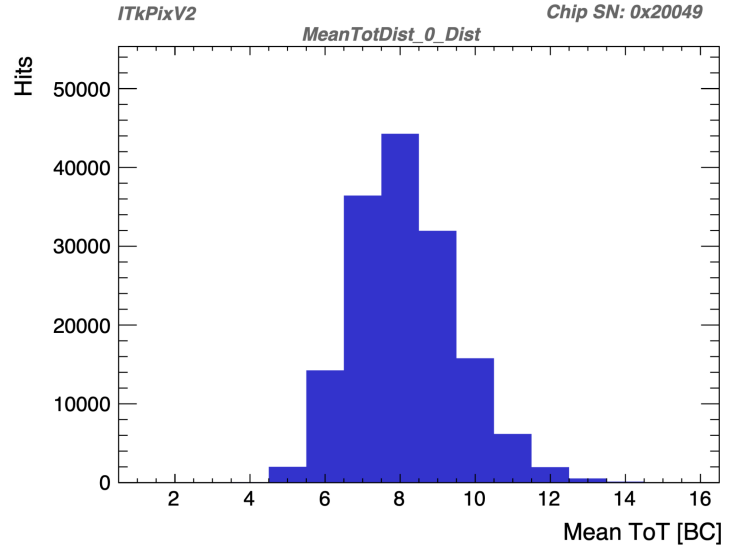
- Inject a charge a certain amount of times, and count how many of the injections each pixel sees
- **Digital injection tests:**
  - Using digital injections
  - Observe uniform map with observed number of hits matching the expected
  - Very narrow ToT distribution
- **Analog injection tests:**
  - Using analog injection circuit
  - Observe reasonable ToT distribution → **ToT works in ITkPixV2**



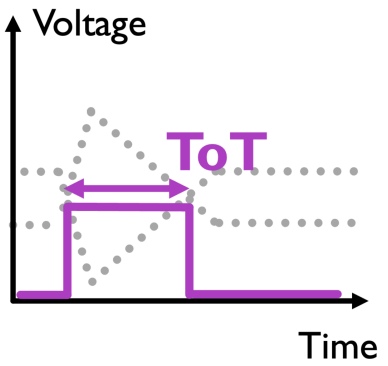


Analog scan





ToT modes in ITkPixV2



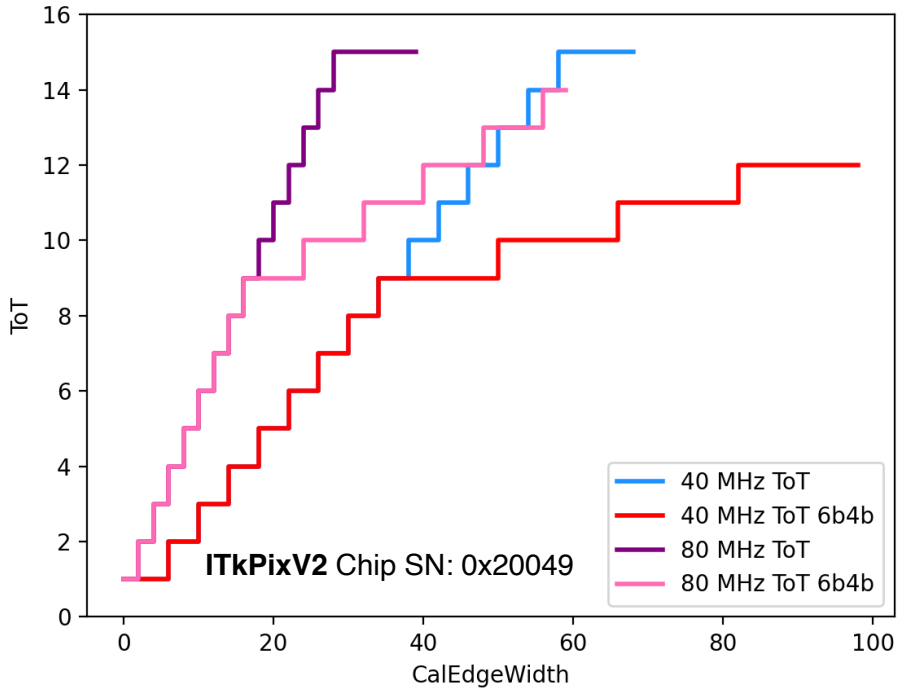
- Different time-over threshold (ToT) modes available in ITkPixV2
- Validate ToT value as a function of injection duration of digital injection
- **80 MHz ToT** has twice the slope of 40 MHz ToT, as expected

→ Additionally, bug fixed for 80MHz ToT which was observed in CMS CROC chip v1

- **6-to-4 bit ToT** available with increased step sizes at longer injections/higher charges

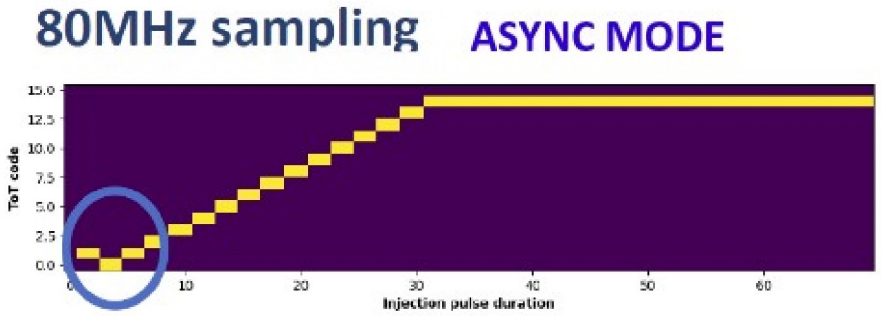
→ **All ToT modes verified to work in ITkPixV2**

Test of different ToT modes



(Injection duration in bunch crossings)

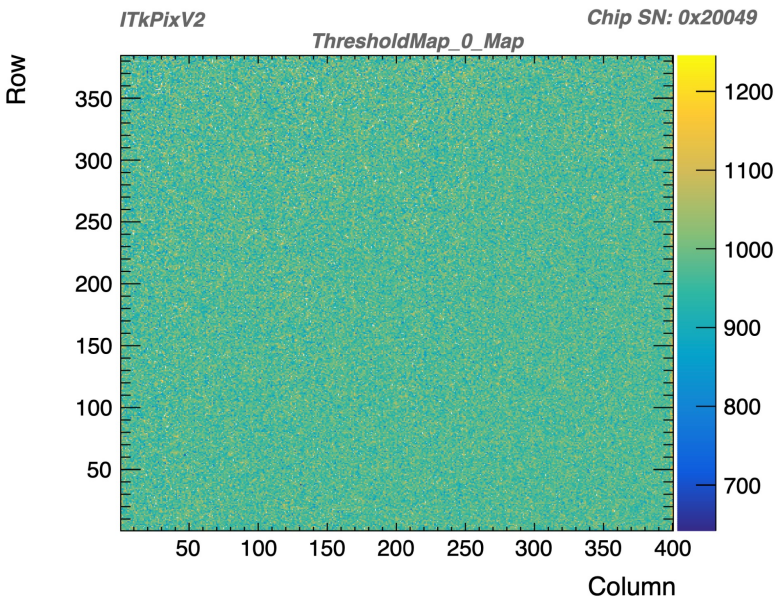
ToT bug in CROC



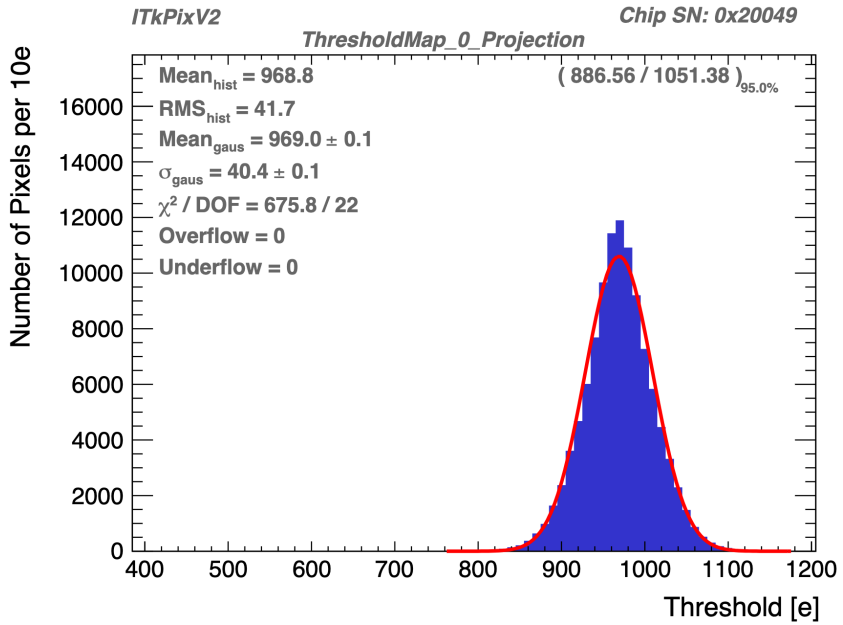
Threshold tuning

- Can tune chip threshold value using global and pixel-specific parameters
- Threshold tuning works as expected in ITkPixV2, tested with targets of 1500e and 1000e
- **Threshold Mean = (968.8 ± 41.7) electrons**
- **Noise Mean = (53.0 ± 10.1) electrons**

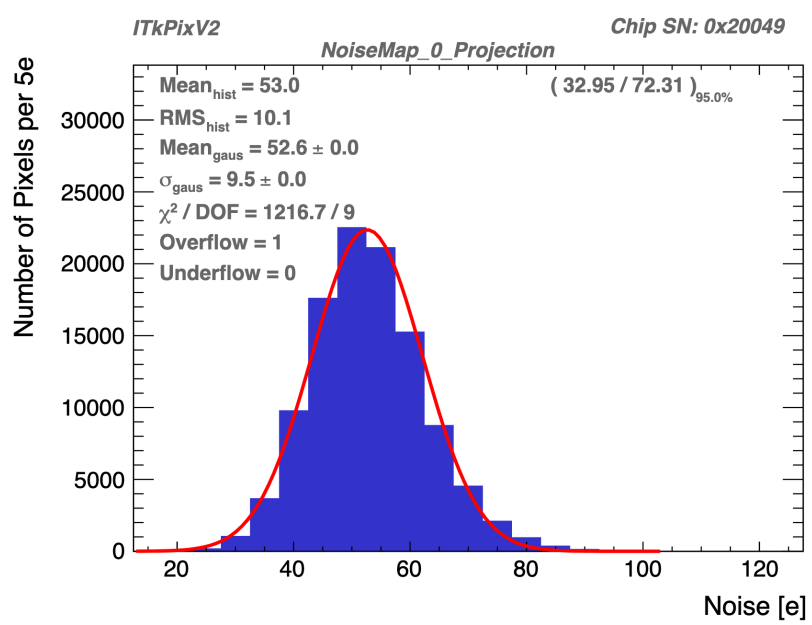
Threshold map



Threshold distribution

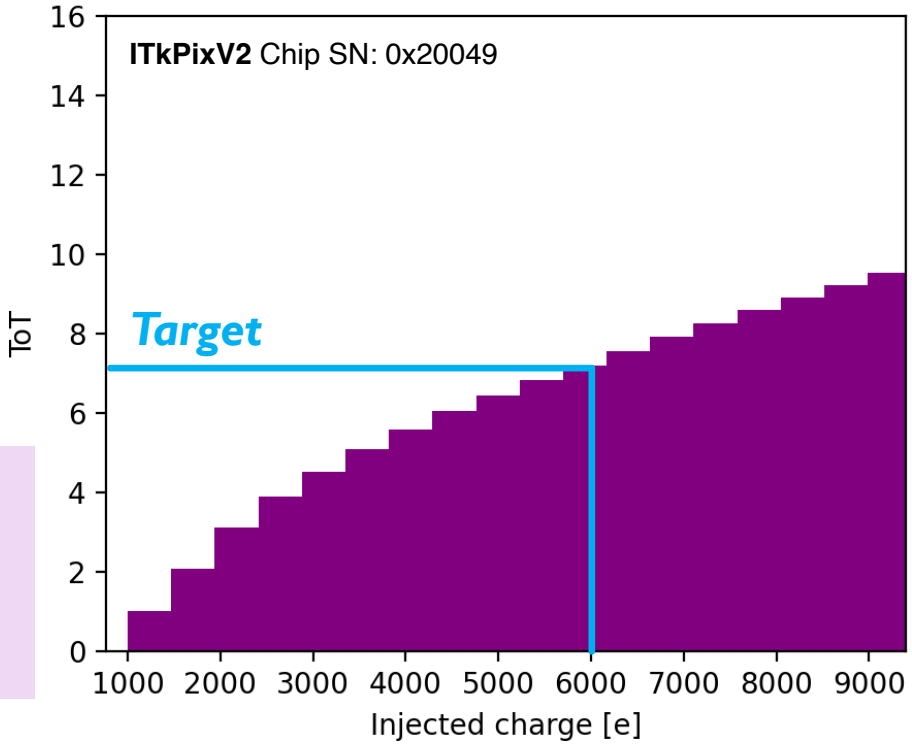


Noise distribution

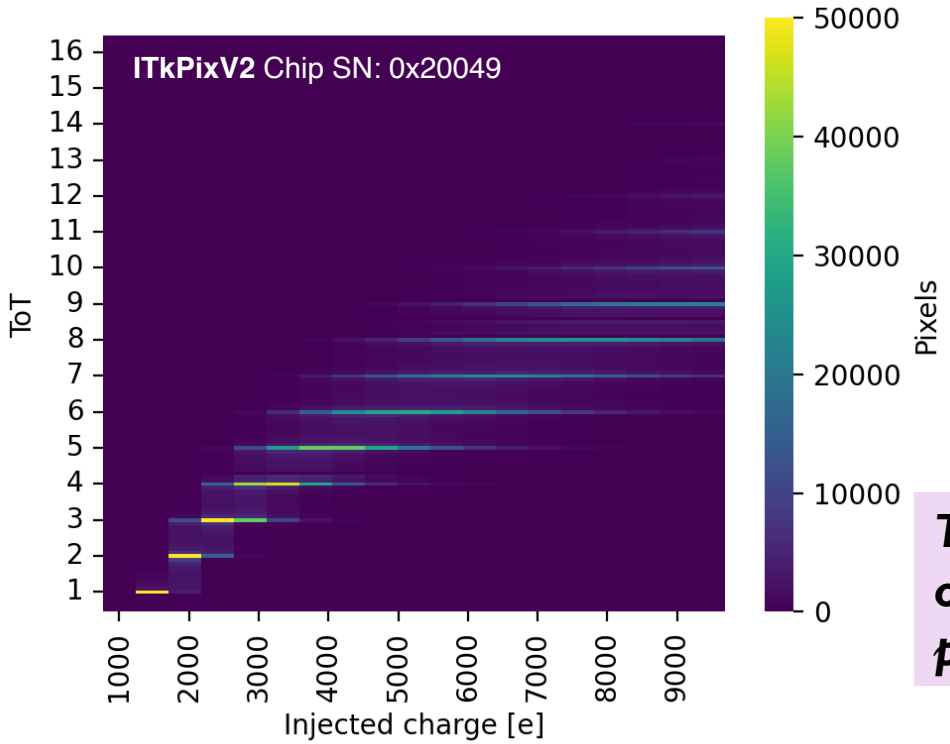


ToT tuning

- With working ToT functionality, it is possible to tune ToT to have a particular ToT at a given charge
- **ToT tuning works**, for example with a target of 6000 electrons at a ToT of 7
- Verify ToT tuning by measuring ToT as a function of injected charge



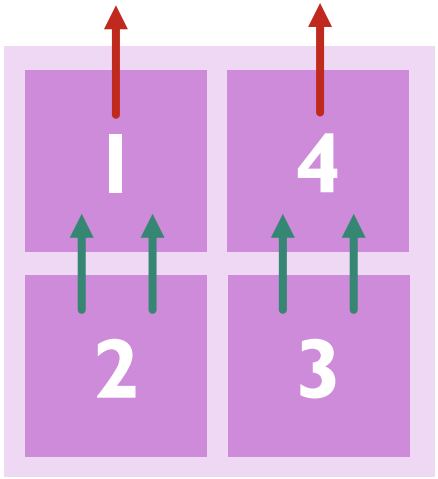
ToT averaged across all pixels



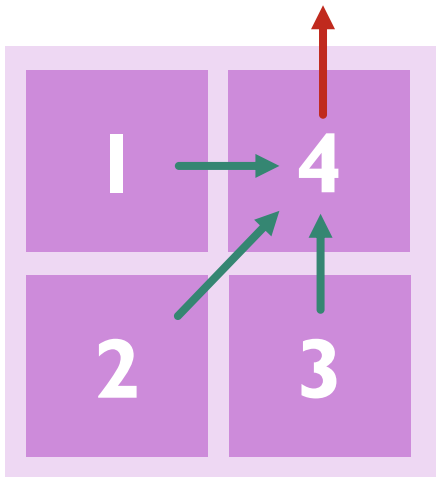
ToT map of all pixels

Data merging

- In the ITk detector we will use **data merging** to reduce the number of output links in the detector (in the outer layers)
- Primary chip(s) talk to outside, secondary chips talk to primary
- In ITkPixV1 data merging did not work properly for all delay values between primary and secondary
- Fixed in ITkPixV2, verified in setup with two single chip cards at CERN (not quad modules yet)

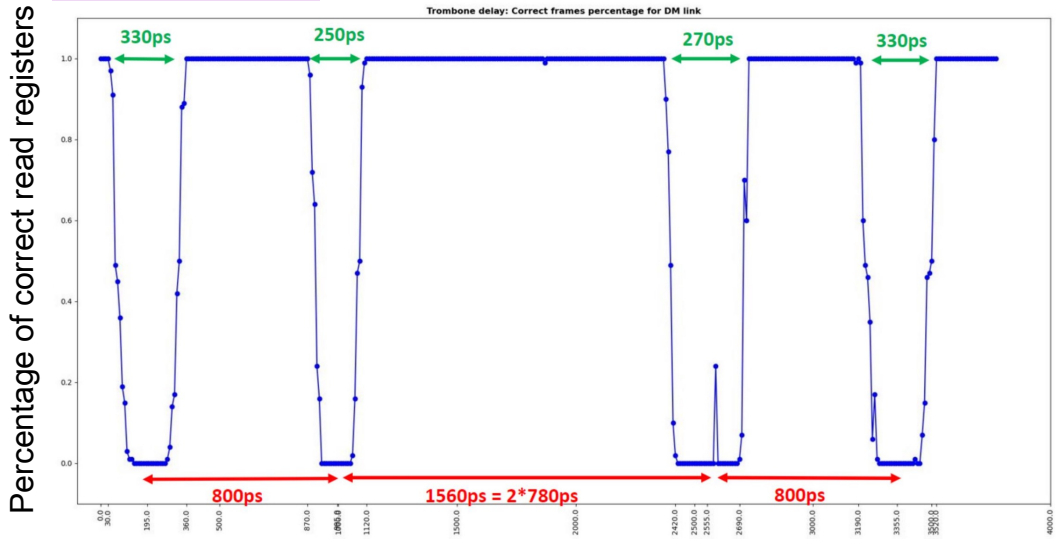


2 to 1 data merging

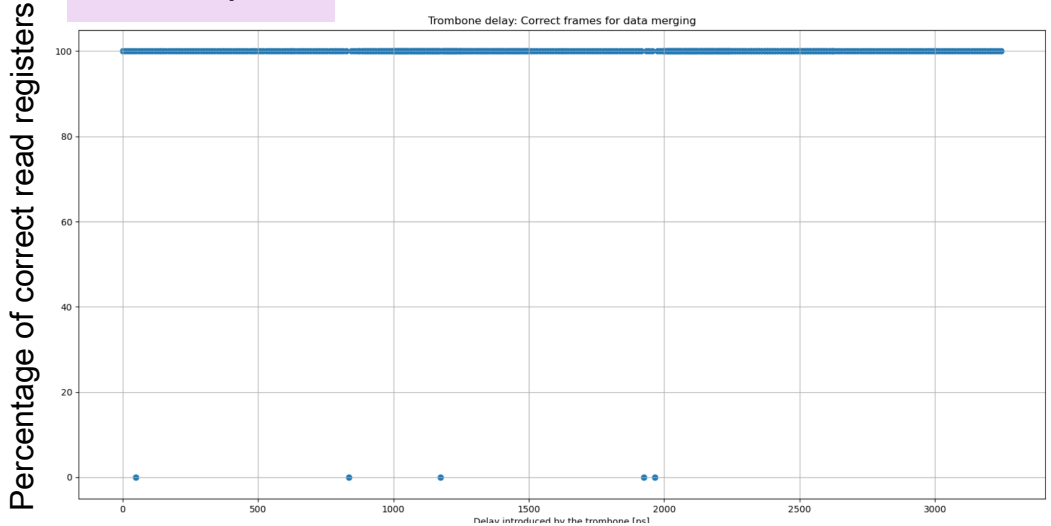


4 to 1 data merging

ITkPixV1.1



ITkPixV2

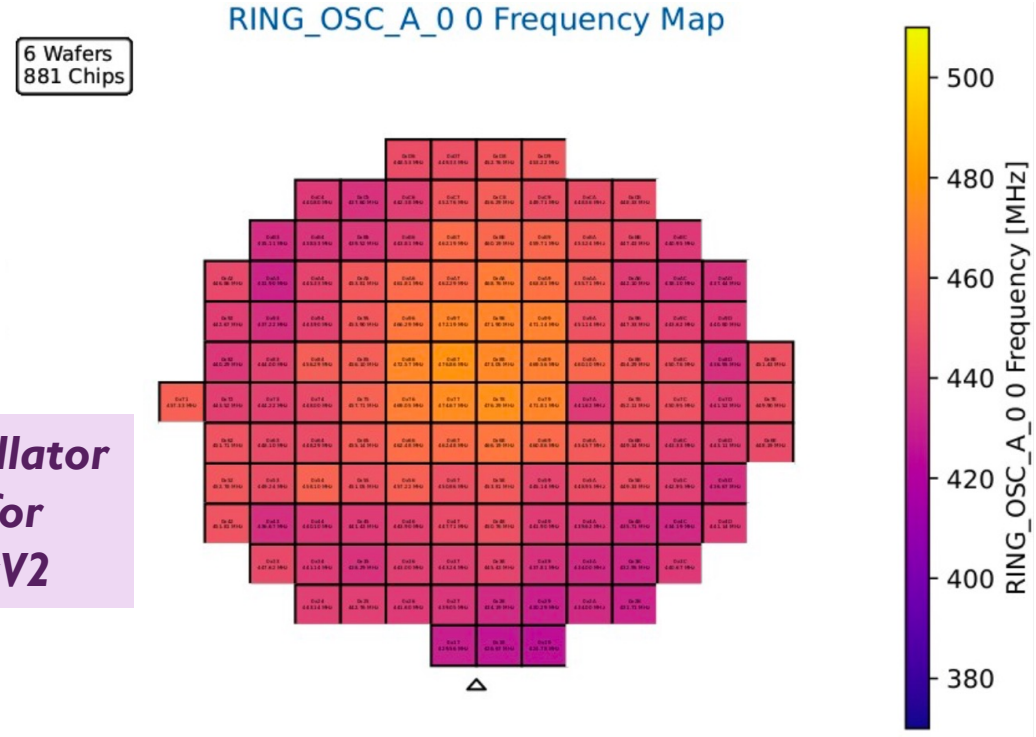


Wafer probing

- Quality control procedure for ITkPixV2 chips done at wafer level
- **Wafer probing routine** defined and tested using ITkPixV1 chip → expected yield 75-85 %
- 3-4 sites expected to perform wafer probing during production
- First ITkPixV2 wafers probed with reasonable results, currently in the process of adjusting QC cuts for ITkPixV2

Wafer probing setup in Bonn

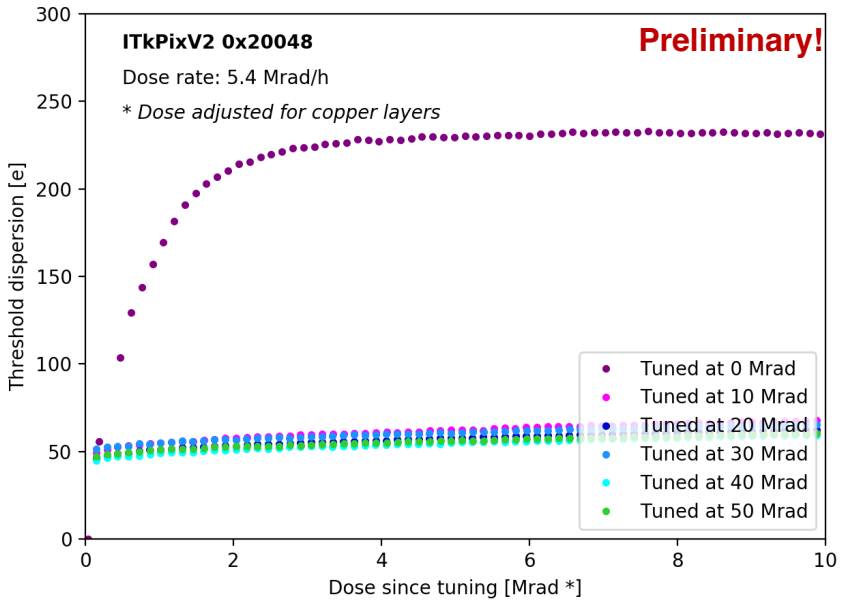
Ring oscillator map for ITkPixV2



X-ray irradiations

- Characterised in detail the radiation tolerance of the ITkPixV1 chip
  → Currently repeating main measurements for ITkPixV2
- So far, results look consistent with ITkPixV1 (after irradiation to 500 Mrad at 5 Mrad/h), and no operational issues observed during irradiation
- **Most damage to analog front-end occurs in the beginning of irradiation** → consistent with what was seen for ITkPixV1

Tuned threshold dispersion with irradiation

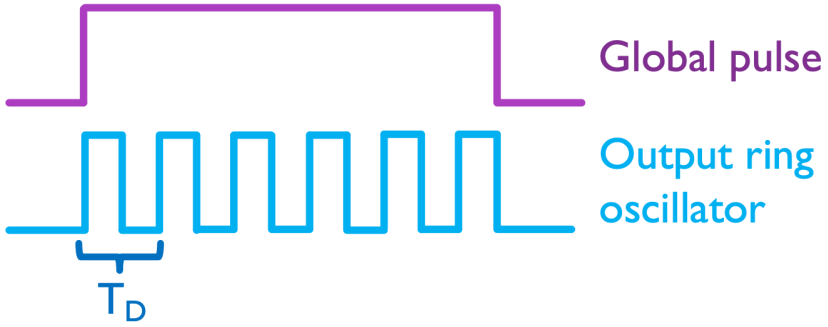


- Dedicated **ring oscillators** included in ITkPixV2 to measure damage to digital gates
- 42 ring oscillators made with different logic cells and different transistor sizes (strength 0, 1 and 4)

→ No strength 0 gates used in ITkPixV2 digital logic

→ Too large increase in gate delay (200%) will cause digital logic to fail

Ring oscillator behaviour



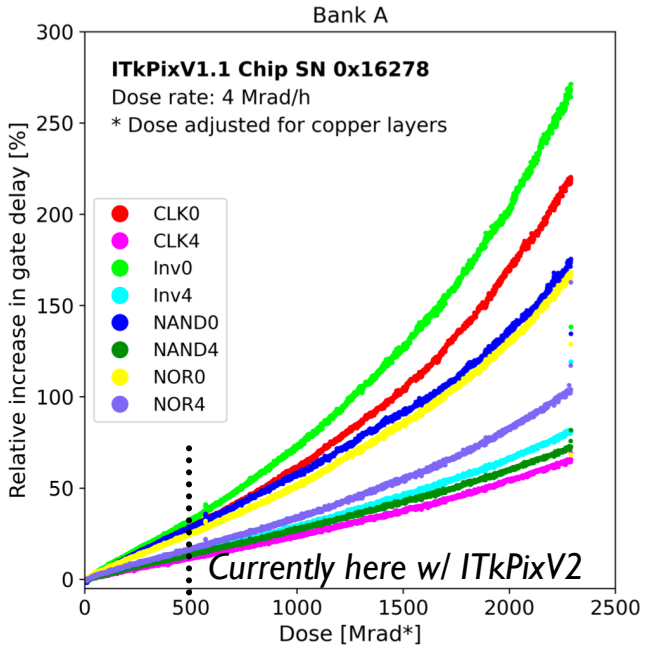
X-ray irradiations

- Digital logic is sensitive to **dose rate effects** → roughly two times more damage at low dose rate
- Need to irradiate to around 2 Grad to simulate the 1 Grad environment in ITk

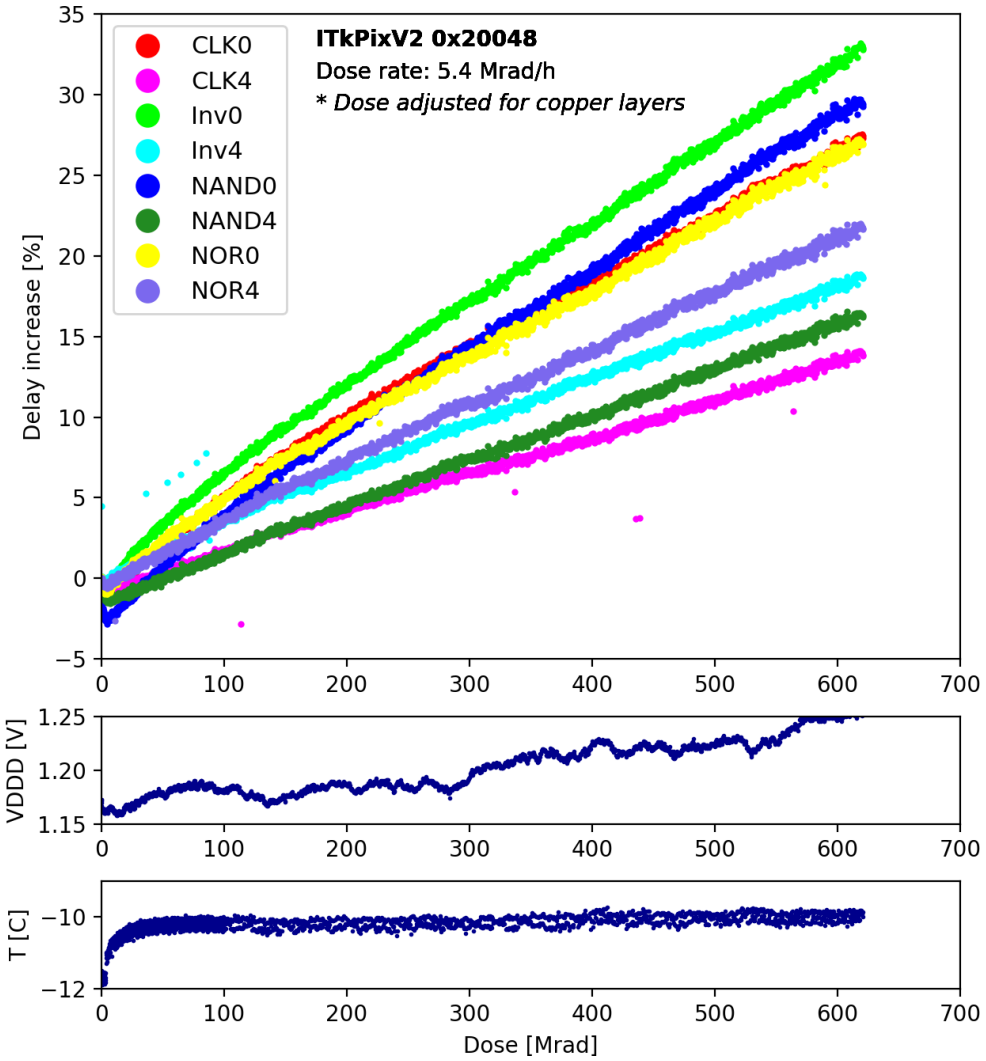
→ So far, ring oscillator behaviour is **very consistent with ITkPixV1**

→ Will reach total target dose in ~ 2 weeks

ITkPixV1 irradiation results



Ring oscillator delay increase with irradiation for ITkPixV2

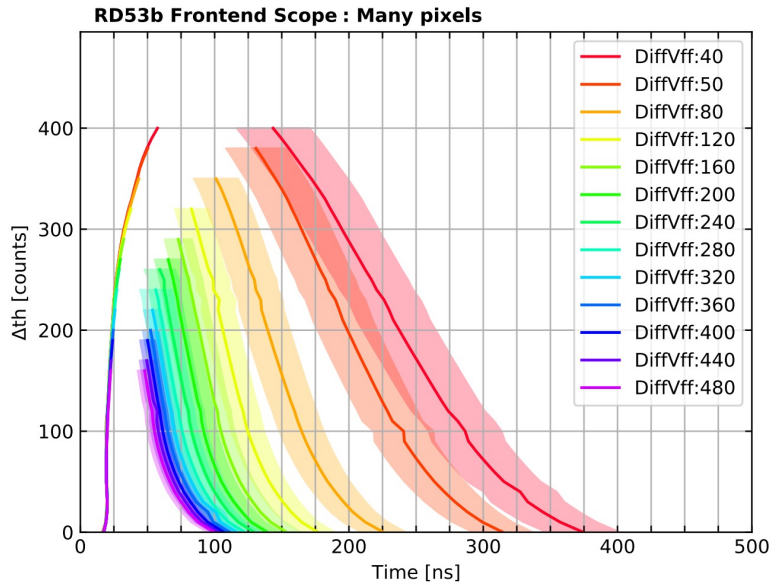


Conclusions

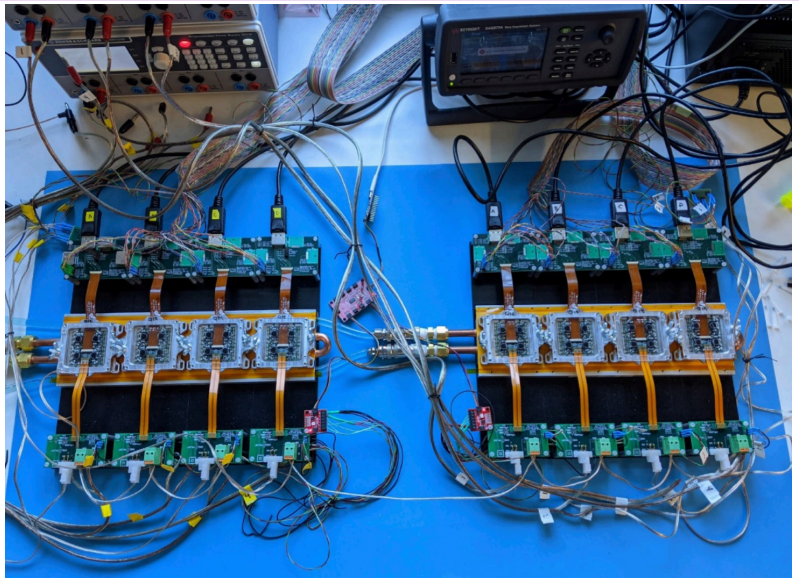
- Received ATLAS ITk production pixel readout chip ITkPixV2
- Result of ~10 years of ASIC development by the RD53 collaboration
- Many improvements implemented in ITkPixV2, and tested thoroughly in verification
- **First tests on ITkPixV2 look promising**, most major design changes verified
- All tested functionality performs as expected, some detailed studies still ongoing

- **Next steps:**
  - More long-term studies on single-chip cards: Long-term irradiations at low dose rate, SEE tests
  - Assemble first digital quad modules with ITkPixV2
  - Dedicated studies to inform detector operation (ToT, larger-scale system tests, e.g. serial power chains with multiple modules)

FE scope: measure analog signal



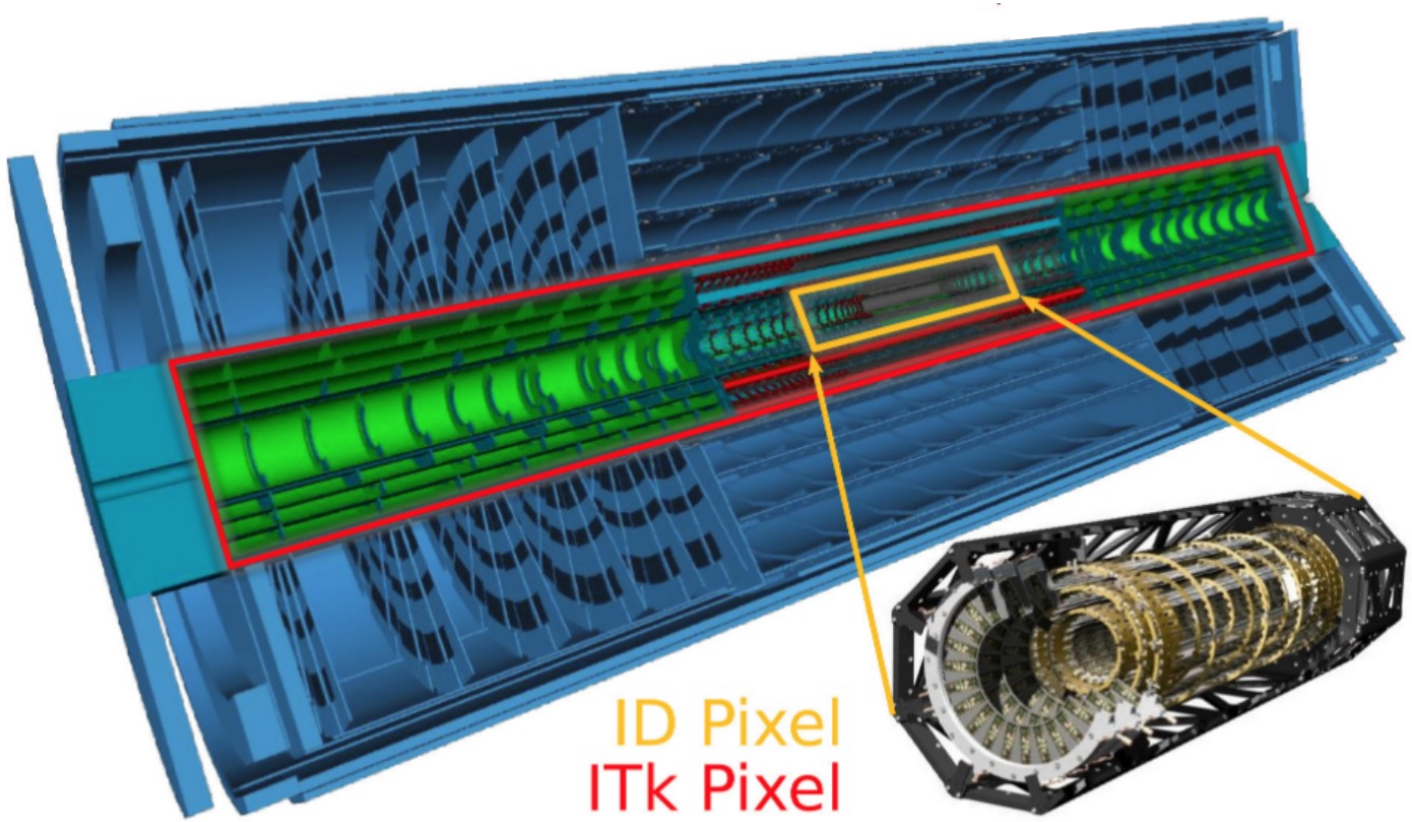
Serial power chain



Thank you!

Questions?

ATLAS ITk Upgrade



All-silicon upgraded tracking detector (ITk) for HL-LHC to cope with increased instantaneous luminosity and pile-up

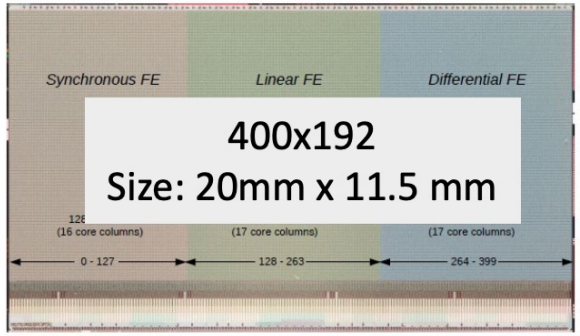
Upgraded pixel detector:

- Larger silicon area → **6x larger than current tracking detector**
  - ~13 m^2 of active area
  - 9400 pixel modules, 5.1 billion pixels
  - Extended η coverage to $|\eta| \leq 4$
- **Smaller pixel pitch:**

  400 x 50 μm^2 → 50 x 50 μm^2
- **New readout chip** to cope with higher data rates and increased radiation

RD53 chip evolution: RD53A

RD53A



- Pixel chips for the HL-LHC upgrade for ATLAS and CMS have been jointly developed by the RD53 collaboration to cope with the harsh requirements for HL-LHC
- First joint prototype was RD53A, submitted in August 2017

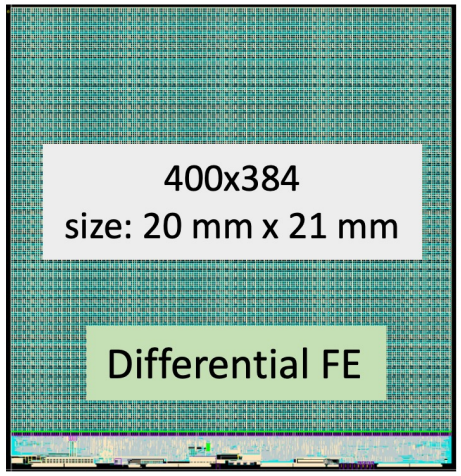
→Half-sized demonstrator chip with three different architectures

- Based on this, improved RD53B chip, produced in two versions: **ATLAS ITkPixV1** and CMS CROC
- Main difference in size and type of front-end used
  - Differential Front-End for ATLAS
  - Linear Front-End for CMS

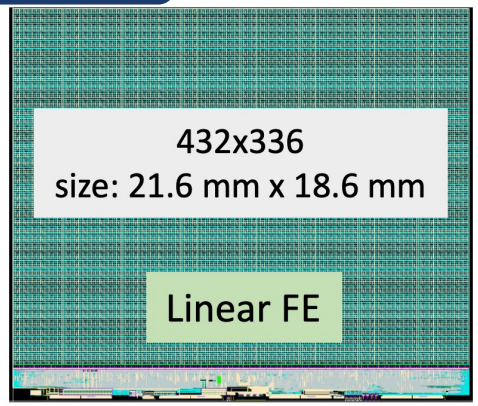
RD53 chip evolution: RD53B

ITkPixV1.0

ITkPixV1.1



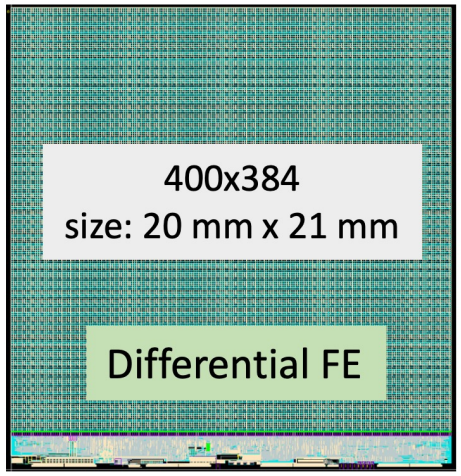
CROC v1



- **ATLAS ITkPixV1** chip submitted in March 2020
- Found a serious issue in the time-over-threshold (ToT) memory
  - Large current for particular configurations of ToT
  - Wrong ToT storage and hit loss
- Fix to the mask on the remaining FE wafers, fixing the issue of large leakage current in ITkPixV1.1 (but ToT still not useable), submitted in October 2020
- ITkPixV1.1 will be used as the **ITk pre-production readout chip**
- **CMS CROC_v1** chip submitted June 2021, including proper fix to the ToT memory

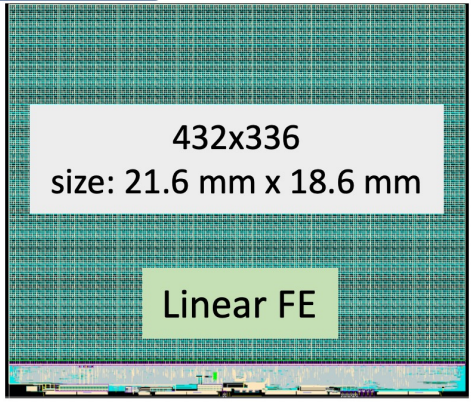
RD53 chip evolution: RD53C

ITkPixV2



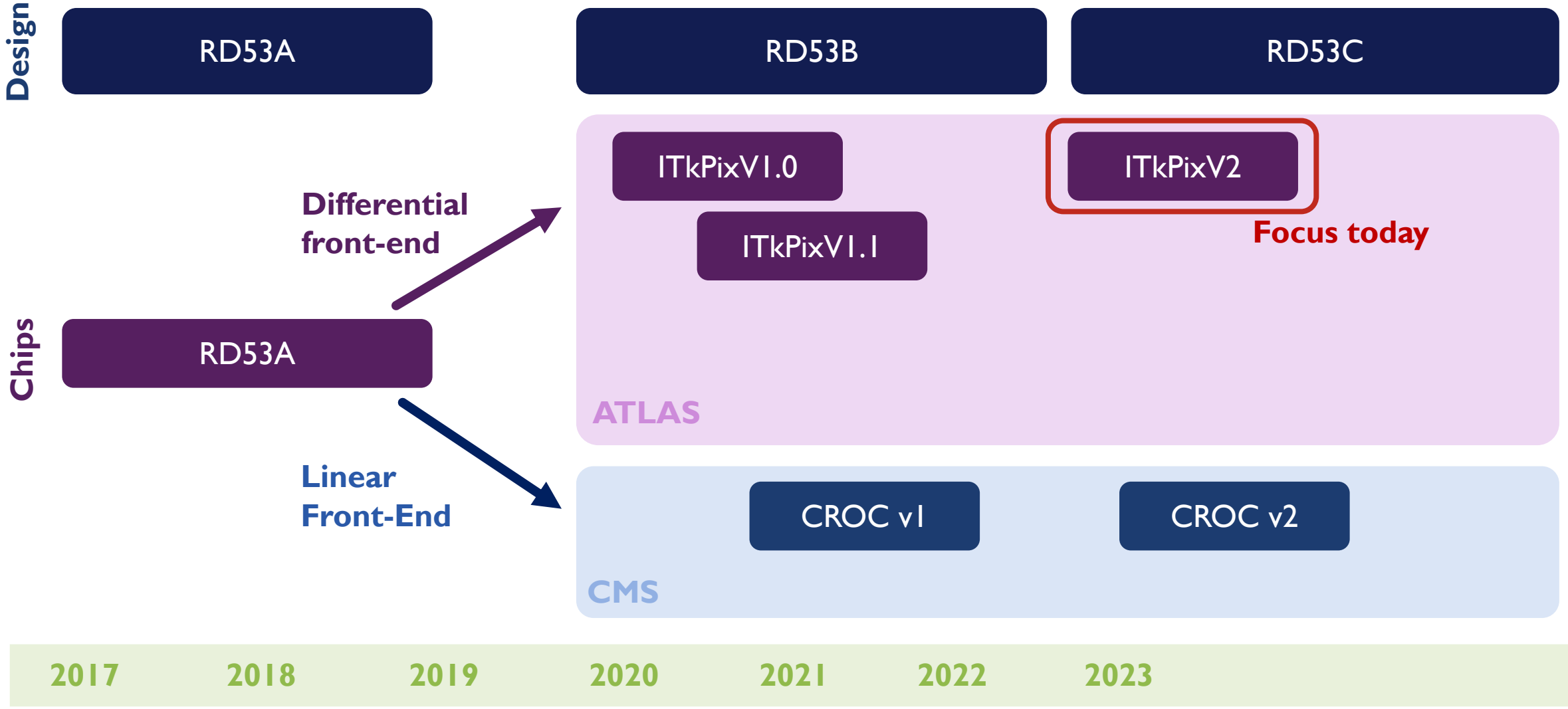
- **ATLAS ITkPixV2** chip submitted in April 2023
- Many small changes to improve:
  - Stability against single-event transients
  - Startup and powering stability
  - Improvements and additional monitoring sensors for temperature and radiation
- Expected to be the final production chip
- Received back engineering run wafers → need to run tests now to decide within a few months if we are happy with the design and would like to produce the remaining wafers

CROC v2



- **CROC v2** to be submitted soon

RD53 chip evolution

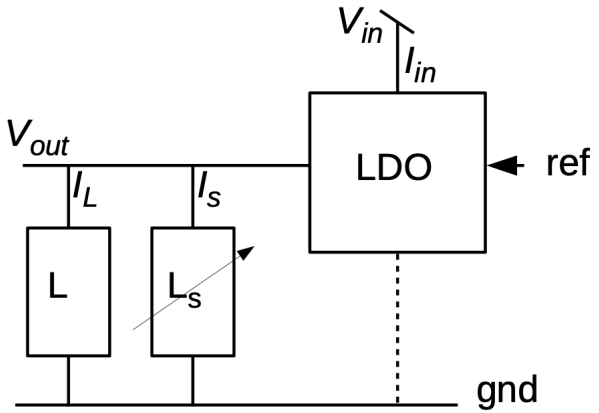


SLDO performance

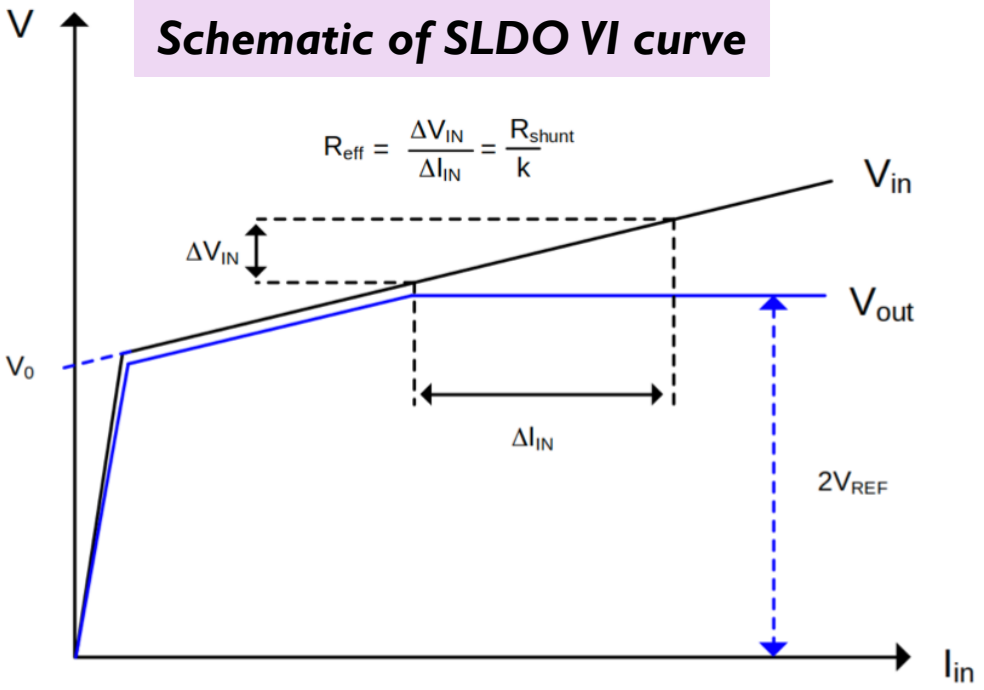
- ITkPixV1 modules will be operated in a **serial power configuration**, suppying a constant current
- Motivation: reduce the number of cables and material in the detector
- To allow this, the chip has a **SLDO circuit**, which powers the main load (the chip) and the internal load (shunt element)
- The shunt element is designed such that it achieves the required input current, regardless of what the chip does
- Put in V_{in} which regulates voltage to V_{out}
- Linear behaviour driven by R_{eff}
- Offset voltage V_0 (or V_{ofs}) is set by a separate circuit
- Overall behaviour can be described as:

$$I_{in} = I_L + I_s = \frac{V_{in} - V_0}{R_{\text{eff}}} \qquad [V_{in} > V_0]$$

Schematic of LDO circuit



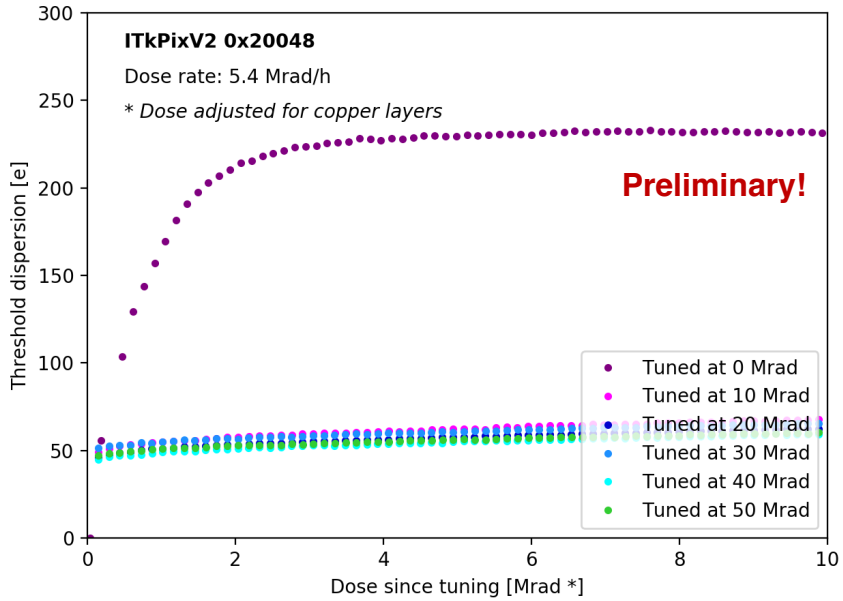
Schematic of SLDO VI curve



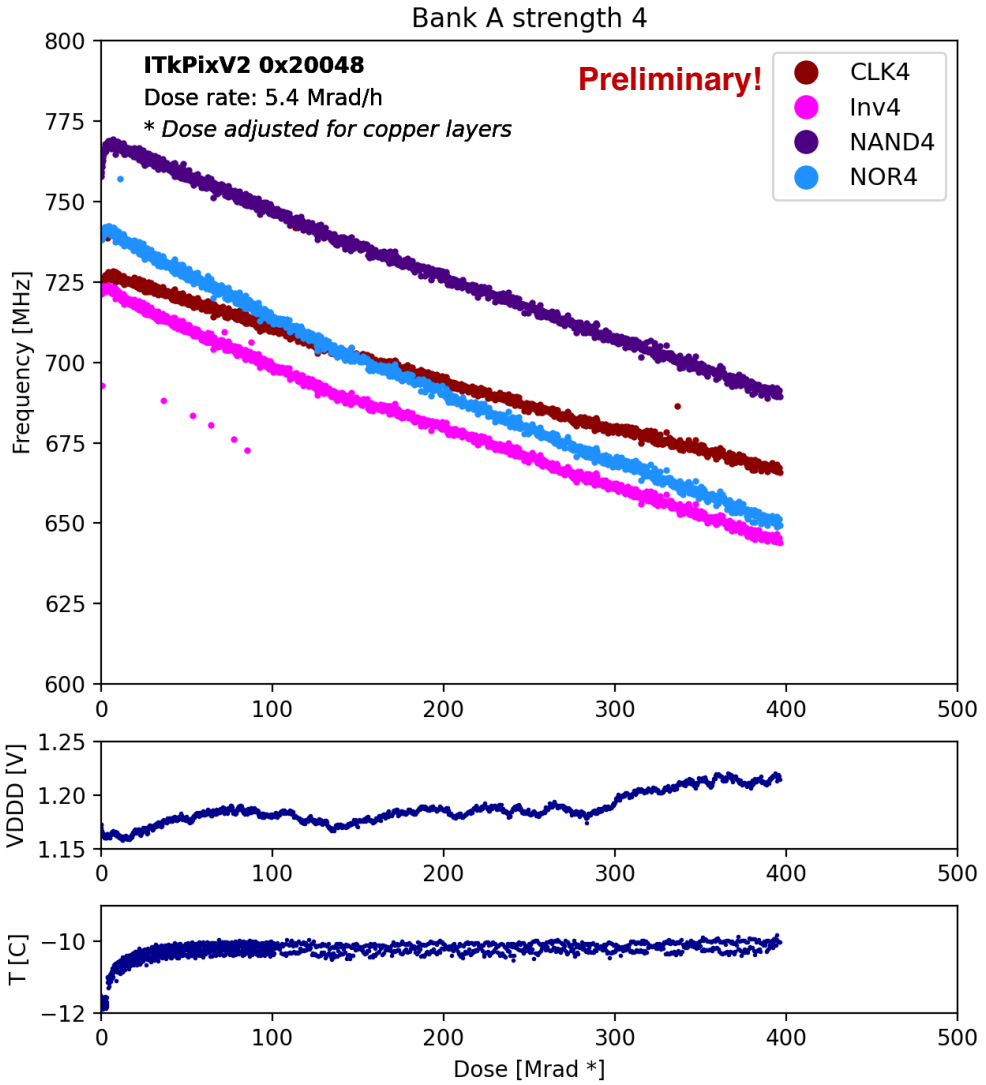
Irradiations

- Characterised in detail the radiation tolerance of the ITkPixV1 chip → Currently repeating main measurements for ITkPixV2
- So far, results look consistent with ITkPixV1 (after irradiation to 400 Mrad at 5 Mrad/h)
- Dedicated ring oscillators to measure damage to digital gates → sensitive to dose rate effects
- Damage to analog front-end is most severe in the beginning of irradiation

Tuned threshold dispersion with irradiation



Ring oscillator frequencies with irradiation



FE scope

- ToT in ITkPix-V1 chips is controlled by global registers only. Scan the feedback current DAC to decide configuration for different detector regions
  - Study with **FE scope**: get the profile of analog signal using PToT and ToA
  - ToT to charge conversion can be performed in DAQ software