Characterization of a Digital SiPM

Introduction & Lab Characterizations

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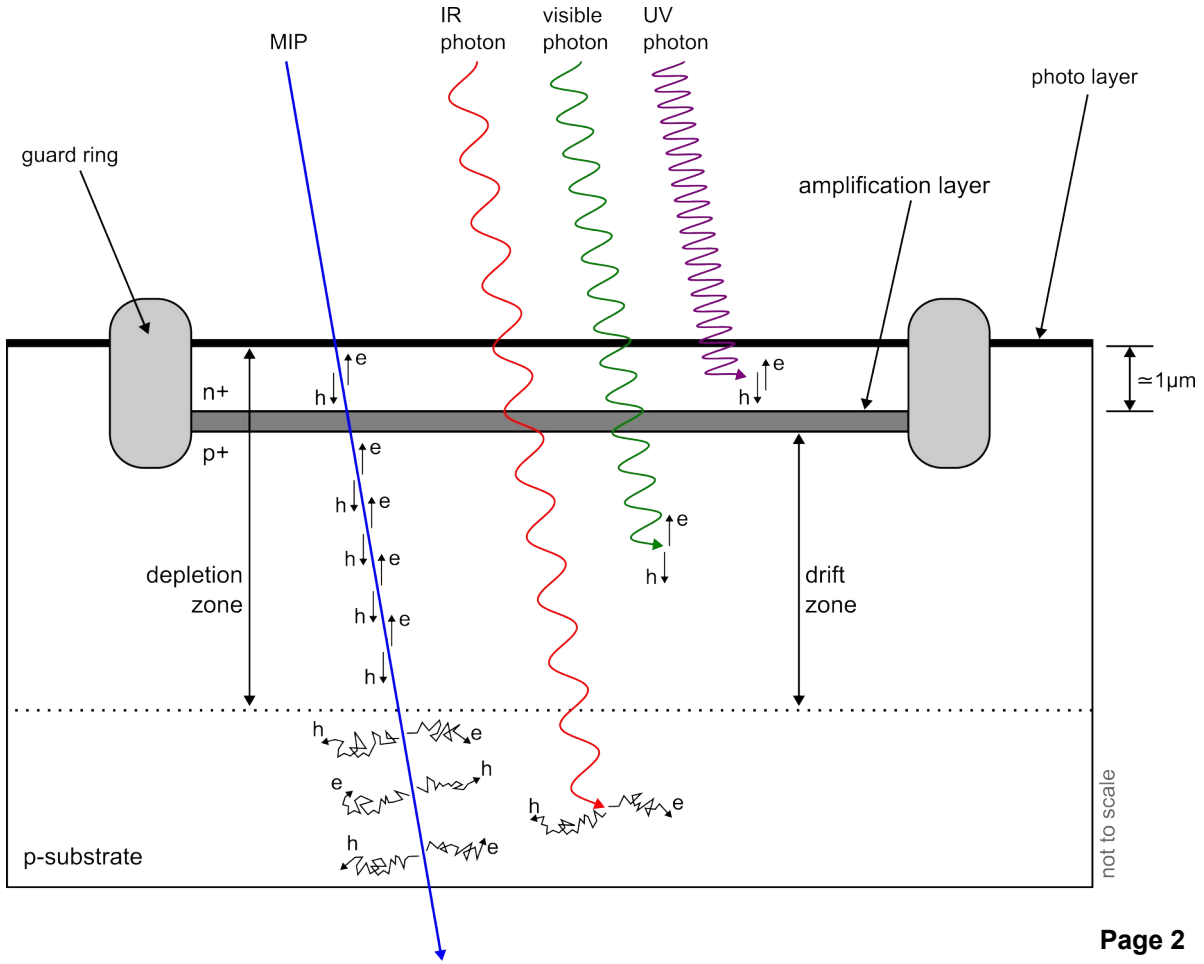
DESY.

What is a SiPM?

Overview of Silicon Photomultipliers

- Single-Photon sensitive detector consisting of SPADs (Single-Photon Avalanche Diode)
- PN-junction with avalanche layer for charge multiplication above breakdown voltage
- Gain typically $\mathcal{O}$(10^6), binary information
- Dark counts from thermal noise
- Photon Detection Efficiency (PDE)
  typically small outside of visible range
- Geometry also limits PDE (fill factor)
- MIP detection efficiency
  mainly limited by fill factor

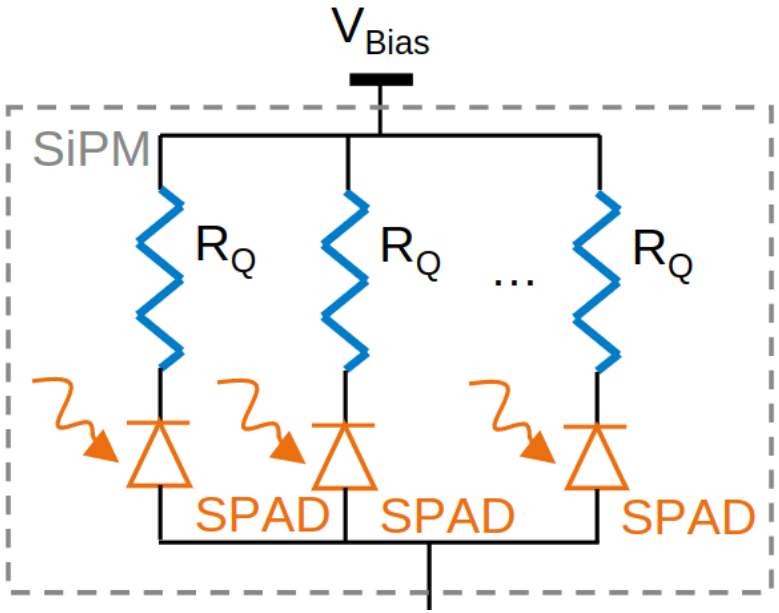


Analog vs Digital SiPM

Why go digital?

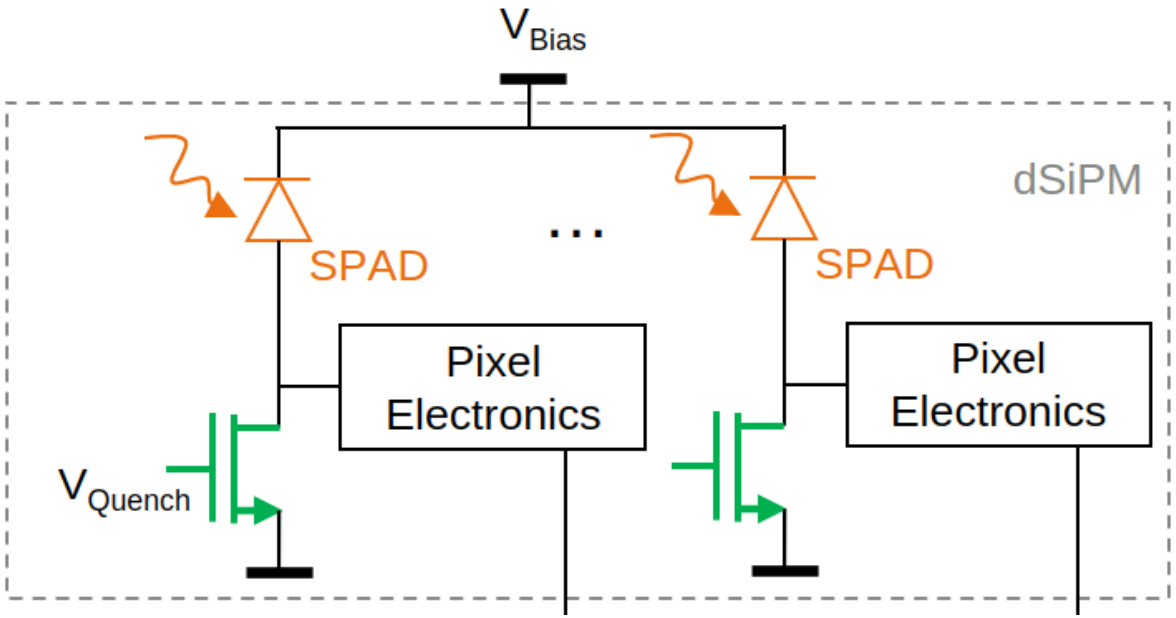
Analog SiPMs

- Specialized manufacturing processes
- Analog output requires digitization
- SPADs connected in parallel
  - No information which pixel was hit



Digital SiPMs

- CMOS imaging processes (if monolithic)
- Optional ASIC features like:
  - Spatial information with hitmap readout
  - Masking noisy pixels



DESY dSiPM Specifications

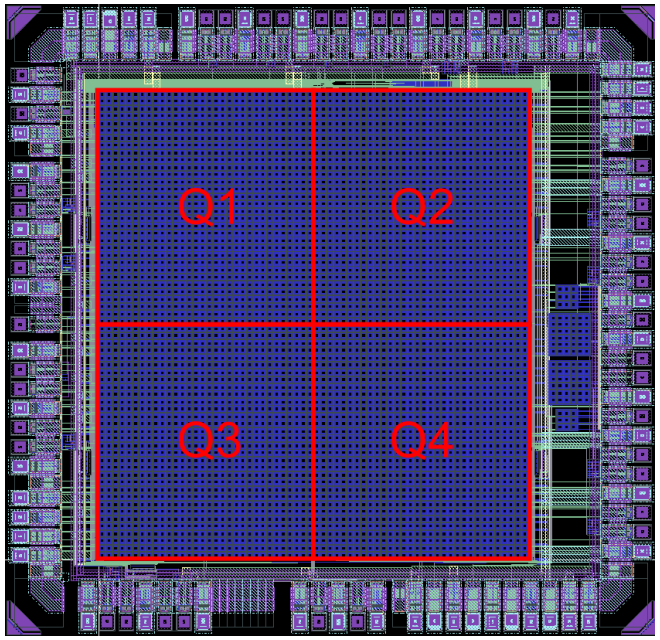
Designed and tested at DESY

Layout

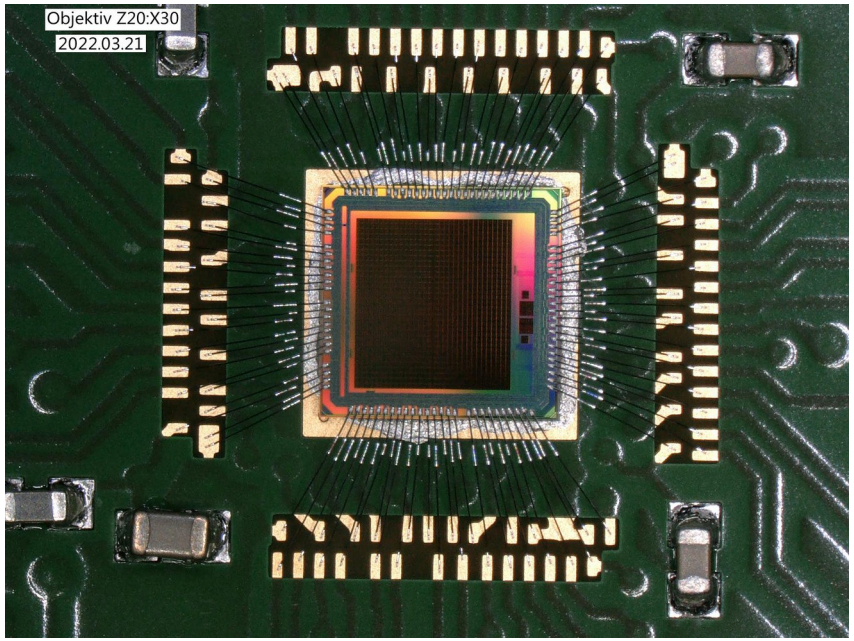
- Monolithic digital SiPM
- 32 × 32 pixels with 76µm x 70µm pitch
- 4 SPADs + frontend per pixel, 30% fill factor
- LFoundry 150nm CMOS process

ASIC features

- Masking of noisy pixels
- Hitmap readout with timing information
- 4 quadrants with <100ps resolution
- Frame-based readout (3MHz frame rate)
- 2-bit in-pixel hit counting
- Validation logic



Quadrant structure



Chip bonded to a PCB

Pixel Design & Frontend

4 SPAD Layout

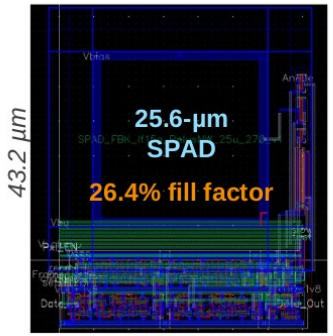
Pixel Design

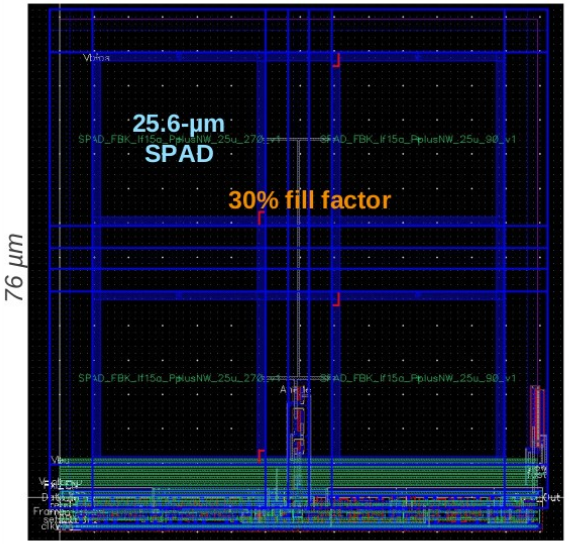
- Four SPADs per pixel sharing the pixel frontend and readout electronics
- Combining SPADs maximizes fill factor (limited by single SPAD ~33% fill factor)

Pixel Frontend

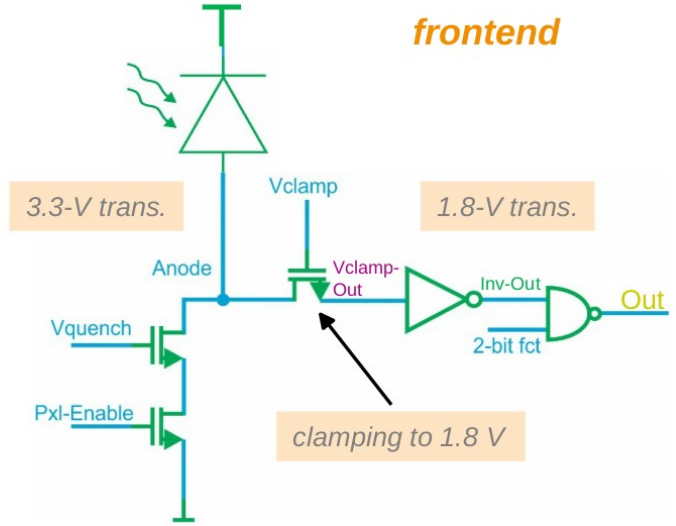
- Per-pixel enable transistor for masking
- Frontend clamps output voltage, required to protect readout electronics
- Pulse duration $\mathcal{O}$(10ns to 100ns) controlled by quenching voltage
- Global fixed threshold

layout with pixel electronic

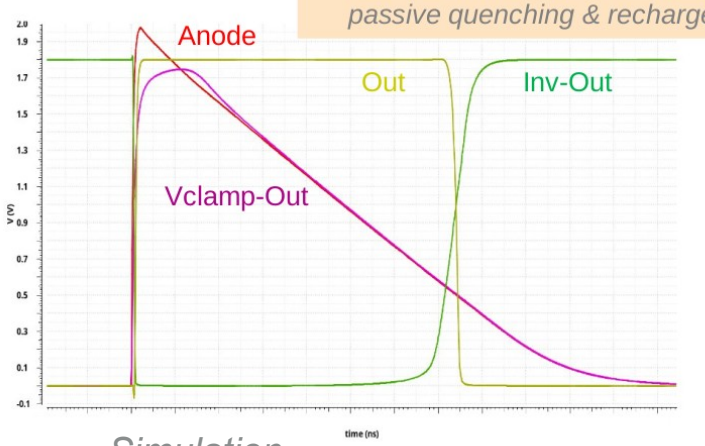




frontend



passive quenching & recharge

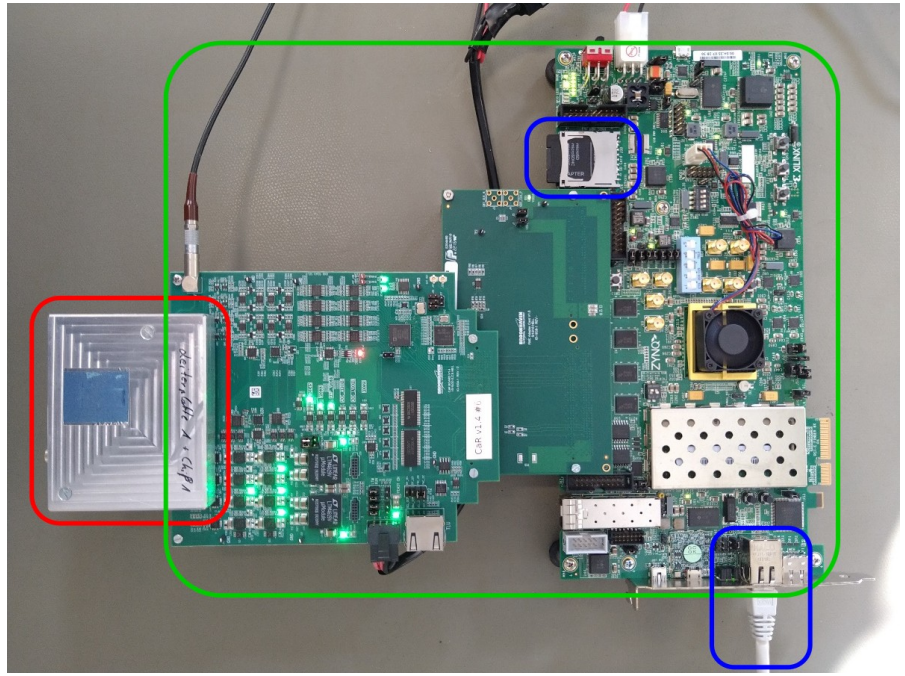


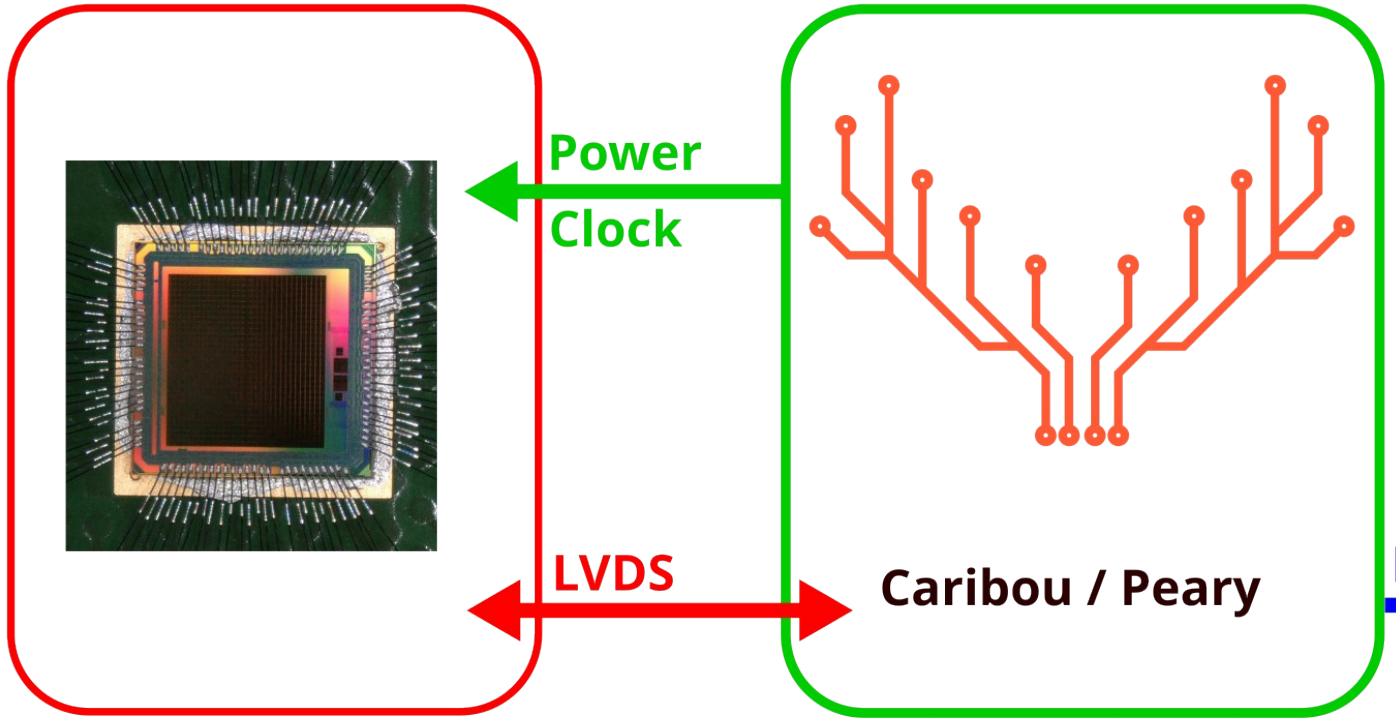
Simulation

DAQ Chain

Using the Caribou System

Caribou reference publication: https://dx.doi.org/10.22323/1.370.0100





Caribou

Allowing for fast R&D

Joint Development

- Versatile readout system developed by CERN, BNL, DESY and University of Geneva
- Already used by several sensors, e.g. ATLASpix, FASTPIX, etc

System on Chip (SoC) Board

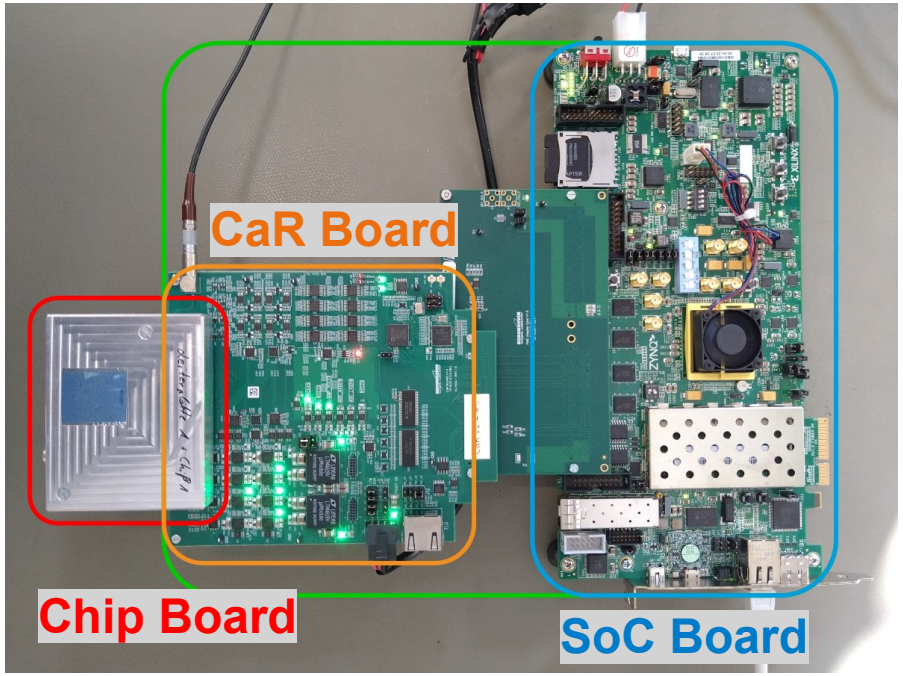
- Embedded CPU running Linux with DAQ software
- FPGA to control the sensor and receive data

Control and Readout (CaR) Board

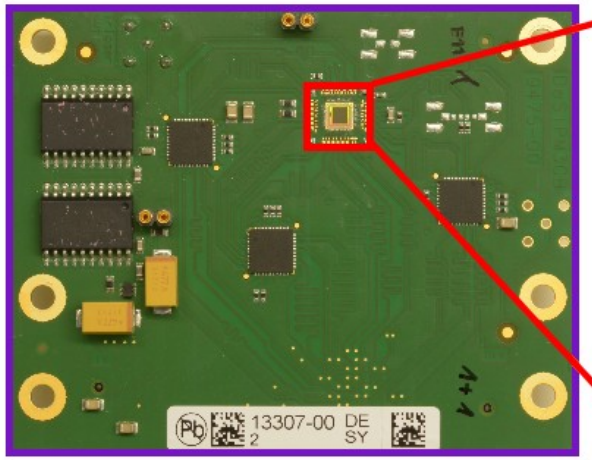
- Physical interface between SoC Board and Chip Board
- Contains peripherals required to interface with the chip

Chip Board

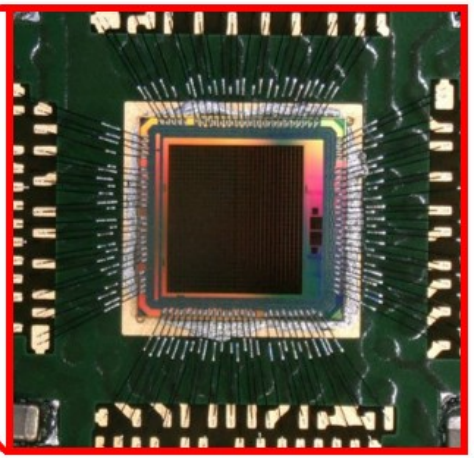
- Sensor-specific board with passive components



Caribou DAQ system



Chip Board

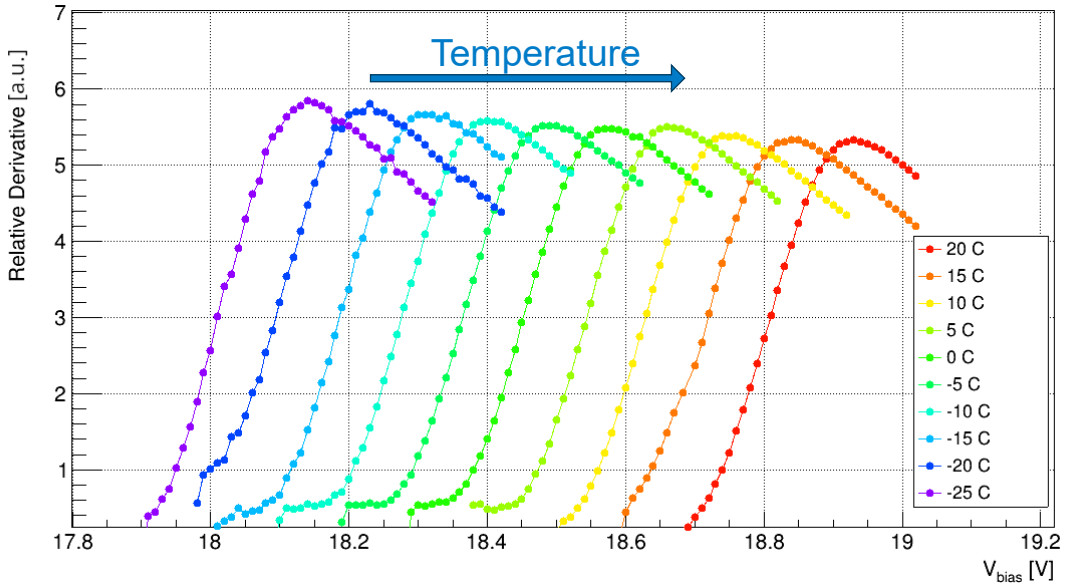


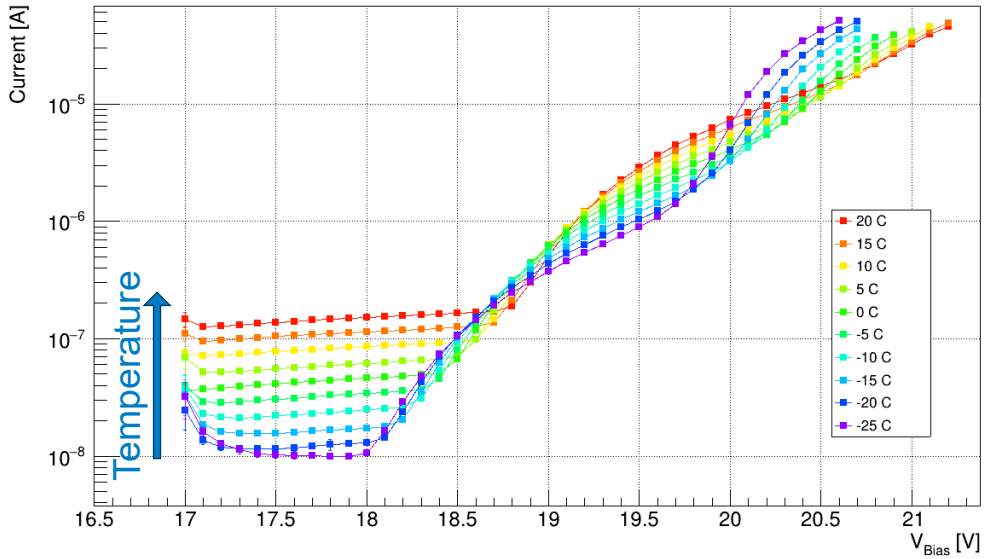
Chip Glued & Bonded

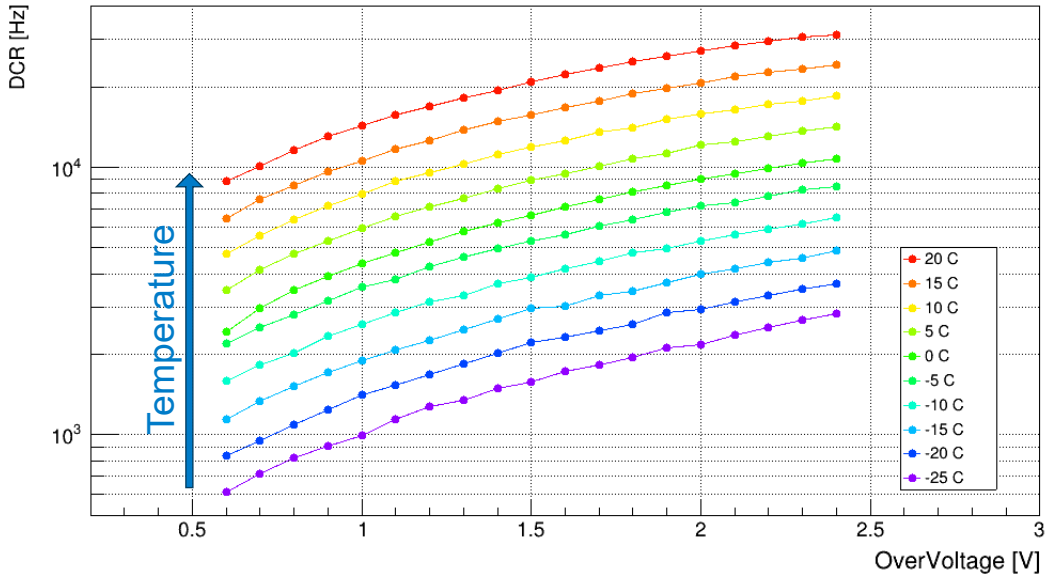
IV Curves & Dark Count Rate

Chip Characterization

- Detailed characterization performed on several samples (Chip4 shown in figures)
- IV & Dark Count Rate studies performed with controlled temperature (from -25 to 20°C) and humidity (~0%) in a dark environment
- Measurements in line with expectations





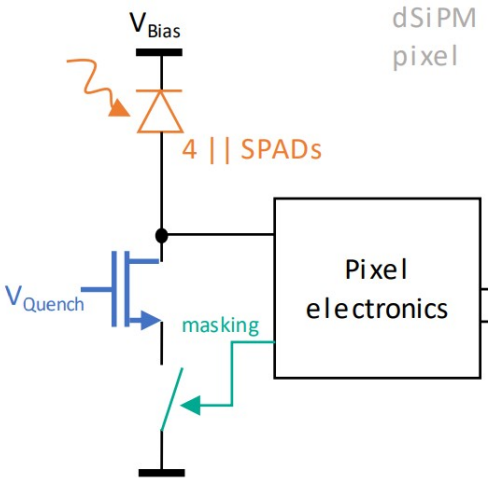


Quenching & Pixel Masking

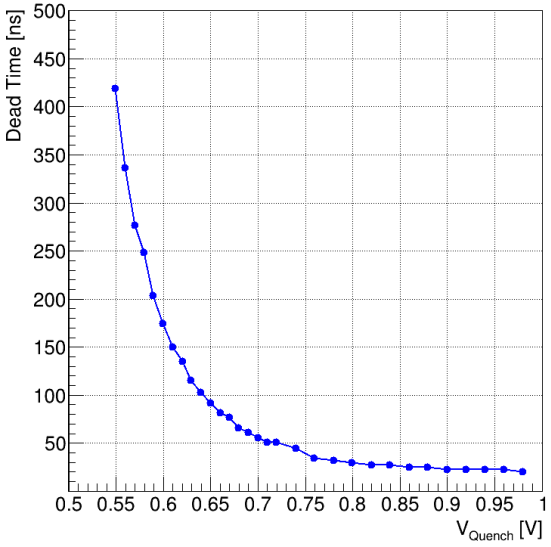
Features in the Chip itself

Quenching

- In-pixel quenching circuit is a single transistor
- Configurable R_{Quench} to tune the pulse length
- Within the frame (~333ns) up to 3 non-overlapping hits can be distinguished and counted



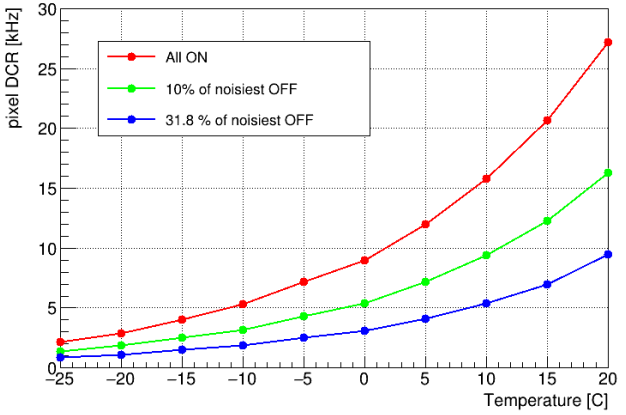
In-Pixel Quenching Circuit



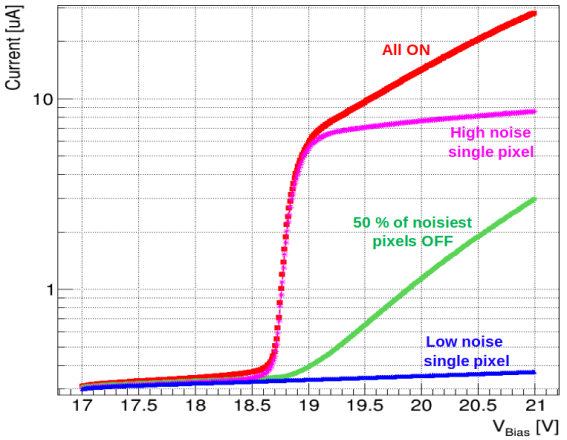
Dead Time vs V_{Quench}

Pixel Masking

- Individual pixels can be disabled
- Allows deactivation of noisy / unused pixels (DCR & power consumption reduction)
- Allows in-depth characterization of SPAD arrays
  - Single noisy pixel dominates IV measurements



DCR with different maks (2OV)



IV curves with different maks

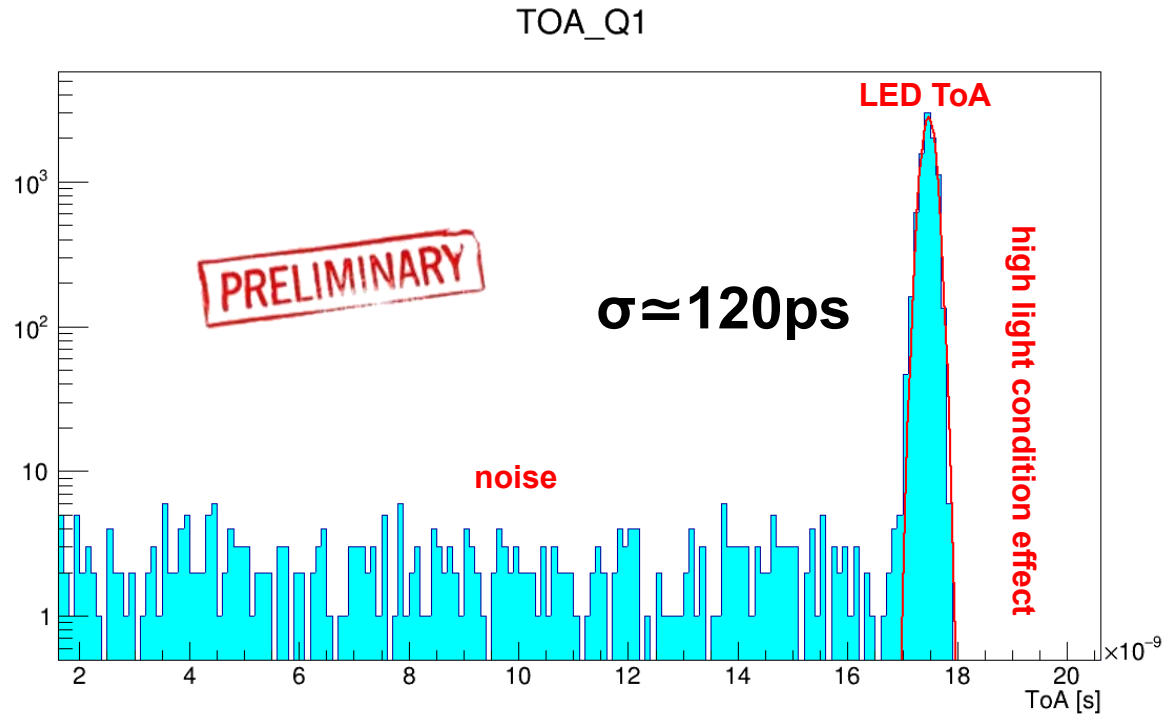
LED Studies

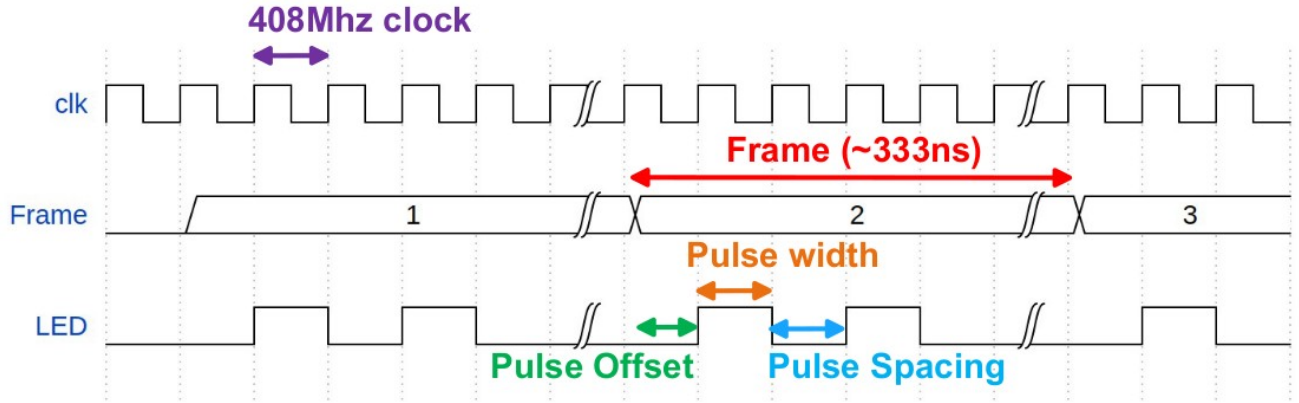
First Timing Measurements

- FPGA has circuit to pulse LED output
- Measure time difference between frame start and LED pulse measurement on chip (ToA)
- Configurable settings, for example:
  - Offset of pulse rising edge from frame start
  - Number of consecutive pulses

Results

- No peak after LED → high light condition effect
- 120ps sigma of LED ToA peak
- Note: ToA ≠ time resolution
- Reason: LED does not turn on instantly
- LED too slow, requires Laser for time resolution





Laser Studies

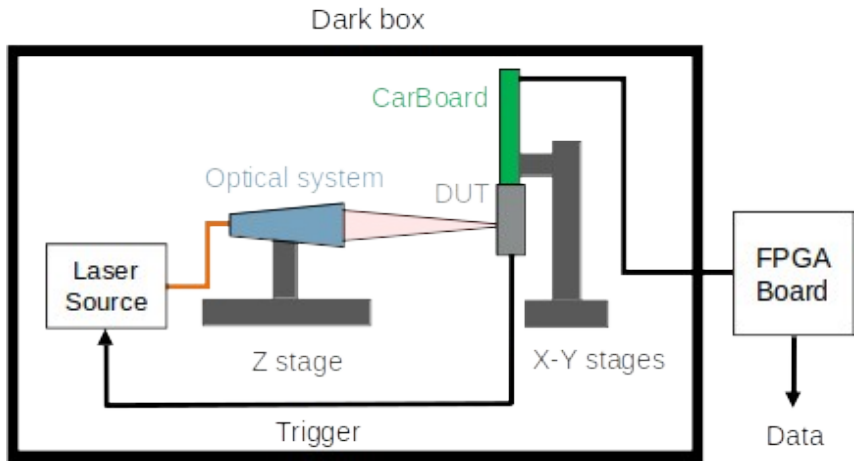
Studying Single Pixels

Setup

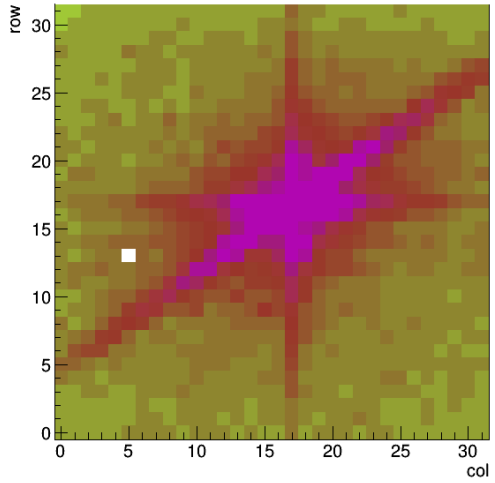
- 1064nm pulsed laser
- High intensity → high light condition
- Optical reference with 20ps resolution
- Laser triggered by DAQ
- DUT mounted on x-y stage

Planned & Ongoing Studies

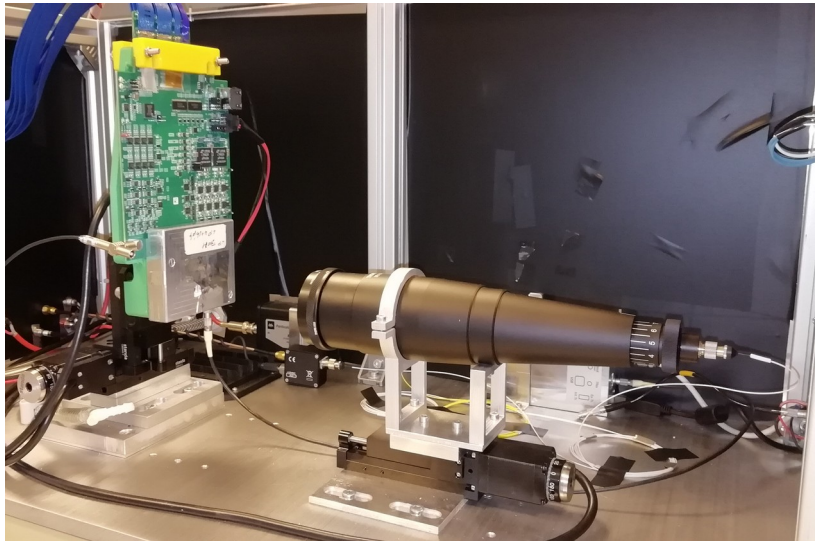
- Study single pixels by masking
- 2D scan of time resolution and delay of response
- Uniformity of pixel array



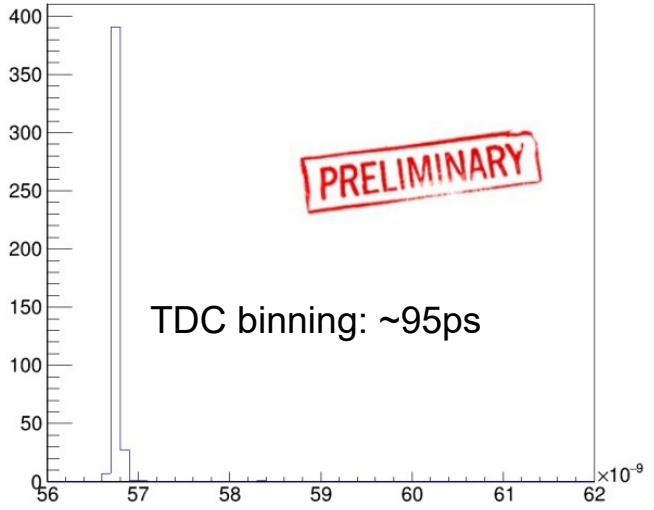
Schematic overview of the setup



Example hitmap



Setup in the lab



ToA distribution of single pixel

Summary & Outlook

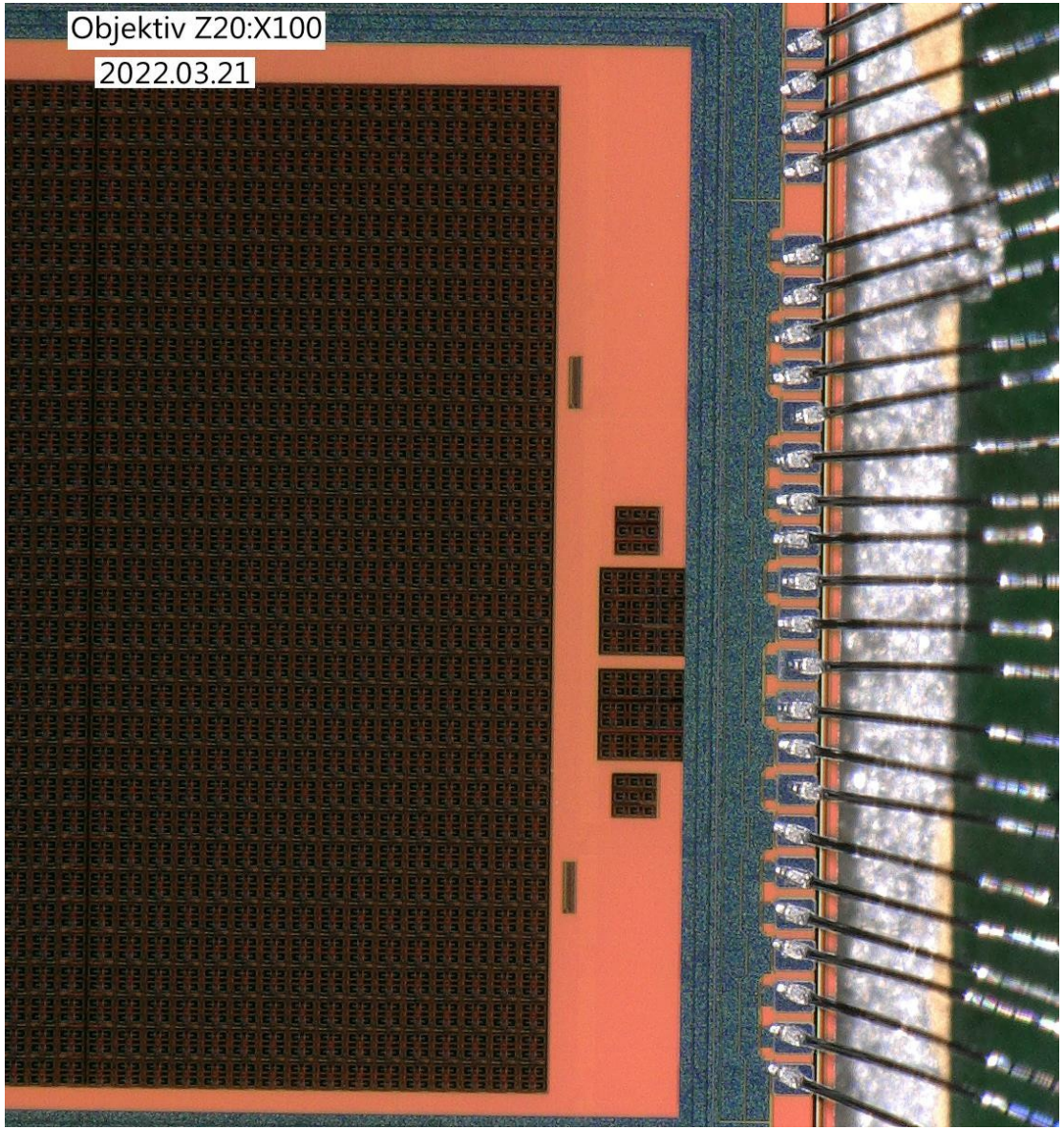
Promising R&D

dSiPM Chip

- Working prototype of a digital SiPM designed and tested at DESY
- ASIC features validated in the lab, characterizations in line with expectations
- Promising results on timing capabilities

Planned & Ongoing Studies

- Timing measurements with laser setup
- Analysis of testbeam data, see Gianpiero's talk (https://indico.cern.ch/event/1232761/contributions/5321422/)
- Reference publications currently being written



Thank you

Contact

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Backup Slides

Readout & Validation Logic

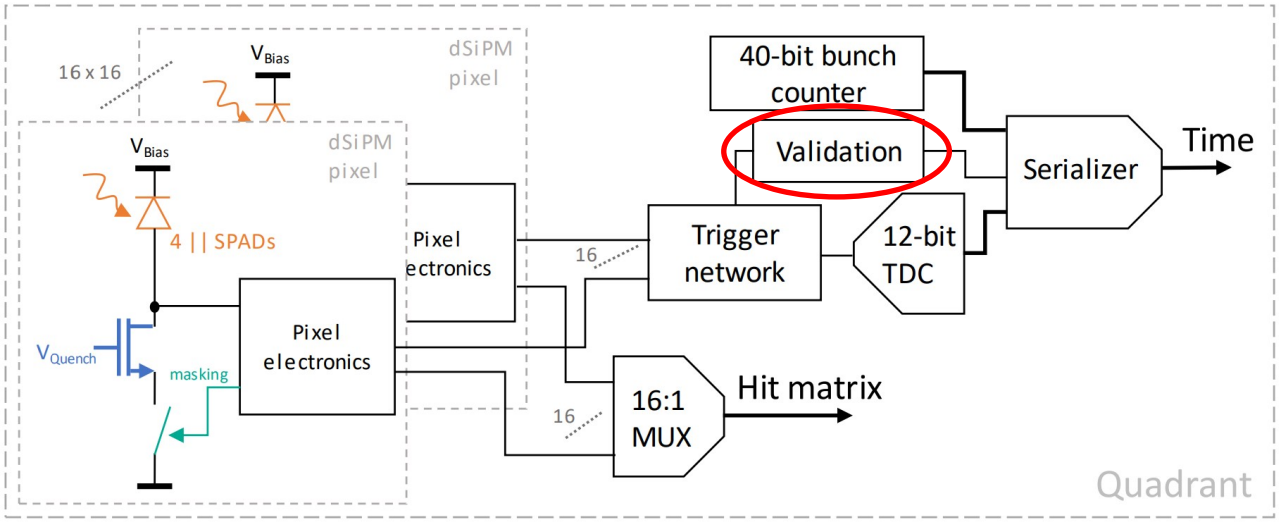
Digital ASIC Features

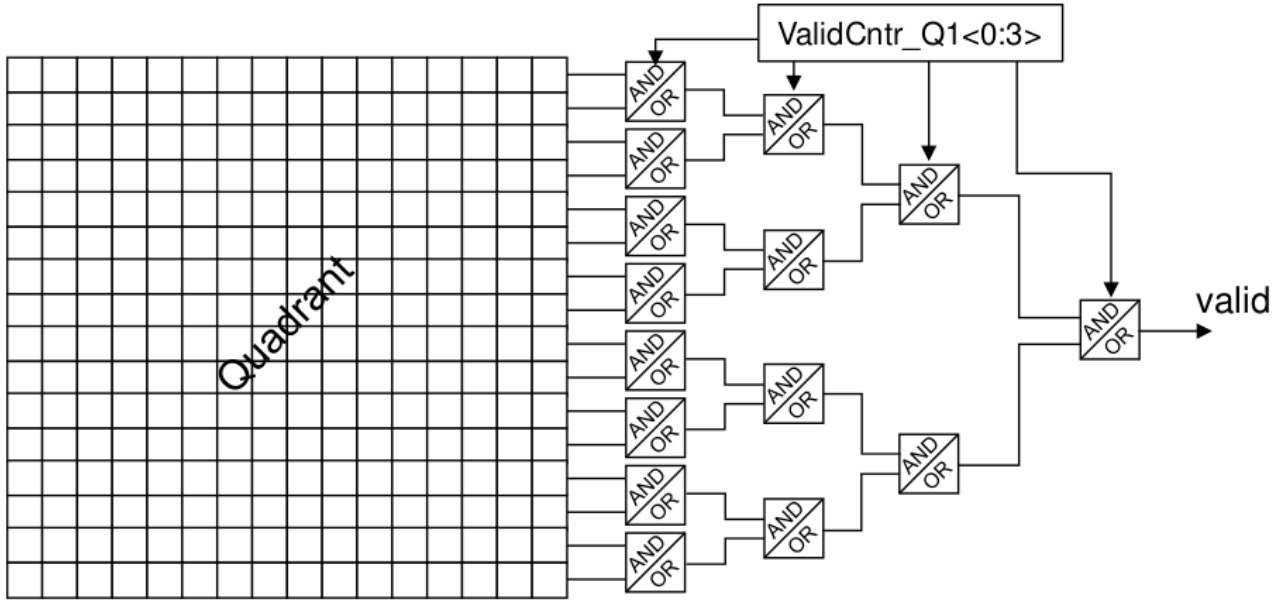
Frame-based readout

- Data taken in frames lasting ~333ns (3MHz clock)
- Four quadrants with one TDC each
  - First hit sets quadrant timestamp in frame

Validation Logic

- 4-step validation logic per quadrant
- Each step can be configured to be an AND or OR gate
- A valid bit is generated within 2ns
- Potential use-case: filtering of single pixel noise events in calorimeters





Wired-OR & TDC

Towards 4D Tracking with ps Resolution

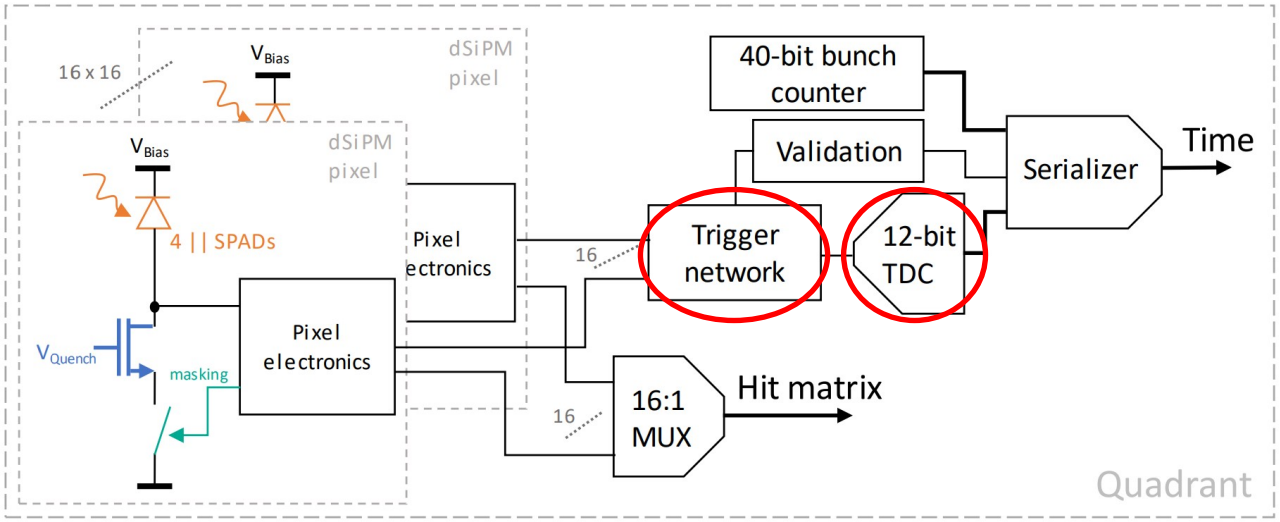
Fast wired-OR

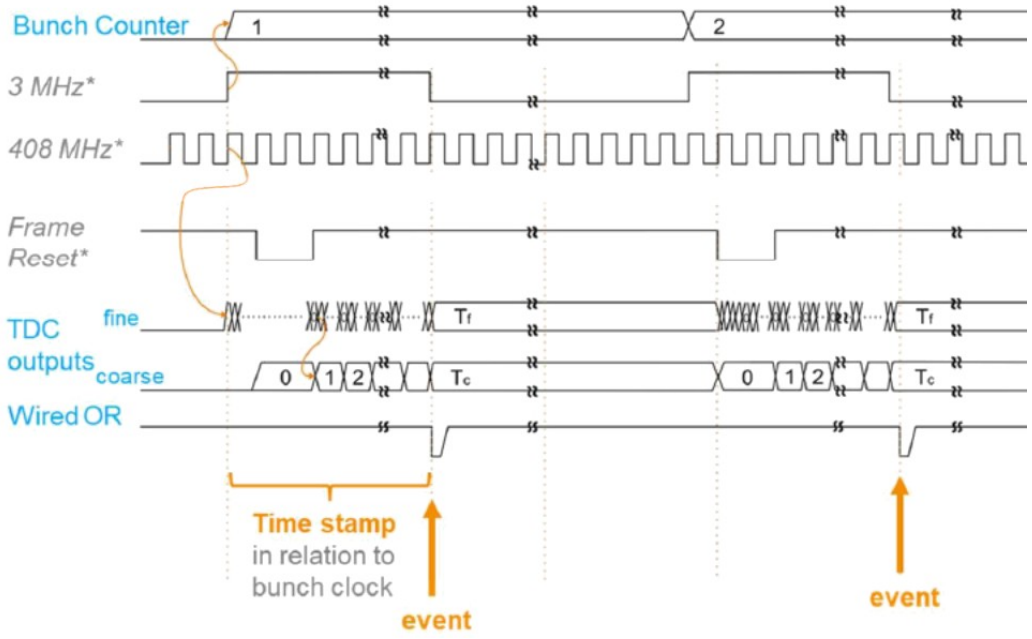
- Output of all pixels combined in wired-OR
- Potential use-case: fast trigger in testbeam

Time-to-Digital-Converter (TDC)

- Timestamp has three components:
  - Bunch Counter (3MHz 40-bit frame counter)
  - Coarse TDC (408Mhz 7-bit counter)
  - Fine TDC (5-bit ripple counter on top of 408MHz)

- When using external trigger, trigger timestamp also available from FPGA





Testbeam Studies

Work in Progress

- Studies on spatial resolution, efficiency and timing performance for MIPS detection @ DESY II
- In particular: coincidence measurement between two dSiPMs to measure time resolution of the chip
- Goal: evaluate dSiPM as detector for 4D-Tracking
- Analysis still ongoing
- More details in Gianpiero's presentation (https://indico.cern.ch/event/1232761/contributions/5321422/)