Simulations and Test Beam Characterization of a MAPS in 65 nm CMOS Imaging Technology

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11th Beam Telescopes and Test Beams Workshop Hamburg, April 19th 2023









The Tangerine Project



✓ Develop the next generation of silicon pixel sensors:

- Vertex detector for future lepton colliders
- Reference detector at DESY-II test beam







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- ✓ Performance parameters:
 - $\, {}^{\prime}\,$ Material budget: $\sim 50 \ \mu m$ silicon
 - ✓ Spatial resolution: \leq 3 µm
 - Time resolution: ~ ns





Monolithic Active Pixel Sensor (MAPS)



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Characteristics and Advantages

- Readout electronics integrated inside in sensor volume
- $\rightarrow\,$ reduction of costs and material
- ✓ 65 nm CMOS imaging process
- $\rightarrow\,$ improvement in logic density of pixels and power consumption
- ✓ Small collection electrode
- \rightarrow small capacitance
- \rightarrow improvement in S/N and power consumption



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It's not all fun and games...

Small pn-junction \rightarrow small depleted volume

 \rightarrow low efficiency and slow charge collection **Electric Field Optimization**

Sensor Design



collection

electrode

p-well electrode

p-well (electronics)

oxide layer

p-epitaxial layer

Sensor Modifications

Standard Layout

N ⁺	P ⁺		
P			
P ⁺			

N-blanket Layout



N-gap Layout



Sensor Modifications

Standard Layout

			L 1
N ⁺	D+		
	Ρ.		
P⁻			
P ⁺			

N-blanket Layout



N-gap Layout



Sensor layouts are studied with **simulations** and **prototype testing**

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Simulation Tools



- Model semiconductor fabrication and device operation
- ✓ Electric Fields: accurate and realistic



Electric field of MAPS near collection implant

S. Spannagel et al.

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Allpix²: Monte Carlo Simulations for Semiconductor Detectors S. Spannagel et al.

- Simulate full response of semiconductor detector
- ✓ Particle Events: fast and high statistics



TCAD Workflow | N-gap Layout

- ✓ Results in BTTB10
- Create realistic design with generic doping profiles
- Scans over different geometrical and functional parameters
- Observe the behavior of the electric field, lateral electric field and depleted volume
- ✓ Select sensible parameters



TCAD Workflow | N-gap Layout

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TCAD electric field input for **Monte-Carlo simulations** with Allpix² to produce performance plots.

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Prototype Testing



The Prototype

- ✓ International collaboration for common submissions to foundry with 65 nm CMOS process
- ✓ A first submission was done as a Multi Layer Reticle (MLR1)



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Analog Pixel Test Structure (APTS) W. Deng et al.

- ✓ Designed by ALICE
- ✓ Available in all layouts



- ✓ 4x4 pixels
- ✓ More about this in G. Alocco's talk



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The Test Beam

Facility

- Used for testing and characterizing new devices under realistic conditions
- Tests performed at DESY-II with 4 GeV e⁻ beam and MIMOSA26 telescope
 J. Dreyling-Eschweiler et al.
 H. Jansen et al.



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Inny

Setup

- ✓ Telescope: 6 detector planes perpendicular to beam \rightarrow tracking
- ✓ Trigger plane: Telepix (See A. Wintle's talk) L.Huth et al.
- ✓ DUT: Device Under Test \rightarrow placed in the center
- ✓ DAQ system based on Caribou
- Corryvreckan framework for track reconstruction
 D. Dannheim et al.



Data Analysis

Corryvreckan

- ✓ Particle tracks reconstructed with Telescope data
- ✓ DUT pulse shape per pixel acquired
- Threshold applied to pixel with highest charge (seed pixel) and surrounding pixels to form clusters
- Clusters associated to tracks
- Perform studies: detection efficiency, spatial resolution, charge distribution, etc.
- ✓ ADC units calibrated to charge
- ✓ 1000 ADC units ~ 200 e



Efficiency vs. Threshold

Simulation vs. Experiment

✓ Similar trend in experimental data and simulation



Experimental Data vs. Simulations

N-gap Layout 25

APTS 25 µm pitch Bias = -4.8 V

Efficiency vs. Threshold

Simulation vs. Experiment

- ✓ Similar trend in experimental data and simulation
- ✓ Experimental efficiency < simulated efficiency → might recover experimental efficiency with finer analysis



N-gap Layout 25

APTS 25 µm pitch Bias = -4.8 V





In-pixel Efficiency

Simulation vs. Experiment

✓ Efficiency affected by inner structures of pixel?

N-gap Layout

APTS 25 µm pitch Bias = -4.8 V Threshold = 200 e



In-pixel Efficiency

Simulation vs. Experiment

- Efficiency affected by inner structures of pixel?
- ✓ Fairly uniform in-pixel efficiency

N-gap Layout

 $\begin{array}{c} \text{APTS} \\ \text{25} \ \mu\text{m pitch} \\ \text{Bias} = -4.8 \ \text{V} \\ \text{Threshold} = 200 \ \text{e} \end{array}$

- Similar trend in experimental data and simulation
- Difference due low statistics in measurements



Charge Distribution

Simulation vs. Experiment

- Seed pixel: pixel with highest collected charge per event
- ✓ Charge Distribution: Landau*Gaussian
- ✓ MPV ~ 550 e
- Similar trend in experimental data and simulation



N-gap Layout

APTS

25 µm pitch

Conclusions

- ✓ First development cycle of a MAPS in a 65 nm CMOS Imaging Technology
- ✓ Detector Layouts: standard, n-blanket and n-gap
- ✓ TCAD simulations using generic doping profiles have provided very useful insights for future sensor optimization
- Monte Carlo simulations produced results comparable with measurements
- ✓ Beam test of Analog Pixel Test Structure (APTS), thanks to the ALICE collaboration and EP R&D
- ✓ Preliminary detection efficiency and charge collection results
- ✓ TCAD + Monte Carlo Simulations and experimental results follow a similar trend
- See other studies in the following talks by M. A. Del Rio Viera and S. Ruiz Daza!

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Prospective Work

- \checkmark More measurements \rightarrow more statistics
- Continue analysis of test beam data
- ✓ More studies, including spatial resolution and timing
- Validate TCAD + Monte Carlo Simulations
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Back-up

TCAD Workflow

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- ✓ Select sensible parameters



Combining Tools

TCAD + Monte Carlo Simulations

Performance parameters:

- Spatial resolution
- Timing resolution
- Detection efficiency

Why do we need to combine TCAD + Allpix²?

Electric Fields:

- Linear
- Customized (TCAD)



S. Spannagel et al. https://doi.org/10.1016/j.nima.2020.163784

APTS Operational Parameters

- ✓ Samples: 19 (AF25), 24 (AF25B), 29 (AF25P)
- ✔ Pitch: 25 µm
- ✓ Type: standard, n-blanket and n-gap
- ✓ Split: 4
- ✓ V_{sub} = V_{pwell} = -1.2 V, -2.4 V, -3.6 V, -4.8 V (,-5.2 V only for sample 19)
- ✓ $I_{reset} = 1 \ \mu A$
- ✓ I_{biasn} = 20 µA
- ✓ $I_{\text{biasp}} = 2 \ \mu A$
- ✓ I_{bias4} = 546 µA
- ✓ I_{bias3} = 200 µA
- ✓ V_{reset} = 0.5 V

Preliminary Fake-Hit Rate



Calibration

events

3000

2500

2000

1500

1000

500

0

800

- Test pulse measurements to characterize non-linearity and ~ pixel-to-pixel variations
- Apply inverse gain curve from test pulse measurements (per pixel)
- Perform ⁵⁵Fe measurements to determine absolute calibration factor
- Check calibration with Ti X-ray fluorescence ~

Entries

Std Dev

Constant

 χ^2 / ndf

Mean

Sigma

1000

Mean

Calibration for all samples and combinations of bias V voltage



1200

- data

F. Feindt

Selection Cuts

efficiency

0.9

0.8

0.7

0.6

0.5

0

20

60

- A cut is performed to associate tracks to DUT clusters
- Chosen cut at 30 μ m \rightarrow covering beyond full pixel to take into account tracking uncertainties



association cut [um]

Selection Cuts

- A cut at the sensor edge is performed to correct for the tracking uncertainties
- Chosen cut at 0.3 pixel fraction \rightarrow more than 2 times the tracking resolution

Total Effiency vs. Edge Cut