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Simulations and Test Beam Characterization of a MAPS in 65 nm CMOS Imaging Technology

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Monolithic CMOS sensors produced in a 65 nm imaging technology are being investigated for an application in particle physics for the first time. Their main characteristic is the integration of an active sensor and readout circuit in the same silicon wafer, which provides a reduction in material budget. Compared to the previously investigated 180 nm process, the 65 nm technology offers a significant improvement in the logic density of the pixels. The small collection electrode sensor is characterized by a low input capacitance, granting a high signal to noise ratio (S/N) and a low power consumption. The Tangerine project aims to develop the next generation of silicon pixel sensors intended as vertex detectors for future lepton colliders and as reference detectors in test beam measurements. The first sensor is envisioned to potentially be used as a telescope in the DESY-II test beam facility. TCAD Device and Monte Carlo simulations are used to develop an understanding of the sensor technology and provide important insight into performance parameters of the sensor. Prototypes are characterized in laboratory and test beam facilities by studying their charge collection, spatial resolution and efficiency. Combining results from all these studies it is possible to optimize the sensor layout. This contribution will present the first comparison of simulation results to test beam data of a 65 nm CMOS sensor with a small collection electrode.

Primary author: SIMANCAS, Adriana (Deutsches Elektronen-Synchrotron (DE))

Co-authors: VELYKA, Anastasiia; FEINDT, Finn (Deutsches Elektronen-Synchrotron (DE)); VIGNOLA, Gianpiero (Deutsches Elektronen-Synchrotron (DE)); WENNLÖF, Håkan (Deutsches Elektronen-Synchrotron (DE)); SPANNAGEL, Simon (Deutsches Elektronen-Synchrotron (DE))

Presenter: SIMANCAS, Adriana (Deutsches Elektronen-Synchrotron (DE))

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