

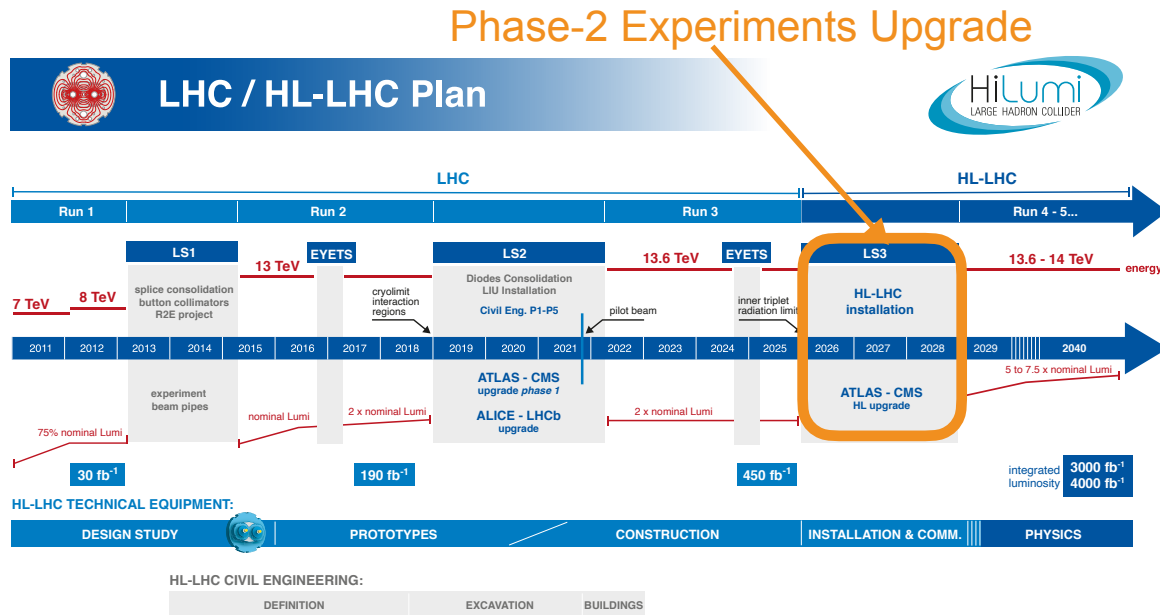
Younes Otarid

On behalf of the DESY CMS Phase 2 Tracker Team

Test-beam qualification of a Pixel-Strip module for the CMS Tracker Phase-2 Upgrade

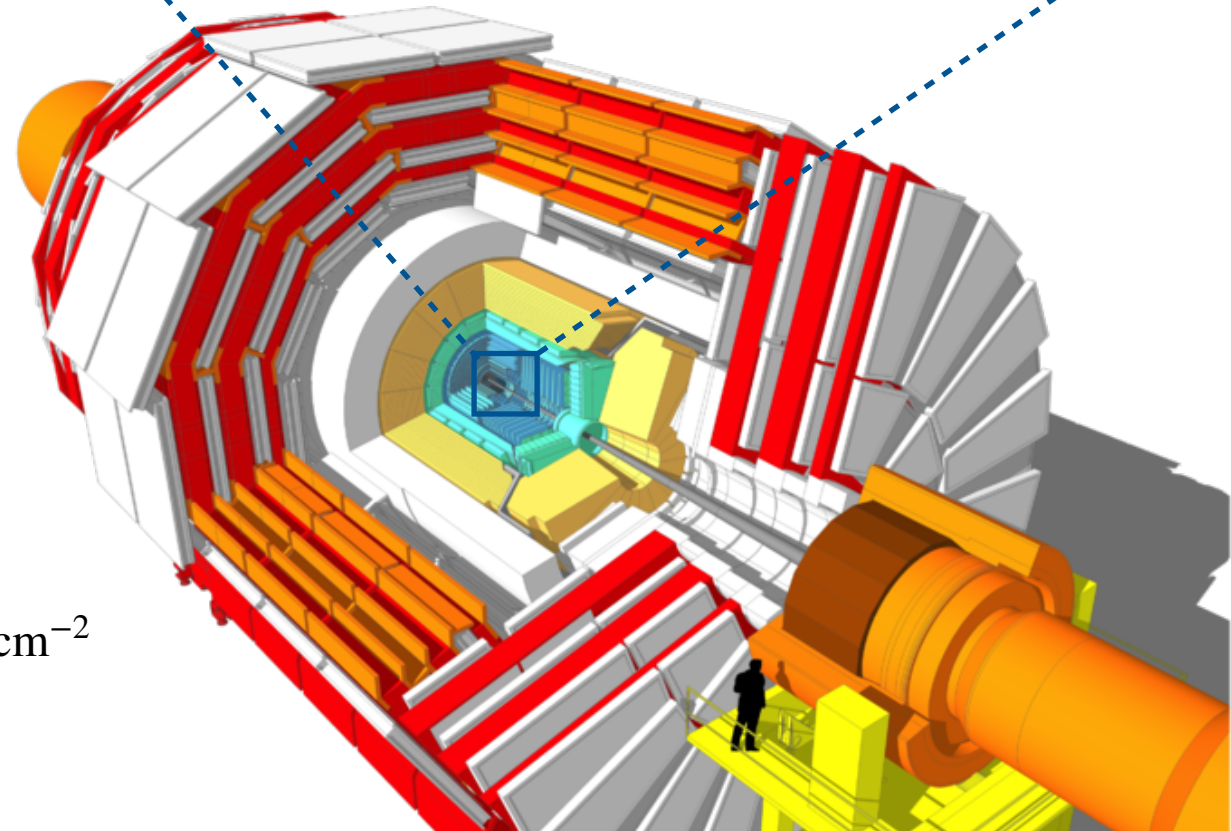
BEAM TELESCOPES AND TEST BEAMS WORKSHOP
17.04.2023

Introduction



New Tracker

- Radiation tolerant - higher granularity - less material
- Tracks in hardware trigger (L1)
- Coverage up to $\eta = 4$

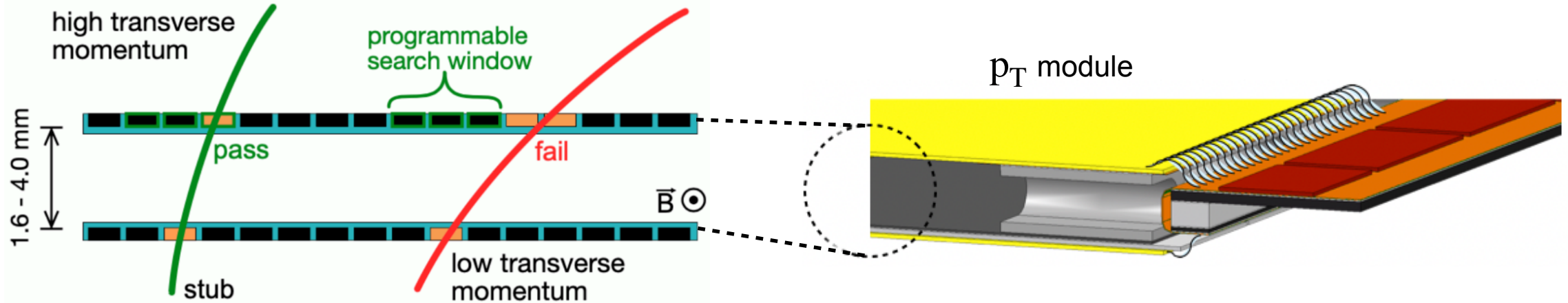


Accelerator performance :

- Peak instantaneous luminosity $5 - 7.5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$
- $300 \text{fb}^{-1} / \text{year}$ and up to 3000fb^{-1} over 10 years

CMS environment :

- Unprecedented radiation levels up to $1.1 \times 10^{15} \text{n}_{\text{eq}} \times \text{cm}^{-2}$
- 10 times higher pile-up
- Higher data rates

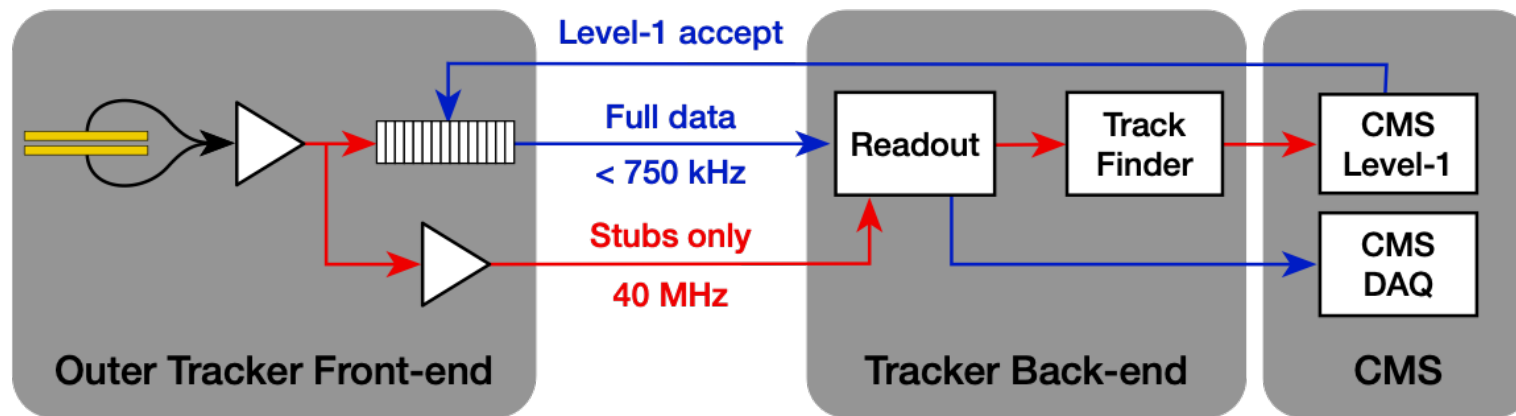


Modules with on-board p_T discrimination

- Strong magnetic field exploited for local p_T measurement
- Correlation of signals from two closely spaced sensors
- Local rejection of low- p_T tracks to reduce data volume

Modules provide both Level-1 and readout data

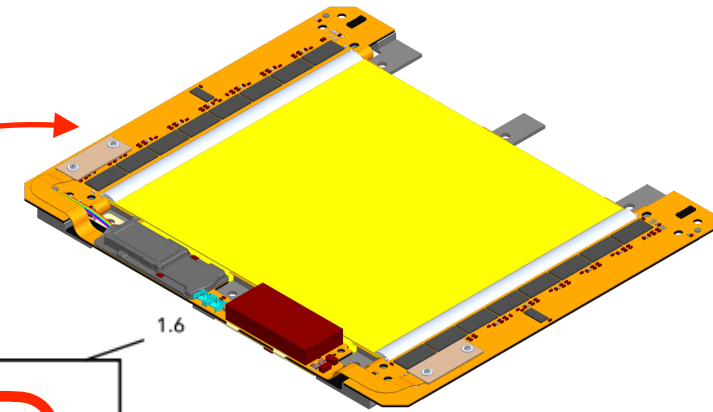
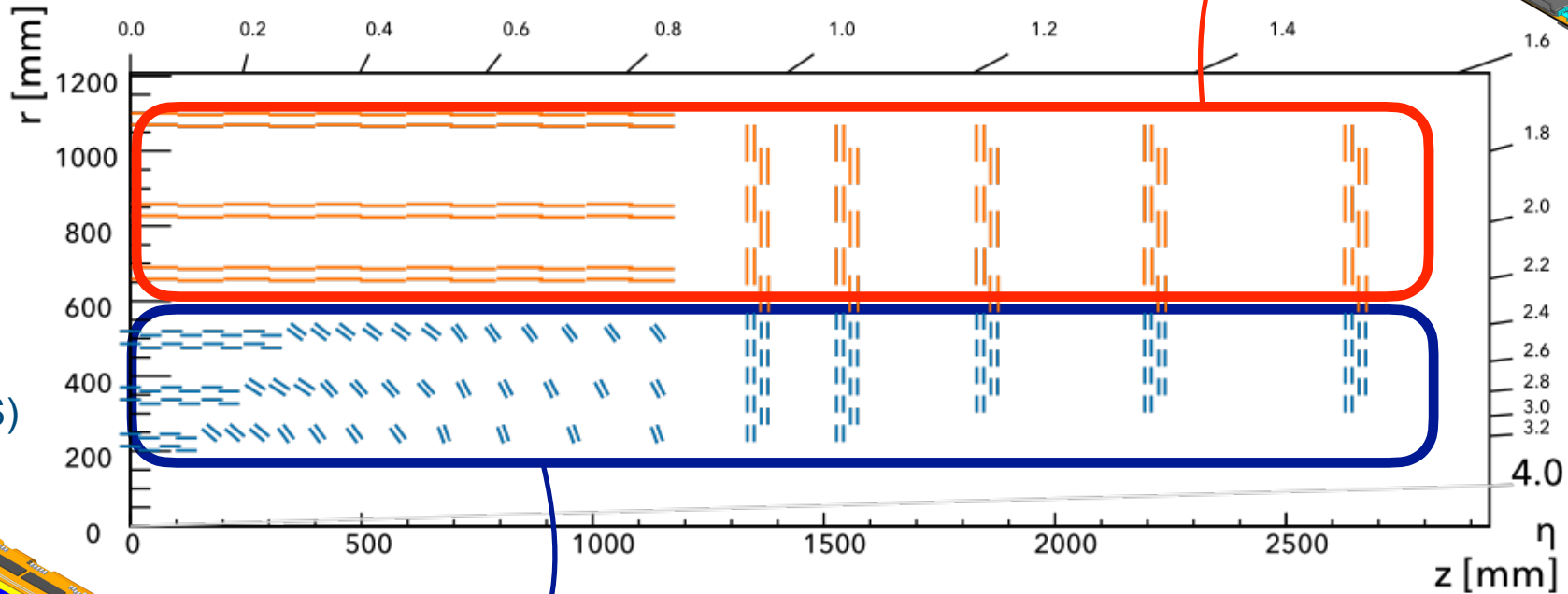
- Level-1 Trigger primitives ("stubs") sent @40MHz
- Full data readout rate up to 750KHz
- "stubs" are used to form Level-1 Track Finding



CMS Outer Tracker upgrade

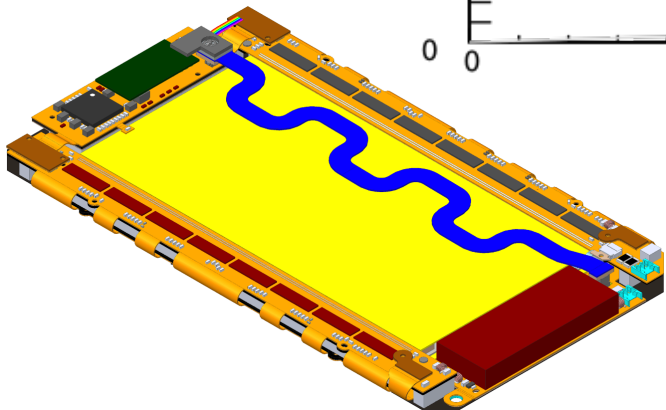
Layout with 6 barrel layers and 5 end cap double disks

- Stack of two strip sensors at $r > 60$ cm (2S)
- Sensor spacings : 1.8 mm and 4 mm



Strip-Strip (2S) Modules

Pixel-Strip (PS) Modules



- Stack of pixel and strip sensor at $r < 60$ cm (PS)
- Sensor spacings : 1.6 mm, 2.6 mm and 4 mm

Pixel-Strip module design

Front-End Hybrid

- *Single-Strip ASIC (SSA)*
- *Concentrator Integrated Circuit (CIC)*
- Handles signal from strip sensor
- Transfers data to MPA
- Aggregates data from MPA

Power Tail

Read-Out Hybrid

- *Low-power Gigabit Transceiver ASIC*
- *VTRx+ optical module*
- Transmits data over optical fibre

Power Hybrid

- *DC-DC converter*
- Distributes power

Silicon Strip Sensor

- *10 x 5 cm Silicon Strip Sensor*
- *2.5 cm long strips, 100 μ m pitch*

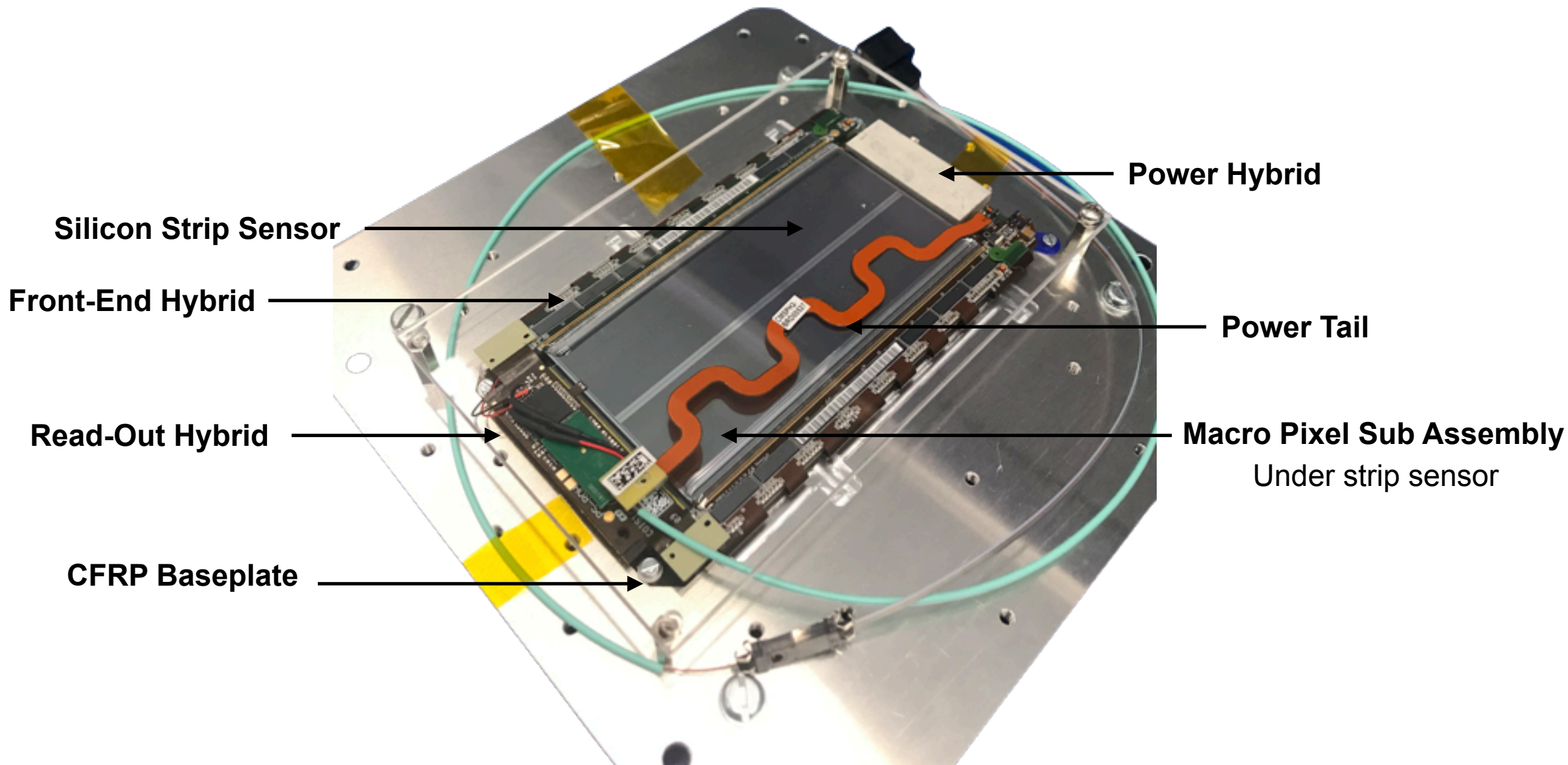
AIN Spacers

Macro Pixel Sub Assembly (MaPSA)

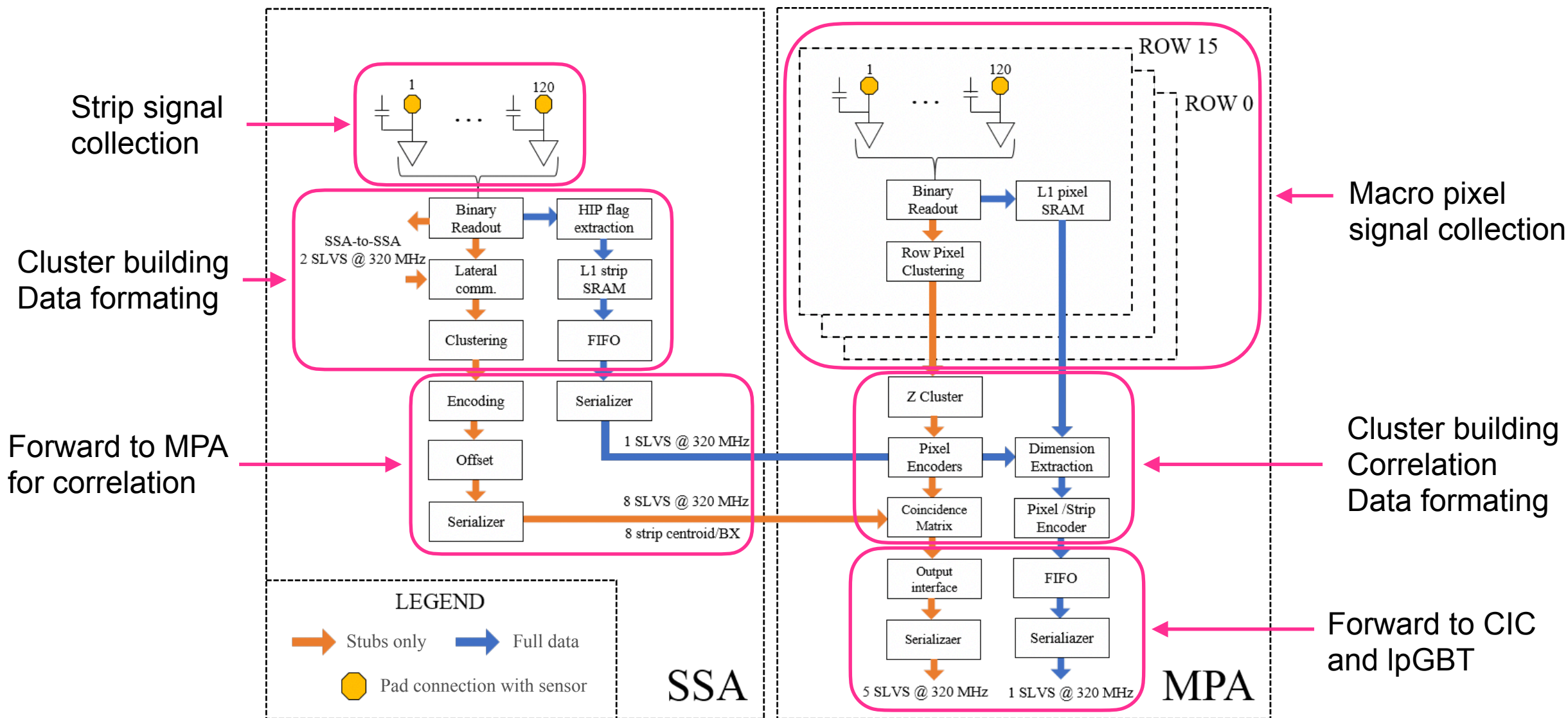
- *Macro Pixel ASIC (MPA)*
- *Macro Pixel Silicon sensor 1400 x 100 μ m*
- Handles signal from pixel sensor
- Receives data from SSA
- Correlates signals from both sensors

CFRP Baseplate

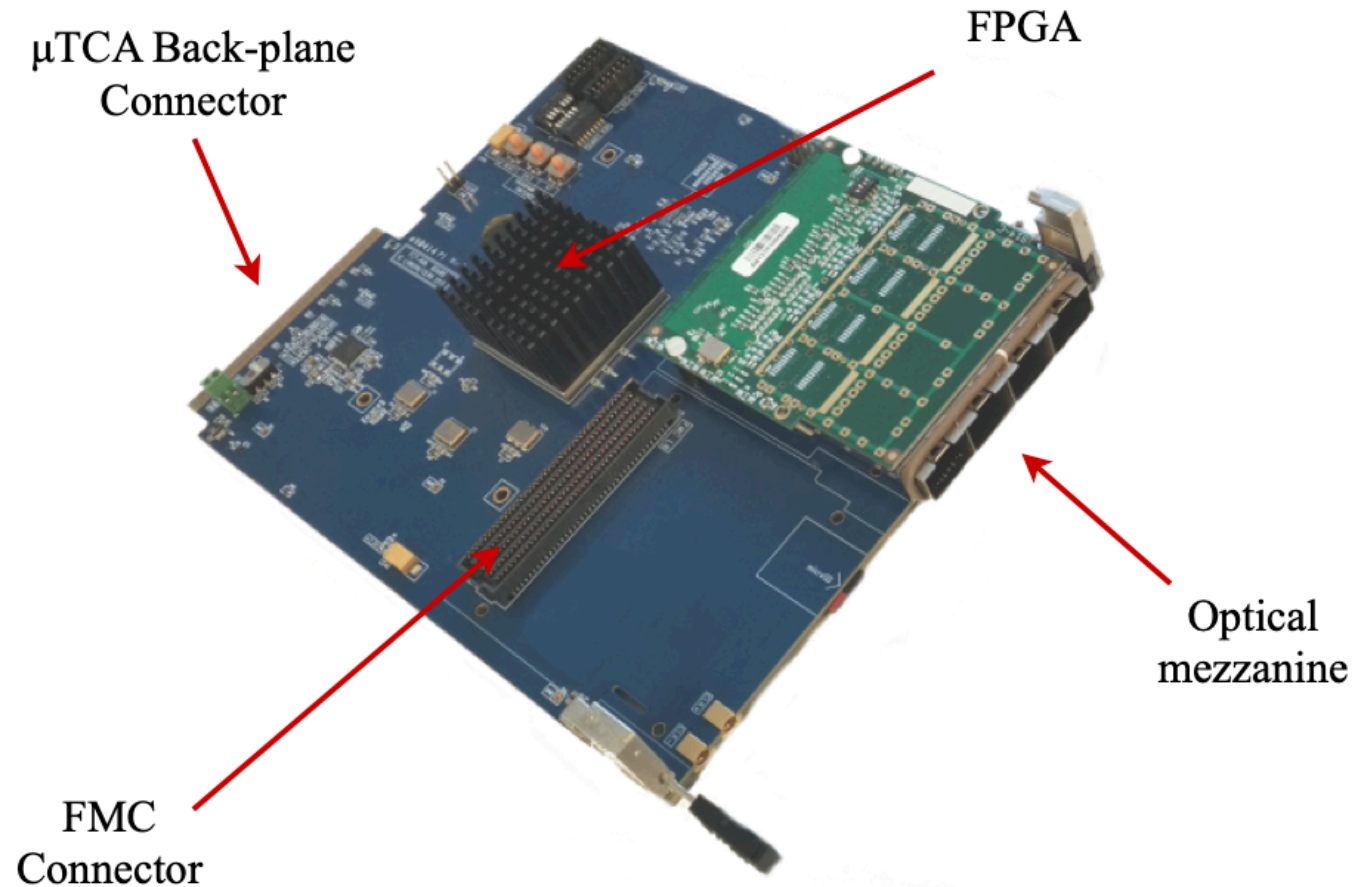
Pixel-Strip module assembly



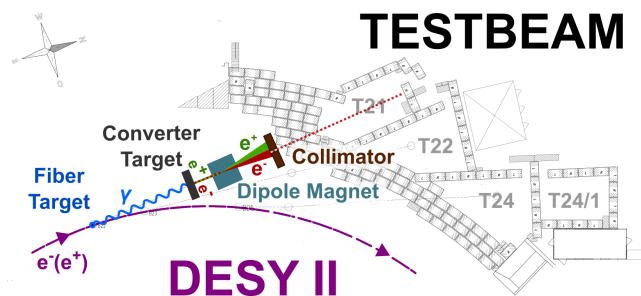
Front-end data flow (MPA-SSA)



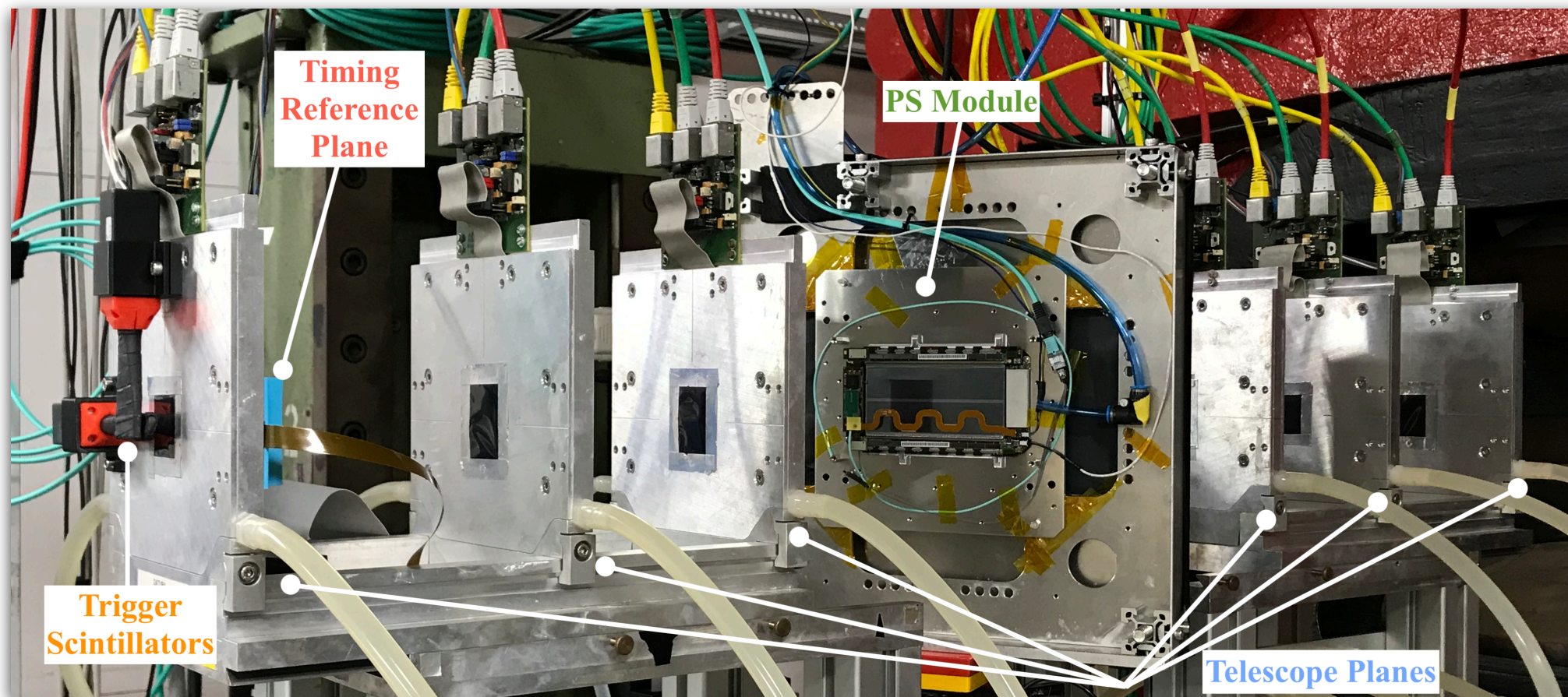
- Exploits **FC7** MTCA-compatible AMC for generic data acquisition and control applications
 - Kintex-7 FPGA
 - 2 FMC Connectors
 - Advanced clock distribution system
 - External DDR3 memory
 - ...
- Several custom interface are supported by the system in case of needed synchronous operation
 - Trigger Logic Unit (TLU)
 - DIO5 (5 LEMO I/O)
 - ...



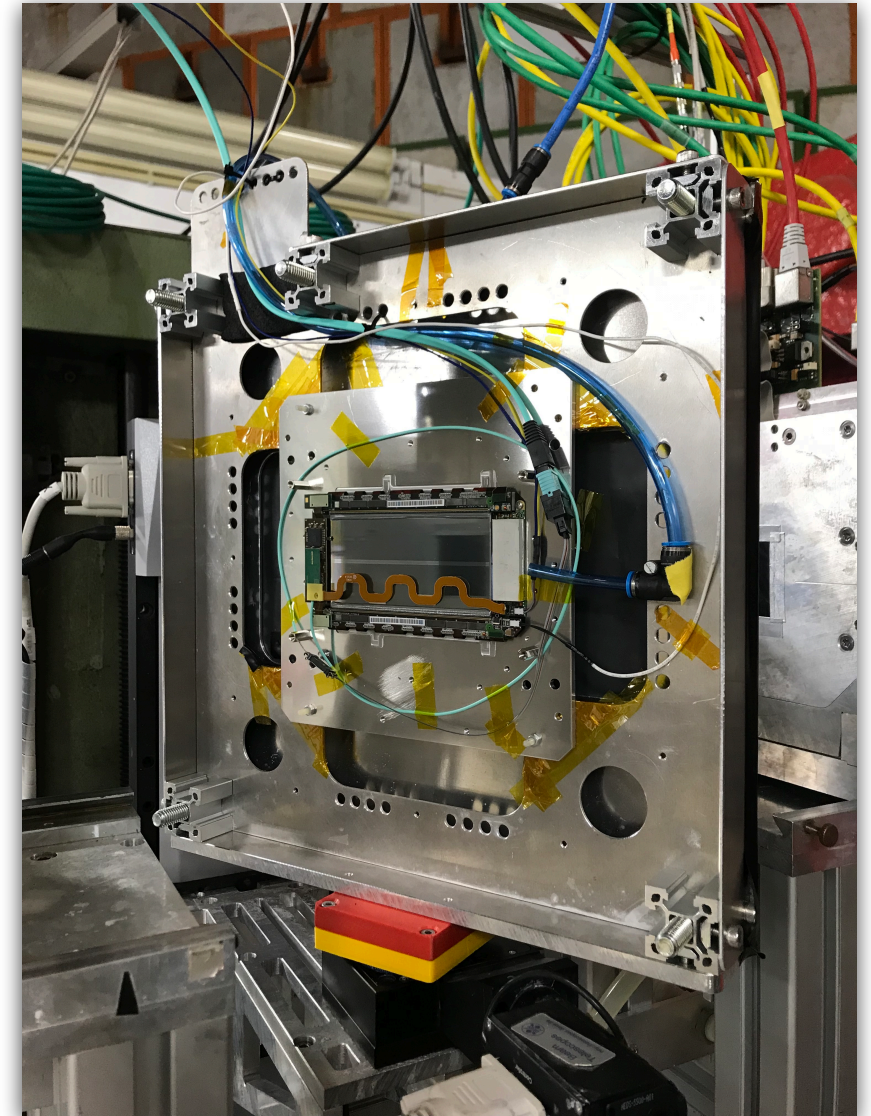
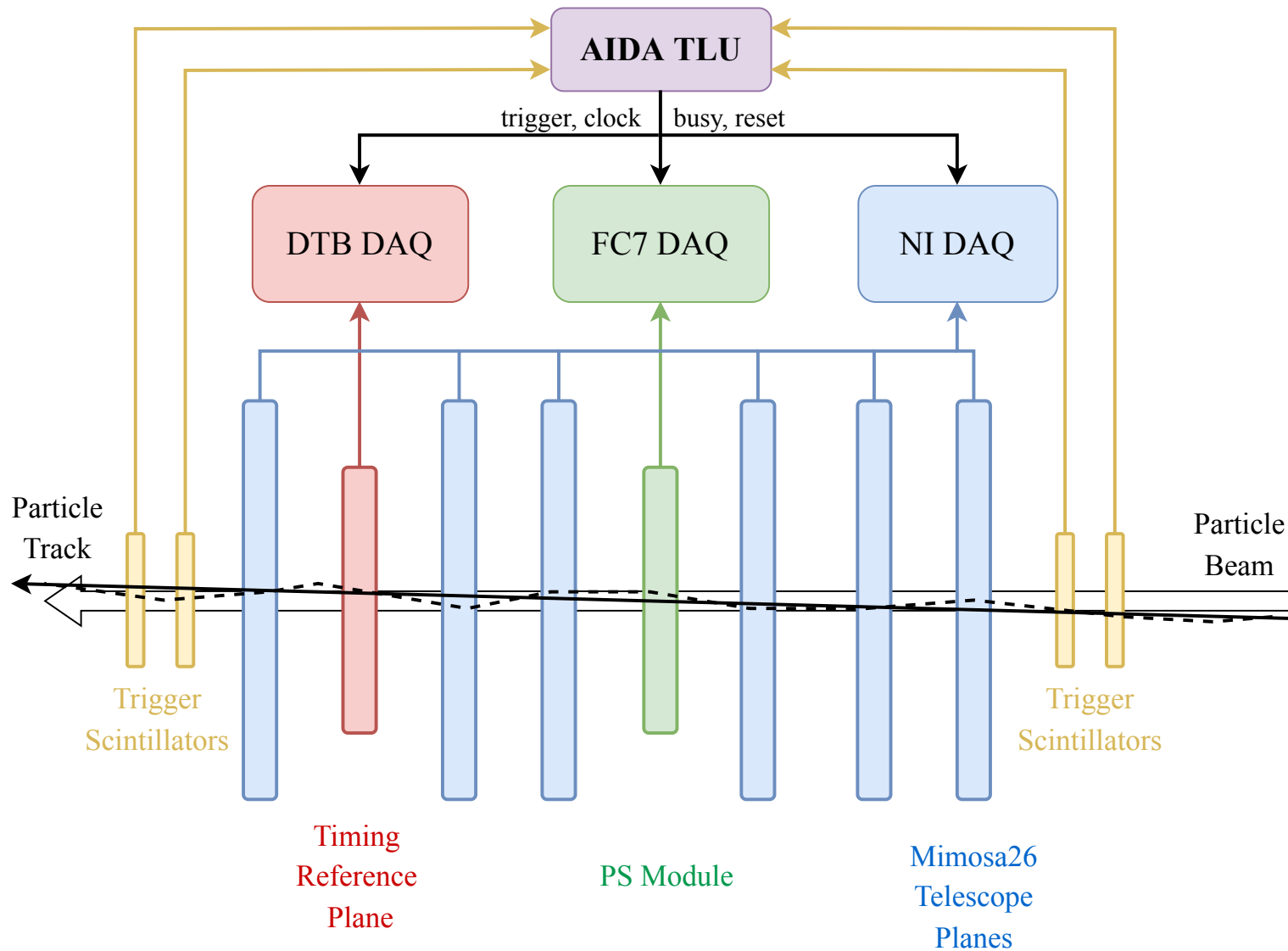
Test-Beam Qualification

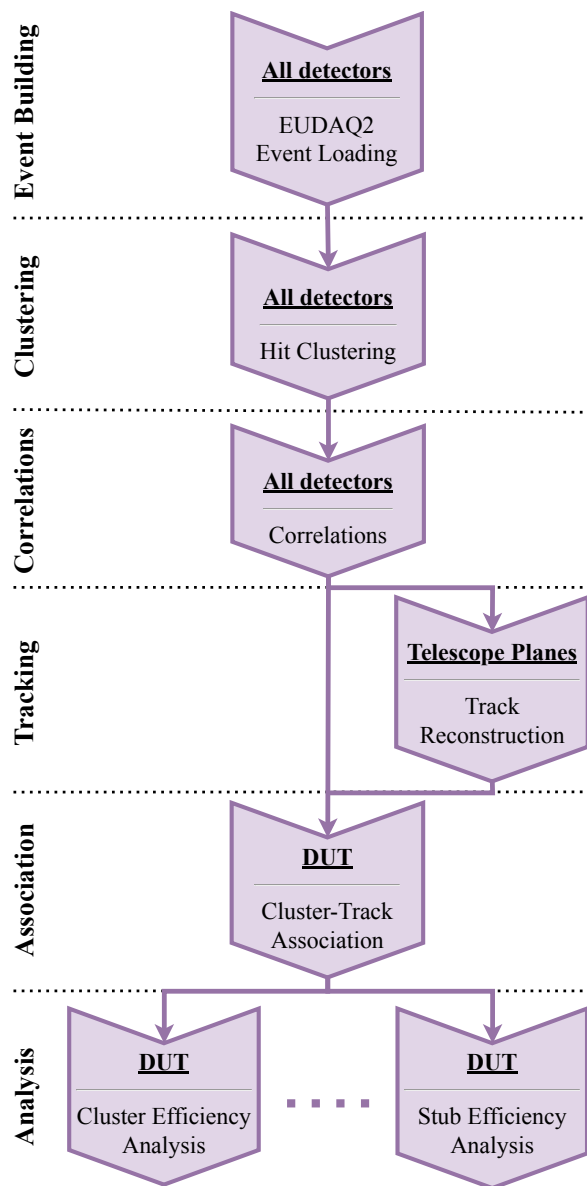


- 4 GeV/c electron beam
- Datura Beam Telescope
- CMS BPIX reference plane
- Trigger scintillators
- AIDA TLU
- EUDAQ2



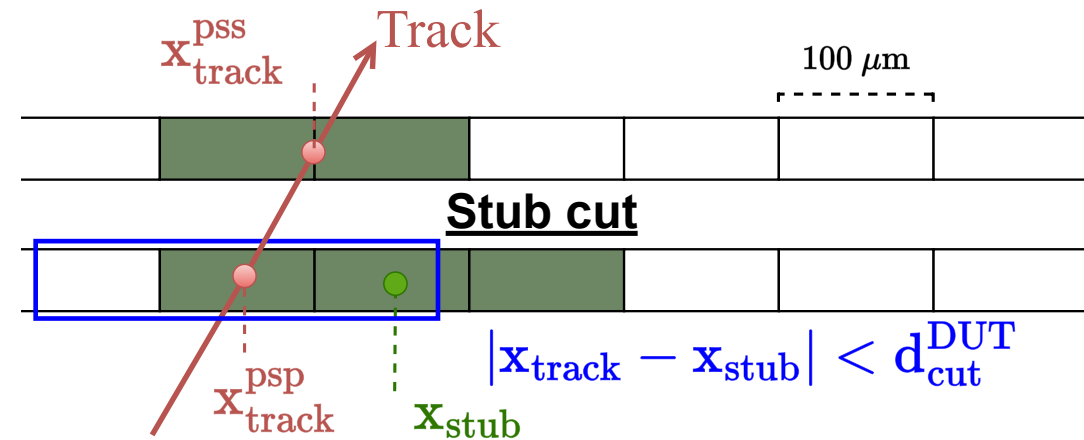
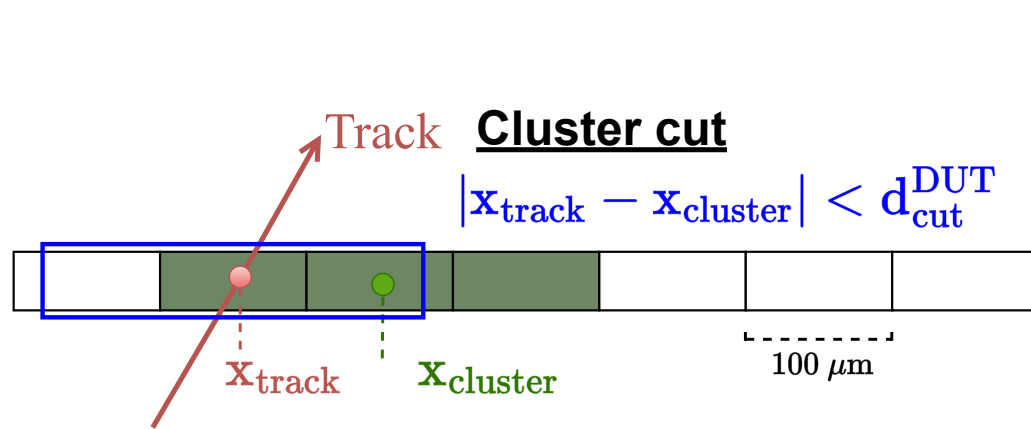
Data acquisition scheme





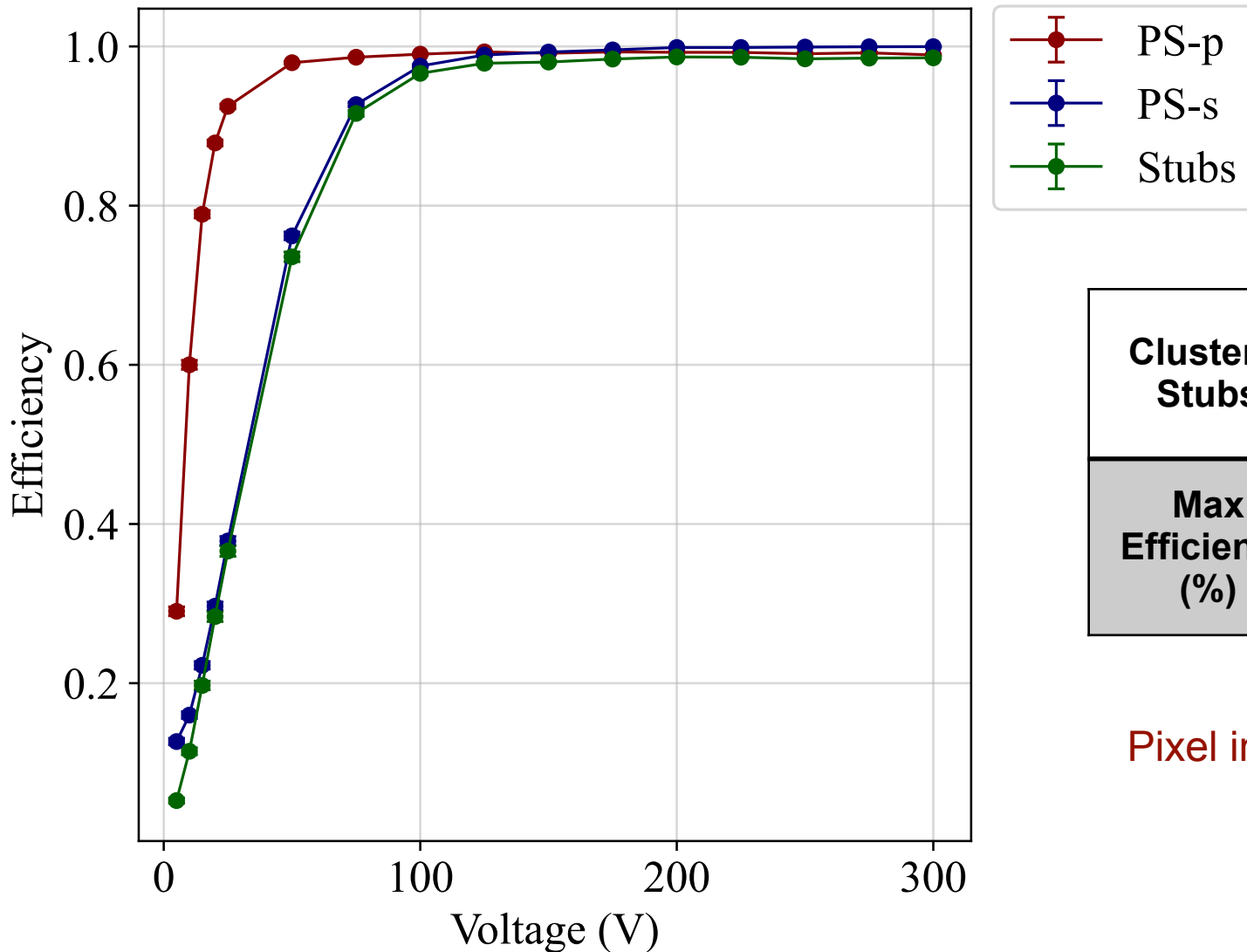
- Iterative pre-alignment using *Prealignment* module and *maximum* method
- Iterative alignment using *AlignmentDUTResidual* module and *GBL* model
- New EUDAQ Tag-based event filtering feature implemented (merged)
- New *BigPixelDetector* module implemented to support BPIX reference module pixel geometry (not merged)
- Cluster efficiency studies using *AnalysisEfficiency* module
- Cluster size and resolution studies using *AnalysisDUT* module
- *AnalysisStubEfficiency* module implemented for *stub* analysis (not merged)

$$\epsilon_{\text{clusters/stubs}} = \frac{n_{\text{efficient clusters/stubs}}}{n_{\text{ref tracks}}} = \frac{\text{telescope tracks} \in \text{DUT}_{\text{clusters/stubs}} \cap \text{REF}}{\text{telescope tracks} \in \text{REF}}$$



$$|x_{\text{track}}^{\text{psp}} - x_{\text{cluster}}^{\text{psp}}| \leq 200 \mu\text{m} \quad ; \quad |y_{\text{track}}^{\text{psp}} - y_{\text{cluster}}^{\text{psp}}| \leq 3000 \mu\text{m} \quad \left. \vphantom{|x_{\text{track}}^{\text{psp}} - x_{\text{cluster}}^{\text{psp}}|} \right\} \text{PS-p clusters}$$

$$\text{PS-s clusters} \quad \left\{ \begin{array}{l} |x_{\text{track}}^{\text{psp}} - x_{\text{cluster}}^{\text{psp}}| \leq 200 \mu\text{m} \quad ; \quad |y_{\text{track}}^{\text{psp}} - y_{\text{cluster}}^{\text{psp}}| \leq 25000 \mu\text{m} \\ |x_{\text{track}}^{\text{psp}} - x_{\text{stub}}^{\text{psp}}| \leq 200 \mu\text{m} \quad ; \quad |y_{\text{track}}^{\text{psp}} - y_{\text{stub}}^{\text{psp}}| \leq 3000 \mu\text{m} \end{array} \right. \text{Stubs}$$

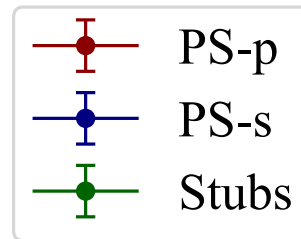
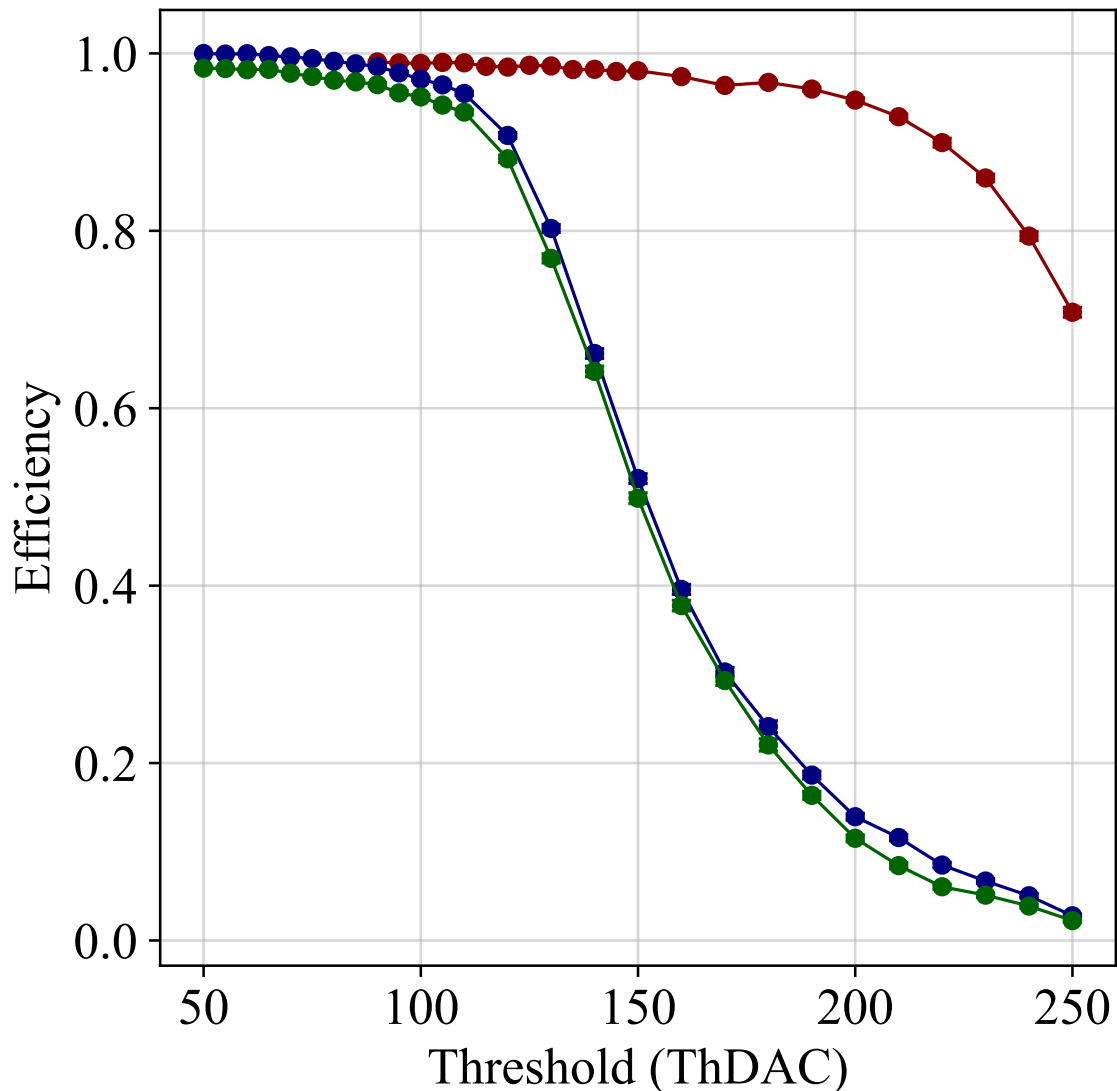


Determination of optimal operation point of bias voltage

Clusters/ Stubs	PS-p	PS-s	Stubs
Max Efficiency (%)	99.31	99.97	98.68

Pixel inefficiency caused by PS-p bias structure
Punch-Through Structure (PTS)

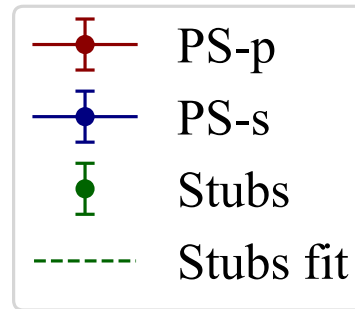
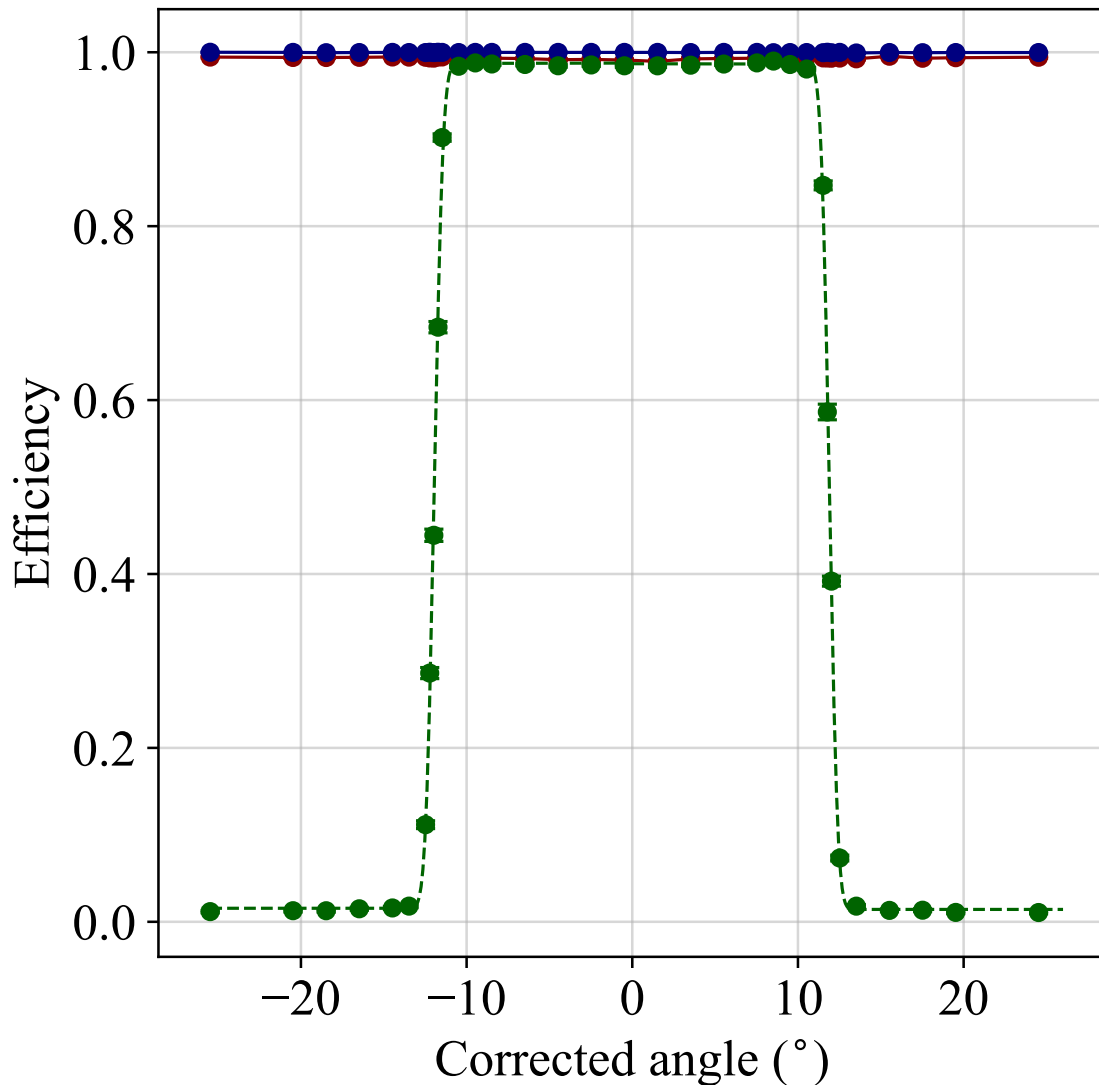
Efficiency - Threshold scan



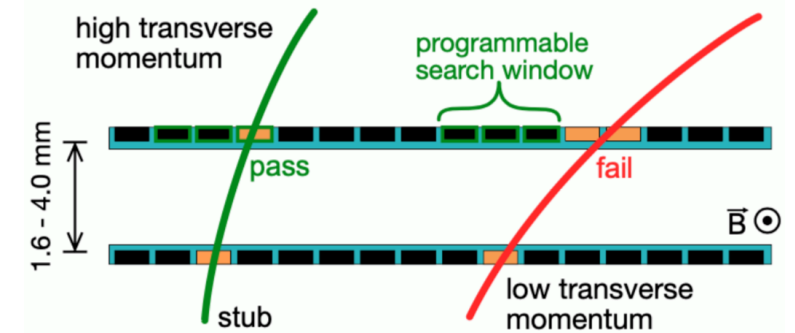
Determination of optimal operation point of signal threshold

Clusters/ Stubs	PS-p	PS-s	Stubs
Max Efficiency (%)	99.03	99.98	98.33

Pixel inefficiency caused by PS-p bias structure
Punch-Through Structure (PTS)



Module rotated to emulate bending particles and p_T discrimination



Clusters/ Stubs	PS-p	PS-s	Stubs
Max Efficiency (%)	99.54	99.99	98.98

Stub efficiency drop at approximately +/- 12°
 Stub logic (p_T discrimination) working as expected

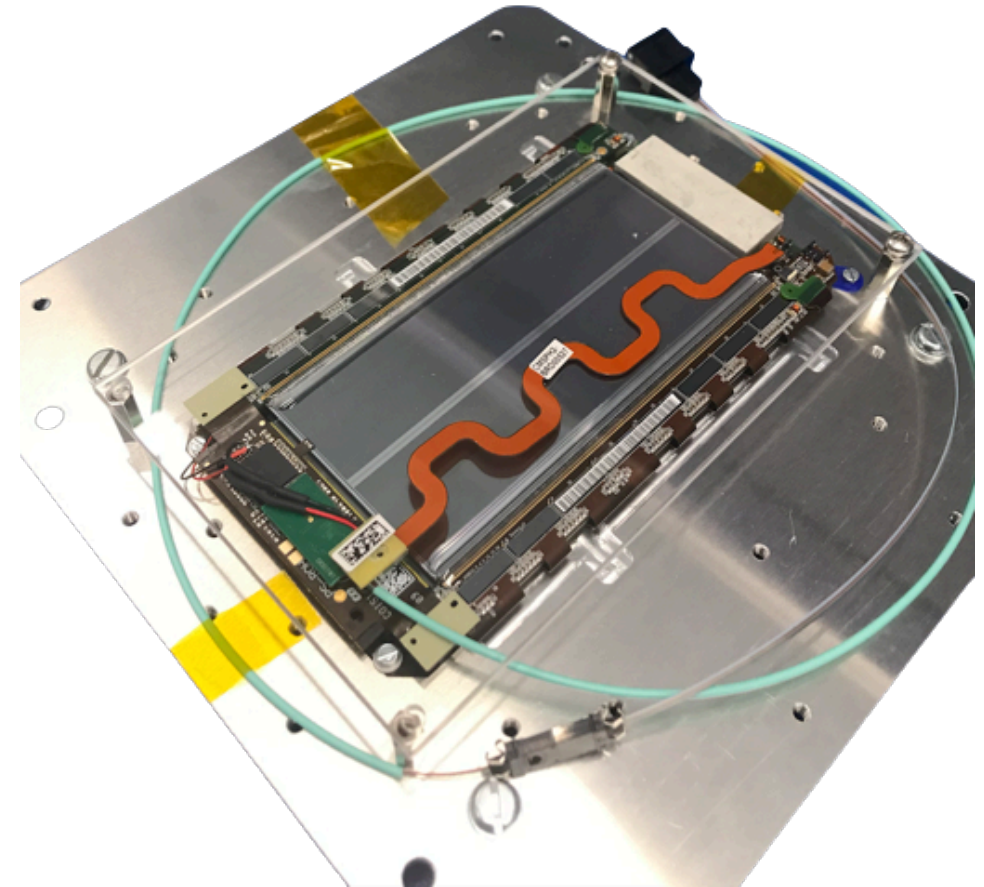
Conclusion

Summary

- Introduction of new Tracker module design for the needs of High Luminosity LHC upgrade
- Momentum discriminating design based on cluster correlation between two closely stacked Silicon sensors
- Pixel-Strip module test-beam qualification results yield excellent efficiency and p_T discrimination performance
- *The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)".*

Outlook

- New modules to be assembled with latest hybrid circuit designs
- Performance studies to be reiterated and complemented using irradiated modules



THANK YOU.

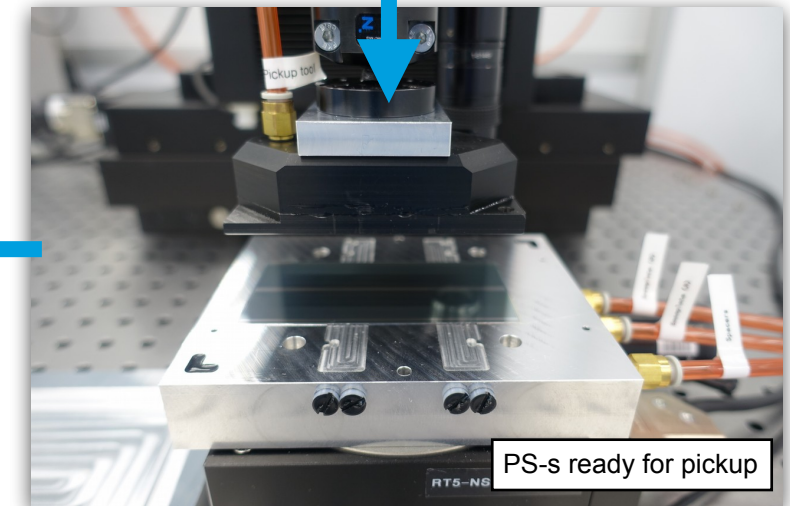
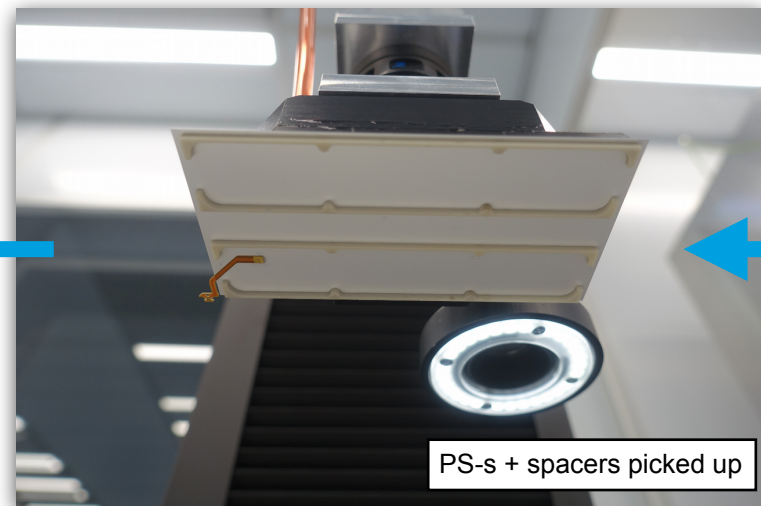
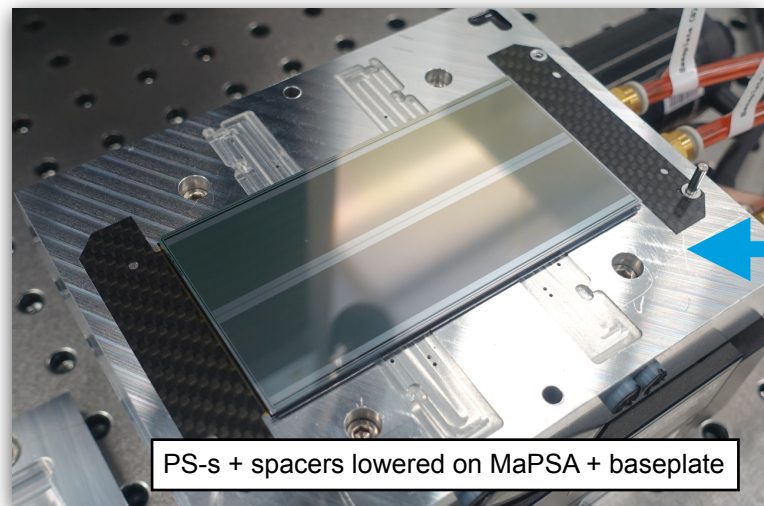
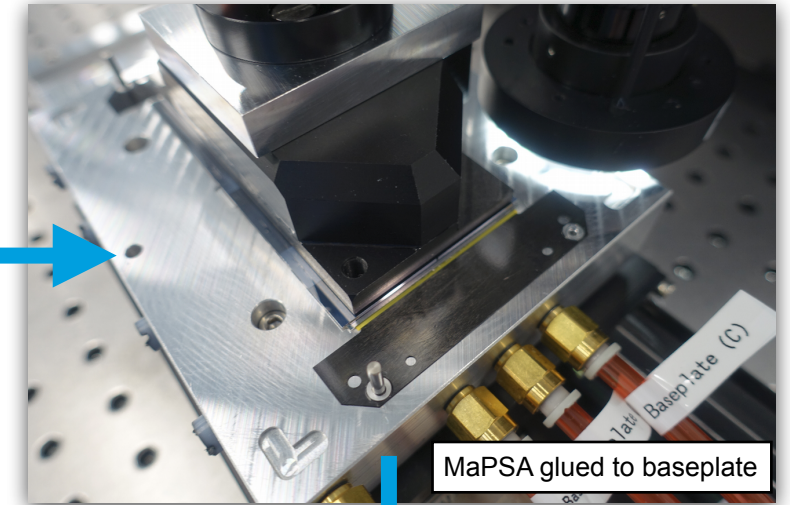
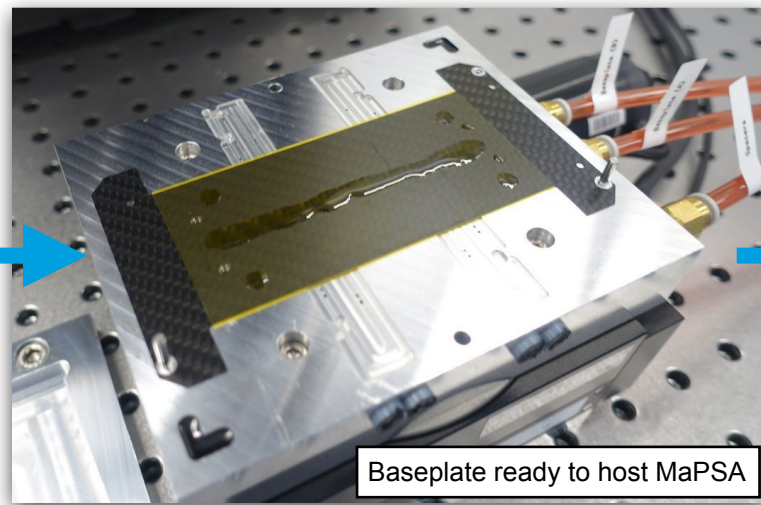
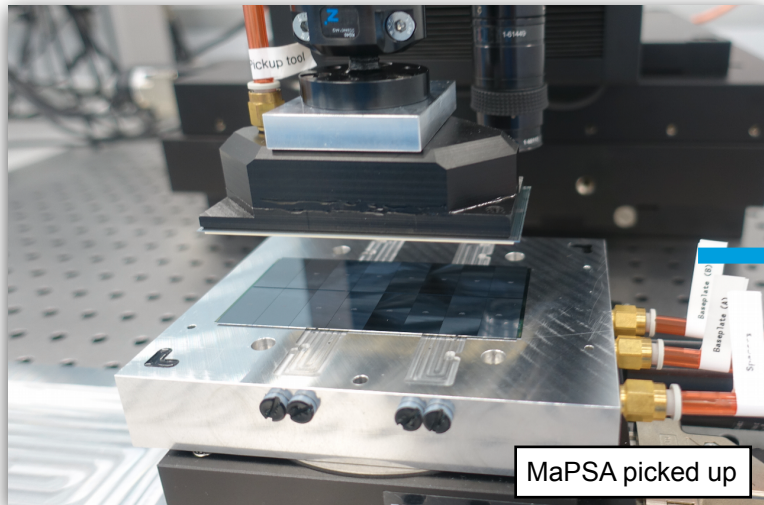
Contact

DESY. Deutsches
Elektronen-Synchrotron

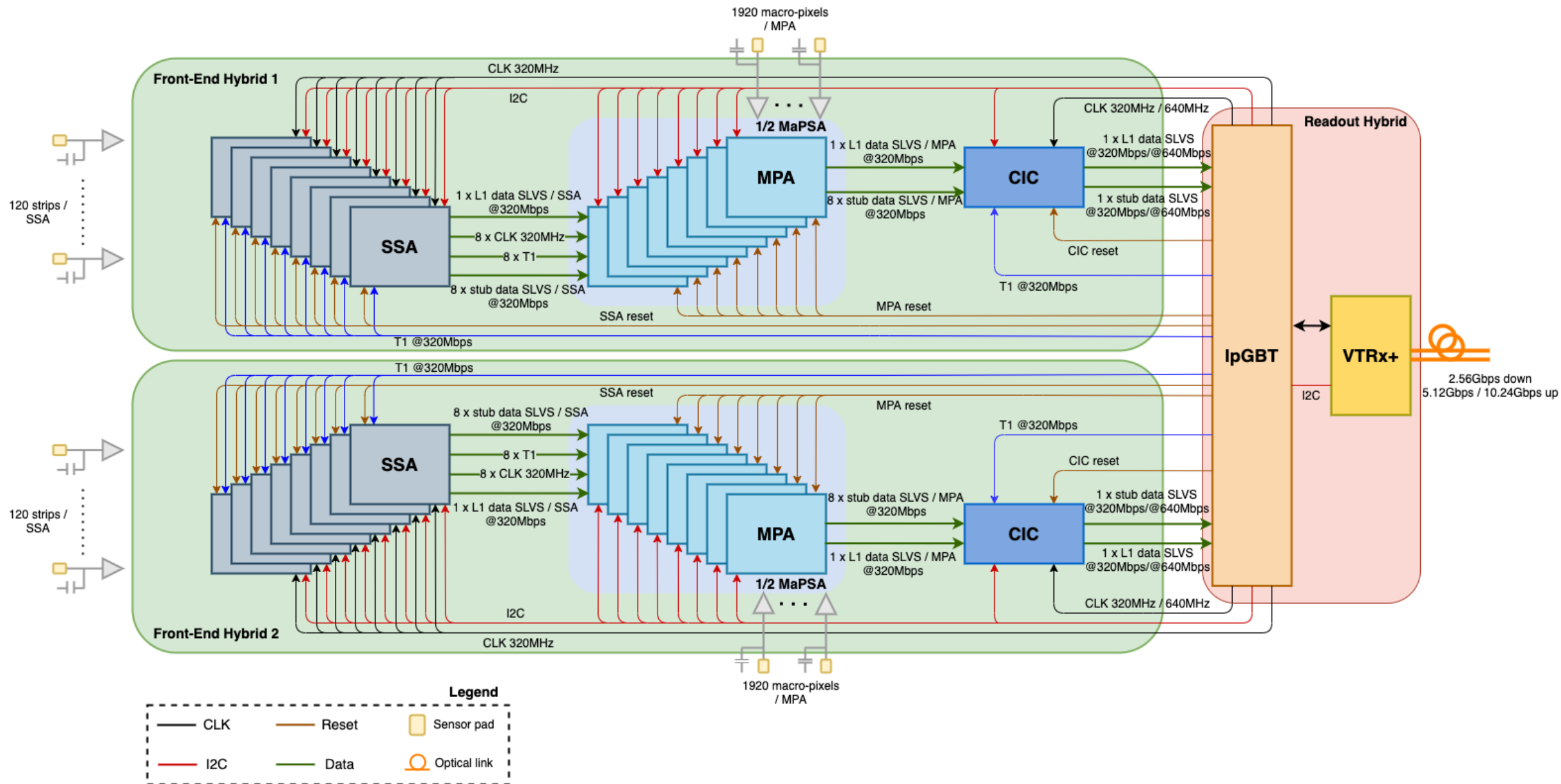
www.desy.de

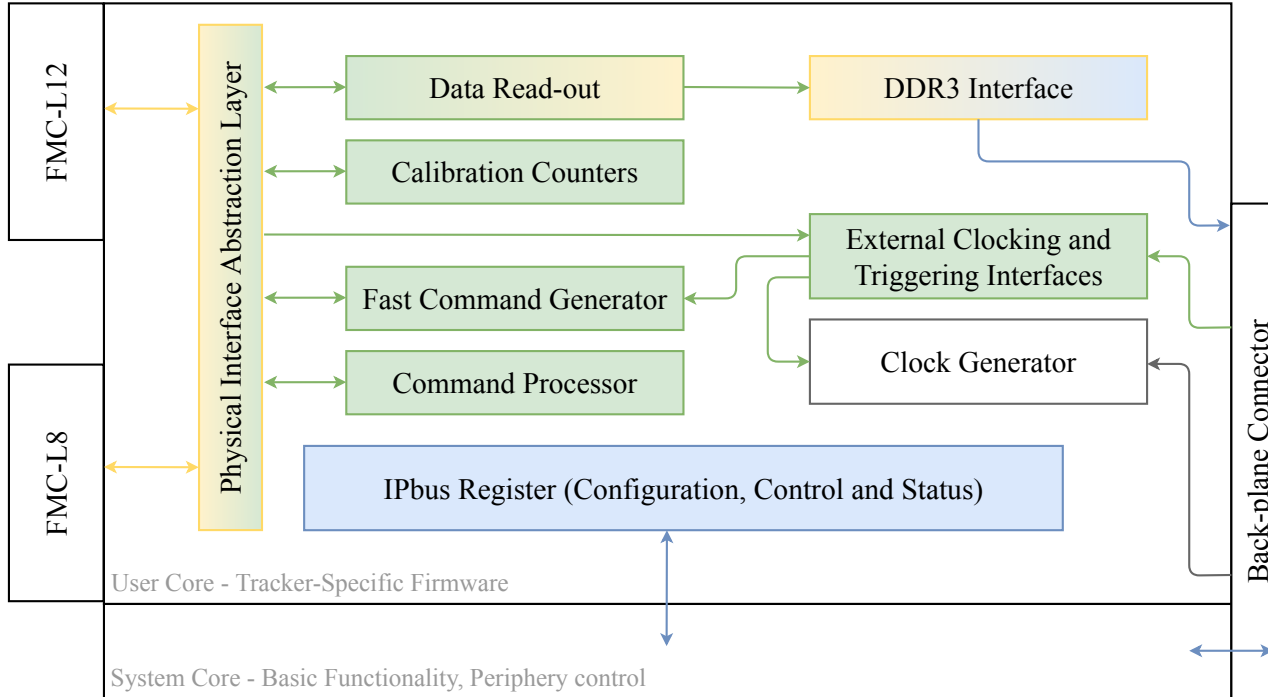
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Pixel-Strip silicon module assembly



Front-end architecture





Clock Domains :



Firmware development specifically dedicated to the prototyping and production phases of the CMS Tracker Phase II Upgrade

IPbus registers :

- Configuration, control or status monitoring

Clock Generator :

- 40MHz to 640MHz clock generation and distribution

Fast Command Generator :

- Interface for synchronisation, calibration and trigger fast signals

Command Processor :

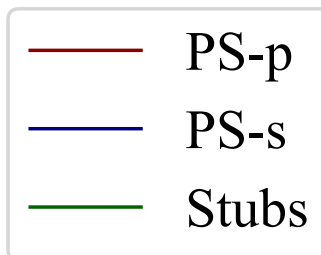
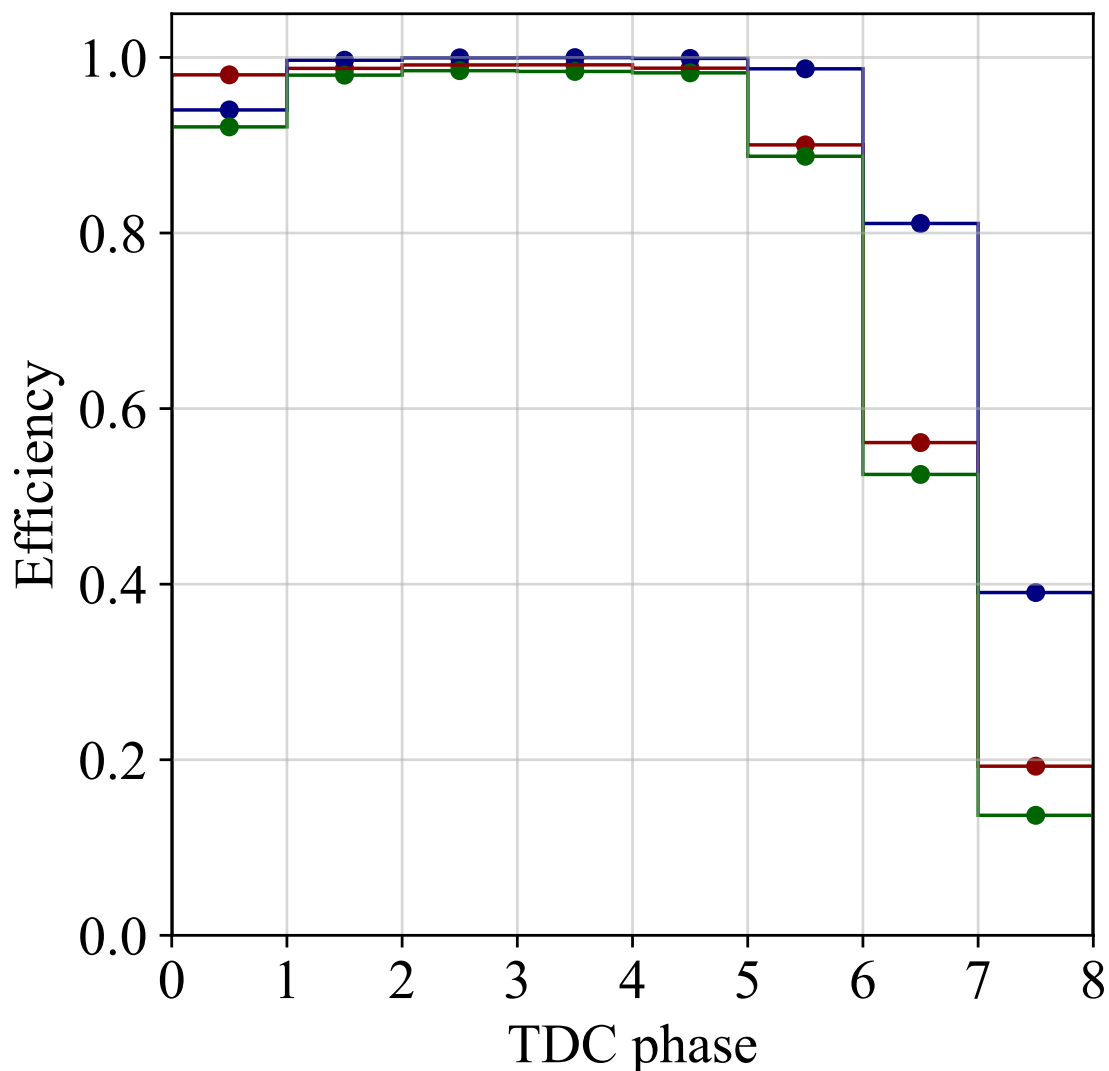
- Slow control, configuration and calibration

Physical Interface Abstraction Layer :

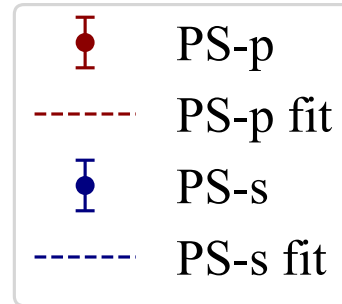
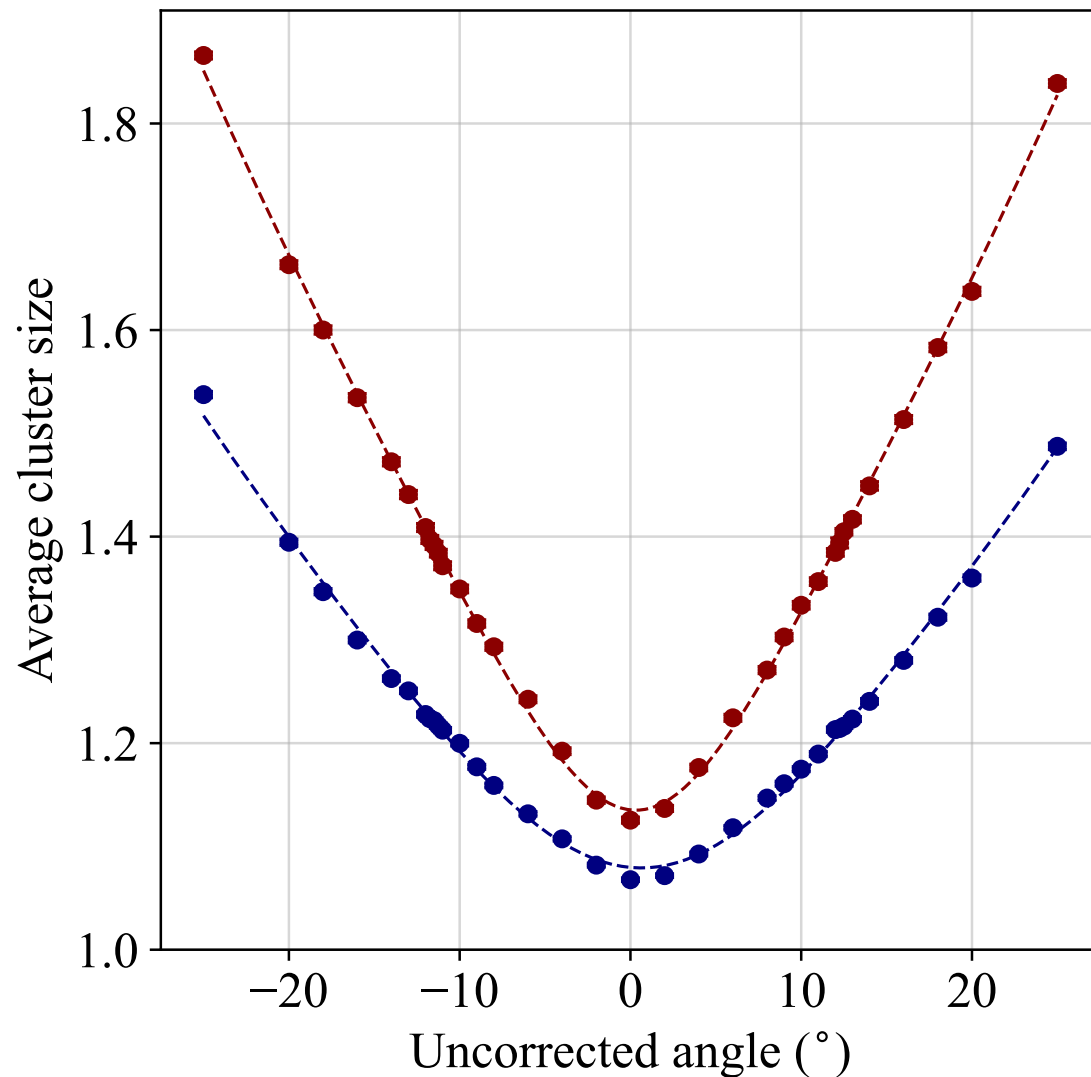
- Abstract interface for optical or electrical readout

Data Readout :

- Processing and aggregation of data from all connected front-end modules/components

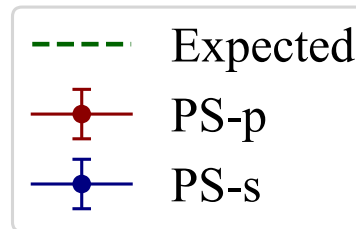
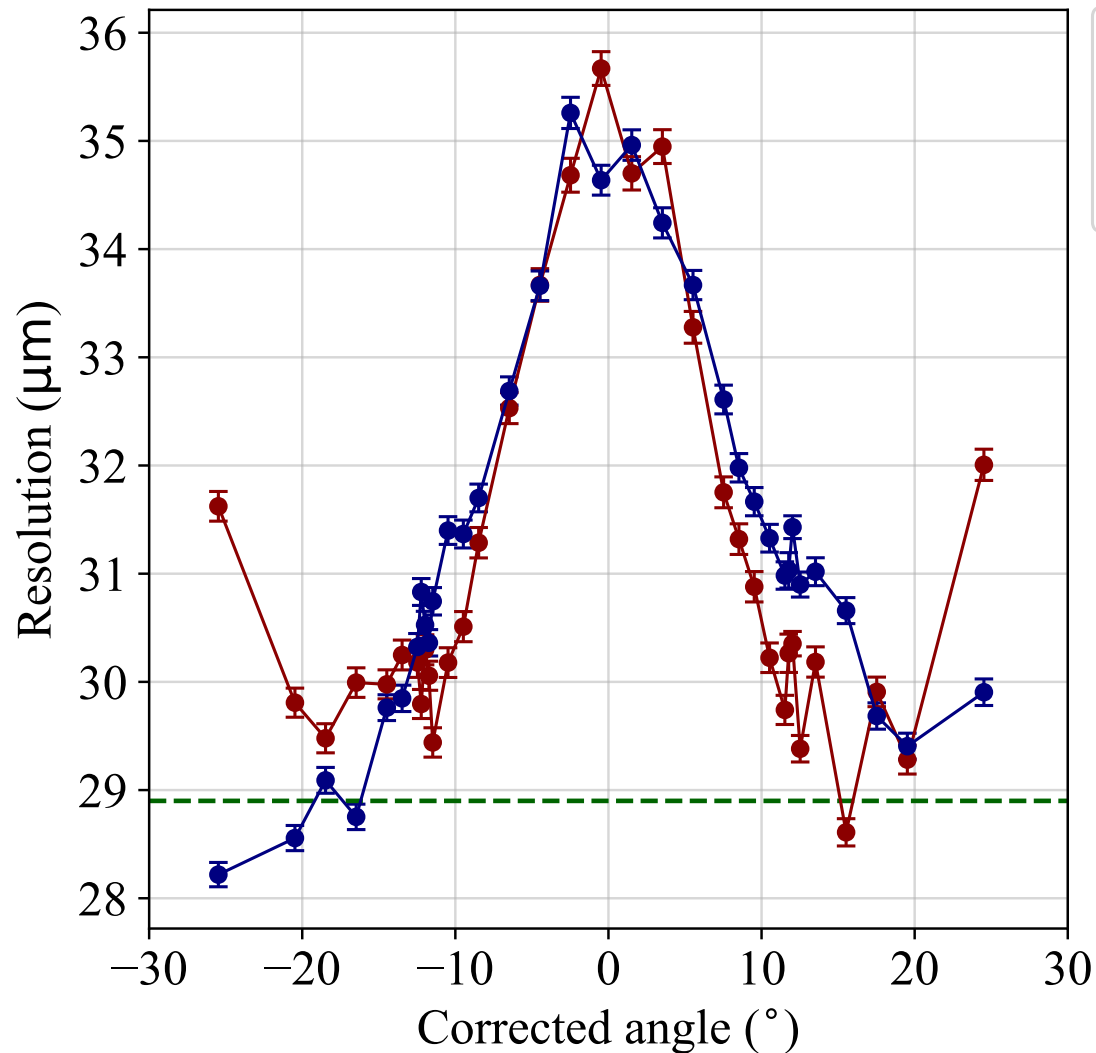


1. DAQ and accelerator clock asynchronous
 - ==> Random trigger arrival time
2. DAQ 40 MHz clock sampled at 320 MHz
3. Efficiency subject to TDC phase dependency over 8 bins
4. Selection of high efficiency TDC phases



Determination of cluster size as a function of rotation angle

- PS-p and PS-s differences due to the different signal thresholds used for the MPA and SSA chips
- Increasing cluster size due to charge sharing
- Distributions also used to extract physical misalignment of the module on the rotation stage



Determination of pixel and strip resolutions as a function of rotation angle

- Lack of statistics exacerbated by further event filtering and strong fluctuations still to be understood
- Resolution measured as $\sigma_{\text{int}} = \sqrt{\sigma_{\text{meas}}^2 - \sigma_{\text{tel}}^2}$
 - σ_{meas} taken as RMS of residual distribution
 - $\sigma_{\text{tel}} = 9.15 \mu\text{m}$ extracted from resolution simulator
- Improved resolution with increasing angle due to charge sharing
- Maximum resolution close to expected $p/\sqrt{12}$ at around 15°