Towards a time-resolved RICH detector

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***On behalf of the LHCb-RICH Collaboration**

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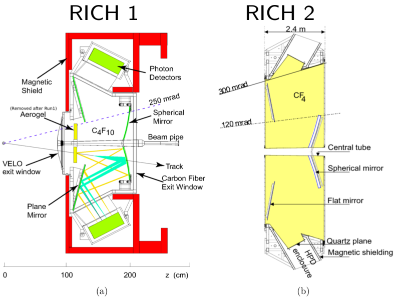
The LHCb-RICH detector

The 2 RICHes provide the PID of charged hadrons in final state: π, K e p

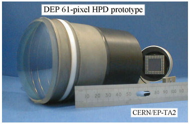
- RICH1
  - Radiator: C_4F_{10}
  - p $\in$ [1-65] GeV/c
- RICH2
  - Radiator: CF_4
  - p $\in$ [15-100] GeV/c

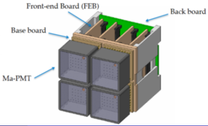


Photodetectors:

- Old RICH (Run 1 and Run 2): Hybrid Photon Detectors
- Pixel size: $2.5 \times 2.5mm^2$

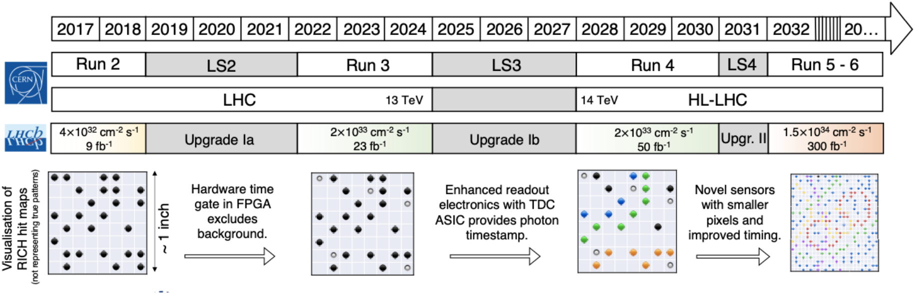
- New RICH (Run 3): MaPMTs
- Pixel size: $3 \times 3mm^2$ (R-type) or $6 \times 6mm^2$ (H-type)





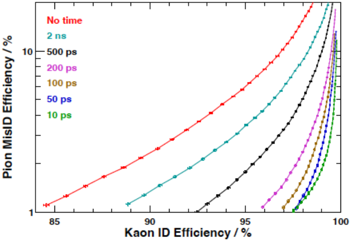
Why we need timing information

- Measuring the time of arrival of the photons is crucial to maintain the excellent performances of the current RICH system throughout the HL-LHC phase after the start of Run 4

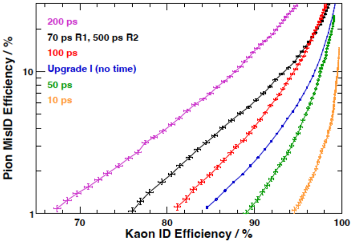


What time resolution do we need?

- The RICH performance is assessed by looking at the PID curves
- Given that the majority of tracks are pions, we look at the curve $\Delta\ln\mathcal{L}(K-\pi) \rightarrow$ Kaon ID efficiency against pion misID efficiency



(a) Run 3-4



(b) Run 5-6

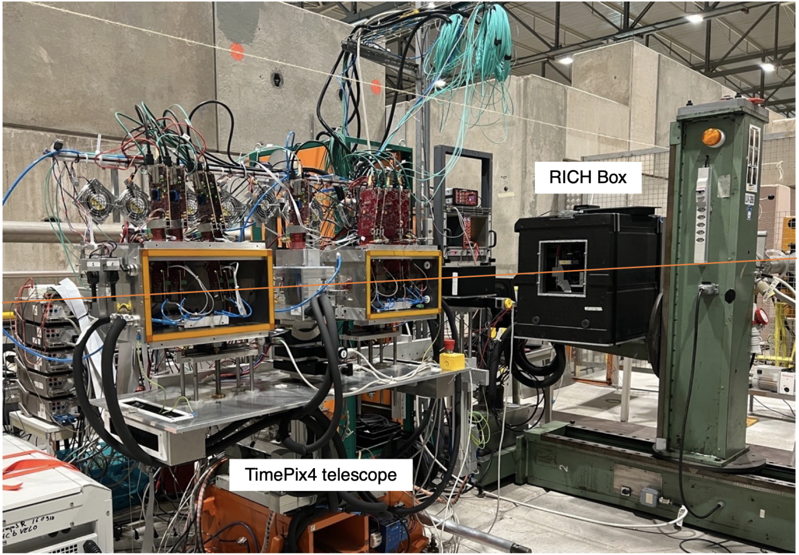
- **A single photon time resolution better than 100 ps is needed for the Upgrade II phase (Run 5-6)** $\rightarrow$ SiPMs among the possible new photodetector candidates

The SPS Campaign

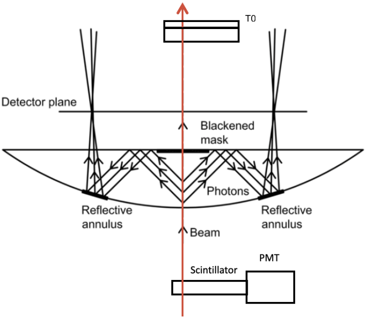
The SPS test beam campaign focuses on the development and testing of a prototype readout chain with fast-timing information

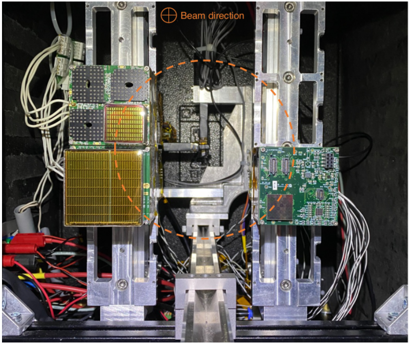
- **3 testbeam campaigns since October 2021 dedicated to Upgrade Ib/II**
- The FastIC is coupled to SiPMs/MAPMTs and read out by a TDC-in-FPGA (temporary solution)
- Valuable information is collected on fast-timing techniques, FastIC operation, sensor coupling, etc.
- Large TB datasets available for many interesting studies

The setup in the beam area



The opto-electronics chain

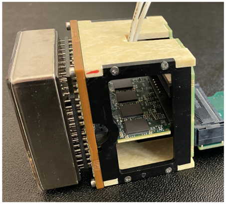


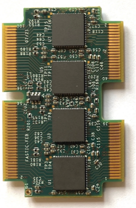


- Borosilicate lens to create Cherenkov light
- Cherenkov rings create arcs on the sensors plane
- 180 GeV hadron beam

- R-type MaPMT, 3mm, 8×8
- H-type MaPMT, 6mm, 8×8
- SiPM matrix, 2mm, 8×8

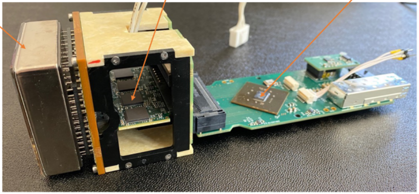
The FastIC chip





- Designed by the micro-electronics section at CERN and the University of Barcelona
- 8 channel ASIC designed in 65 nm CMOS technology for the readout of precise timing detectors
- 6 mW/ch of power dissipation at 1.2 V
- Positive or negative polarity with a wide dynamic range of input current $\rightarrow$ 5 uA to 20 mA
- The output driver can be configured either in single-ended or differential mode

The Digital board



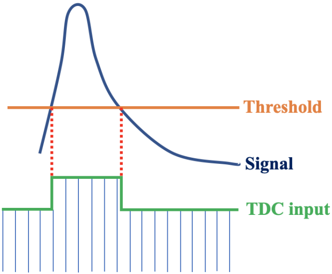
Digital boards:

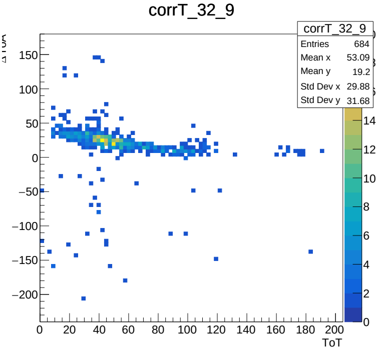
- 3 digital boards, one for every photodetector
- Each board contains a Kintex 7 Chimaera with 34 channel TDC
- When a trigger arrives, data are stored in a buffer and readout by a USB interface.

The TDC firmware

A multi-channel TDC core in a KINTEX-7 FPGA that was succesfully implemented and used in our test beam campaigns

- it uses 16 clock phases @ 420 MHz for a 150 ps timestamp
- The skeleton of the TDC core is based on the work of Wang et. al [1]
- Provides both ToA and ToT information for time-walk correction

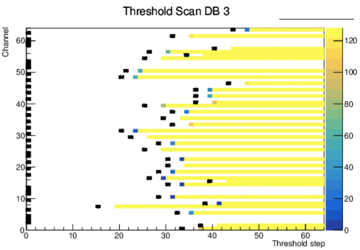


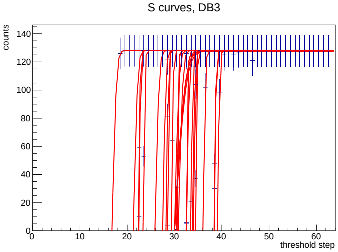


[1] Yu Wang et al.,High-resolution time-to-digital converters (TDCs) with a bidirectional encoder, Measurement

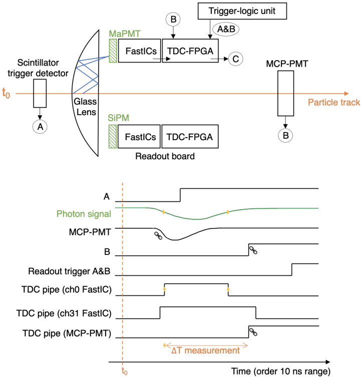
Threshold optimization

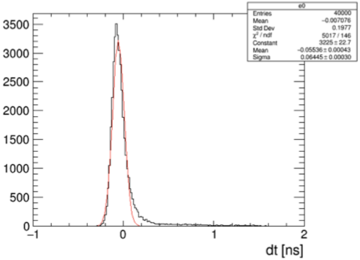
- Channel-to-channel variations mean that careful tuning of the threshold for individual channels is required for optimal signal-to-noise ratio
- Scanning the threshold allows to characterise the noise behaviour per channel and to find the optimal setting
- Sharp and clear transition from signal to noise region





The trigger scheme and the MCP timing reference

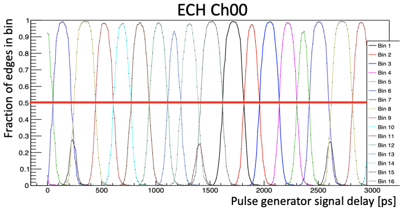


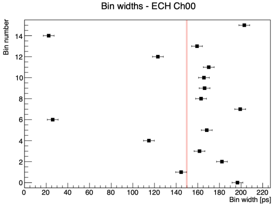


- The MCP is combined with the scintillator in the trigger logic
- When a trigger arrives, the binary traces (35 ns time window) are stored in a buffer and readout.

- $\sigma^2_{t_{MCP}} \approx \sigma^2_{t.w} + \sigma^2_{cfd}$
- The timing jitter introduced by the MCP is $\approx$ 110 ps

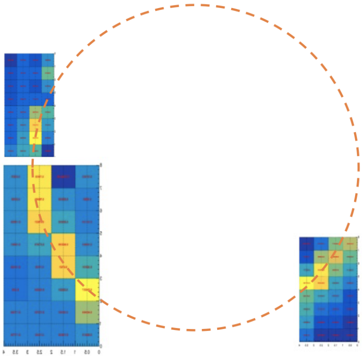
- The TDC bins of each channel are calibrated using a lab procedure whereby a signal from a pulse generator is delayed by small steps in time and sent to the each channel.
- For every signal delay the fraction of edges recorded in each bin is measured
- The bin width is determined by looking the intersection with the 0.5 line

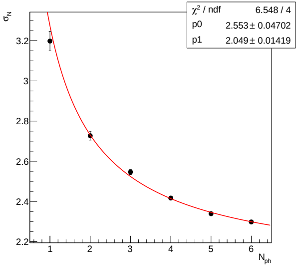




- **The vast majority of TDC bins have a width around the nominal value of 150 ps**

Results (preliminary)



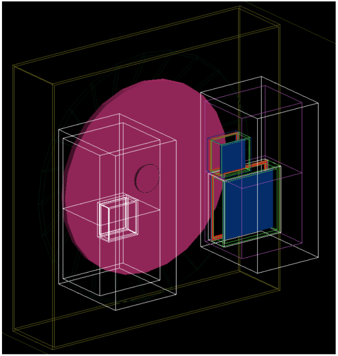


- The reconstructed radius from the occupancy plot is consistent with the expected value of 60 cm

- After time-walk correction the σ_t scales as expected with the number of photons on the ring N_{ph}
- $\sigma_t \propto \frac{a}{\sqrt{N_{ph}}}$
- $\sigma_t^{1p.h} \approx 250ps$ (preliminary)

Geant4 simulation

- Precise timing measurement in single photon regime is challenging and many factors can cause additional timing jitter
- A very detailed simulation of the experimental setup was created to allow for different studies of systematic effects(**see D.F.Holt talk "Time resolved RICH testbeam simulation"**)



Evolution of the opto-electronics chain

- TDC in FPGA limited to 150 ps time bin and data bandwith limited by USB readout
- picoTDC (recently available) will be used in the future testbeams. Its 12 ps bin width will allow more detailed studies of fast sensors
- Use lpGBT (10 Gbit/s) module coupled to back-end compatible with the current LHCb online architecture to increase readout rate