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Test Beam Characterization of a digital SiPM in 150 nm CMOS Imaging Technology

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Silicon photomultipliers (SiPMs) are solid-state light detectors capable of detecting single photons with high quantum efficiency in the ultraviolet to visible energy range with excellent time resolution. Due to their unique characteristics, these devices are increasingly used in high-energy physics, medical and commercial applications. Most SiPMs are implemented as large arrays of single-photon avalanche diodes (SPADs) in a parallel circuit, serving as analog photon counters.

Recently, SPADs have been integrated into standard high-volume CMOS processes. This not only allows the production of large volumes of SiPMs at a relatively low cost, but also offers the possibility of combining SPAD peculiarities with the flexibility and possibilities offered by CMOS imaging technology. The implementation of CMOS circuitry extends the properties of standard SiPMs with features such as in-pixel digitization, full Hitmap readout, masking of noisy SPADs, implementation of trigger logic, on-chip Time to Digital Converter. These features allow exploring new fields of applications for SPAD arrays such as Minimum Ionizing Particle detection with excellent spatial and temporal resolutions (4D-Tracking)

A prototype digital SiPM (dSiPM) with per-pixel CMOS circuits was developed at DESY in a 150-nm CMOS technology offered by LFoundry. The chip consists of a 32 x 32-pixel main dSiPM and test structures. Several characterizations were performed in the laboratory on the prototypes and three Test Beam campaigns were carried out at DESY-II Testbeam facility investigating the 4D-Traking performance of the dSiPM.

In this contribution, the results of the characterizations performed on the Chip will be reported. In particular, the Test Beam setups and techniques used for data taking and Corryvreckan analysis will be presented, along with an overview of planned future studies.

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