Silicon sensor technologies for vertex and tracking detectors at future e^+e^- colliders

BTTB 11 – DESY (Hamburg)

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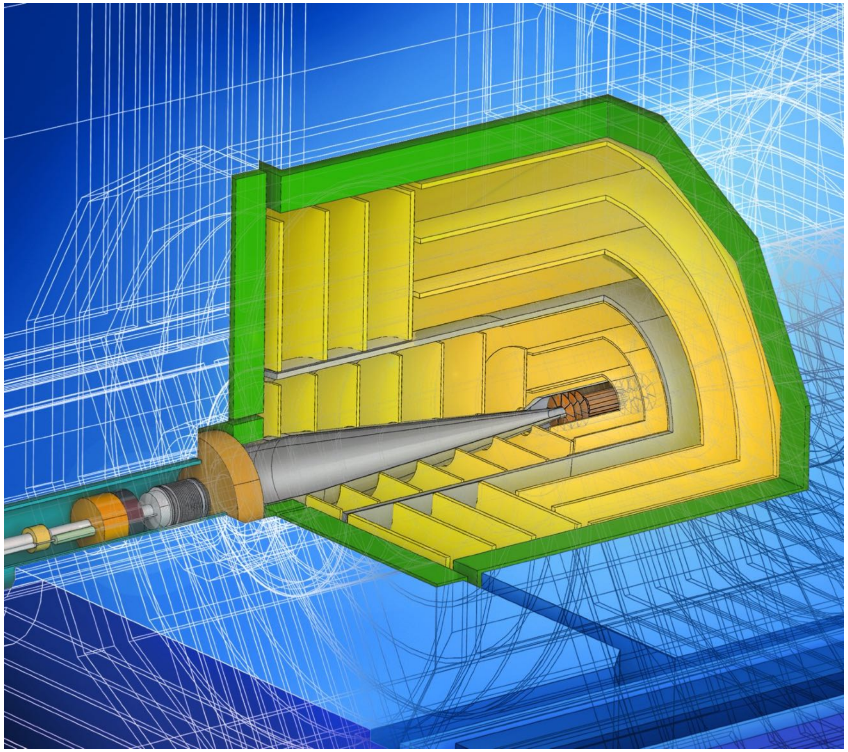
Outline

- Future e^+e^- Higgs Factories
- Vertex and tracker requirements
- Detector concepts
- Technology R&D examples
- Conclusions

Disclaimer:
Not a complete overview;
can show only few examples of
the many ongoing developments!

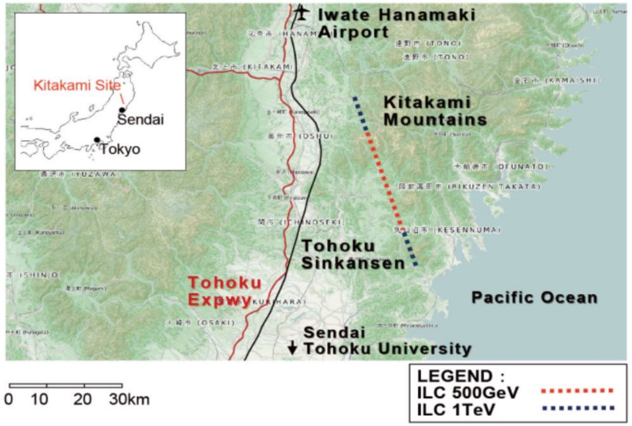


e^+e^- Higgs Factory proposals

- European Strategy Update for Particle Physics in 2020:
  - Higgs Factory highest-priority post-LHC project
  - No decision yet about which and where
- Several e^+e^- collider Higgs-Factory proposals:
  - $\sqrt{s}$ ~ 350 GeV - 3 TeV
  - Circular / linear collider designs
  - Possible sites in Europe and Asia
  - Time scale ~2035-2040

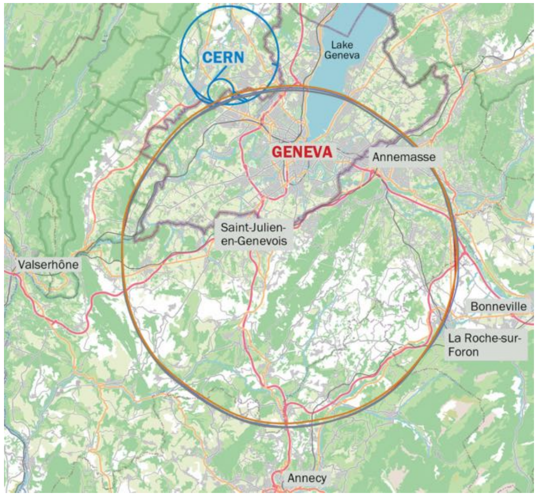
ILC in Japan

$\sqrt{s}_{max}$ =250-1000 GeV



FCC-ee @ CERN

$\sqrt{s}_{max}$ =240-365 GeV



CEPC in China

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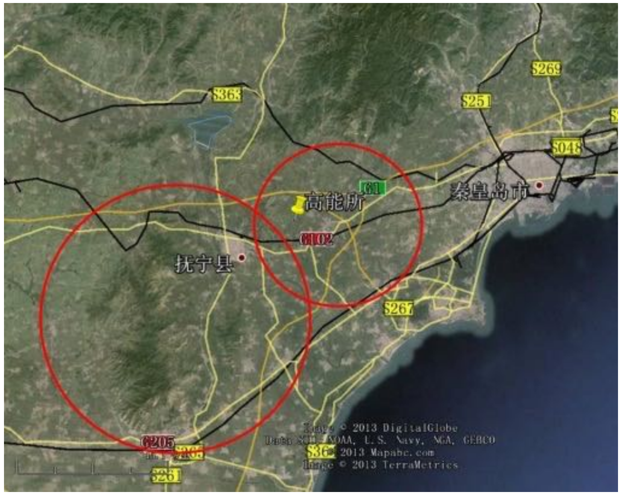
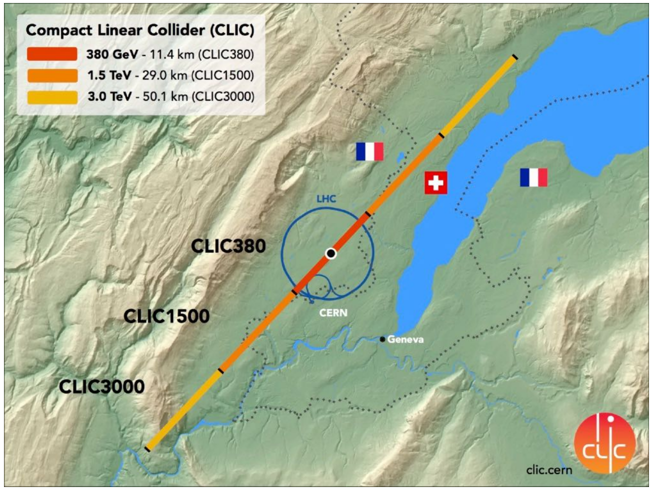


CLIC @ CERN

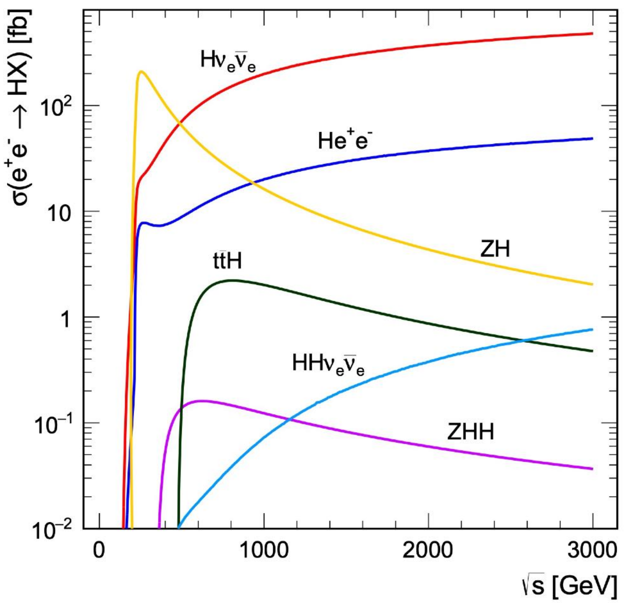
$\sqrt{s}_{max}$ =380-3000 GeV



Higgs Factory vertex/tracker physics requirements

- Physics goals for post-LHC future Lepton Colliders:
  - Precision Higgs / EW / top measurements
  - Direct/indirect BSM searches

Higgs production processes



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  →Vertex resolution: $\sigma(d0) \sim 5 \oplus 15/(p[\mathrm{GeV}]\sin^{3/2}\theta)$ µm

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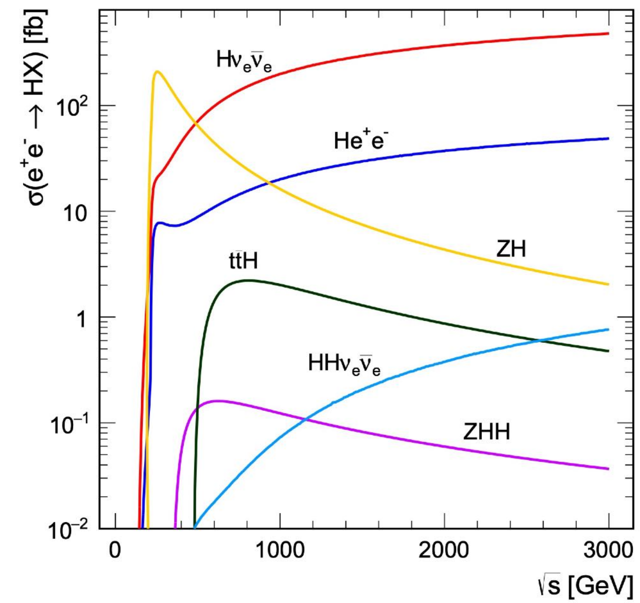
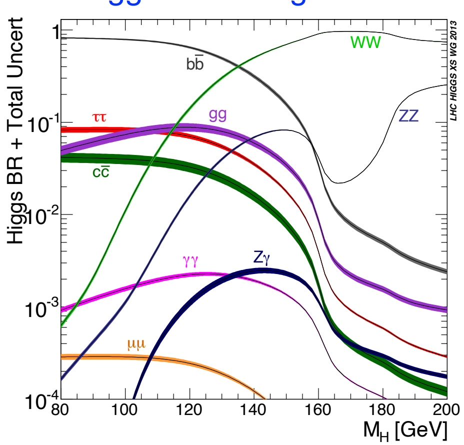


Higgs branching ratios



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  - Precise measurement of leptonic final states (e.g. recoil-mass measurement in ZH)

  → Track-momentum: $\sigma(p_T) / p_T^2 \lesssim 2 \times 10^{-5}$ GeV^{-1}

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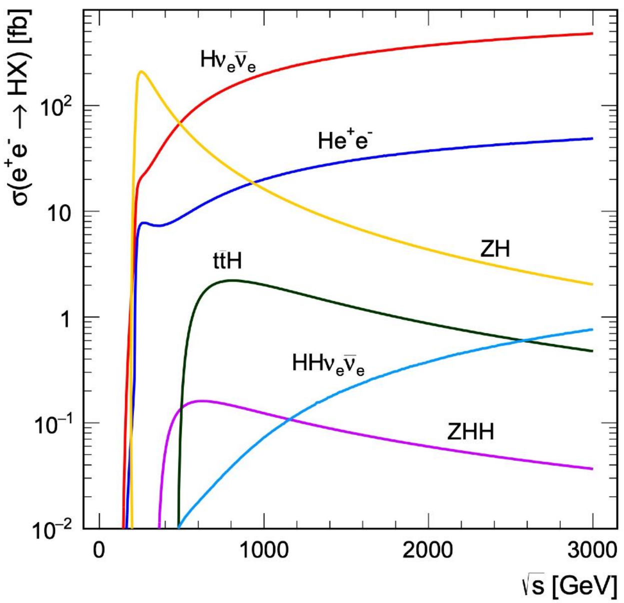

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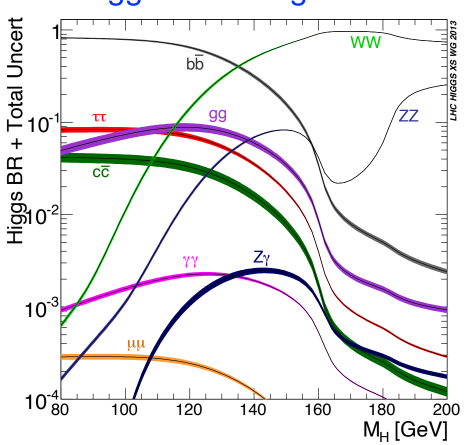
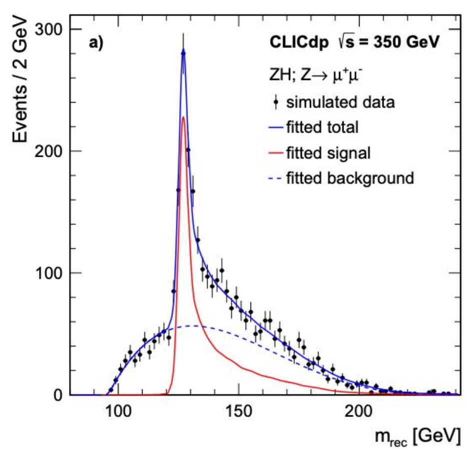


Higgs recoil mass reconstruction



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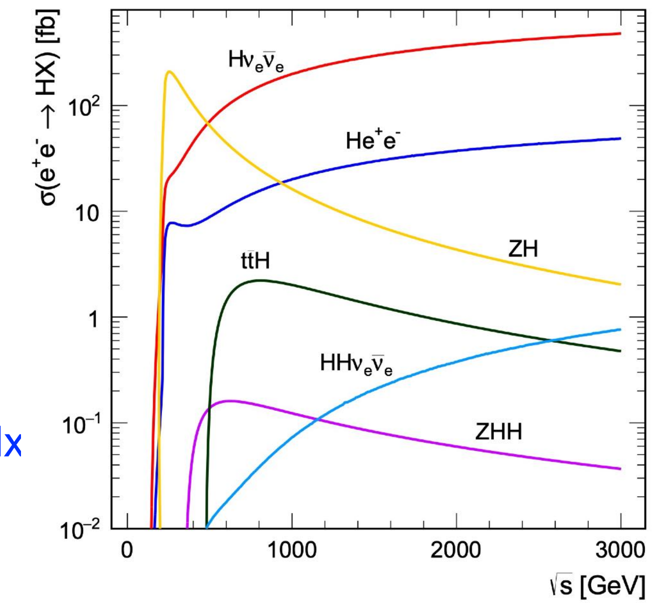
  - Heavy-flavor physics → PID (K/pi separation) by dE/dx, dN/dx and/or 10's of picosecond timing layers
  - Background rejection → low-angle coverage, timing
  - Exotics (e.g. highly ionizing or feebly coupled particles)

  → dE/dx, many layers, large radius, precision timing

Higgs production processes



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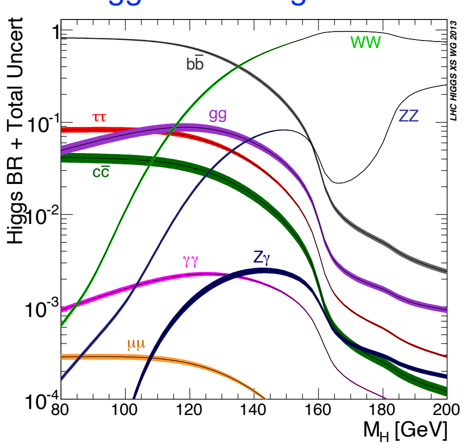

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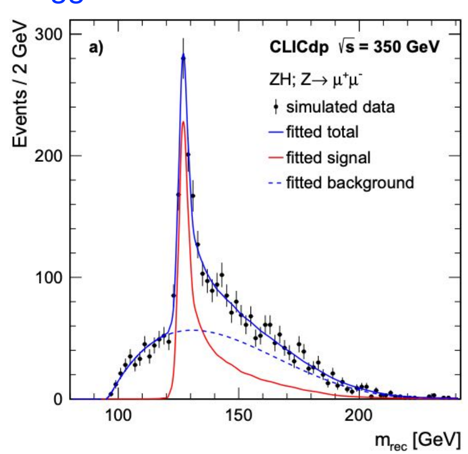
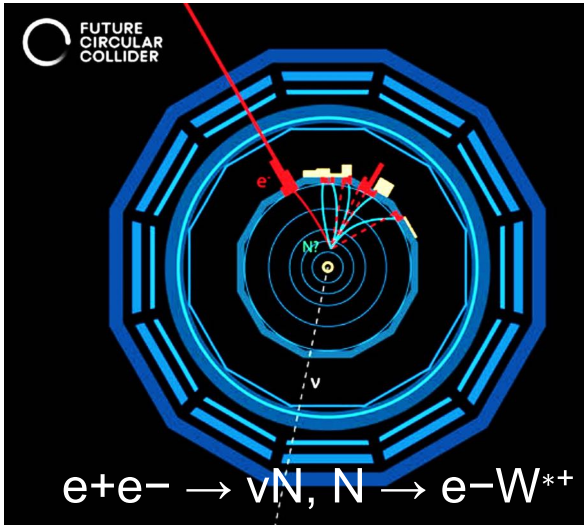


Decay of Heavy Neutral Lepton (1m from IP)



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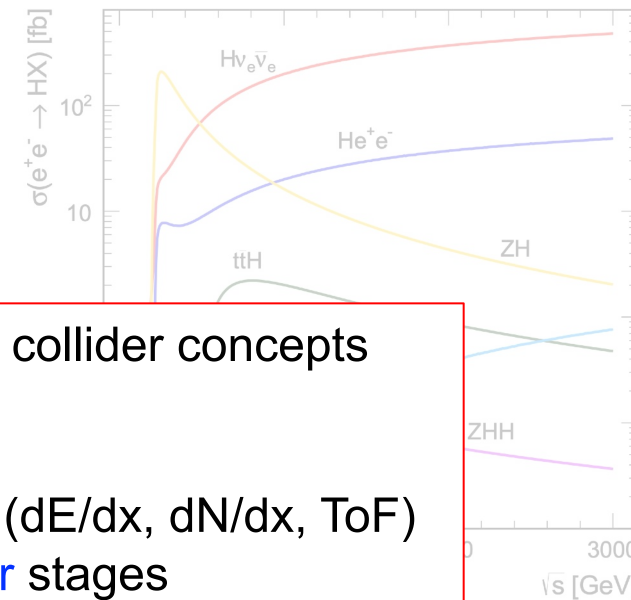


- Similar physics requirements for trackers in all collider concepts
- More focus on asymptotic position resolution for high-energy Linear-Collider stages
- More focus on material budget and particle ID (dE/dx, dN/dx, ToF) for high-luminosity low-energy Circular-Collider stages

Decay of Heavy Neutral Lepton (1m from IP)

Higgs branching ratios

Higgs recoil mass reconstruction

Experimental constraints on vertex/tracker

Main experimental constraints in **linear lepton colliders**:

- Significant rates of beam-induced backgrounds (incoherent e^+e^- pairs, $\gamma\gamma \rightarrow$hadrons):
  - Constrains layout, granularity, impacts physics
- Backgrounds concentrated in very short bunch trains

→ High instantaneous hit rates (up to 6 GHz/cm² @ 3 TeV CLIC)

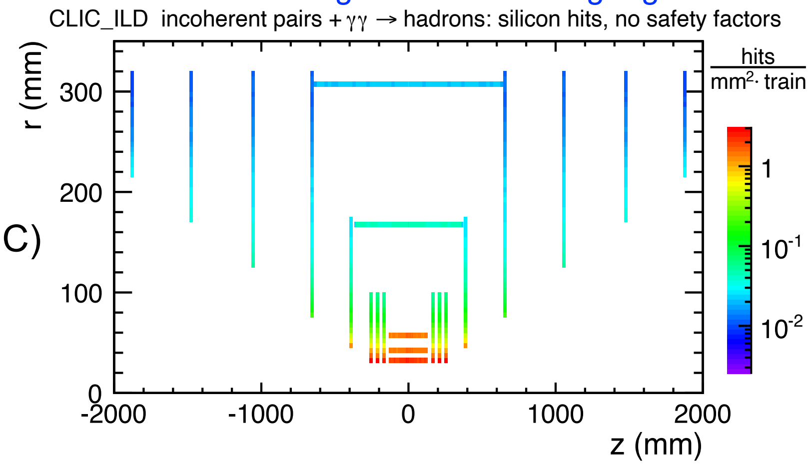
→ Time-stamping: few ns @ 3 TeV CLIC, ~1-10 μs @ ILC

→ Fast detector signals / frontend

- Low duty cycle: ~20-200 ms gaps between bunch trains

→ trigger-less readout, pulsed powering

CLIC backgrounds in tracking region



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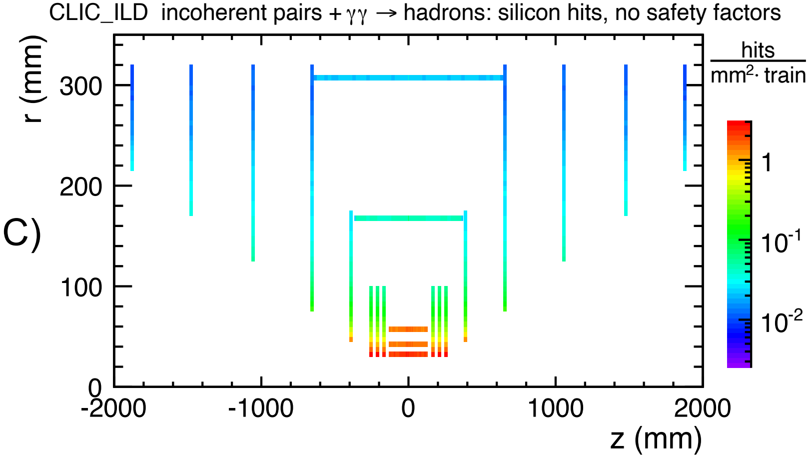


Main experimental constraints in **circular lepton colliders**:

- 30 mrad crossing angle of beams, focusing quadrupoles inside det. volume

→ B-field limited to ~2 Tesla

- High rate of physics events (up to 100 kHz, bunch spacing down to 30 ns)

→ Integration time <~1 μs required for occupancy and pile-up (30 ns @ Z-pole)

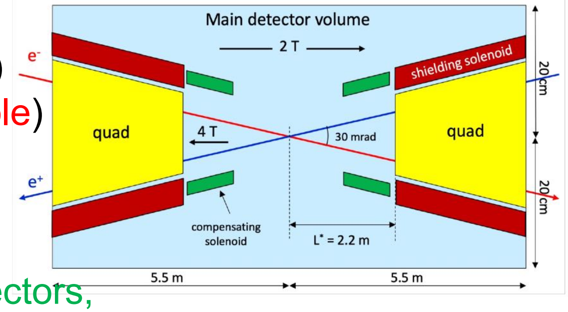
→ Fast detector frontend and DAQ

- Main backgr.: synchrotron radiation (reduced by shielding), incoh. pairs
- Continuous collisions (100% duty cycle)

→ Beam-induced backgrounds more spaced out, less severe impact on detectors,

→ Pulsed powering not possible

FCC-ee detector region



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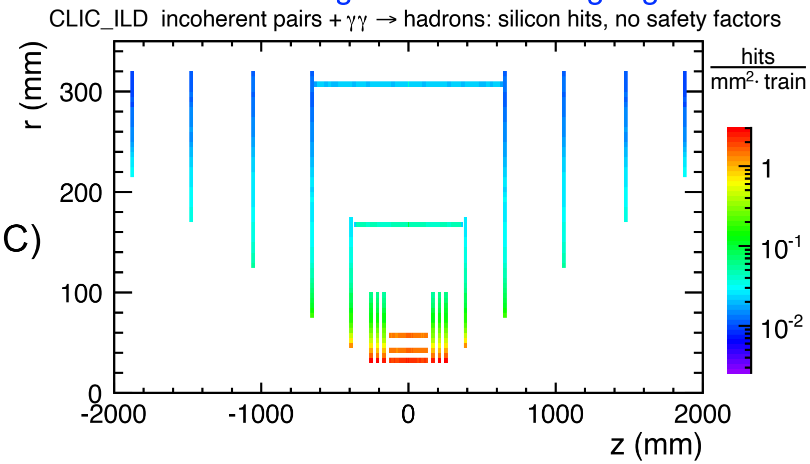

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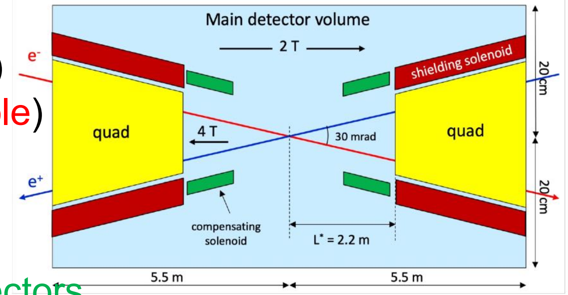

- Moderate radiation exposure (≳10⁴ below LHC run 1!) for all lepton-collider proposals:
  - NIEL: < 10^{11} $n_{eq}/cm^2/y$
  - TID: < 1 kGy / year

Vertex/tracking detector concepts

Collider	ILC		CLIC	FCC-ee			CEPC	
Detector Concept	SiD	ILD	CLICdet	CLD	FCC-ee IDEA	Noble LAr/LKr	CEPC baseline	CEPC IDEA
B-field [T]	5	4	4	2	2	2	3	2
Vertex inner radius [mm]	14	14	31	17 → 12	17 → 12	17 → 12	16	16
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Vertex	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel
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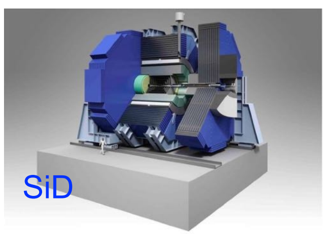
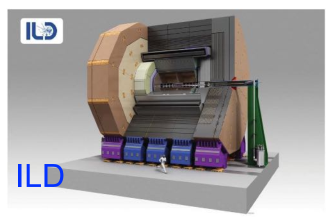
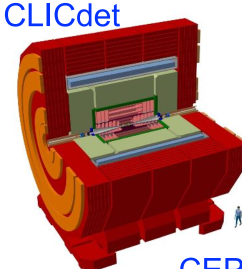
arXiv:1306.6329 *arXiv:1812.07337* *arXiv:1911.12230* *doi.org/10.1140/epjst/e2019-900045-4* *arXiv:1811.10545*

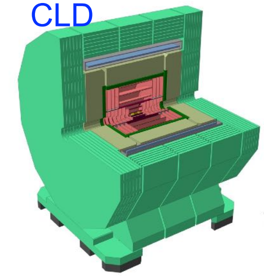




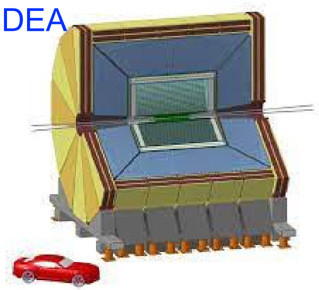
CLICdet



CLD

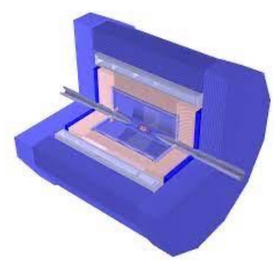


IDEA

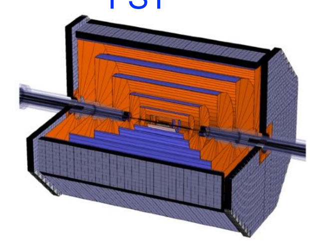


Noble LAr/LCr

CEPC baseline



FST



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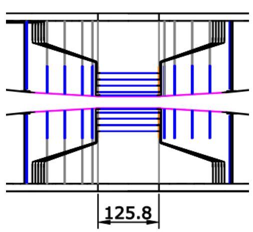
arXiv:1306.6329 *arXiv:1812.07337* *arXiv:1911.12230* *doi.org/10.1140/epjst/e2019-900045-4* *arXiv:1811.10545*

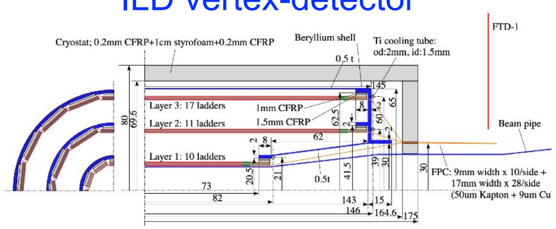
All concepts contain silicon-pixel vertex detectors:

- 5-6 barrel and up to 6 endcap layers (in doublets or singlets)
- high single point resolution per layer: σ_{SP}~3 μm → pixel sizes <~25 μm2
- low material budget: ≲ 0.2% X_0 / layer (equivalent to ~200 μm silicon) → thin sensors, low-power ASICs for air cooling (~50 mW/cm²)

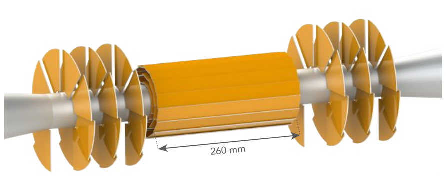
SiD vertex-detector



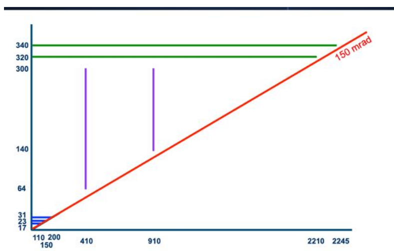
ILD vertex-detector



CLIC vertex-detector



IDEA vertex-detector



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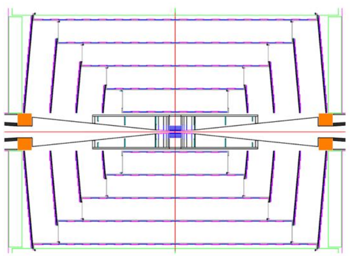
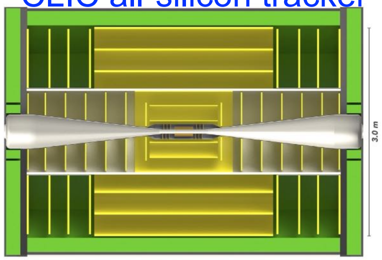
Silicon-based large-area trackers:

- many layers (barrel/endcap), large outer radius (scaling with B field)
- Large pixels or strip detectors
- ~7 μm single-point resolution in bending plane
  → ~25-50 μm Rφ pitch
- ~1-2% X0 per layer
  → low-mass supports + services,
  low power ~150 mW/cm^2

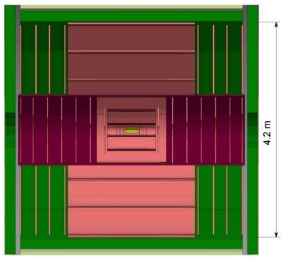
SiD all-silicon tracker



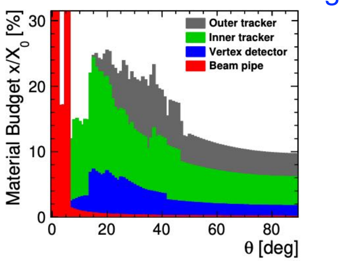
CLIC all-silicon tracker



CLD all-silicon tracker

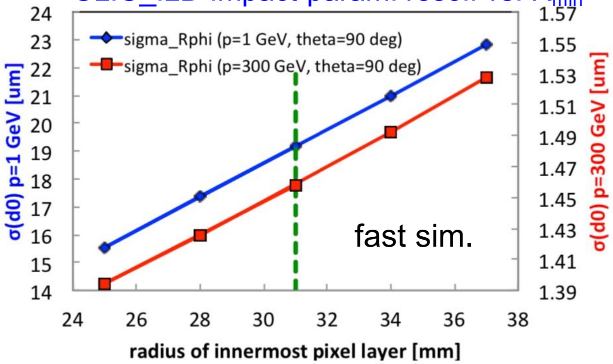


CLIC inner det. mat. budg.

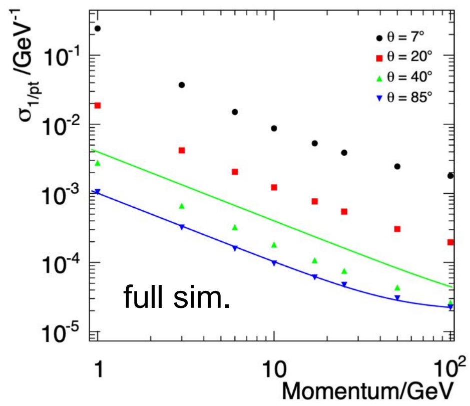


Detector concept optimization / validation

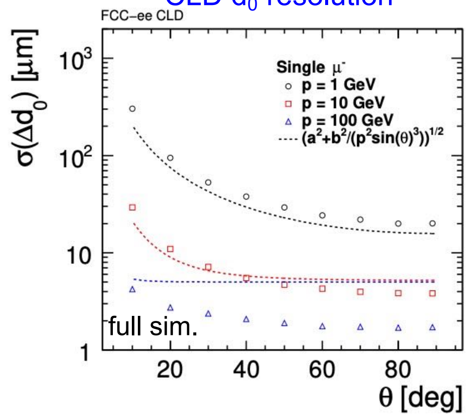
CLIC_ILD Impact-param. resol. vs. R_{min}



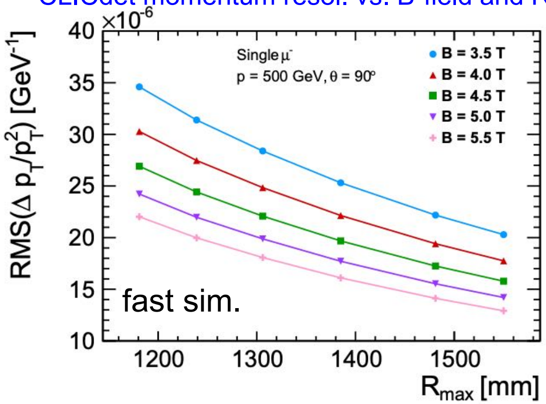
ILD momentum resolution



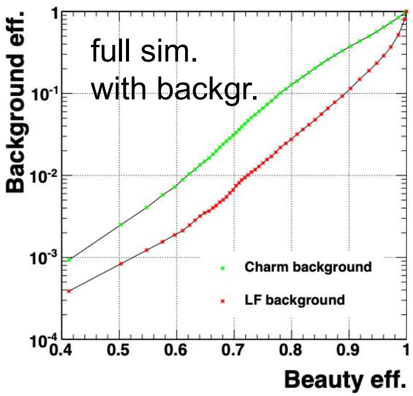
CLD d_0 resolution



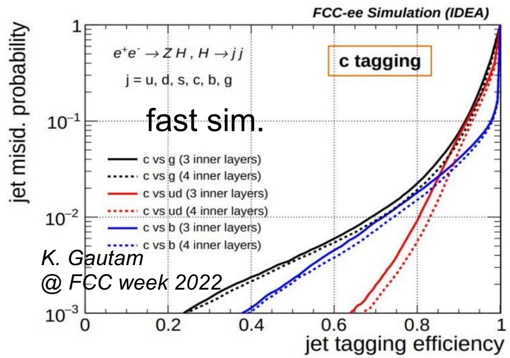
CLICdet momentum resol. vs. B-field and R_{max}



SiD b-tagging performance



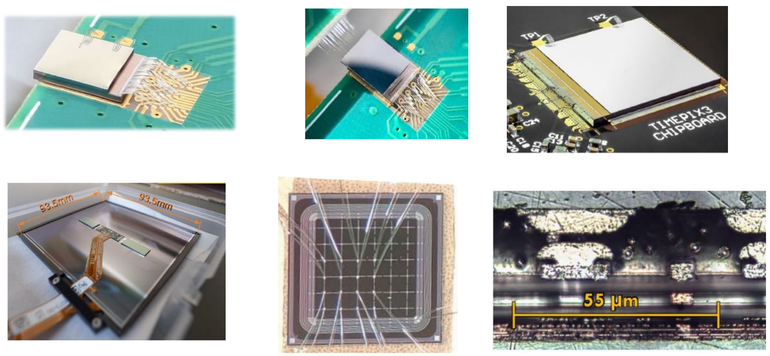
IDEA c-tagging performance



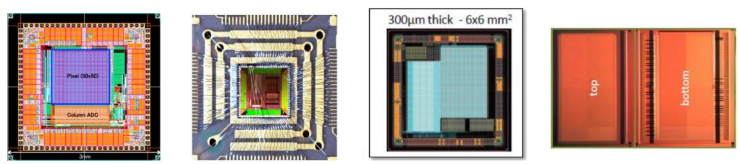
- Detecor concepts are optimised with fast parametric and full Geant-4 simulations;
- All detector concepts fulfil physics requirements in simulations;
  - So far: SiD,ILD,CLICdet,CLD validated in Geant4 based full-detector simulations
  - Other concepts validated in fast simulation, full simulation in progress
- All concepts contain 4π trackers with barrel+endcap → similar to ATLAS, CMS, *ALICE3,* but different from Belle, ALICE ITS3, Mu3e with their barrel-only inner trackers

Silicon pixel-detector R&D examples

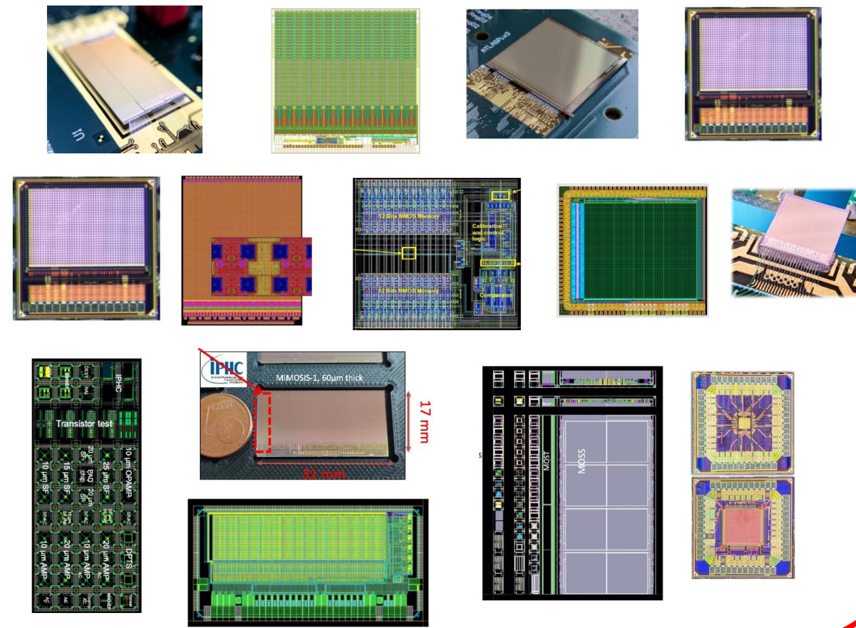
Hybrid detectors



Silicon on Insulator

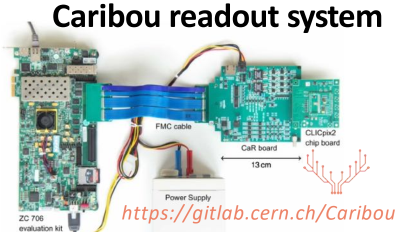


Monolithic Sensors



Tools

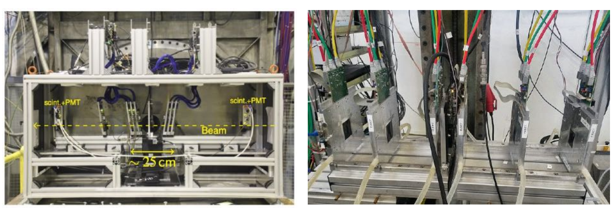
Caribou readout system



https://gitlab.cern.ch/Caribou

PoS 2020 (TWEPP2019), 100

CLICdp + AIDA telescopes



MC Simulation framework: Allpix Squared

https://gitlab.cern.ch/allpix-squared/allpix-squared

NIM A 901 (2018) 164-172

Analysis & reconstruction framework: Corryvreckan

https://gitlab.cern.ch/corryvreckan/corryvreckan

2021 JINST 16 P03008

- Diverse R&D performed within various collaborative frameworks (ILD, SiD, CLICdp, IDEA, CERN EP R&D, AIDAinnova, DRD3/7, …), with strong links to other developments (HL-LHC, Belle II, Mu3e, CBM@FAIR, …)
- Mostly focusing on conceptual studies + technology demonstrators

→ Flexible tools developed, to support the R&D and exploit synergies between the various R&D lines

Silicon pixel-detector R&D examples

Hybrid detectors

Monolithic Sensors

Silicon on Insulator

Tutorials at this workshop!

Tools

Caribou readout system

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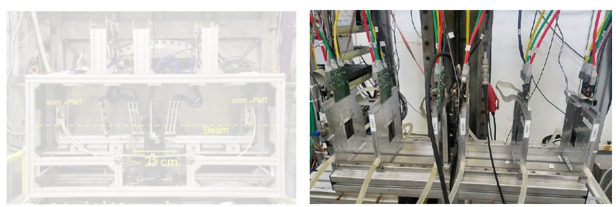
PoS 2020 (TWEPP2019), 100

CLICdp + **AIDA telescopes**



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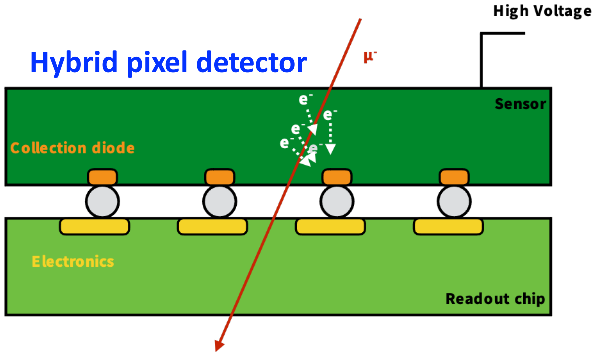
Hybrid pixel detectors



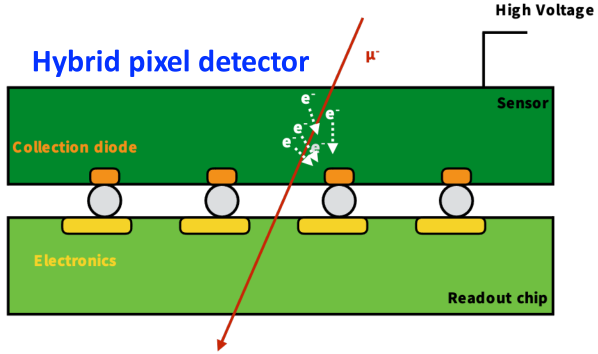
Hybrid pixel detectors

- Target applications: CLIC vertex detector, track-timing layers
- Separate interconnected sensor and readout ASIC layers

→ Factorise R&D on sensors and readout ASICs

- Develop new sensor concepts, e.g.:
  - Thin sensors (50 µm) with large fill factor (active edge)
  - Active / passive CMOS sensors
  - Sensors with enhanced lateral drift (ELAD) for optimal position resolution
  - Sensors with charge amplification (LGAD) for picosecond timing
- Profit from advanced industry technologies for highest ASIC performance (rate, timing)
- Profit from synergy with (HL)-LHC developments, medical imaging, gaseous detector r/o (GridPix)
- Refine and develop new interconnect technologies
- Challenges: material budget, interconnect: cost, minimum pitch

Hybrid pixel detectors



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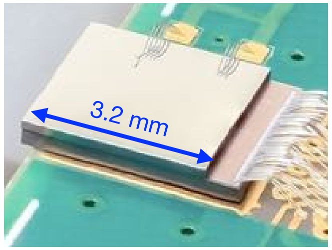
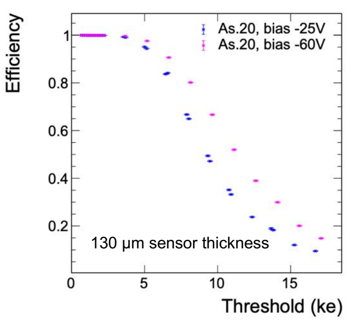
Talk by Peter Svihra on CLICpix2 test-beam results on Thursday

Test-beam studies for 65 nm CLICpix2 with thin active-edge sensors (25 µm pitch)

CLICpix2 hybrid assembly

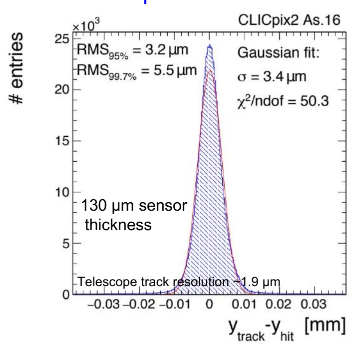


Efficiency

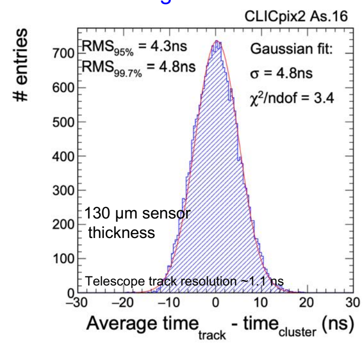


CERN-THESIS-2020-338

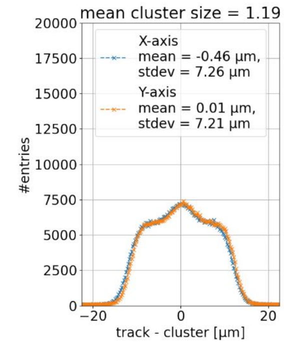
Spatial residuals



Timing residuals



Spatial residuals for 50 um thick sensor



arXiv:2210.02132

- Efficiency, spatial and timing resolution targets are achieved, but not yet simultaneously with material budget target
  → need advanced sensors / smaller pitch (→ 28 nm ASICs, also considered for HL-LHC)

Fine-pitch hybridization

- Sensor/ASIC interconnect is one of the main challenges for hybrid pixel-detectors:
  - Cost / complexity, material budget, minimum pitch, single-die processing during R&D
- Different interconnect technologies are under study for future-collider detectors

Fine-pitch hybridization

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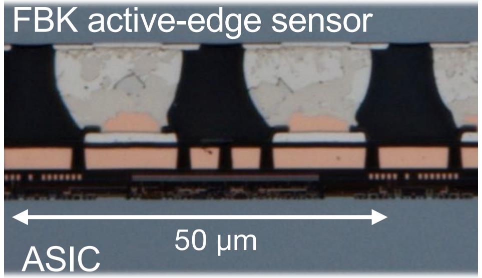
Single-die bump-bonding process developed by IZM:

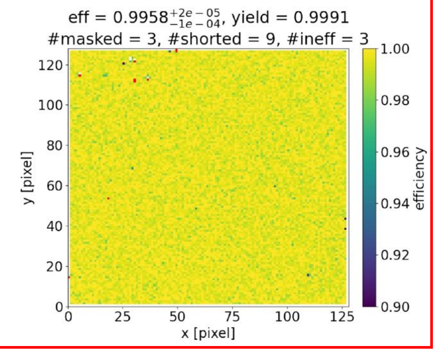
- pitch 25 µm, sensor thickness down to 50 µm
- Support-wafer processing of CLICpix2 ASICs from MPW for UBM and SnAg bump deposition
- Excellent interconnect yield >99.7% observed in laboratory and test-beam measurements

https://arxiv.org/abs/2210.02132

25 µm bump bonding @ IZM



TB pixel effic. 50 µm CLICpix2 ass.



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Talk by Peter Svihra on Hybridisation on Thursday

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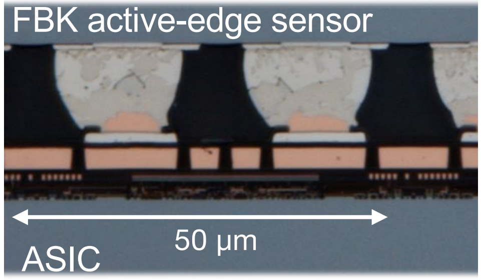
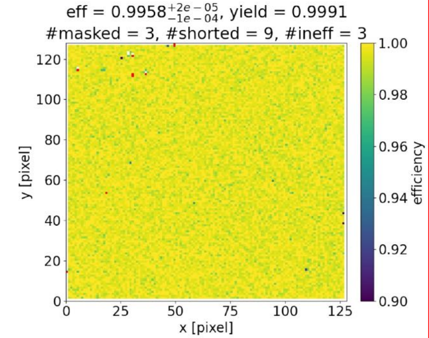


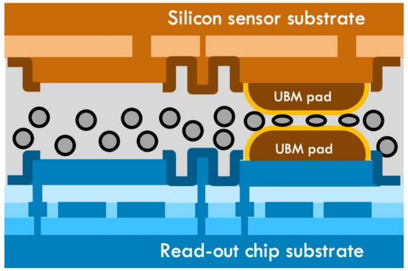
TB pixel effic. 50 µm CLICpix2 ass.



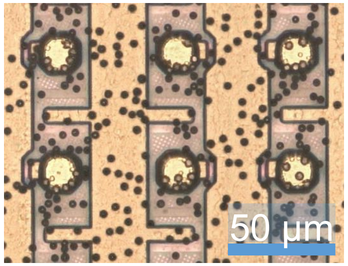
Hybridisation with **Anisotropic Conductive Films (ACF):**

- Adhesive epoxy film with embedded conductive micro-particles, electrical connection through thermo-mechanical compression
- Ongoing development / optimization of two single-die in-house processes:
  - Chemical Electroless Nickel Immersion Gold (ENIG) deposition for Under Bump Metallization (UBM)
    → uniformity, thickness, edge effects
  - Semi-automatic flip-chip bonding with ACF layer
    → ACF material (particle diameter and density), epoxy thickness, bonding profile
- Proof-of-principle results for Timepix3 hybrid assemblies
  → high interconnect yield in regions with good UBM
  → ongoing optimization of UBM process for single dies
- ACF also under study for module integration
  → 'easier' use case (large-pitch interconnect)
- Also tests with paste (ACP) and non-conductive (NCP)

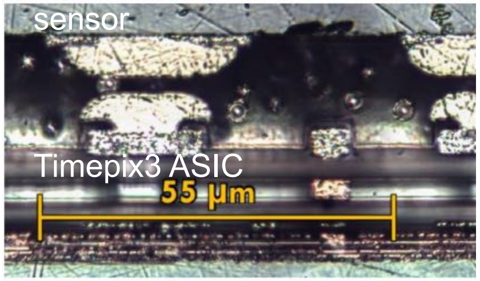
ACF bonding w/ conductive micro-particles



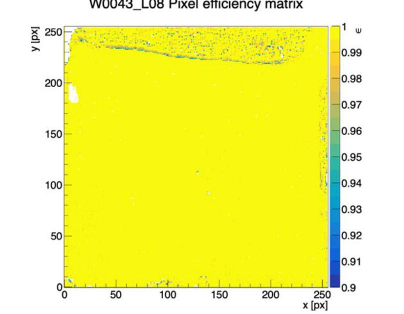
ACF on Timepix3



55 um ACF interconnect

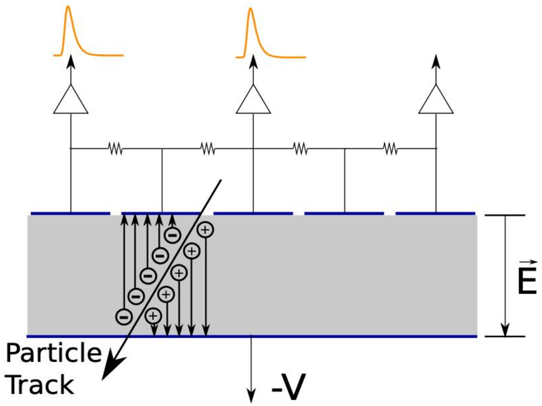


TB pixel effic. Timepix3 ACF ass.



https://arxiv.org/abs/2210.13046

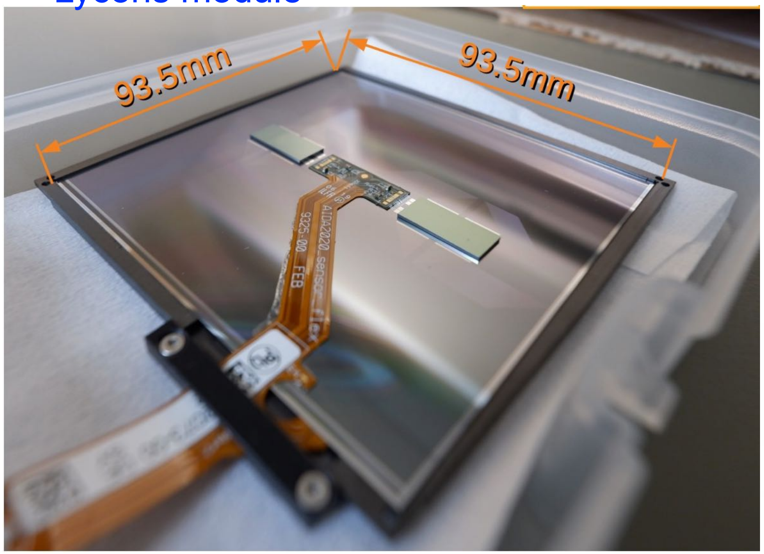
Hybrid strip detectors



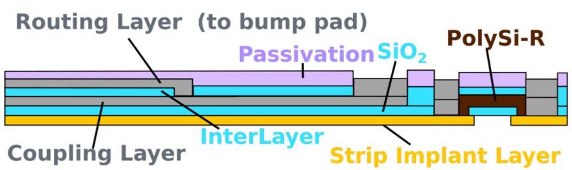
Hybrid strip detectors:

- Baseline for ILC trackers (also suitable for CLIC outer layers)
- Well-established technology (e.g. HL-LHC)
  - low material + power (sparse readout)
  - large and fast signals (dE/dx)
  - high spatial resolution (charge interpolation) in R/phi direction
  - Advanced sensor concepts (e.g. stitched passive CMOS strip sensors)
  - Challenges: not for high occupancy regions; complex interconnect

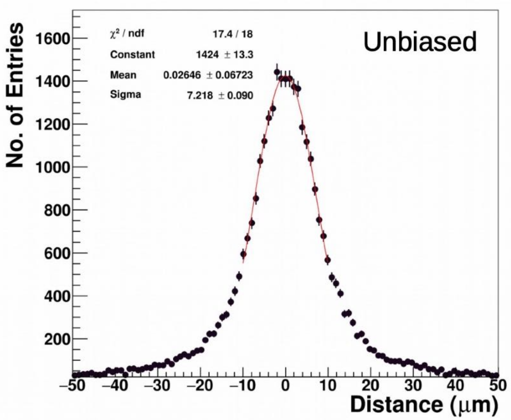
Lycoris module



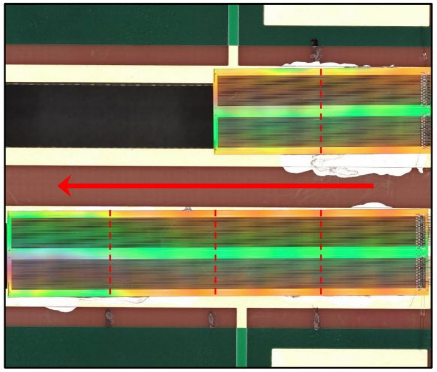
- Lycoris development DESY / SLAC:
  - 320 µm thick SiD sensors, 25 µm strip pitch, 50 µm r/o pitch
  - KPiX r/o ASIC bump-bonded on-sensor → high fill factor
  - 7 µm single-point resolution achieved in test beam
  - Test-case: beam telescope for PCMAG@DESY



https://indico.cern.ch/event/995633/contributions/4259345



Stitched passive CMOS sensors



Freiburg, DESY, Bonn

https://indico.cern.ch/event/995633/contributions/4259384/attachments/2209268/3738710/Passive%20CMOS%20Strip%20Sensors.pdf

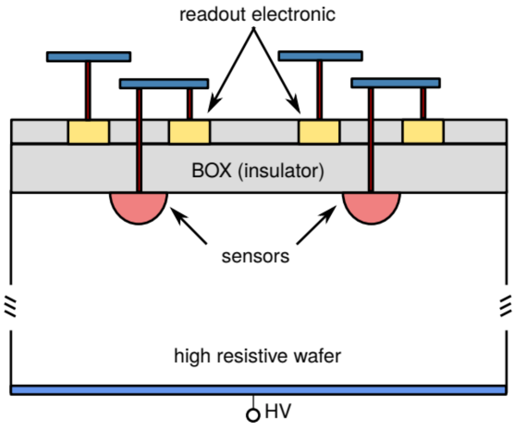
→ talks by Geetika J. on ATLAS ITk strip upgrade, Younes O. on CMS pixel-strip modules, Naomi A.D. on pass. CMOS strips

Silicon-on-Insulator (SOI) / 3D integration

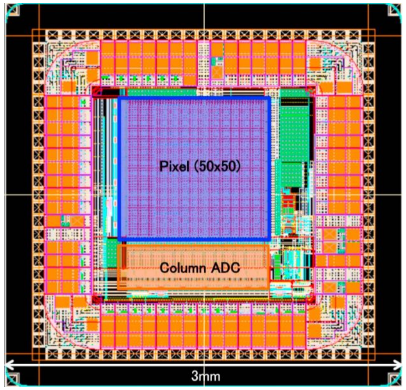
- Silicon-On-Insulator (SOI): r/o electronics on thin low-resistivity electronics wafer, separated from high-resistivity sensor wafer by buried insulation oxide layer

- Thin + fast (fully depleted) "monolithic" sensors
- Challenge: specialized + complex production process (wafer bonding)
- Various developments targeting LC vertex and tracking detectors, e.g.:
  - SOFIST V1 in 200 nm LAPIS SOI
    20x20 μm² pitch, 200 μm thickness → σ_{SP}~1.4 μm
  - Cracow SOI test chip in 200 nm LAPIS SOI process
    30x30 μm² pitch, 500 μm thickness → σ_{SP}~1.5 μm
  - CPV4 SOI-3D LAPIS SOItest chip (IHEP)
  - IPHC LAPIS SOI test chip (with KEK)
  - 3D developments @ IPHC (with TJ, T-Micro)
- Precision timing not yet demonstrated

SOI pixel detector

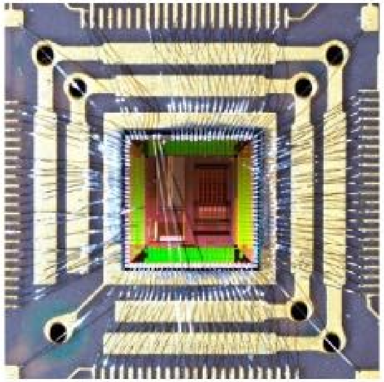


SOFIST v1



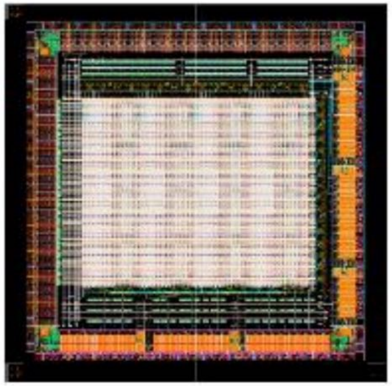
https://doi.org/10.1016/j.nima.2018.06.075

Cracow SOI test chip



Nucl. Instrum. Methods Phys. Res., A 988 (2021) 164897

CPV4 SOI-3D



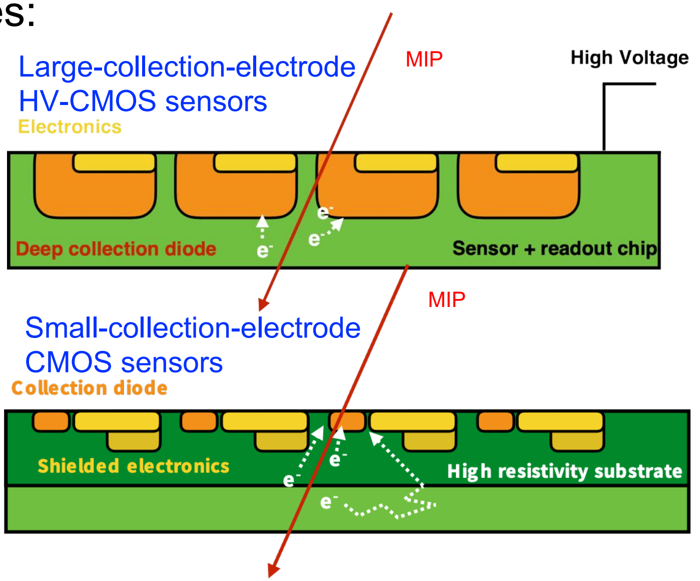
IPHC double-tier 3D TJ 180

https://indico.cern.ch/event/995633/contributions/4259377/attachments/2208714/3738410/LCWS2021_BESSON_vf.pdf

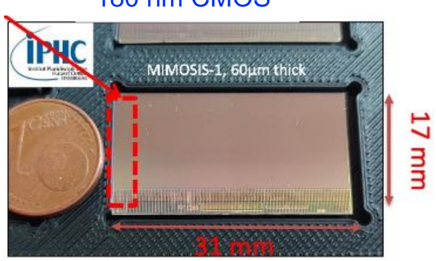
Monolithic CMOS sensors

Monolithic CMOS sensors using (adapted) industry technologies:

- Sensor and readout electronics fully integrated
- Different concepts:
  - Large-collection electrode High-Voltage (HV-CMOS) for large + fast signals, radiation hardness
  - Small-collection-electrode designs for low capacitance, high signal/noise, low power
- Simplified construction (no bonding)
- Challenges: complex non-uniform sensor structures (simulation), interplay sensor/readout, process modifications are foundry dependent / parameters not publicly available
- Many ongoing developments, exploiting progress in semiconductor industry and synergies (HL-LHC, Mu3e, Belle II, CBM@FAIR, …)
- Trend towards smaller feature sizes (180 nm → 65 nm) for improved performance
- Target: vertex/tracker of all Higgs Factory detectors

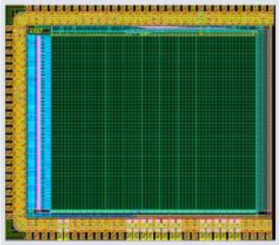


MIMOSIS-1
180 nm CMOS

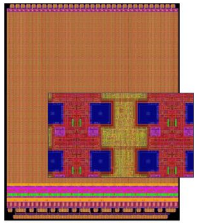


CLICTD
180 nm CMOS

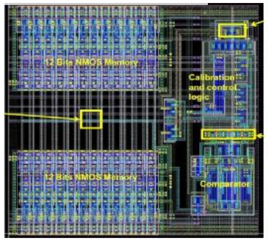
JadePix2
180 nm HV-CMOS



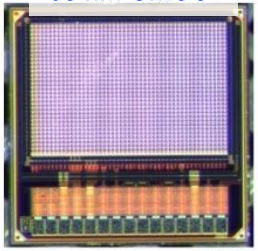
ARCADIA MD1
110 nm CMOS



Chronopix
90 nm CMOS

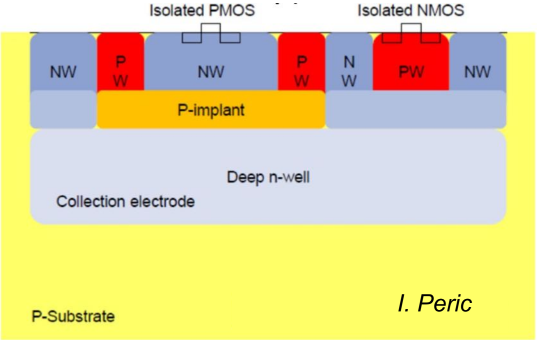


CE-65
65 nm CMOS

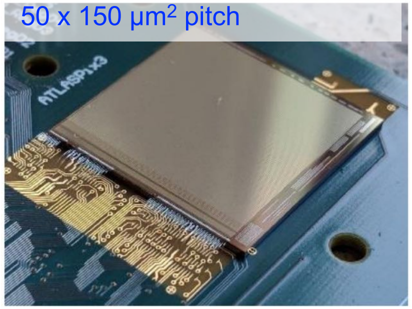


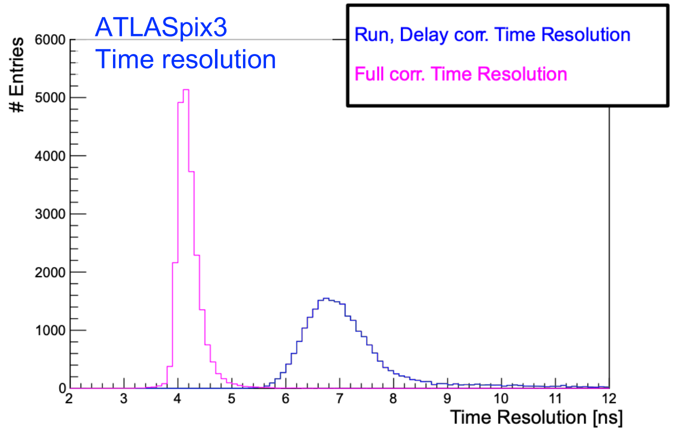
180 nm High-Voltage CMOS

- Active HV-CMOS sensors with fully integrated readout
- Large collection electrode shielding CMOS circuitry, depleted thin sensors (high-resistivity substrates, >100 V bias), fast frontend
  → large signal (dE/dx), fast, radiation hard
- Studies for CLIC tracker + IDEA outer vertex / tracker
- Same technology initially considered for ATLAS outer tracker and chosen for Mu3e tracker (MuPix8), also under study for LHCb Mighty Tracker upgrade and for DESY beam-telescope timing+trigger planes
- Very good performance observed in test beam:
  - >99.7% efficiency (ATLASpix3)
  - Timing precision ~4 ns (ATLASpix3)
  - Spatial resolution <10 μm (Telepix, 25 μm pitch in R/phi)
  - Power consumption down to 140 mW/cm² (ATLASpix3)
- Plans for dedicated CEPC design in 55 nm HV-CMOS process

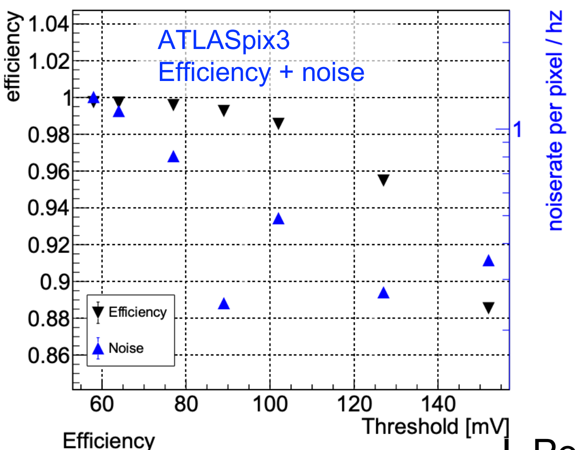


ATLASpix3
180 nm HV-CMOS
50 x 150 μm² pitch





Time resolution (RMS) for every pixel
Uncorrected 6.7ns +- 0.5ns
ToT corrected 4.1ns +- 0.1

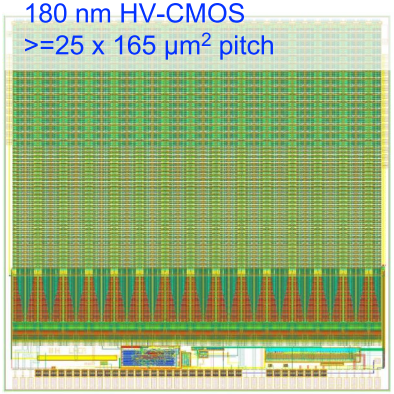


Efficiency

I. Peric et al.

https://agenda.linearcollider.org/event/9211/contributions/49477/

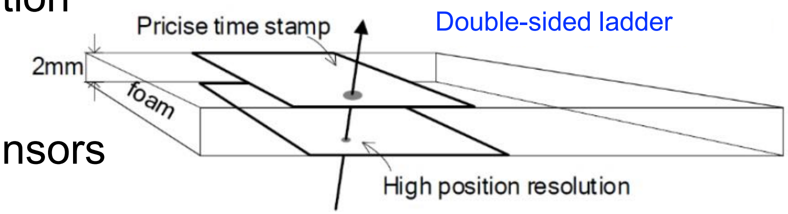
LHCb/CLIC/Telepix
180 nm HV-CMOS
>=25 x 165 μm² pitch



Talk by Ryunosuke O'Neil on ATLASpix3 test-beam results this afternoon
Talk by Arianna Wintle on Telepix test-beam results on Tuesday morning

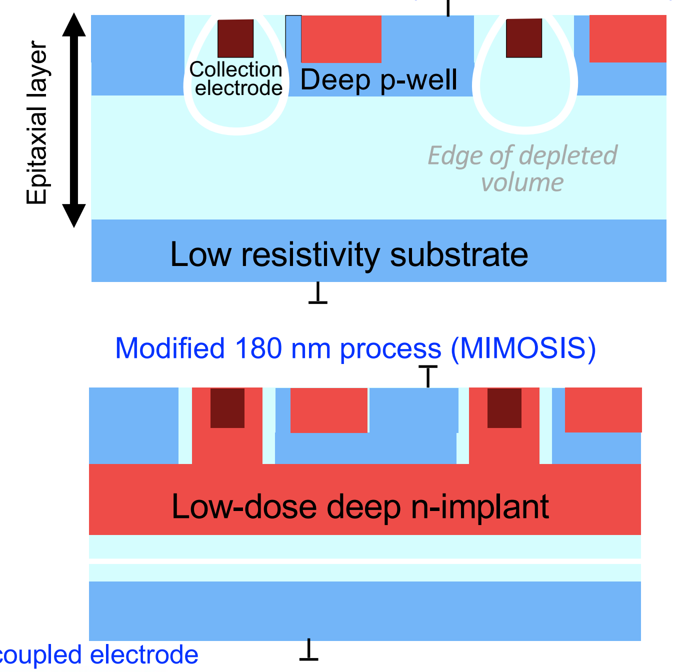
180 nm small-collection-electrode CMOS (I)

Several ongoing developments targeting Higgs-factory vertex detectors with separate layers for timing (~1 μs) and position resolution (<=3 μm)



TaichuPix and JadePix (IHEP et al.) 180nm monolithic sensors

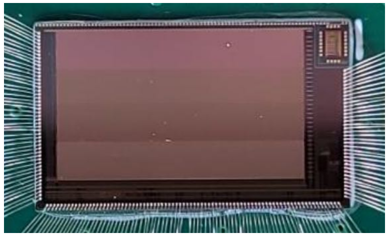
- Standard 180 nm CMOS imaging process with small-collection electrode + high-resistivity epitaxial layer
- Main target: CEPC vertex detector
- Several prototypes, focusing on different aspects (spatial resolution, data rates, timing, full-scale tests)



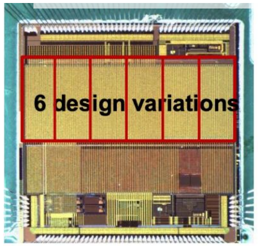
MIMOSIS (IPHC)

- 180 nm CMOS imaging process with small-collection electrode + high-resistivity epitaxial layer + modifications for improved performance, including AC coupled electrodes
- Main target CBM@FAIR, in the future: ILC vertex detector
- Evolution of monolithic sensors since 1999, used in various experiments (EUDET telescopes, STAR-PXL, ALICE-ITS2)

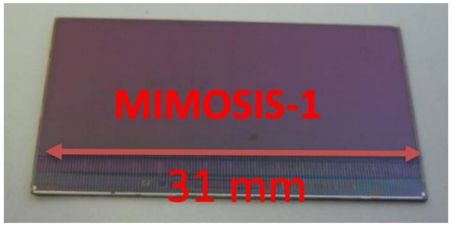
JadePix 3



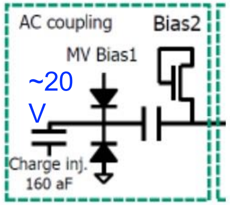
TaichuPix 2



MIMOSIS-1



AC-coupled electrode

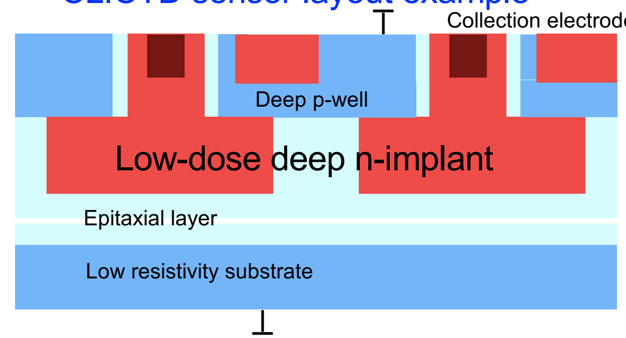


See also talks by Shuqi Li on TaichuPix and Roma Bugiel on Mimosis on Tuesday morning

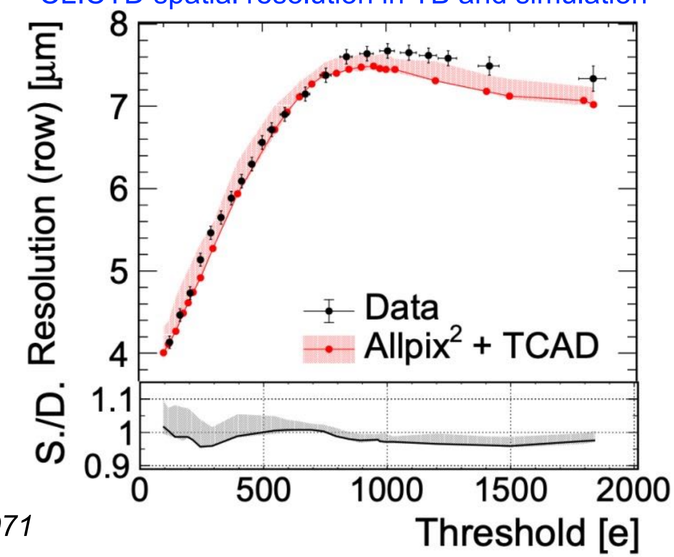
180 nm small-collection-electrode CMOS (II)

CLICTD 180nm monolithic sensor
- Modified 180 nm CMOS imaging process with small-collection electrode
- Target: CLIC tracker
- Innovative sub-pixel segmentation, Channel pitch: (8 x 37.5) μm x 30 μm
- Simultaneous time and energy measurement per channel
- Exploring large parameter space of sensor-design modifications, substrate materials (epitaxial, high-resistivity Czochralski) and thicknesses (40-300 μm), in collaboration with ATLAS MALTA / STREAM
- Detailed TCAD/Geant4-based simulations (Allpix^2), validated with test-beam data

CLICTD sensor layout example



CLICTD spatial resolution in TB and simulation



	Required (CLIC tracker)	Epi	Cz*
Spatial resolution (transv.)	< 7 μm	4.6 μm	4.3 μm
Time resolution*	~ 5 ns	5.2 ns*	4.4 ns*
Efficiency	> 99.7 %	> 99.7 %	> 99.7 %
Material content	< 200 μm	40 - 100 μm	100 μm

IEEE TNS 67.10 (2020): 2263-2272
NIM A 1006 (2021) 0165396
NIM A 1041 (2022) 167413

K. Dort, CERN-THESIS-2022-071

- Excellent performance observed in test-beam measurements and reproduced by simulations
- Validated simulations used for parameter extraction
- Results have served as input to sensor optimization, also for 65 nm process

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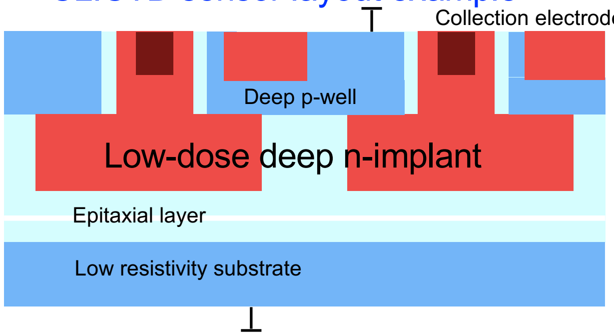
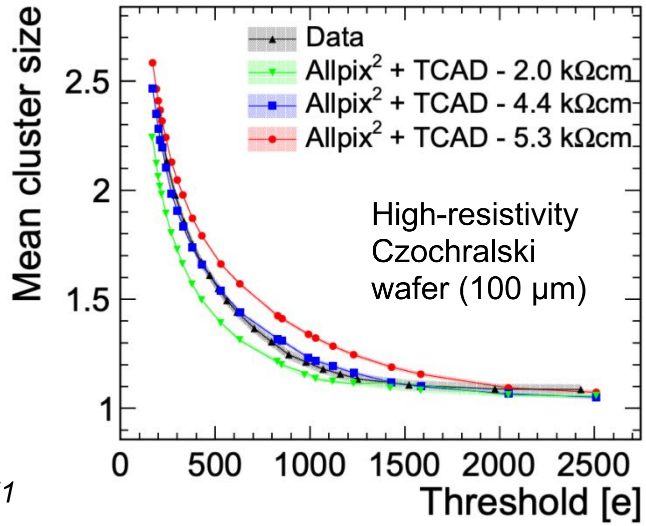


CLICTD cluster size in data and simulation



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K. Dort, CERN-THESIS-2022-071

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- Validated simulations used for parameter extraction
- Results have served as input to sensor optimization, also for 65 nm process

65 nm monolithic CMOS (I)

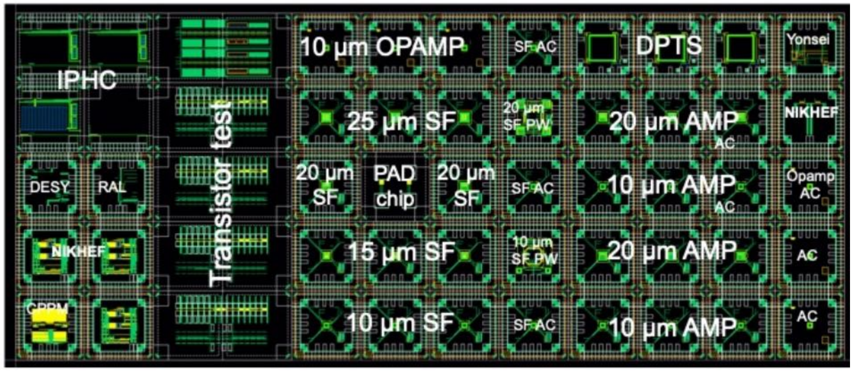
TPSCo 65 nm ISC CMOS imaging process currently being validated for HEP:

- Collaboration CERN EP R&D, ALICE ITS3, TANGERINE, many institutes + other projects
- Smaller feature size → smaller pixels (~10-35 μm), enhanced performance
- Candidate technology for Higgs-Factory vertex/tracker developments
- Encouraging results from first MLR1 test-chip production in 2021:
  - Common submission of technology demonstrators from various groups
  - Successful and ongoing large-scale testing + simulation campaigns
  - Process modifications and sensor-design optimizations proven to work as expected

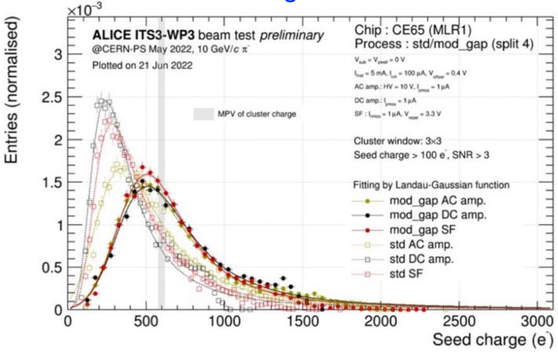
  → Full efficiency + nanosecond sensor timing achieved for optimized designs, up to 10^{15} n_{eq}/cm^2

TANGERINE test-beam + simulation talks by Adriana S., Manuel A.D.R.V., Sara R.D.; APTS talk by Giacomo A. on Thursday

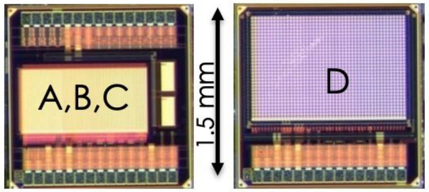
MLR1 reticle 2021



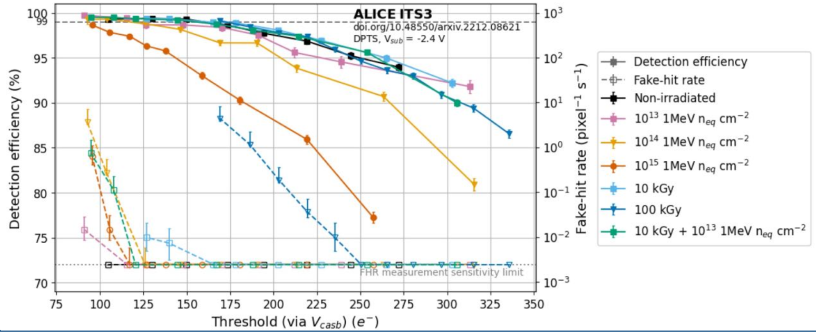
CE-65 cluster-see charge in test beam



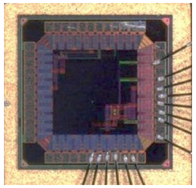
CE-65, 15-25 μm pitch IPHC



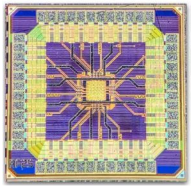
DPTS efficiency + fake-hit rate in test beam



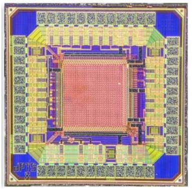
TANGERINE CSA1 2x2, 16 μm pitch DESY



Analog pixel test structure (APTS) 10-25 μm pitch CERN



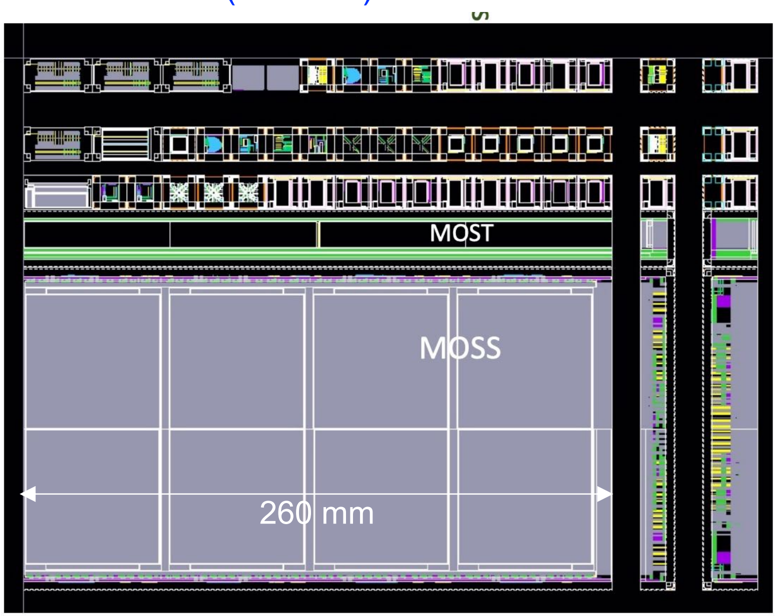
Digital pixel test structure (DPTS) 15 μm pitch CERN



65 nm monolithic CMOS (II)

- Recent TPSCo 65 nm submission in stitched engineering run ER1:
  - Wafer-scale MOST/MOSS (ALICE ITS3)
  - H2M test-chip (hybrid architecture in monolithic process)
  - Improved versions of several test chips from previous MLR1 submission
- Production completed, dicing of samples ongoing, testing to start in coming weeks
- Outlook on future submissions:
  - Expect strong focus on ALICE ITS3 for ER2 (2024)
  - More focused designs for Higgs factories proposed for MLR2 (~2025), to be developed within ECFA detector R&D collaborations DRD3 and DRD7
  - Longer term prospects: Explore advanced technology features (pinned diodes, special photodiodes, wafer-stacking to 65 nm CMOS readout wafer, …)

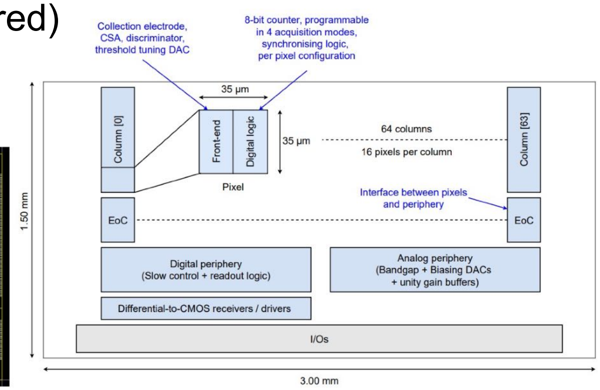
ER1 reticle (2022/23)



H2M – Hybrid to Monolithic

- Demonstrator for porting hybrid readout architecture (Timepix, CLICpix2) to monolithic sensor
- Target applications: large-area trackers; general purpose
- 64x16 pixels, 35 um pitch, 8-bit counters per pixel (ToA, ToT, γ count., triggered)

H2M - DESY, CERN, IFAE

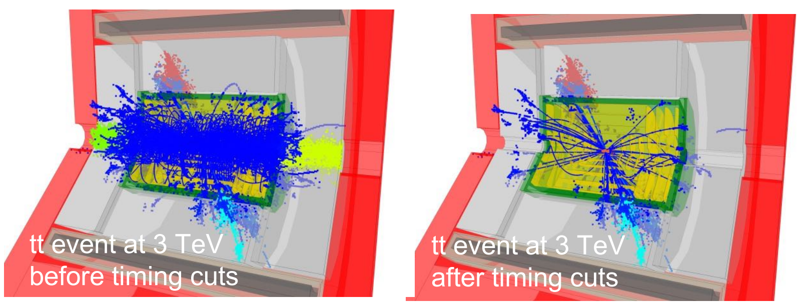


Silicon track-timing detectors

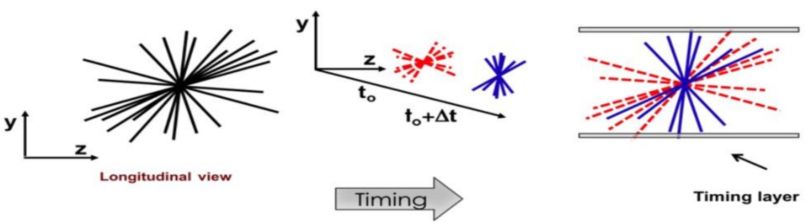
- Several (technology-driven) developments targeting ~20-100 ps pixelated timing for MIPs
  - Dedicated timing layer or integrated in tracker
- Use cases for precision timing:
  - enhanced background/backscatter rejection
  - 4D tracking
  - particle ID by Time-of-Flight for heavy-flavour physics
    → <30 ps / 2m for K/pi/p separation up to 3 GeV

} Not part of the core Higgs-Factory requirements

CLIC background suppression with nanosecond timing

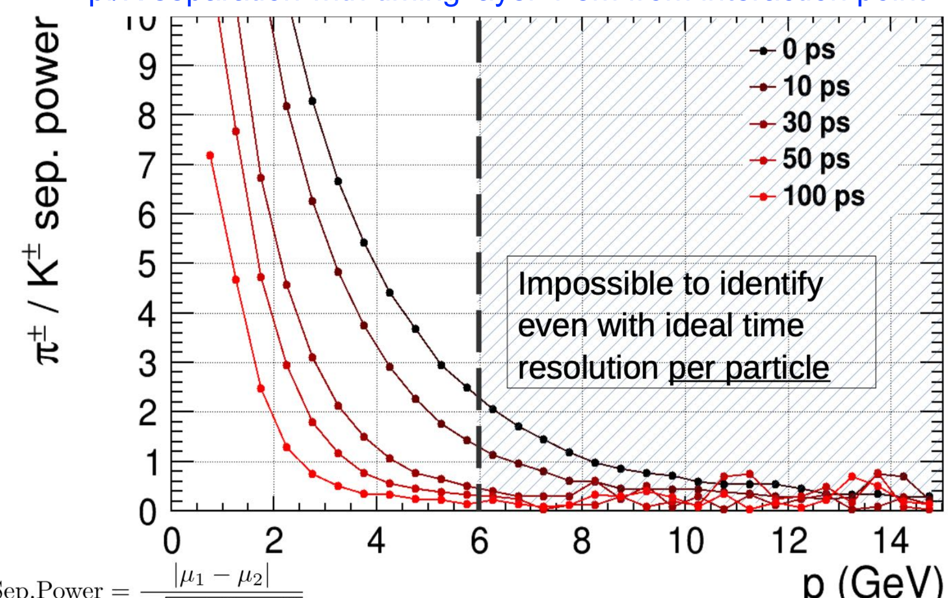


4D tracking



https://agenda.linearcollider.org/event/8217/contributions/44430

pi/K separation with timing layer 1.8m from interaction point



$$\text{Sep.Power} = \frac{|\mu_1 - \mu_2|}{\sqrt{0.5(\sigma_1^2 + \sigma_2^2)}}$$

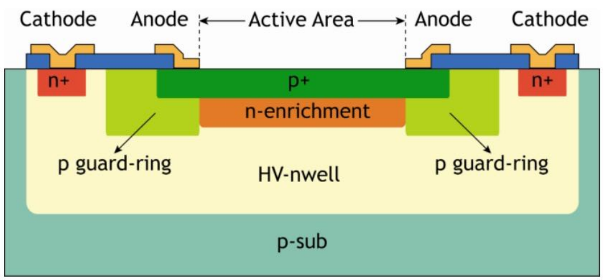
Bohdan Dudar, ECFA Workshop 2022
https://indico.desy.de/event/33640/contributions/128388/

Track-timing detectors: Sensors with internal gain

Silicon Photomultipliers (SiPM):
- Arrays of Single Photon Avalanche Detectors (SPADs)
- High gain ($\sim 10^6$) from thin highly doped multiplication layer
- Challenges: fill factor, quenching, readout, rad. hardness
- Several ongoing developments (hybrid / monolithic)

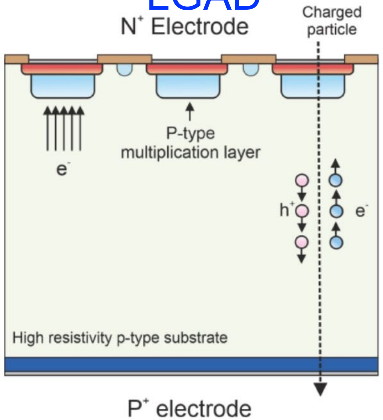
Talks by Stephan Lachnit and Gianpiero Vignola on digital SiPMs on Wednesday

SPAD

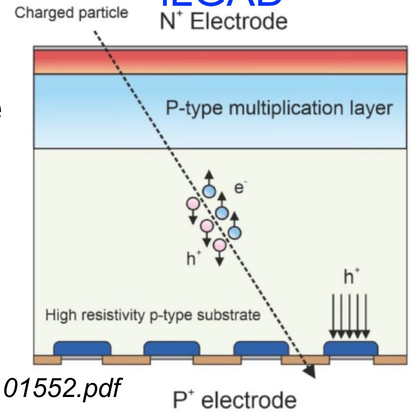


Low Gain Avalanche Detectors (LGAD):
- Signal amplification in thin multiplication layer, ~10x gain
→large (4 fC) and fast (<70 ps RMS) MIP signals
- Achieved so far: $\sim 1\ \text{mm}^2$ cell sizes, ~95% fill factor, rad.hard. $>10^{15}\ n_{eq}/cm^2$
- In production now for ATLAS and CMS timing layers ($6\text{-}16\ \text{m}^2$)
- Challenges:
  - Hybridisation
  - Resolution limited by time walk, readout ASIC
  - Cell size / fill factor limited by inactive regions between pixels
  → inverted LGADs (iLGAD): continuous multiplication layer on backside

LGAD



iLGAD



Talks by Oleksii Kurdysh on ATLAS HGTD LGAD test beams on Wednesday and by Peter Svihra on pixelated iLGAD test-beam results on Thursday

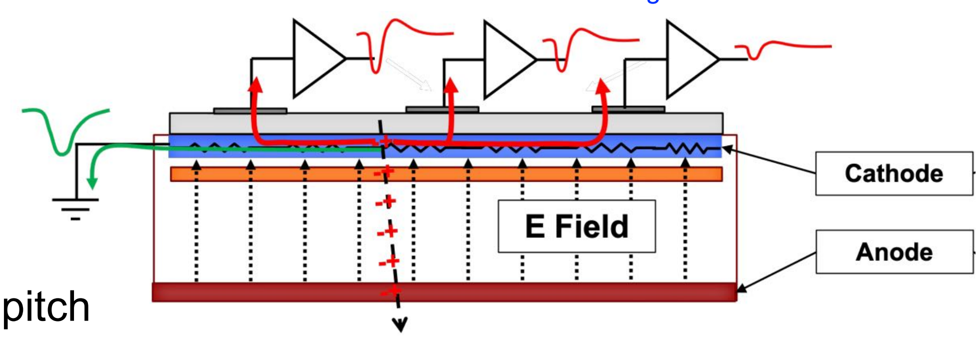
https://arxiv.org/pdf/2202.01552.pdf

Track-timing detectors: AC-coupled LGAD

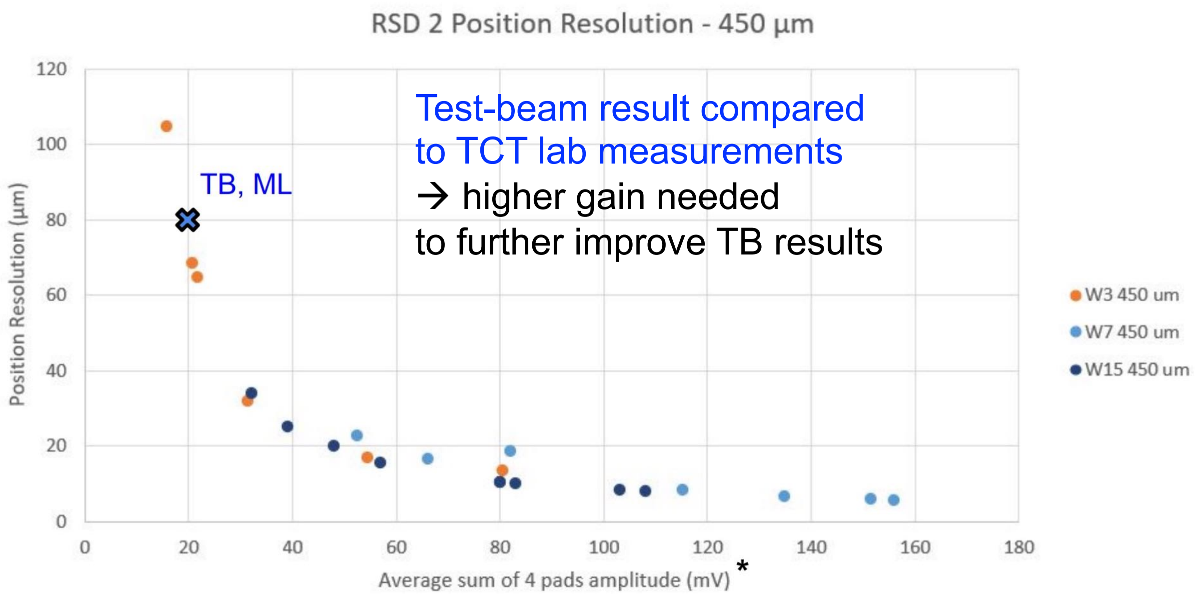
Resistive (AC-coupled) LGAD (RSD)

- Resistive cathode, AC-coupled to r/o pads
  → enhanced position resolution through amplitude interpolation
  → suitable as timing layer in low-occupance regions
- Time resolution of ~25-30 ps achieved
- Position resolution of 80 μm for 450 μm r/o pitch
  → significantly better than standard LGAD with same pitch

RSD-based tracking detector

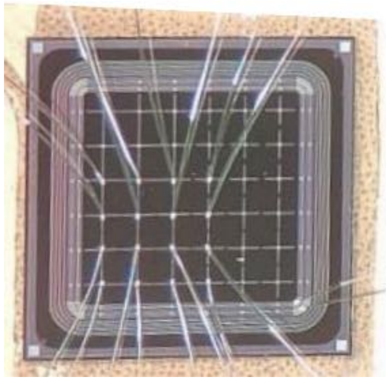


http://dx.doi.org/10.1016/j.nima.2022.167228
N. Cartiglia et al.



F. Siviero, Trento Workshop 2023
https://indico.cern.ch/event/1223972/contributions/5261996/

RSD prototype, 450 μm pitch

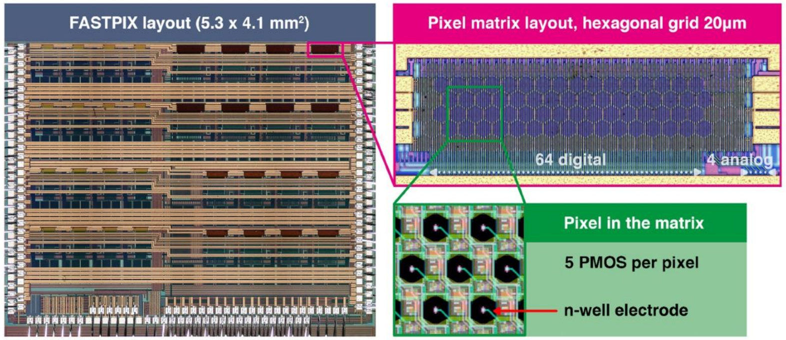


Talk by Shirsendu Nanda on AC-LGAD on Thursday

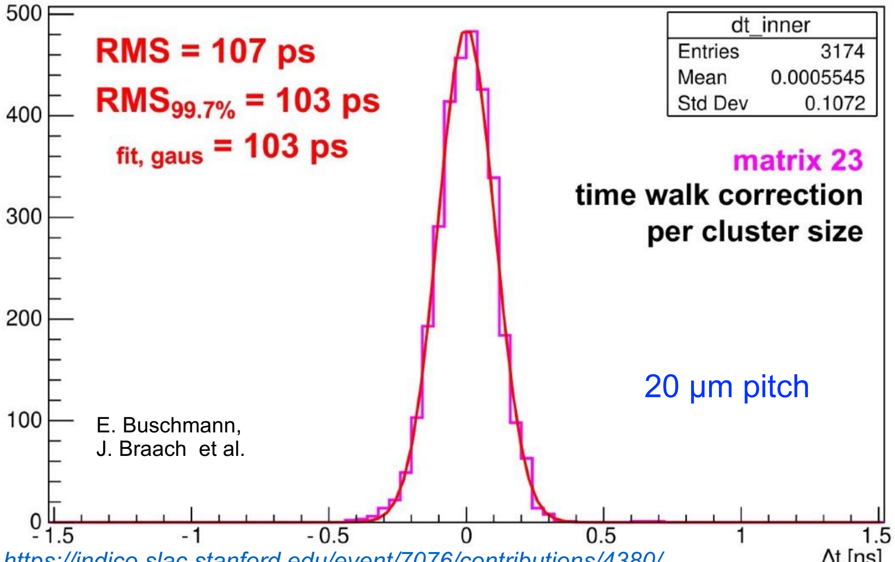
Track-timing detectors: monolithic

FASTPIX technology demonstrator for sub-ns timing

- Modified 180 nm CMOS imaging process, design optimisations for for fast charge collection
- Small hexagonal pixels (8.7 to 20 µm pitch)
- Focus on sensor performance, with limited in-pixel circuitry and not optimised for low power yet
- Exploring large parameter space of process and design variations
- Time resolution of ~100 ps achieved in test beam at >99% efficiency
- Position resolution ~1 µm for 8.7 µm pitch

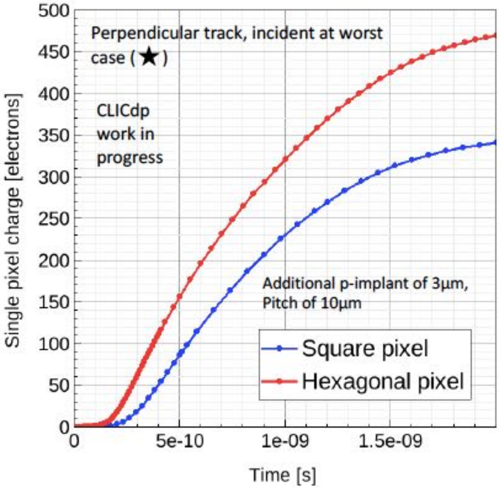


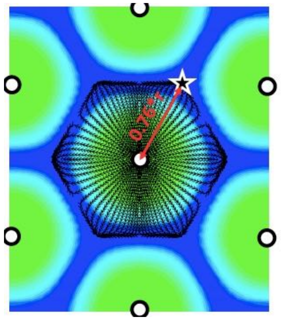
FASTPIX time resolution in test beam



https://indico.slac.stanford.edu/event/7076/contributions/4380/
http://dx.doi.org/10.3390/instruments6010013

FASTPIX 3D TCAD Simulation





T. Kugathasan et al: Monolithic CMOS sensors for sub-nanosecond timing, Hiroshima 2019

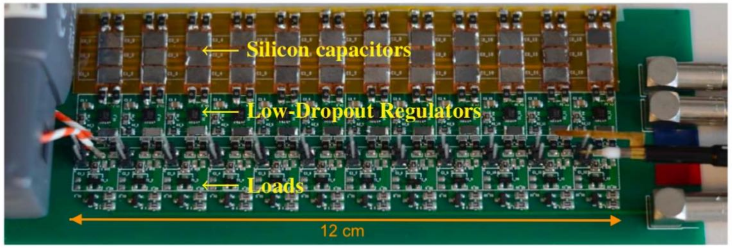
- Optimised for precise sensor timing in 3D TCAD simulation studies
- Hexagonal pixel layout:
  - Improved charge collection at pixel edges
  - Reduced number of neighbouring pixels → Less charge sharing

M. Munkeret al.

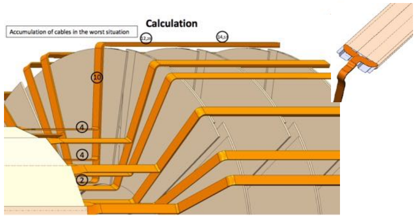
Small-pitch monolithic timing also explored in SiGe BiCMOS process: talk by Théo Moretti on MONOLITH on Thurdsday

Silicon detector integration

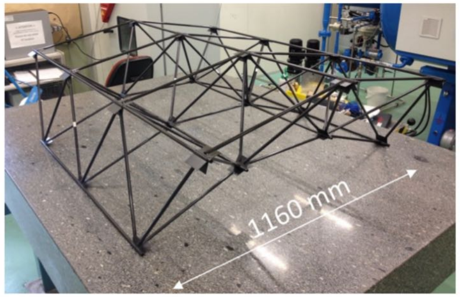
Power-pulsing mockup



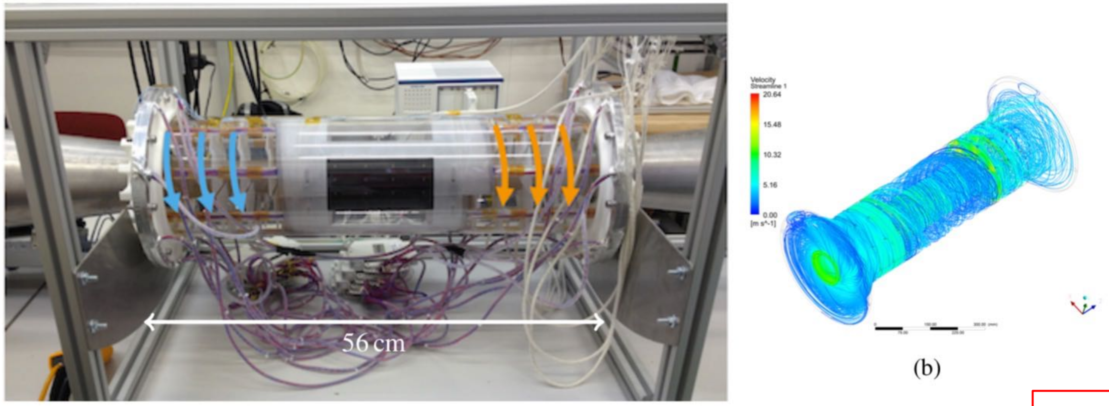
Vertex-detector services



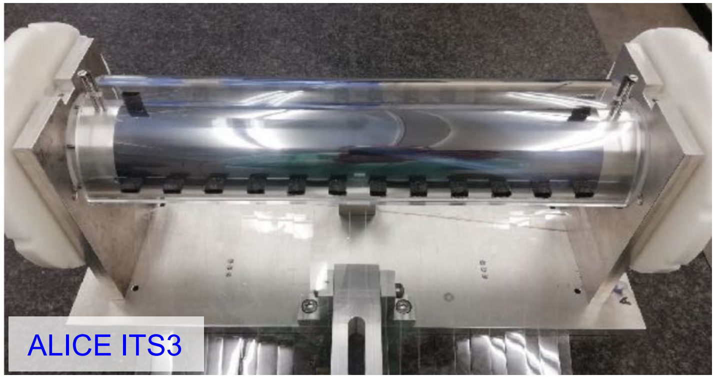
Outer barrel tracker support structure



Air-flow cooling mockup and simulation



Bent wafer-scale dummy sensor on foam support



Talk by Mihail Bogdan Blidaru on bent ALPIDEs on Thursday

- Engineering studies based on calculations, simulations, prototyping
  → confirm feasibility of detector concepts + provide input for realistic performance simulation
- Profit from recent developments in approved projects (Belle II, ALICE ITS3, CMB@FAIR)
- However: not all critical Higgs-Factory requirements are fulfilled by these developments (e.g. barrel/endcap geometries, combination of low material budget and precise timing)
- More focused effort required, but depends also on choice of project (linear vs. circular)

Conclusions + Outlook

- Stringent requirements for Higgs-Factory vertex and tracking detectors:
  - Precision physics needs
  - Environmental conditions
- Several optimized detector concepts with different technology choices are proposed
- Broad silicon R&D profiting from advancements in semiconductor industry + simulations
- Focus on sensor (test-beam) performance; engineering/system aspects not yet fully addressed (many of them depend on accelerator choice)
- Large synergies with approved projects, but no complete overlap of requirements
- Fulfilling all Higgs-Factory requirements simultaneously remains challenging

Thanks to everyone who provided material for this lecture!

Additional Material

ACF for module integration

ACF module integration

Larger bonding pads: 80 μm – few mm diam.

→ Similar to industrial ACF usage

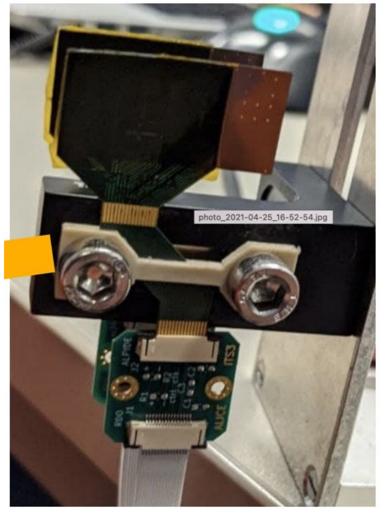
→ Good interconnect results

→ Topology / uniformity of UBM important

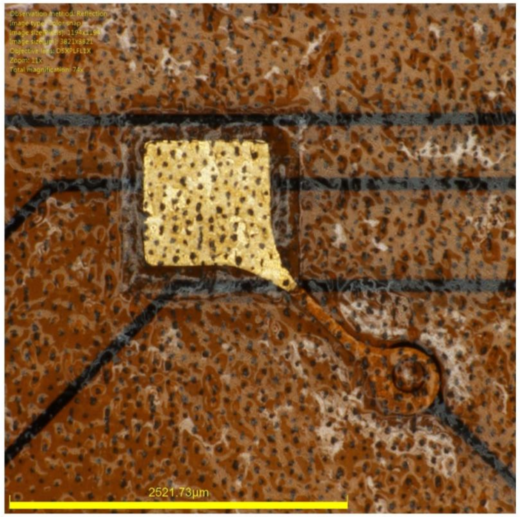
Various proof-of-concept projects:

- Beam tests of ALPIDE ACF modules
- Bonding tests with MALTA silicon bridges
- Tests with FCAL LUXE pad sensors

ALPIDE ACF module in DESY TB

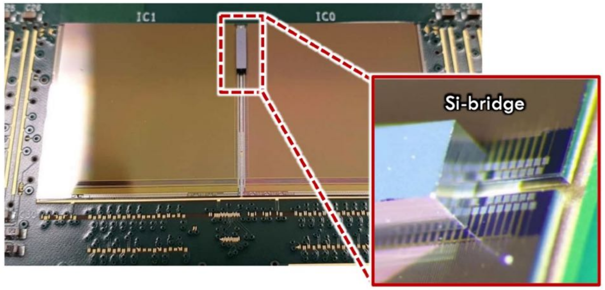


ACF on LUXE pad

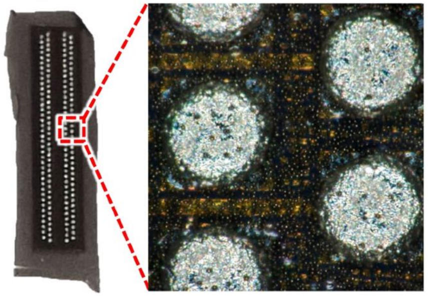


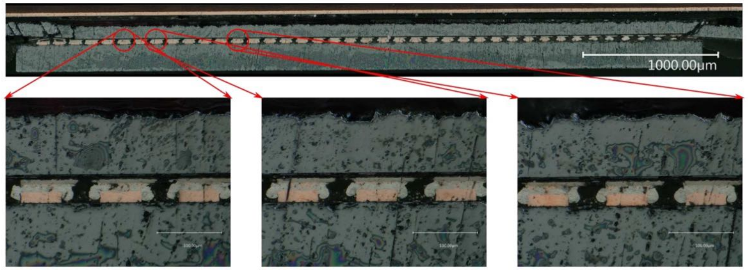
MALTA module building with silicon bridge and ACF bonding

MALTA double module with Si-bridge chip (images credit: Florian Dachs)



Si-bridge with ACF   ACF over Si-bridge pads





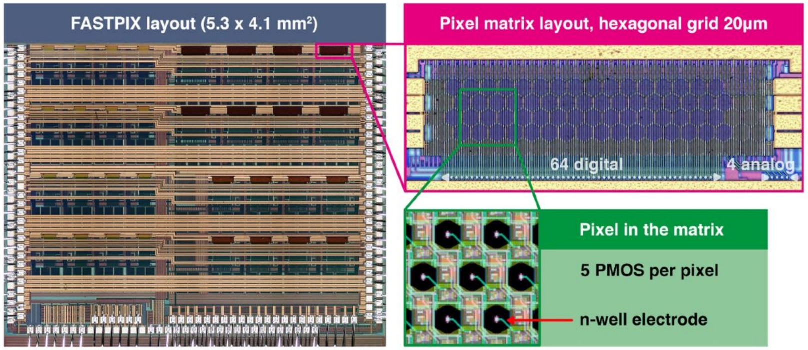
Cross section for 5kg of pressure.

M. Mager, F. Dachs, Y. Benhammou

ATTRACT FASTPIX

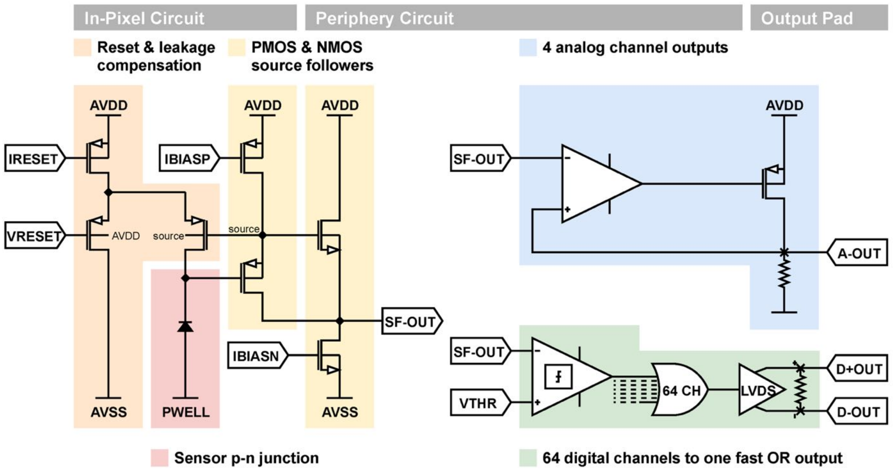
FASTPIX technology demonstrator for sub-ns timing

- Modified 180 nm CMOS imaging process
- 32 mini matrices of hexagonal pixels (8.66 to 20 µm pitch)
- 4 analogue outputs + 4x16 pixels with ToT/ToA
- Various sensor designs and process options
- Position and ToT encoding via delay lines (asynchr. r/o)



On-chip readout circuit

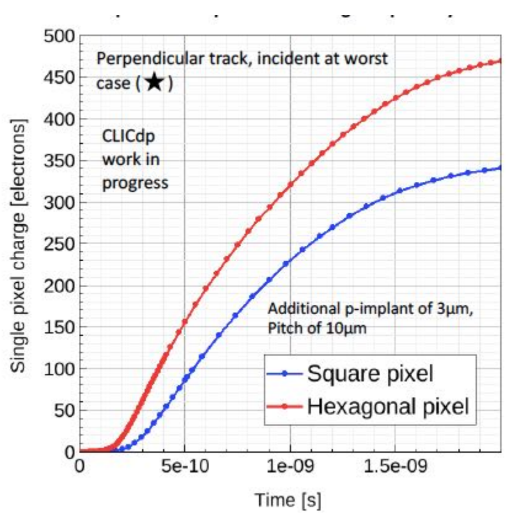
W. Snoeys, T. Kugathasan

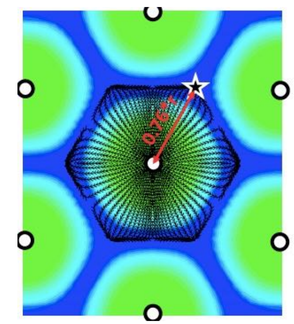


Simulated chip parameters:

Sensor capacitance		1 fF
Equivalent Noise Charge		11 e⁻
Jitter (for Q_{in} = 1000 e⁻)		20 ps
Power	In pixel source follower	18 µW
	Periphery discriminator	150 µW
	Analog monitoring buffer	20 mW

3D TCAD Simulation





T. Kugathasan et al: Monolithic CMOS sensors for sub-nanosecond timing, Hiroshima 2019

- Optimised for precise sensor timing in 3D TCAD simulation studies
- Hexagonal pixel layout:
  - Improved charge collection at pixel edges
  - Reduced number of neighbouring pixels → Less charge sharing

Caribou DAQ

Versatile data acquisition system based on programmable hardware

https://gitlab.cern.ch/Caribou

System-on-Chip (SoC) board

- Embedded CPU for DAQ, user interface, operating system (Linux)
- Field programmable gate array (FPGA) for detector control and data processing

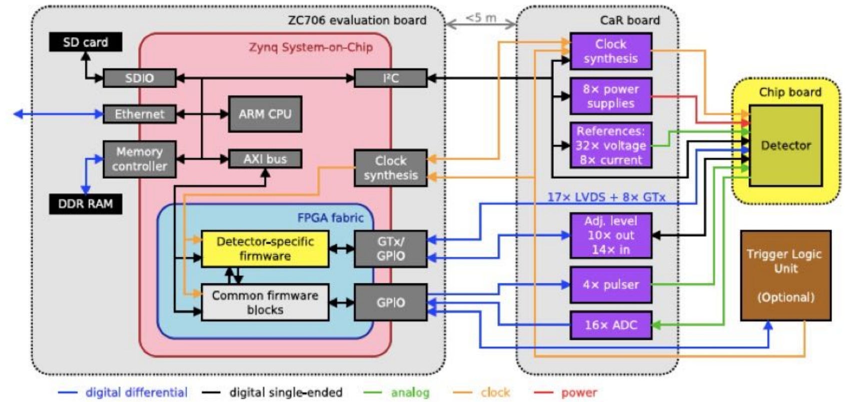
Control and Readout (CaR) interface board

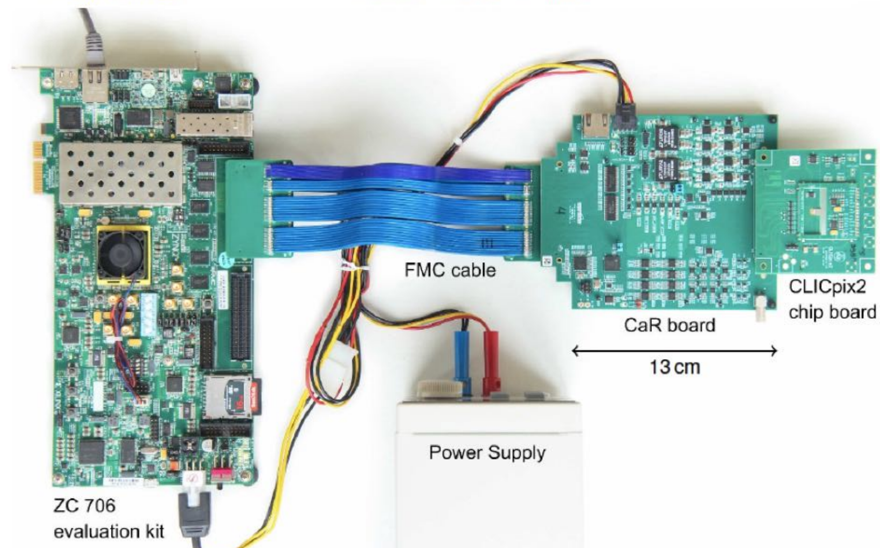
- Physical interface from SoC board to detector chip
- Voltage regulators, ADCs, pulse/clock generator

Application-specific detector carrier board

- Only detector chip and passiv components

- Successfully used for ATLASPix, ATLASPix2, ATLASPix3, CLICpix2/C3PD, H35Demo/FEI4, RD50-MPW1





https://iopscience.iop.org/article/10.1088/1748-0221/12/01/P01008

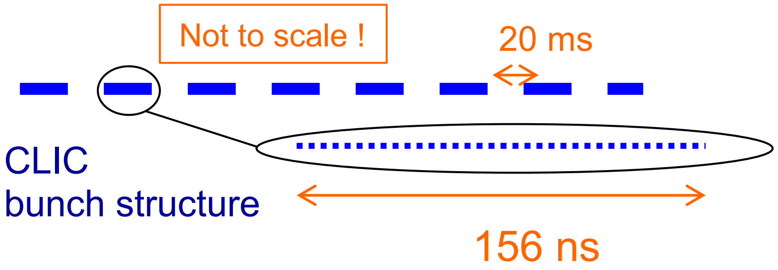
Experimental conditions at CLIC

- CLIC operates with bunch trains, 50 Hz repetition rate

→ Low duty cycle

→ Trigger-less readout between trains

→ Allows for power-pulsed operation of detector, to reduce average power consumption

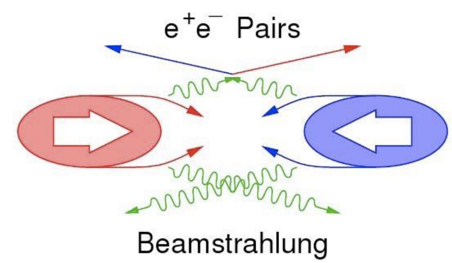


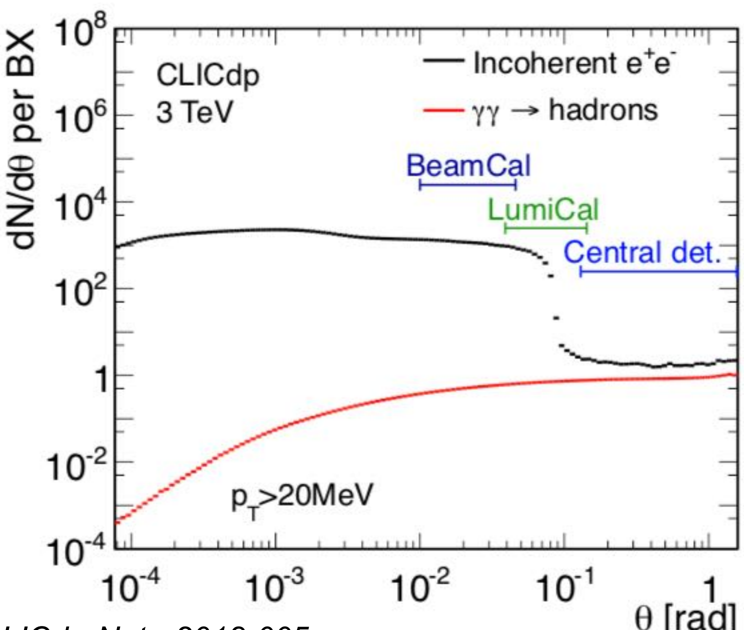
- Collisions within 156 ns bunch trains
- High E-fields lead to Beamstrahlung

→ High rates of beam-induced background particles

→ Drives detector design (layout, granularity, timing)

Very small bunches:
40 nm (x) x 1 nm (y) x 44 µm (z)
(at 3 TeV)





CLICdp-Note-2018-005

Main backgrounds in detector

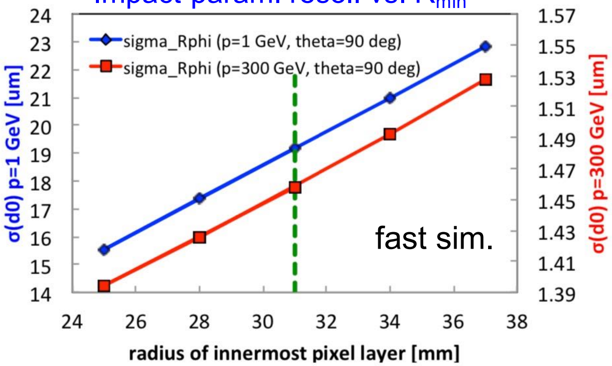
- **Incoherent e+e- pairs**
  - 19k particles / bunch train at 3 TeV
  - Constrains beam pipe radius, granularity
- $\gamma\gamma$ →hadrons events
  - 17k particles / bunch train at 3 TeV
  - Constrains granularity, layout, impacts physics

High instantaneous hit rates (up to 6 GHz/cm²), however: very low readout rate (50 Hz)

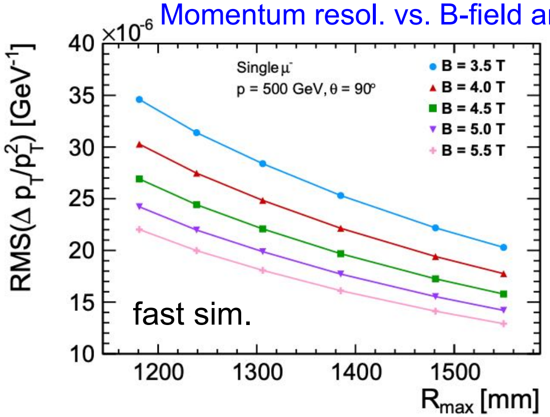
CLICdet detector design optimisation

- Study impact of technology parameters (pixel size, material budget) on detector performance
- Optimization of detector geometry (# layers, placement) for given technology assumptions
- Using fast simulations (LiC detector toy) and Geant-4 based full detector simulations including beam-induced backgrounds
- Main benchmark parameters: impact-parameter and momentum resolution, flavor-tagging performance, reconstruction efficiency

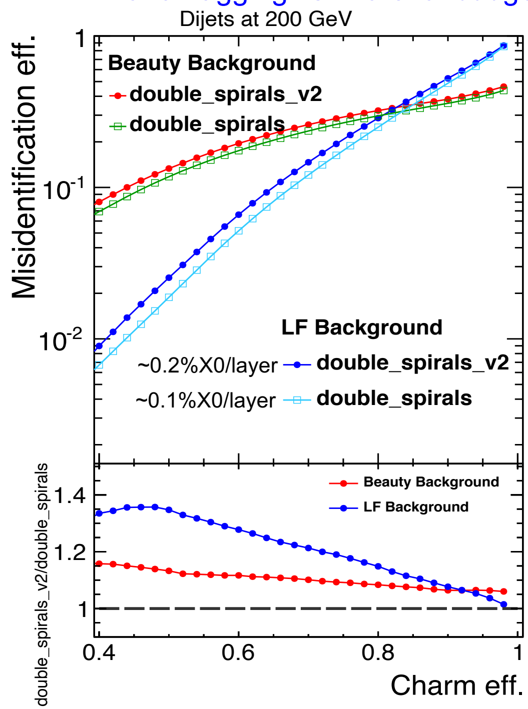
Impact-param. resol. vs. R_{min}



Momentum resol. vs. B-field and R_{max}



Flavor tagging vs. material budget



Flavor tagging vs. resolution