Aachen Graphene & 2D Materials Center

BERGISCHE UNIVERSITÄT WUPPERTAL

AMO

2D Materials for future electronic applications

1. Introduction
2. TMDC based electronics
3. Graphene based RF circuits
4. Production
5. Conclusion

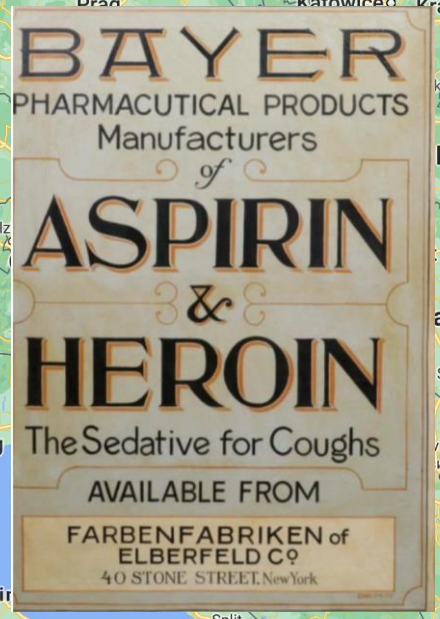
Daniel Neumaier

AMO GmbH

University of Wuppertal

Wuppertal

Aachen

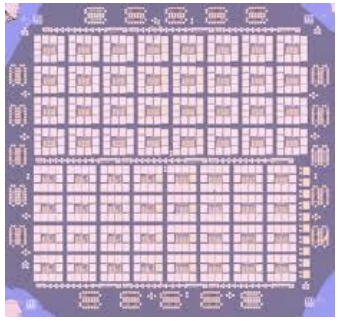


University of Wuppertal:

- Established in 1972
- Covering all disciplines
- 23000 students (mainly from Germany)
- 260 Professors

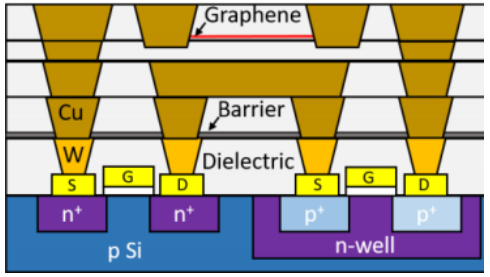
Research Area “Novel Electronics and Photonics”
Chair of Smart Sensor Systems– Prof. Daniel Neumaier

Integrated Circuits



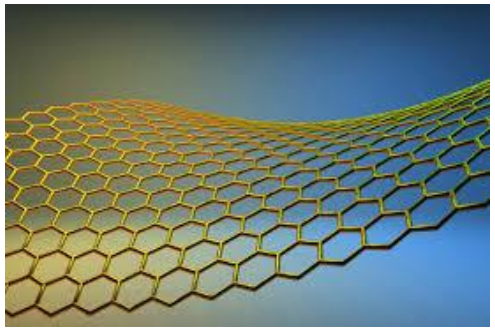
- Sensor Read-out
- Sensor Control

3D Integration on CMOS



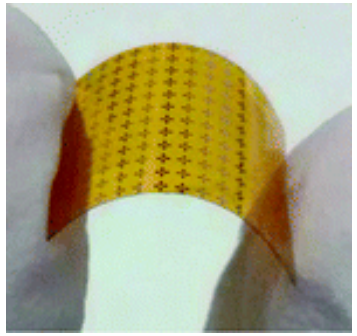
- New Sensor Functionalities in Silicon

2D Materials



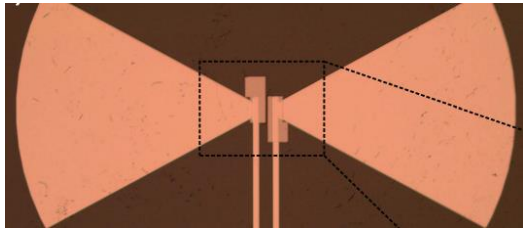
- Graphene
- MoS_2
- hBN

Flexible Electronics



- Wearables
- Health-Care

Energy Harvesting



- Thermo-Electric
- RF-THz

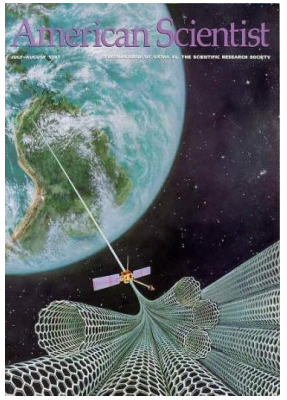
Two dimensional Materials

Diamond

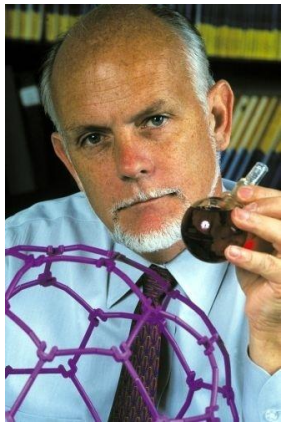
Graphite

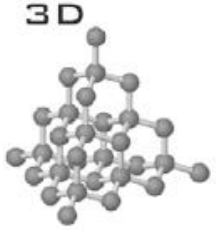
Graphene

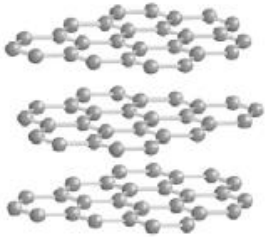
Carbon Nanotubes

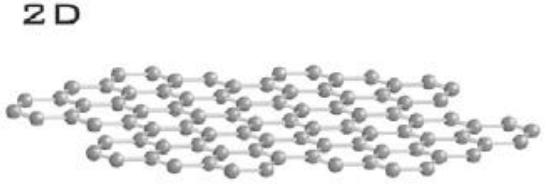


Fullerene / C_{60}

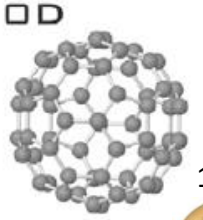








2010



1996

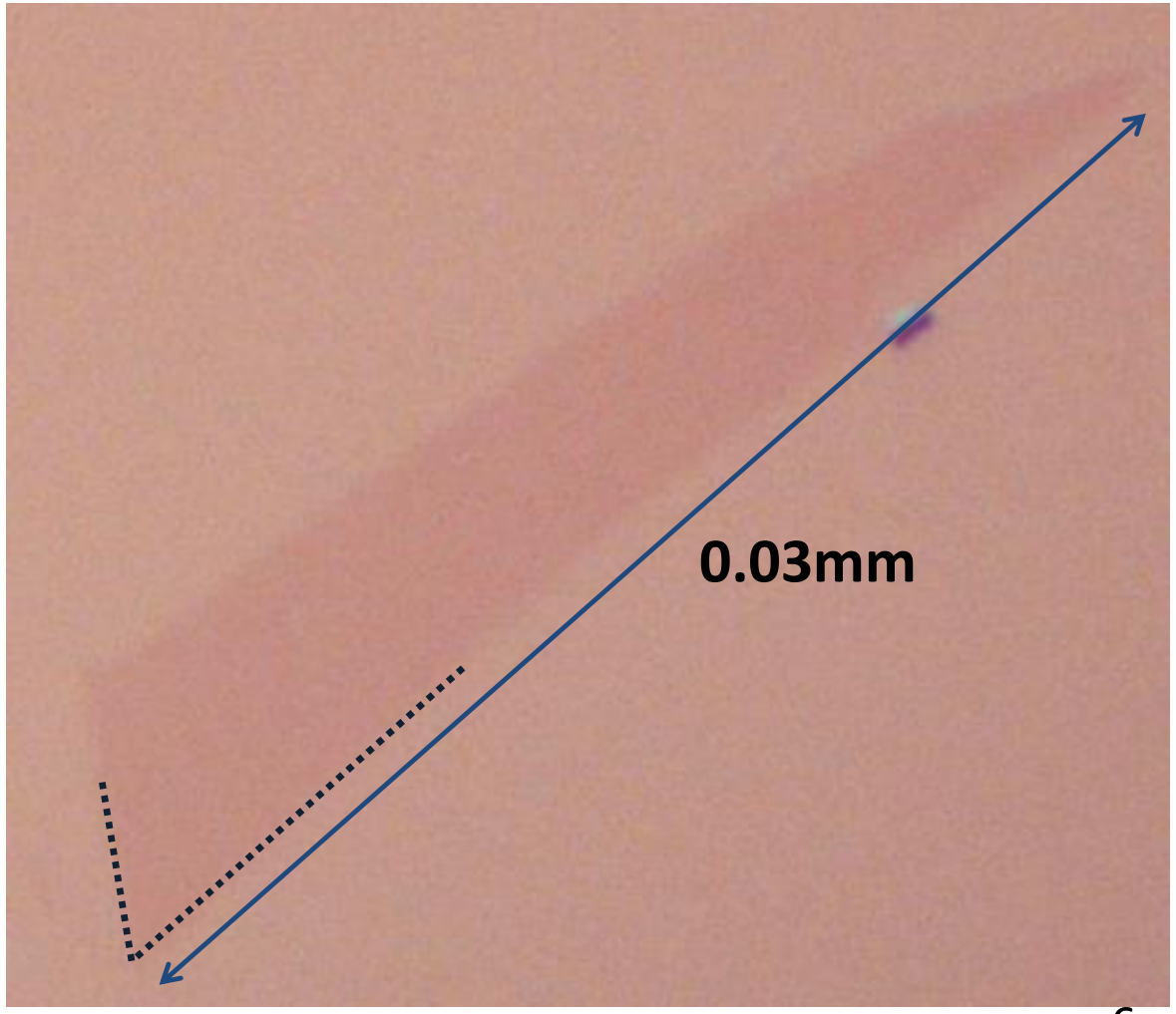
Graphene device production

Photo: Sergeom, Wikimedia Commons

Andre Geim

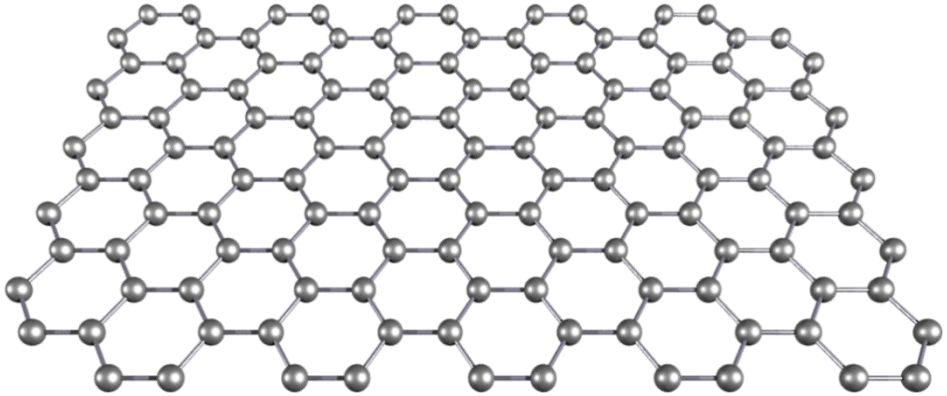
Photo: University of Manchester, UK

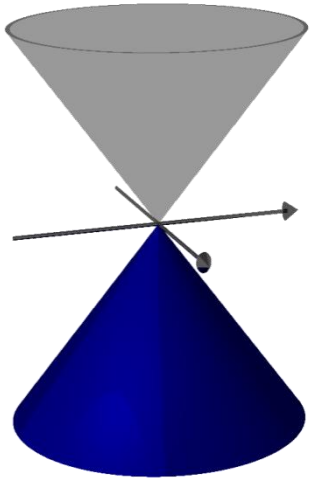
Konstantin Novoselov



Graphene

- Conducting
- High carrier mobility
- Ultimately thin
- Solution processable
- Optical transparent
- Linear dispersion relation
- Flexible and strong
- Chemically inert
- Bio compatible



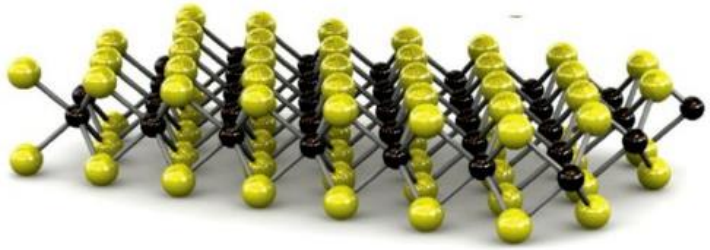


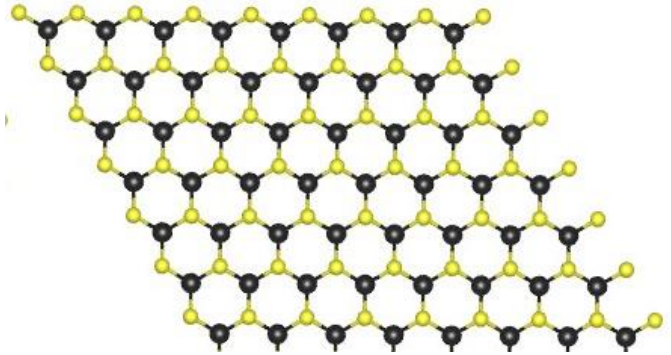
➢ **High performance active components (transistors, diodes)**

➢ **Compatible with Thin-Film-Technology.**

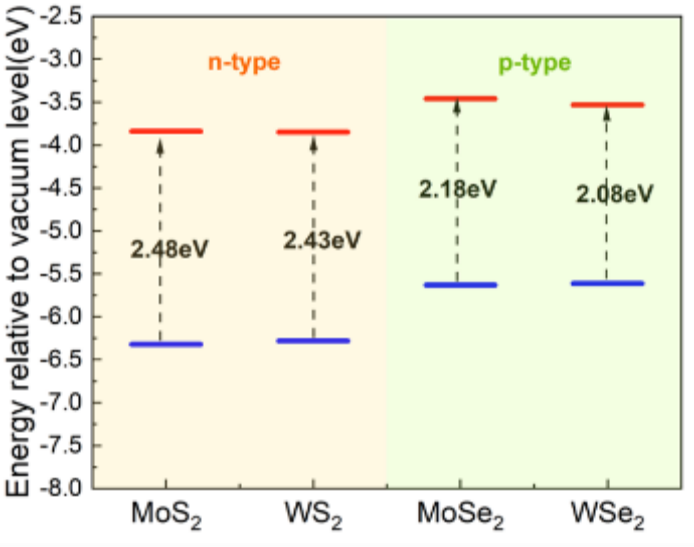
TMDC= Transition Metal DichalCogenide

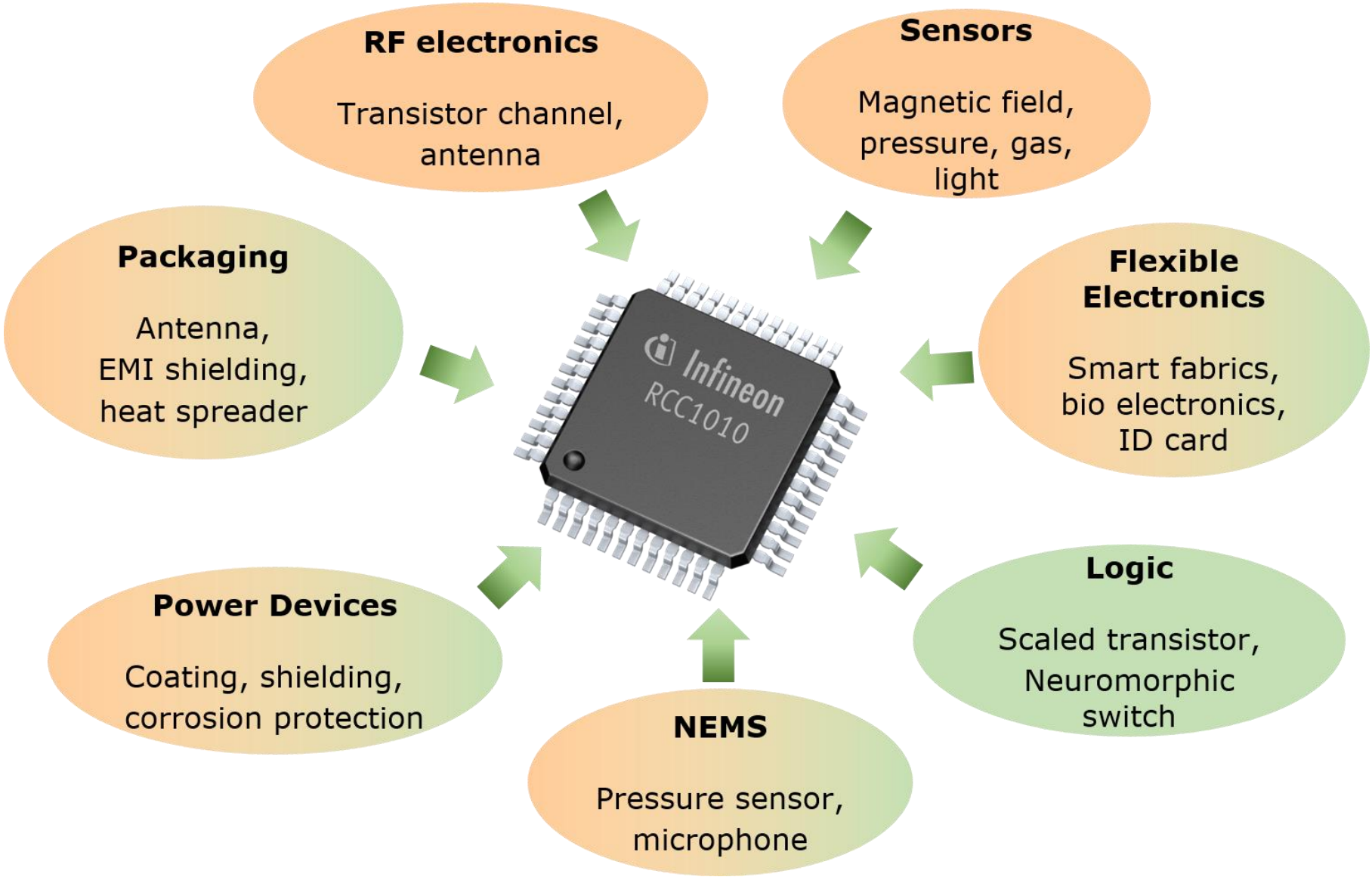
Crystal lattice:





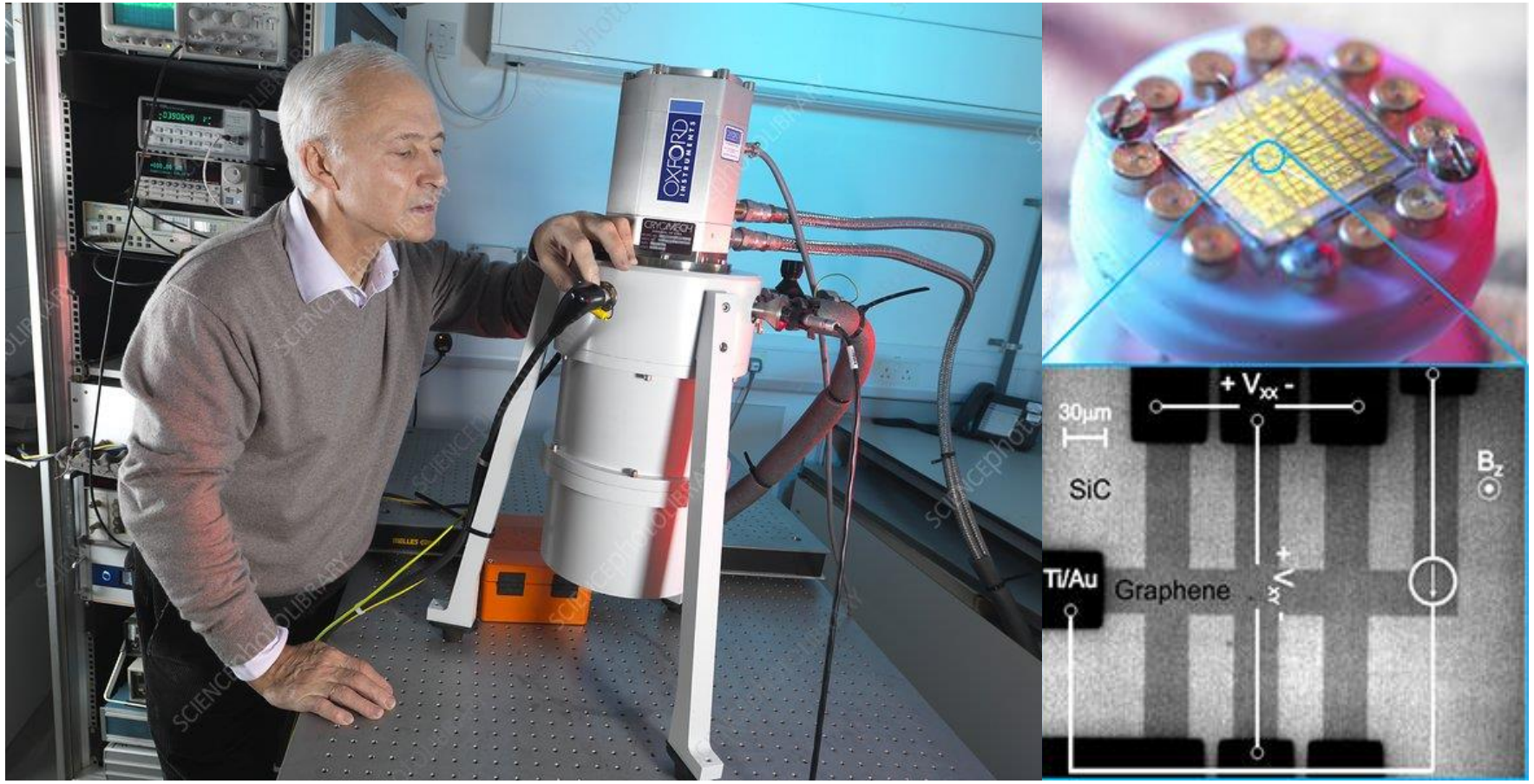
- Atoms: Transition metal (Mo, W..) plus Chalcogen (S, Se..).
- Generally MX_2: M is in the middle, X is on-top and below.
- Three atoms per unit cell.
- Top-view: hexagonal lattice.
- Van der Waals interaction between the different layers.
- k-space is also hexagonal (similar to graphene).
- Density pretty high (heavy metal). Typ. 5 g/cm².





D. Neumaier, Stephan Pindl and Max Lemme Nature Materials 2019

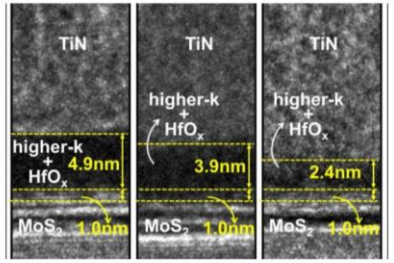
Oxford Instruments



Graphene based photodetectors

- IR imaging with graphene enhanced CMOS technology.
- Commercialized by different companies.

TMDC based FETs for ultra-scaled logic



TSMC heads below 1nm with 2D transistors at IEDM

Technology News | October 18, 2022

By Nick Flaherty

MATERIALS & PROCESSES

Researchers at leading foundry TSMC are developing transistors with feature sizes below 1nm t scale chip designs even further and have shown the first nanosheet transistor with a gate all around (GAA) topology

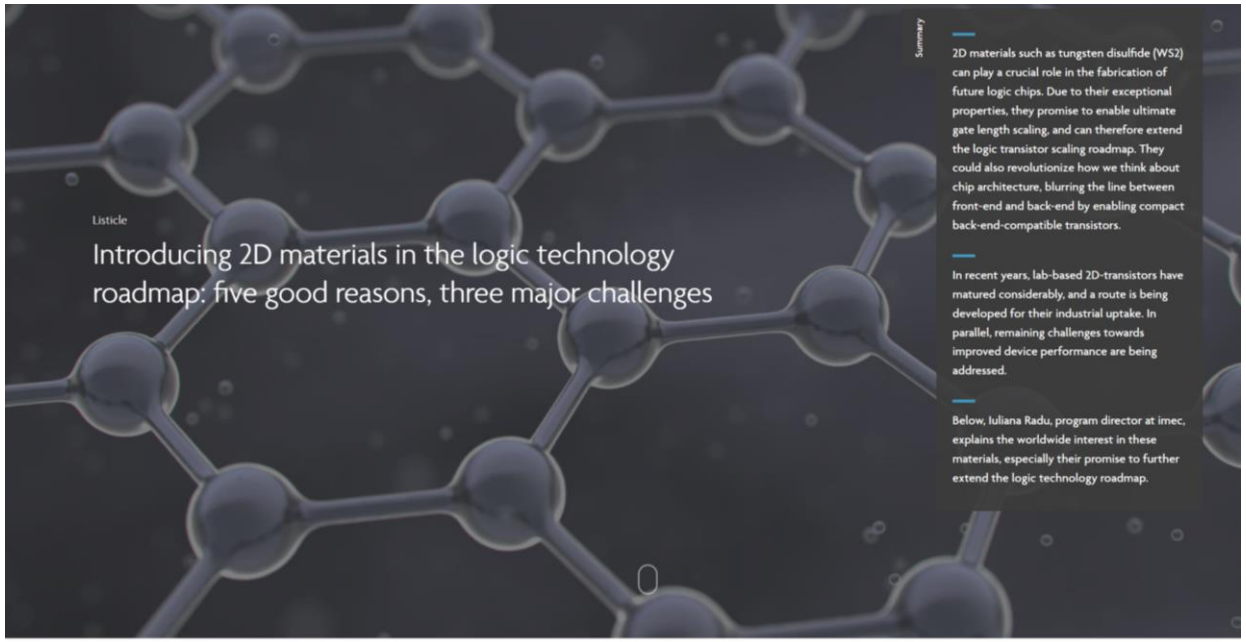
A strand at the coming IEDM device conference in December is looking at the development of 2D transistors using different materials. The conference, now celebrating 75 years, is an important view of the roadmap for scaling transistor device technology.

The researchers at TSMC have been working with layers of transition metal dichalcogenides (TMDs) such as MoS2 that are just one atom thick. A key challenge of these materials is that it's quite difficult to deposit pinhole-free dielectric layers, or insulators, onto them. That makes it difficult to incorporate them into the stack of materials which forms a transistor gate.

The team has integrated hafnium-based dielectrics formed by atomic layer deposition with the monolayer TMD material MoS2, to build a top-gated nFET with a physical dielectric thickness o 3.4 nm and an electrically equivalent oxide thickness (EOT) of ~1 nm.

The subthreshold swing (SS) is key in MOSFET transistors, and the devices had a nearly ideal SS of <70 mV/dec

IMEC



1. 2D materials have remarkable properties

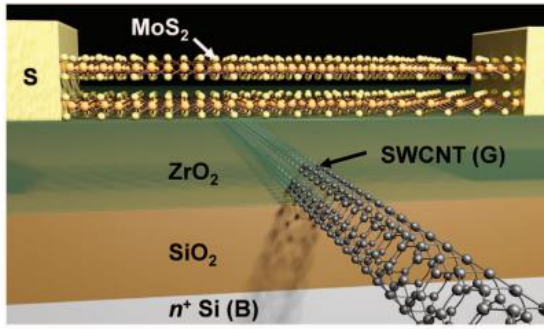
2D materials are a class of materials that form two-dimensional crystals. In this elegant 2D form factor, they have fascinating electrical, thermal, chemical and optical properties. The most famous of these materials is graphene, a hexagonal honeycomb shaped sheet of carbon atoms. Graphene has an outstanding mechanical strength, a large conductivity for both heat and electricity, and odd optical abilities.

But the exploration of 2D materials has moved far beyond graphene. The class of transition metal dichalcogenides, with

Iuliana Radu
Program Director responsible for exploratory logic activities at imec

Iuliana Radu is program director at imec, where she is

TMDC based FETs for ultra-scaled logic



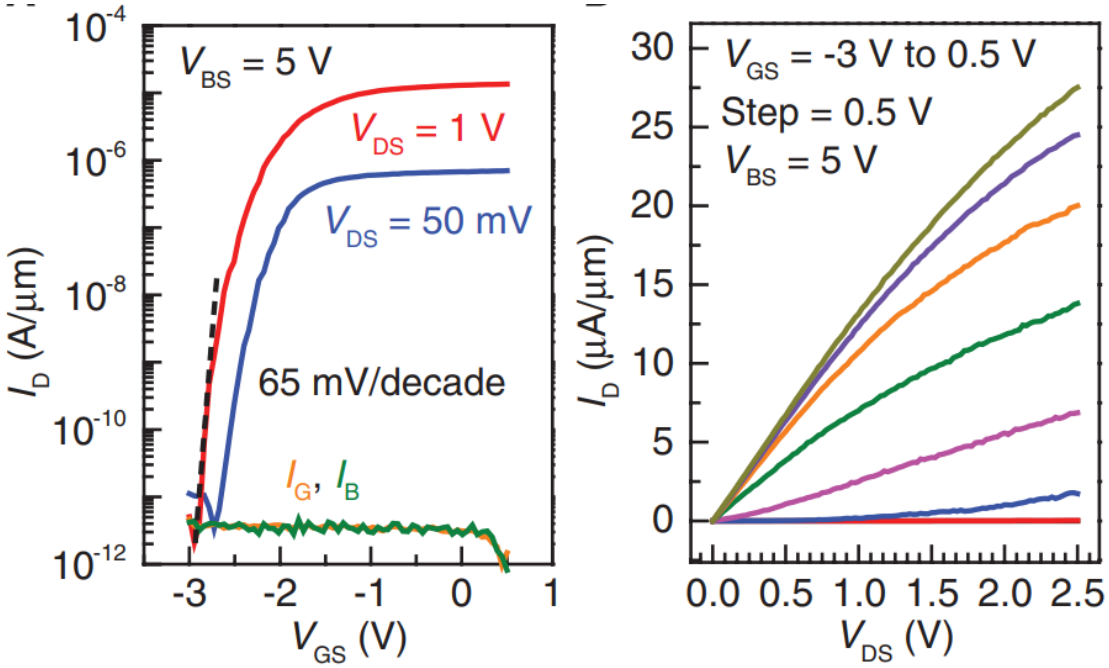
- Metallic CNT used as 1nm long gate for a MoS2 FET.
- ZrO2 (high k) used as dielectric.
- ➢ Still very good FET behaviour.

DEVICE TECHNOLOGY

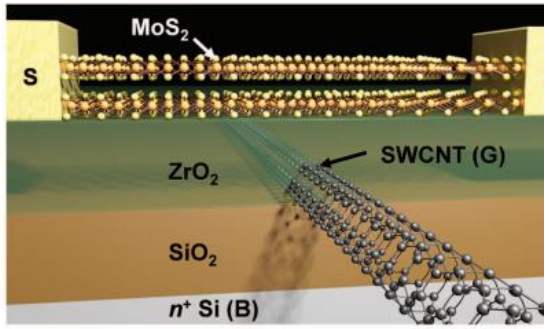
MoS_2 transistors with 1-nanometer gate lengths

Sujay B. Desai,[1,2,3] Surabhi R. Madhvapathy,[1,2] Angada B. Sachid,[1,2] Juan Pablo Llinas,[1,2] Qingxiao Wang,[4] Geun Ho Ahn,[1,2] Gregory Pitner,[5] Moon J. Kim,[4] Jeffrey Bokor,[1,2] Chenming Hu,[1] H.-S. Philip Wong,[5] Ali Javey[1,2,3]*

Berkley team, published in Science 2016



TMDC based FETs for ultra-scaled logic



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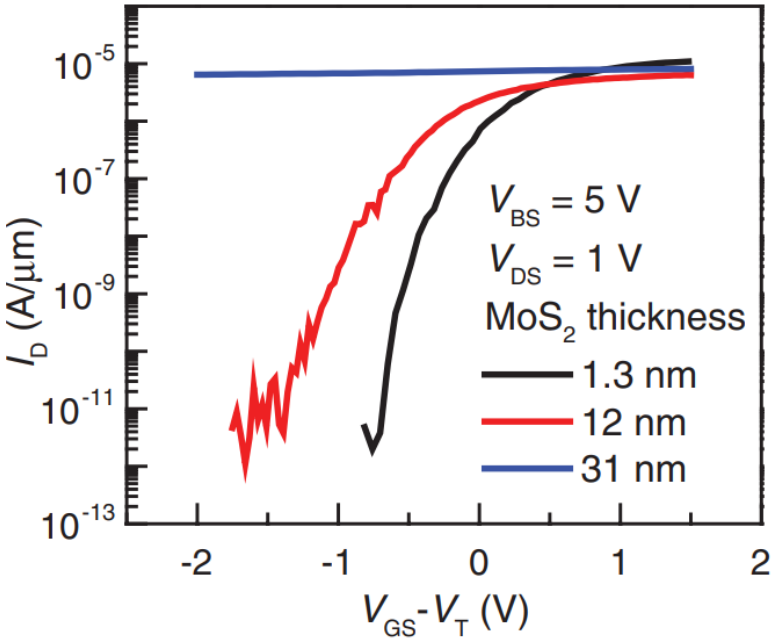


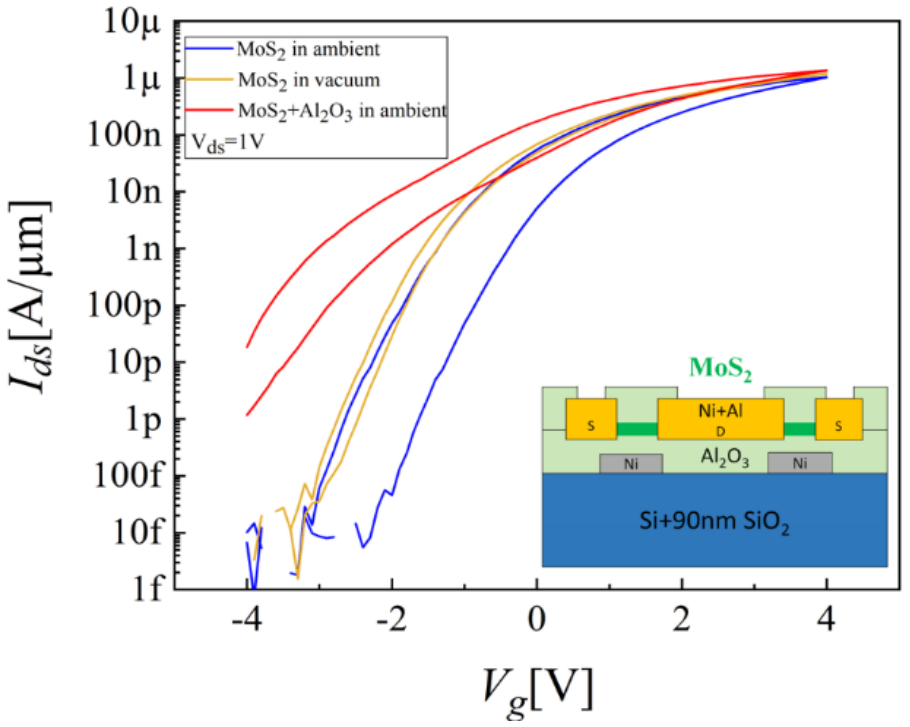
➢ Clear dependence on the layer number!

Target: Reliable nMOS FETs based on MoS_2

<u>Problem to be solved:</u>
Strong n-type doping after encapsulation; large hysteresis

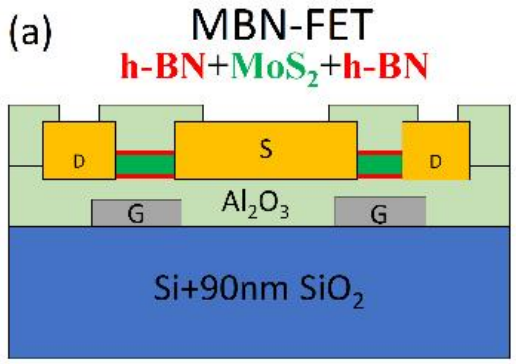
<u>Reason:</u>
Charge transfer from Al_2O_3 to MoS_2; defect bands in Al_2O_3

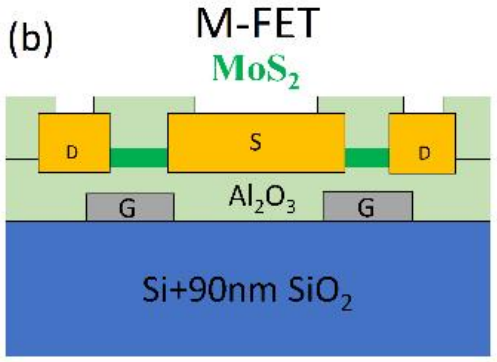
<u>Solution:</u>
Introduction of hBN monolayer at the interface.

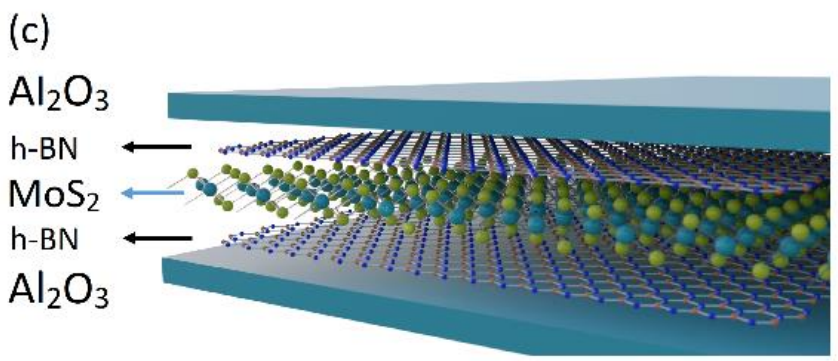


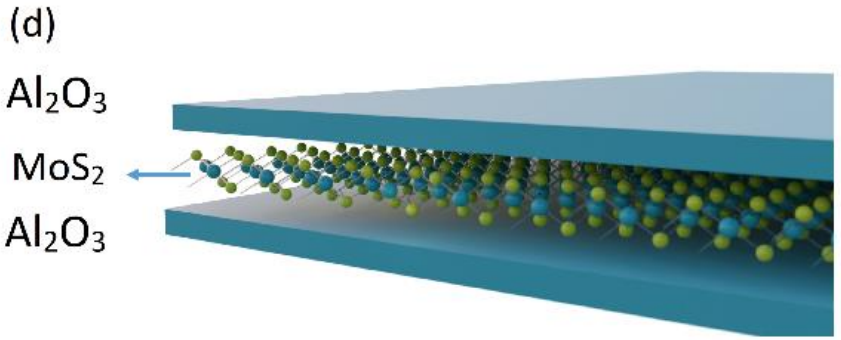
A. Piacentini et al. Advanced Electronic Materials (2022)

TMDC based NMOS FETs









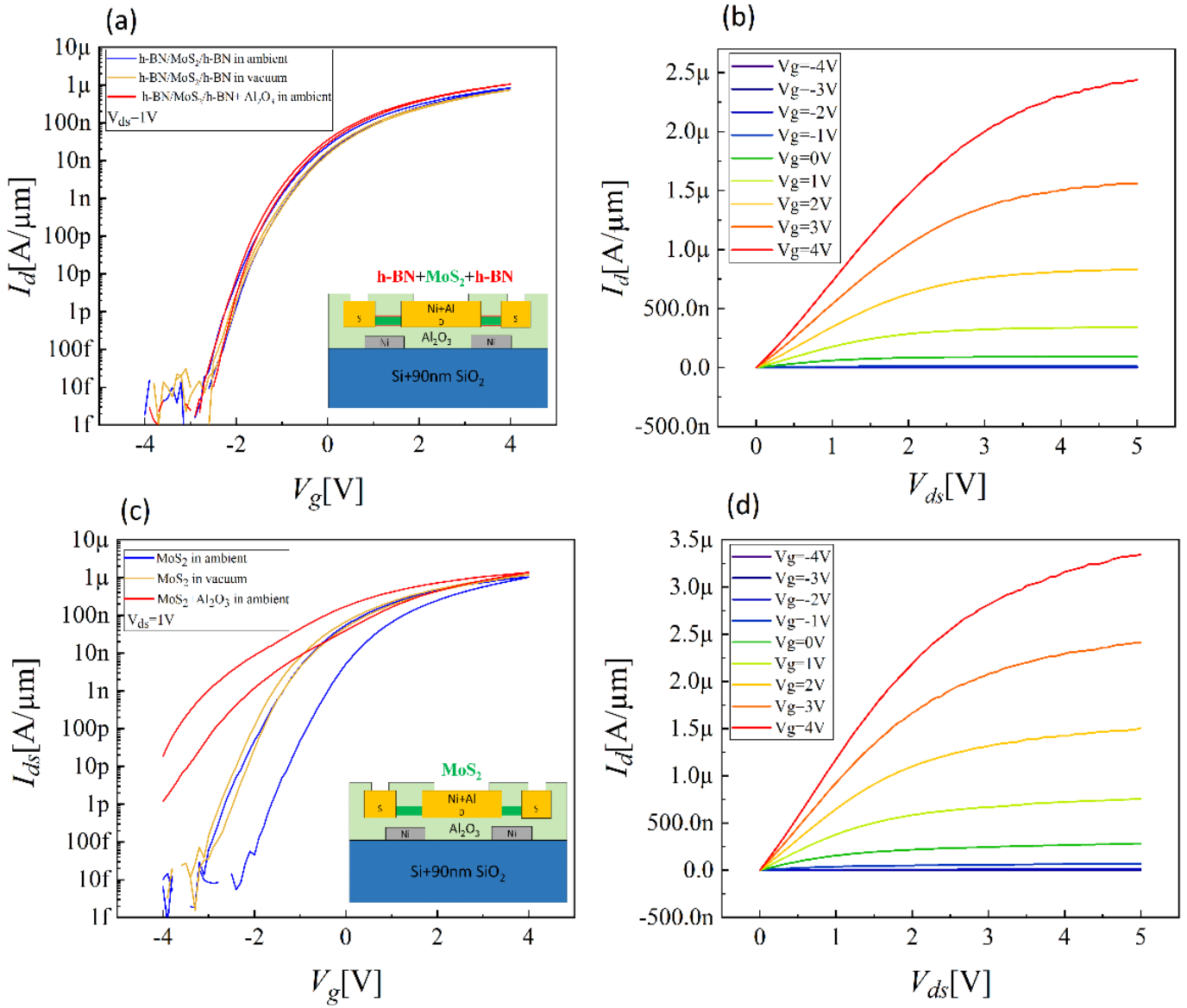
All 2D-Materials are (MO)-CVD grown

Layers stacked by subsequent wet-transfer: Not optimal (contaminations) but good enough.

Back gated FETs fabricated by optical lithography and standard processing

A. Piacentini et al. Advanced Electronic Materials (2022)

TMDC based NMOS FETs

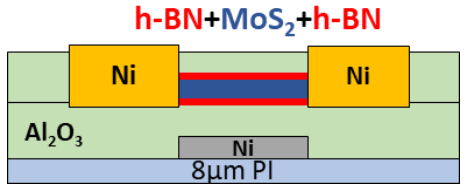


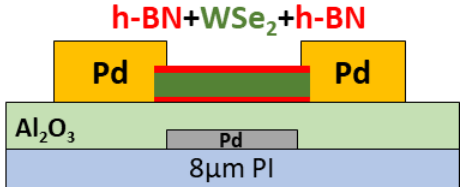
FETs with hBN show:

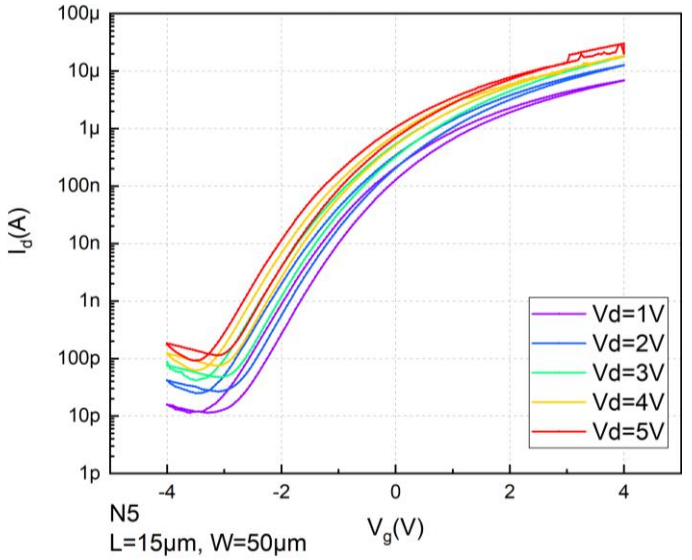
- No shift of threshold voltage after encapsulation with Al_2O_3.
- No difference between vacuum and ambient conditions.
- Little hysteresis.
- Lower subthreshold swing.

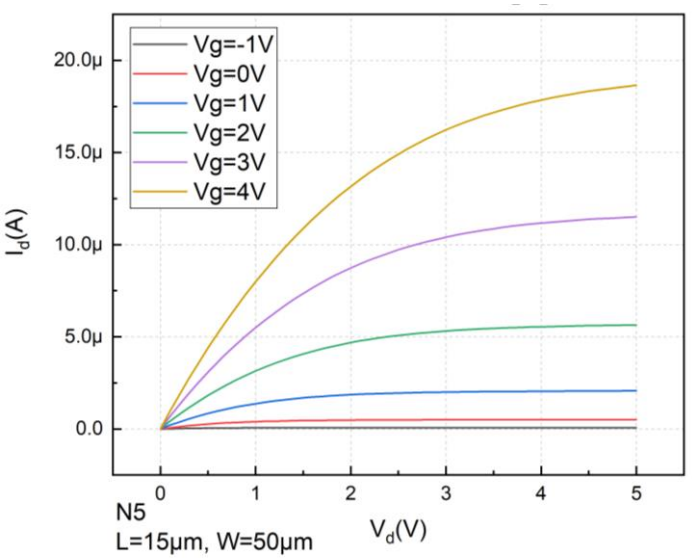
A. Piacentini et al. Advanced Electronic Materials (2022)

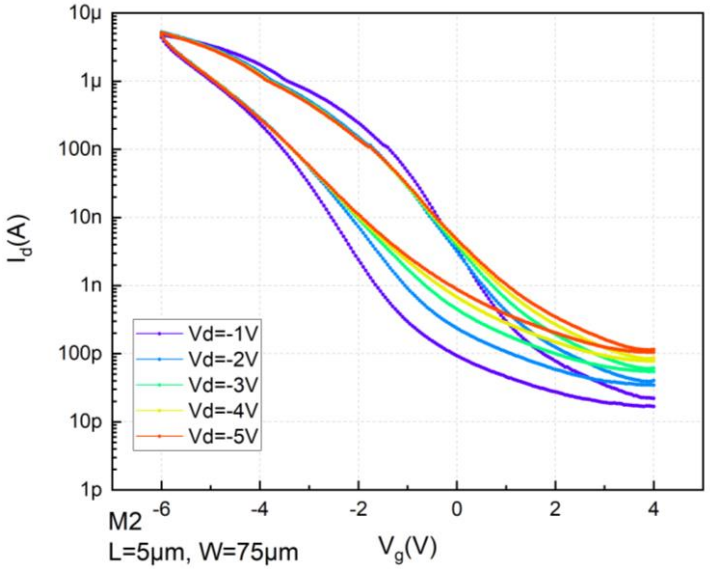
TMDC based PMOS FETs

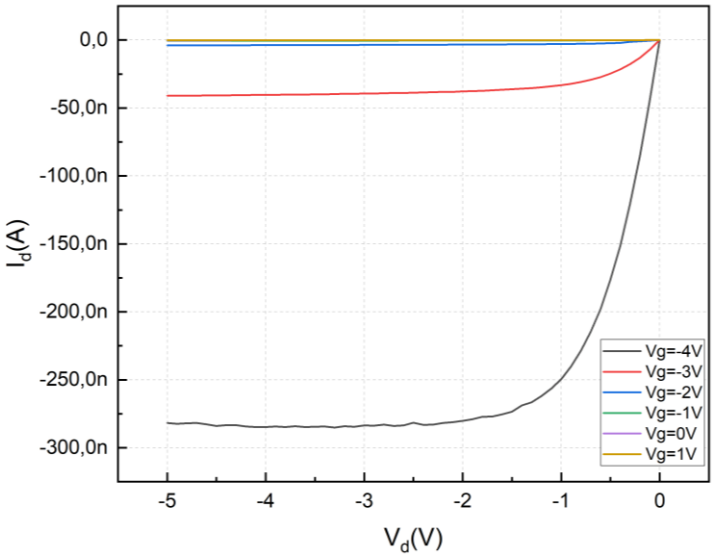






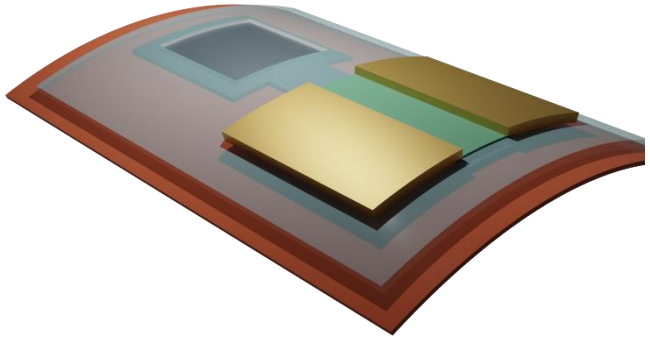


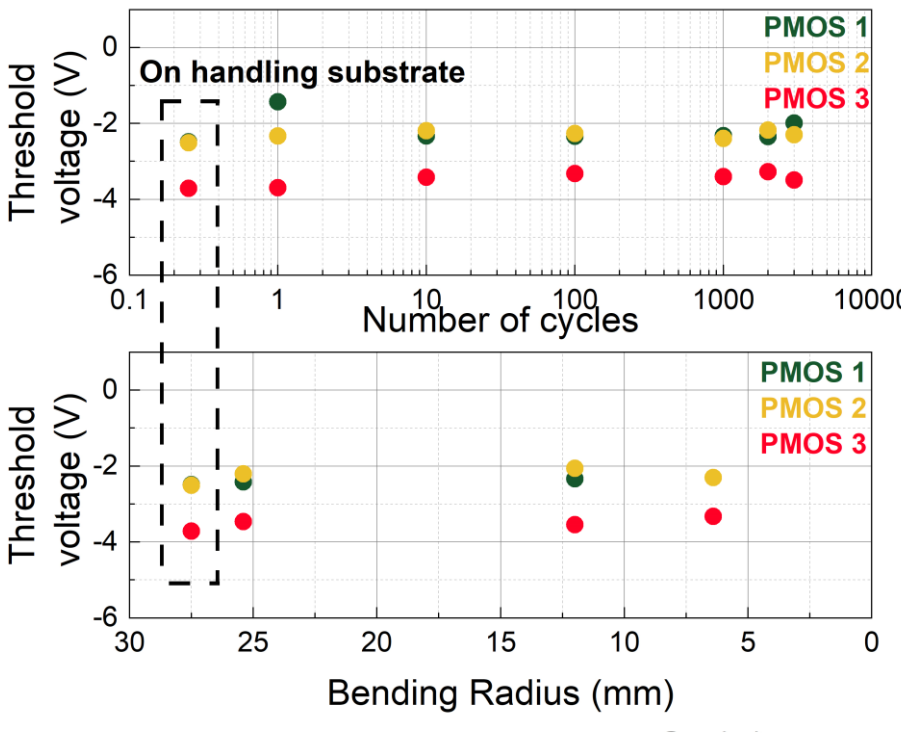


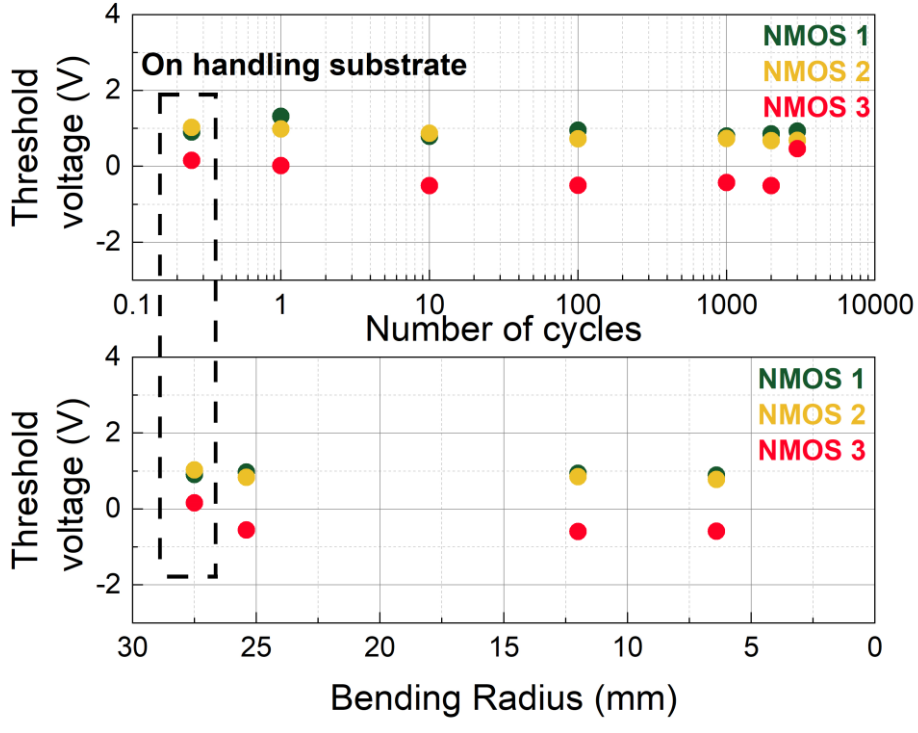


AMO/BUW (unpublished 2023)

Controllable strains were induced by placing the PI substrate on rigid cylinders of different radii







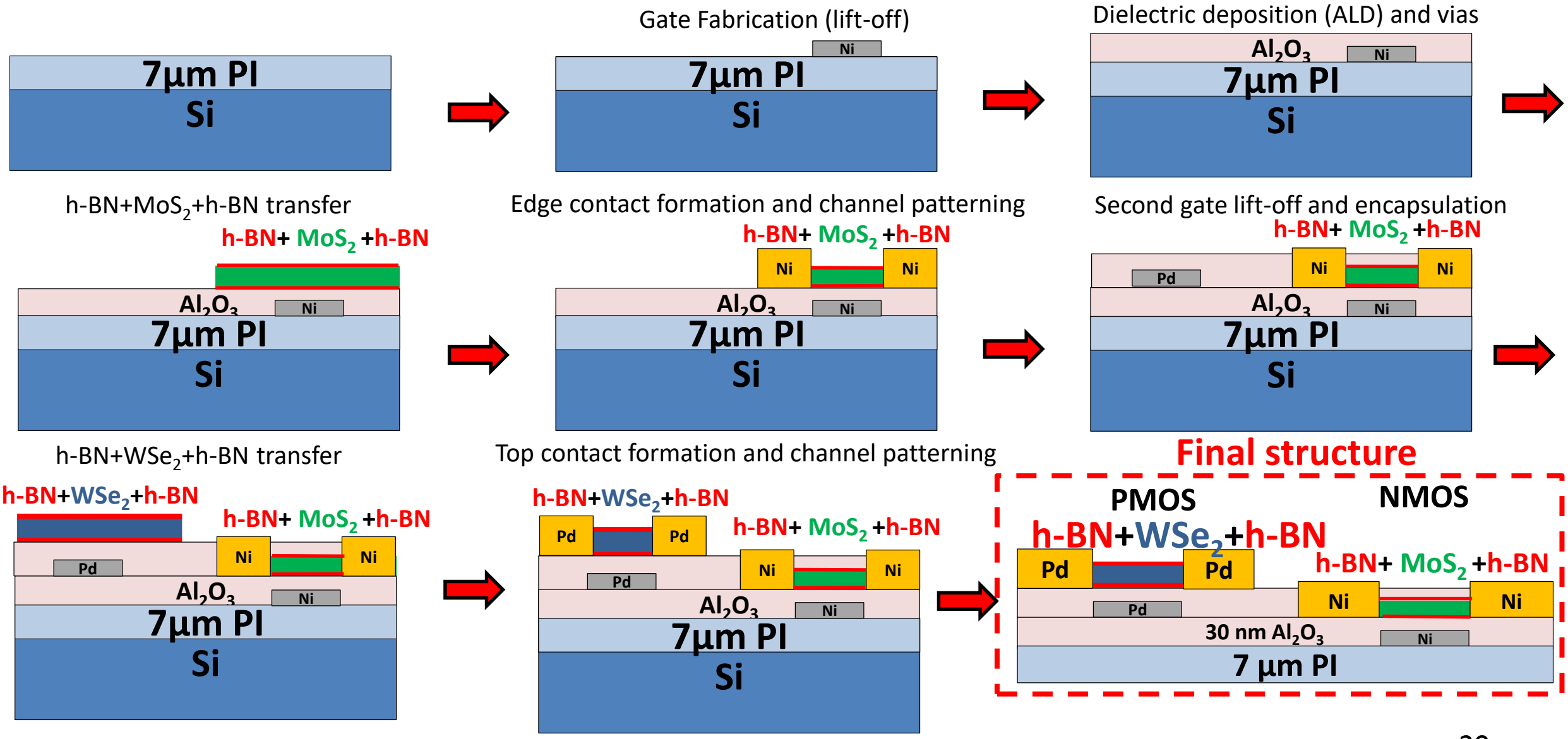
$$strain = \frac{2t}{r}$$

t= substrate thickness (~7 µm)

r= cylinder radius (25.4, 12.7, and 6.4 mm)

AMO/BUW (unpublished 2023)

TMDC based CMOS circuits



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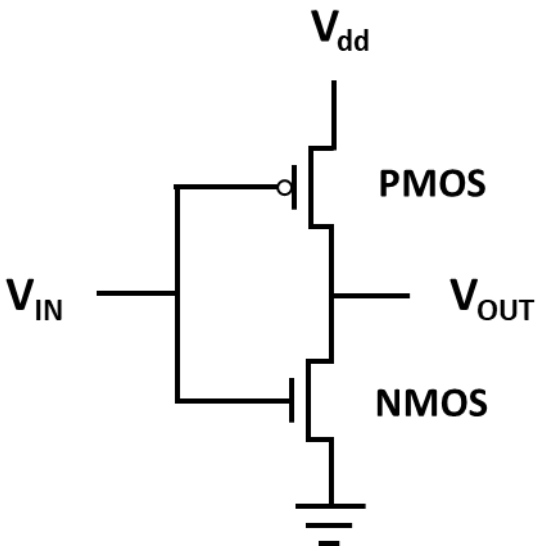
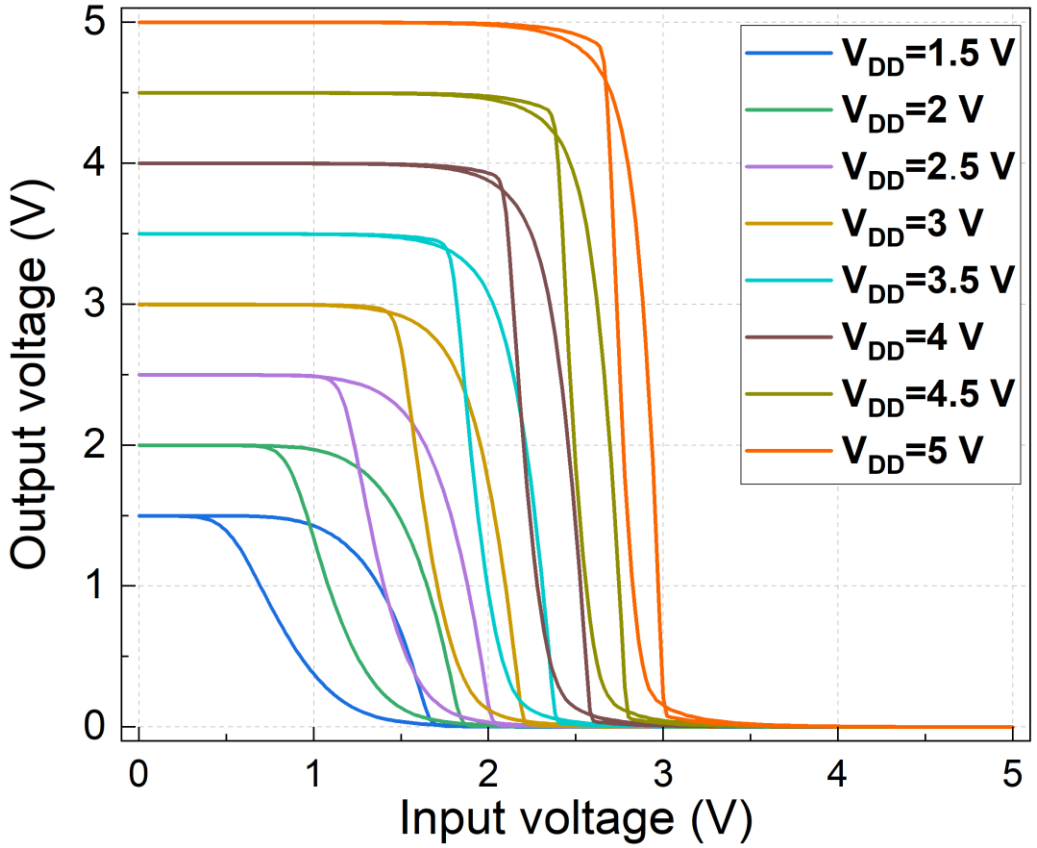


V_{IN}	V_{OUT}
1	0
0	1

1 = logic high
0 = logic low



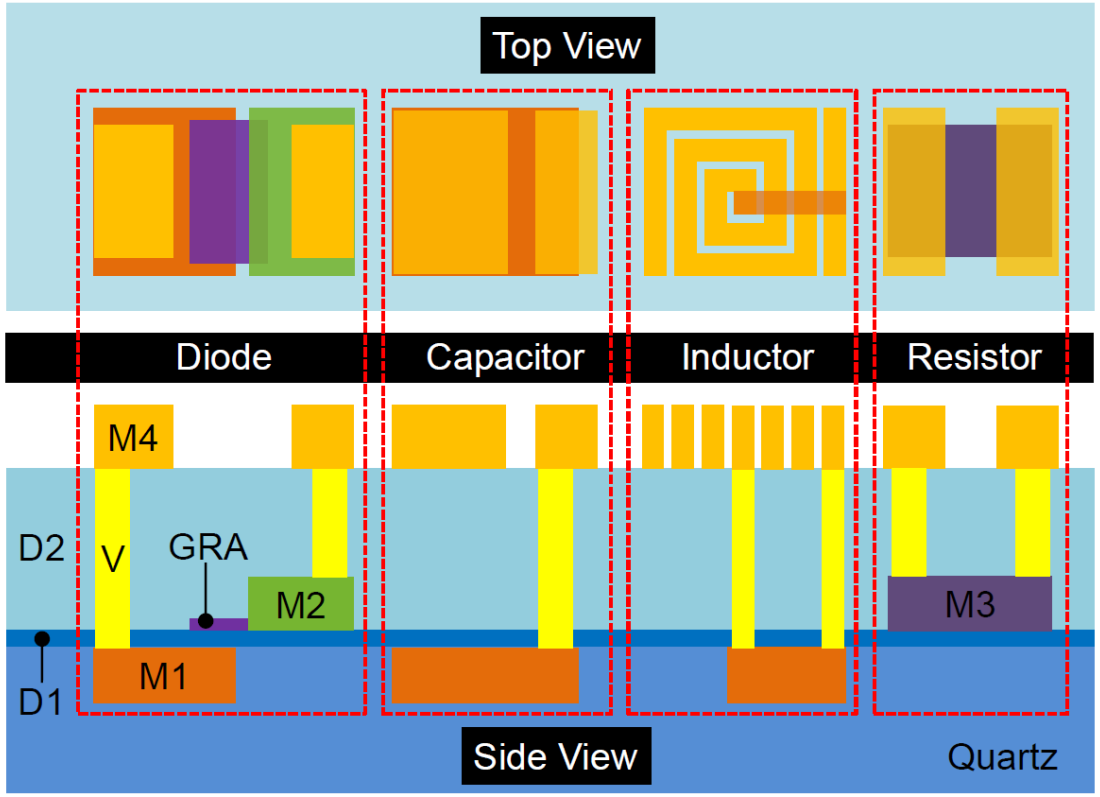
Almost perfect behaviour of the voltage transfer characteristic:
- High V_{OUT} (equal to V_{DD}) for low V_{IN},
- Low V_{OUT} (equal to 0 V) for high V_{IN}

AMO/BUW (unpublished 2023)

TMDC based flexible electronics

	Metal-Oxide	Organic	a-Si	Poly-Si	TMDC (CVD)	TMDC (Chemically Exfoliated)	CNTs (from solution)
Mobility ($cm^2V^{-1}s^{-1}$)	Up to 100	0.1-20	0.1-1	Up to 100	Up to 100	Up to 10	10-80
I_{On}/I_{Off}	High	High	High	Medium-High	High	Medium	Medium
CMOS operation	Poor PMOS	Poor NMOS	Poor PMOS	Yes	Yes	Yes	Medium NMOS
RF performance (max. operation frequency)	~10 GHz	~40 MHz	poor	~60 GHz	~10 GHz	~40 MHz	~10 GHz
Production efforts	Medium	Low	Medium	High	Medium	Medium-Low	Medium
Temperature (°C)	Low*	Low*	~300	~300	Low*	Low*	Low*

A. Piacentini et al. Advanced Electronic Materials (2023)



Graphene / MoS_2 is between D1 and M2, and can be used in diodes, varactors or/and transistors.

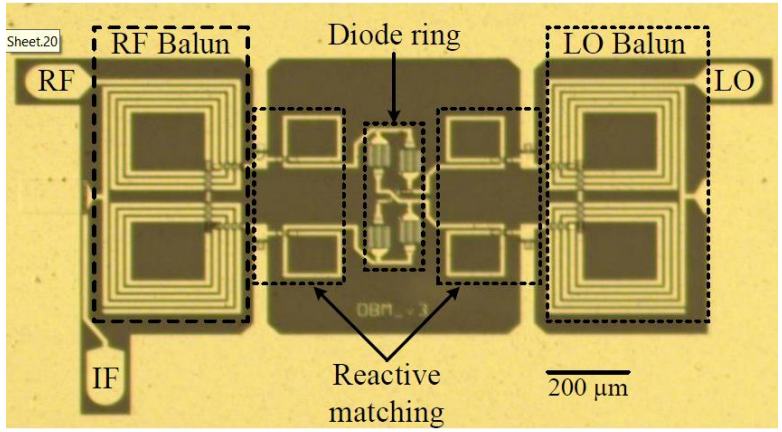
3 Dielectric layers:

- D1: 5 nm TiO2 (diodes) or 5-10 nm Al2O3 (FET)
- D2: 90nm Al203 (encapsulation, capacitors)
- D3 500 nm SU8 (inductors)

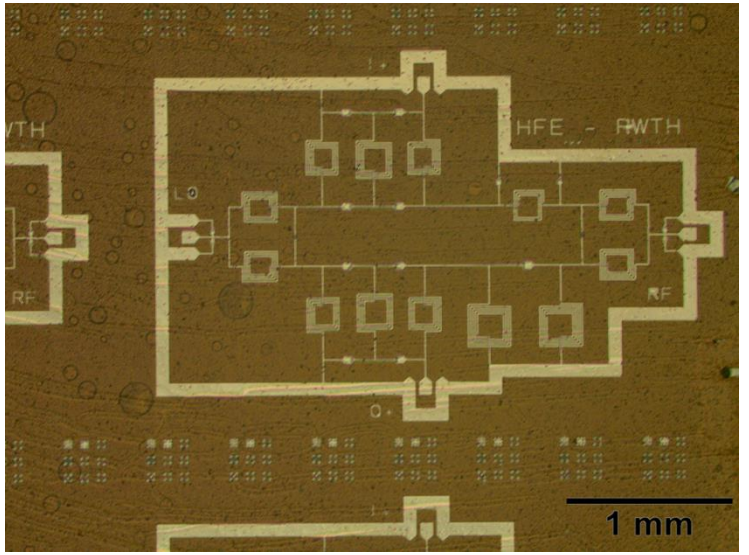
4 Metal layers:

- M1: 100nm Al (gate electrode, passives)
- M2: 20 nm Nickel (graphene contacts)
- M3: 30 nm NiCr (resistors)
- M4: 2 µm Al (passives, interconnects)

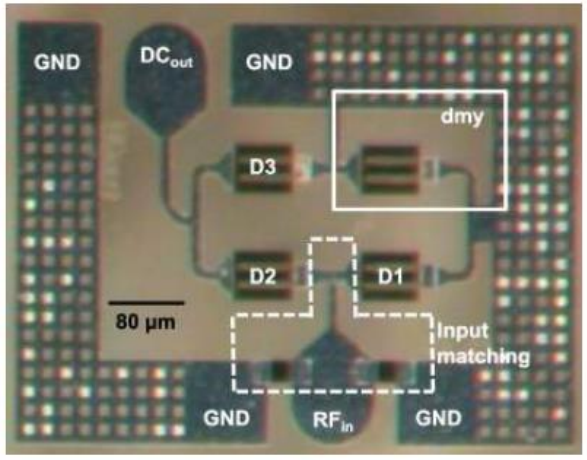
Up-conversion mixer 10 GHz

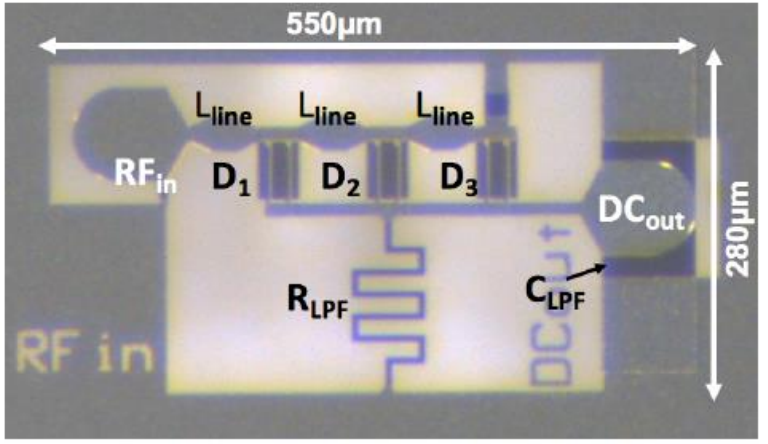


QAM receiver on foil (2.4 GHz)

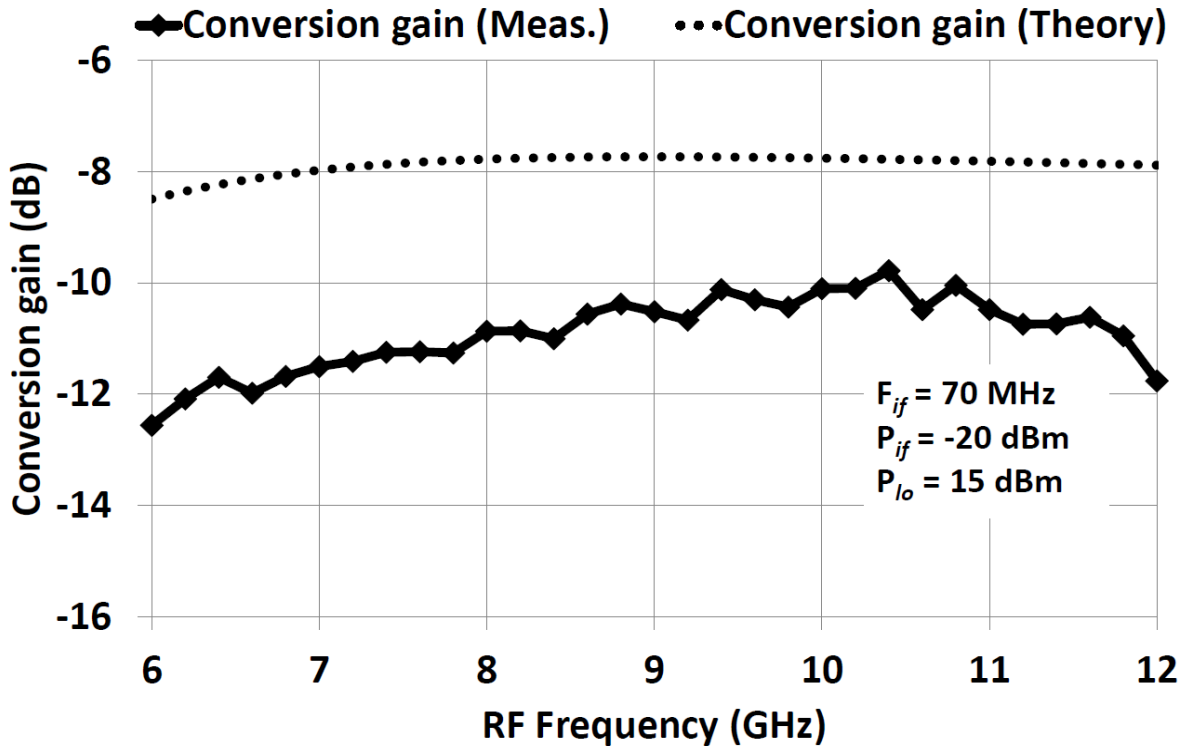


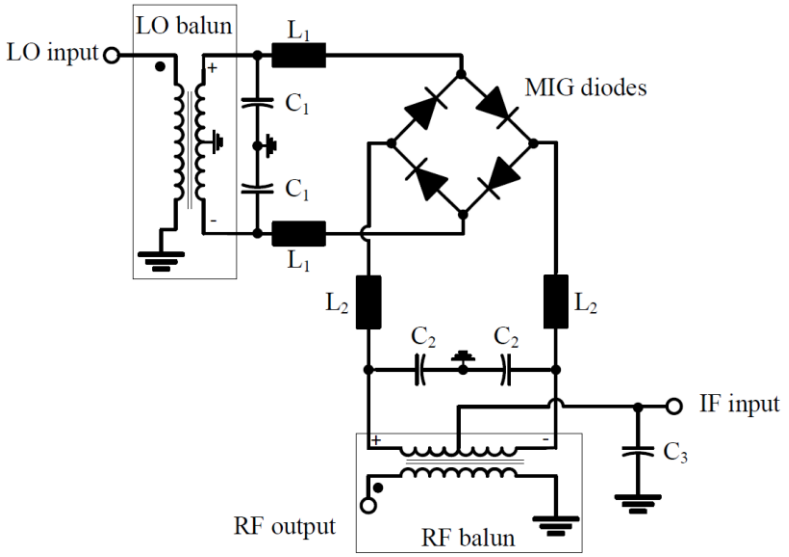
Power detector (60 GHz)

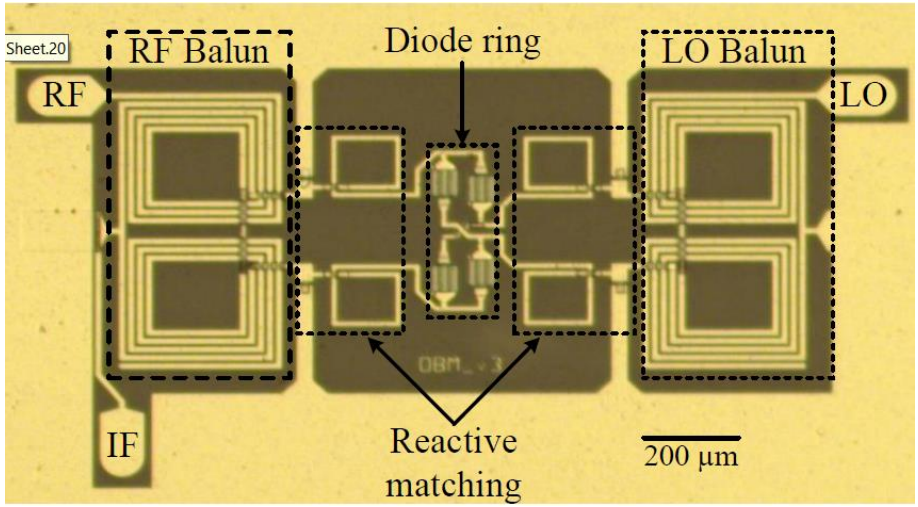




- Fully integrated mixer for 6-12 GHz
- Ring mixer core: 4x MIG diodes,
- MMIC process: Reactive matching, LO & RF balun







A. Hamed, et al., "6–12 GHz MMIC Double-Balanced Upconversion Mixer based on Graphene Diode," IMS 2018, pp. 674–677. DOI: 10.1109/MWSYM.2018.8439211

- Fully integrated mixer
- Ring mixer core: 4x MIG diodes
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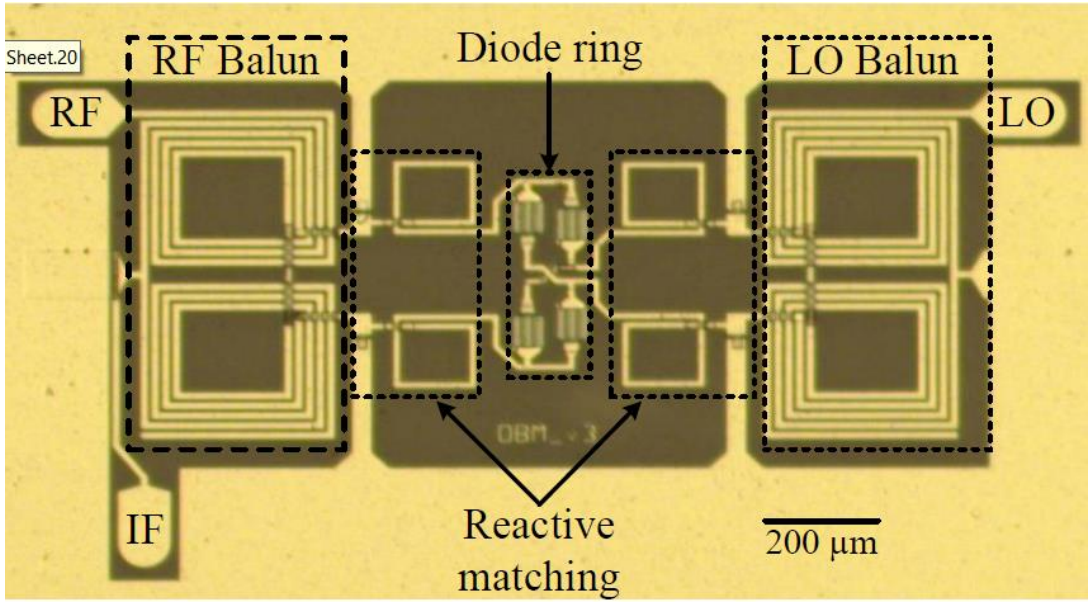
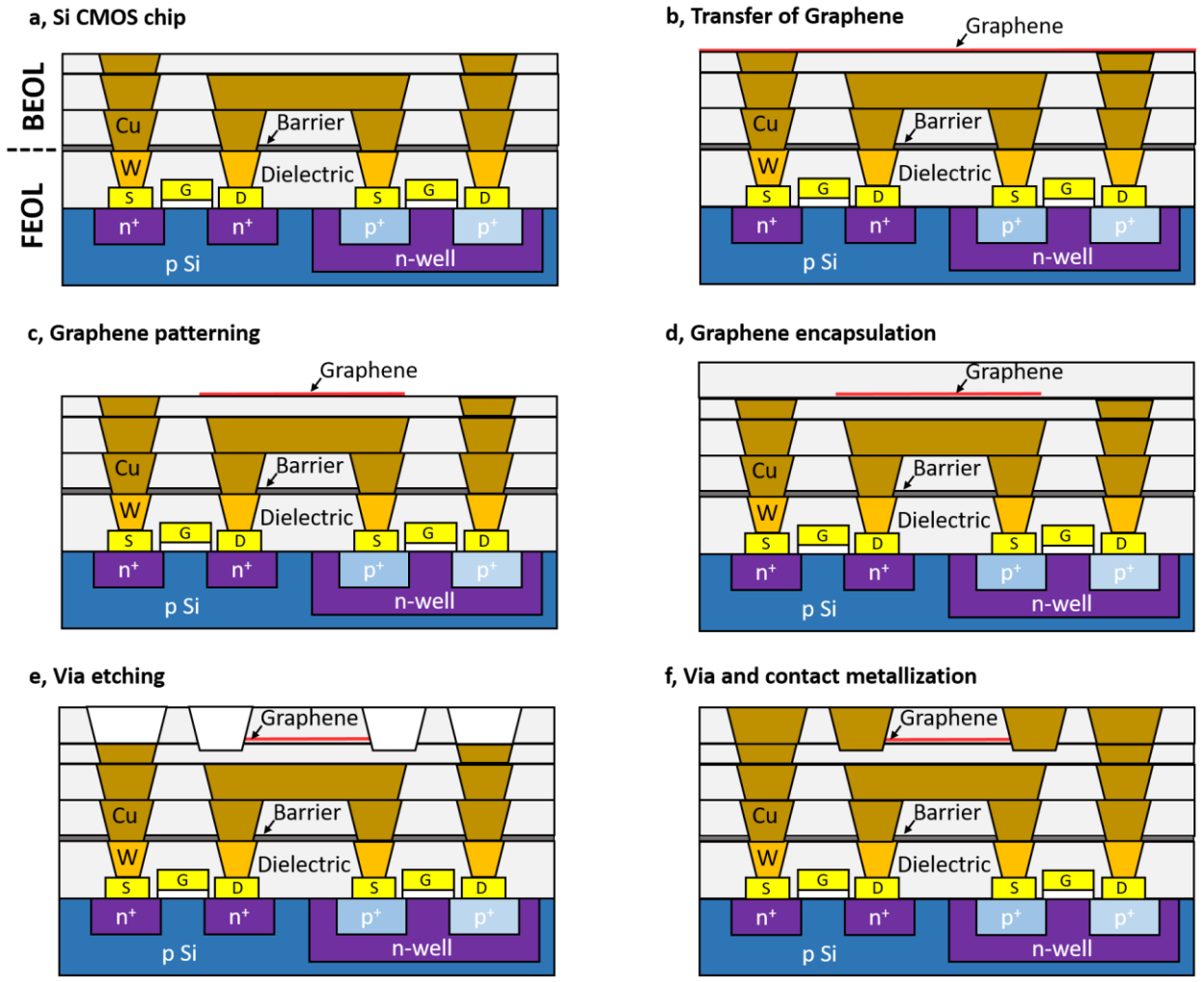


Ref.	Substrate	Device	Scheme	RF frequency	Conversion gain	LO power
[2]	Silicon-CMOS	GFET	Double-balanced, partially integrated, resistive mixer	3.5 GHz	-33 dB	8.9 dBm
[3]	Silicon	GFET	Single-device, hybrid, resistive mixer	4 GHz	-45 dB	15 dBm
[4]	SiC	GFET	Single-device, integrated, resistive mixer	88-100 GHz	-18 dB	8 dBm
[8]	GaAs	Schottky diode	Double-balanced, fully integrated, diode mixer	5-12 GHz	-9 dB	10 dBm
This work	**Glass**	**Graphene-diode**	**Double-balanced, fully integrated, diode mixer**	**6-12 GHz**	**-10 dB**	**15 dBm**

A. Hamed, et al., "6–12 GHz MMIC Double-Balanced Upconversion Mixer based on Graphene Diode," IMS 2018, pp. 674–677. DOI: 10.1109/MWSYM.2018.8439211

Possible integration scheme (e.g. on CMOS)



D. Neumaier et al. Nature Materials 2019

Required process steps

1. Growth on a separate substrate
2. Prepare target substrate
3. Transfer to target substrate
4. Encapsulation
5. Pattering
6. Contact metallization

Decisive Steps

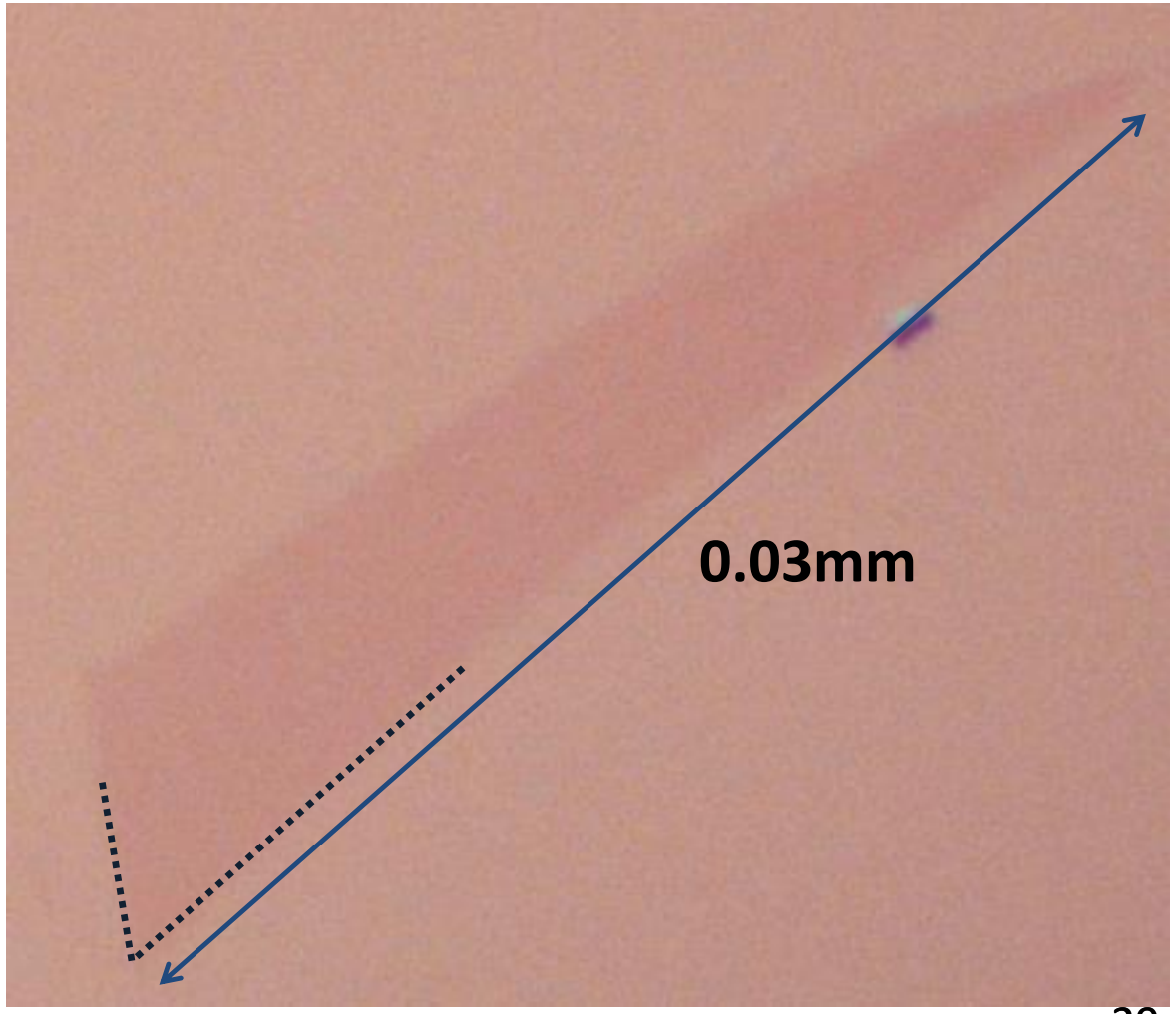
Graphene device production

Photo: Sergeom, Wikimedia Commons

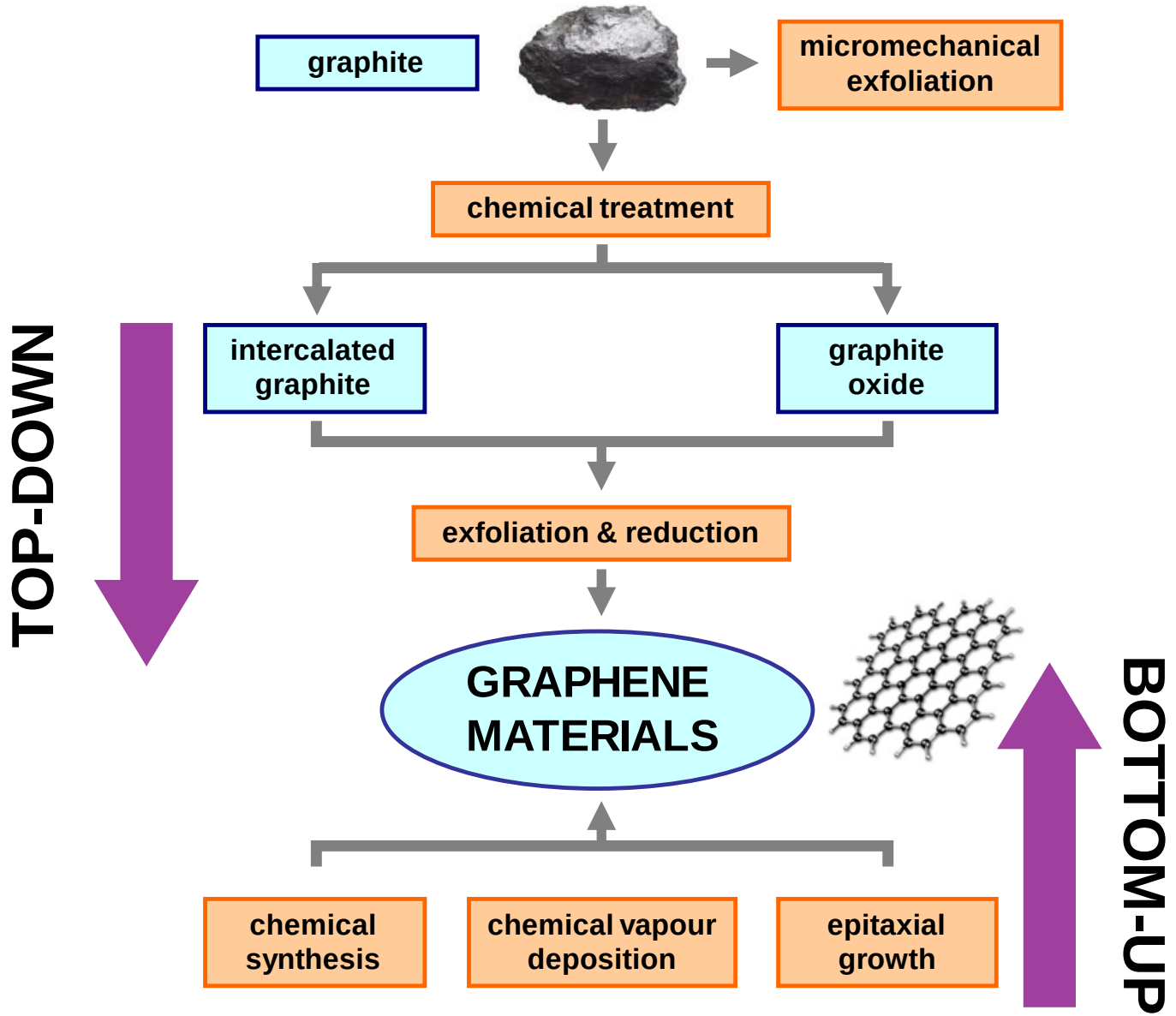
Andre Geim

Photo: University of Manchester, UK

Konstantin Novoselov



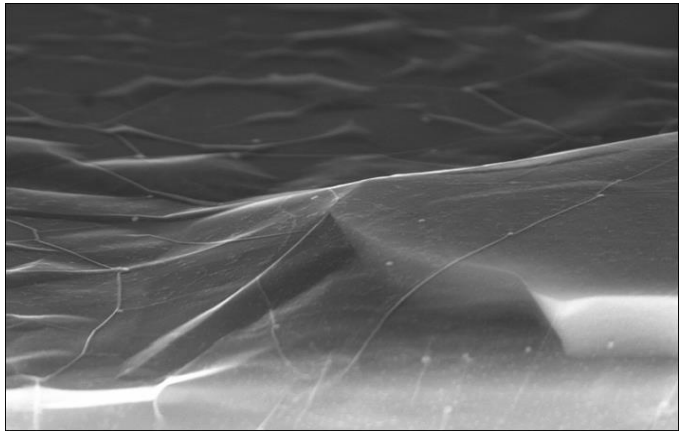
Graphene device production



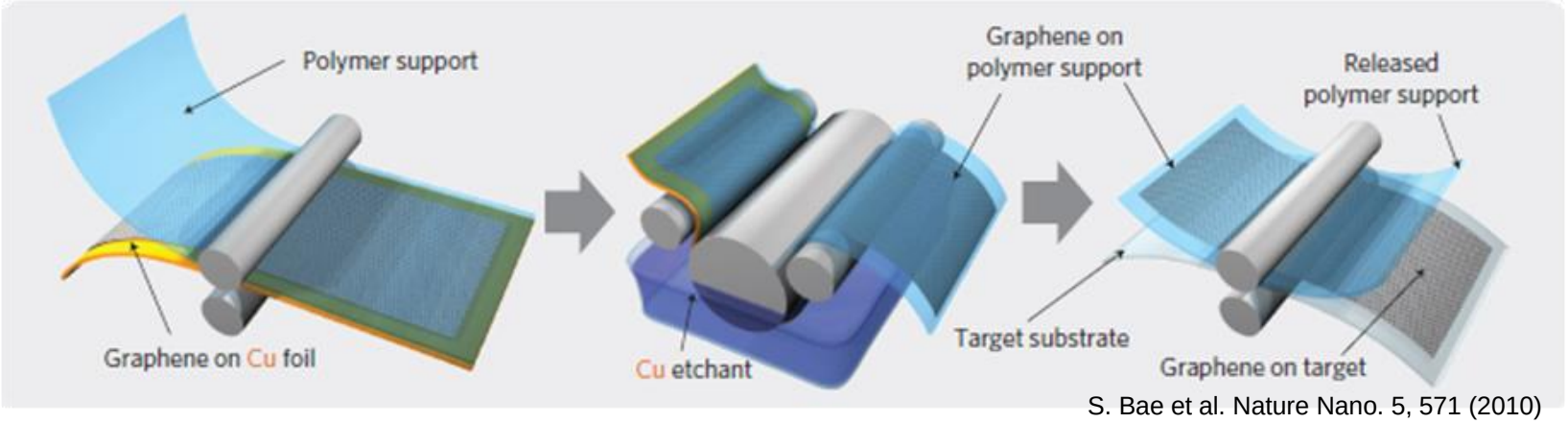
Monolayer Graphene by CVD on copper surface

On Wafers

Courtesy of Aixtron



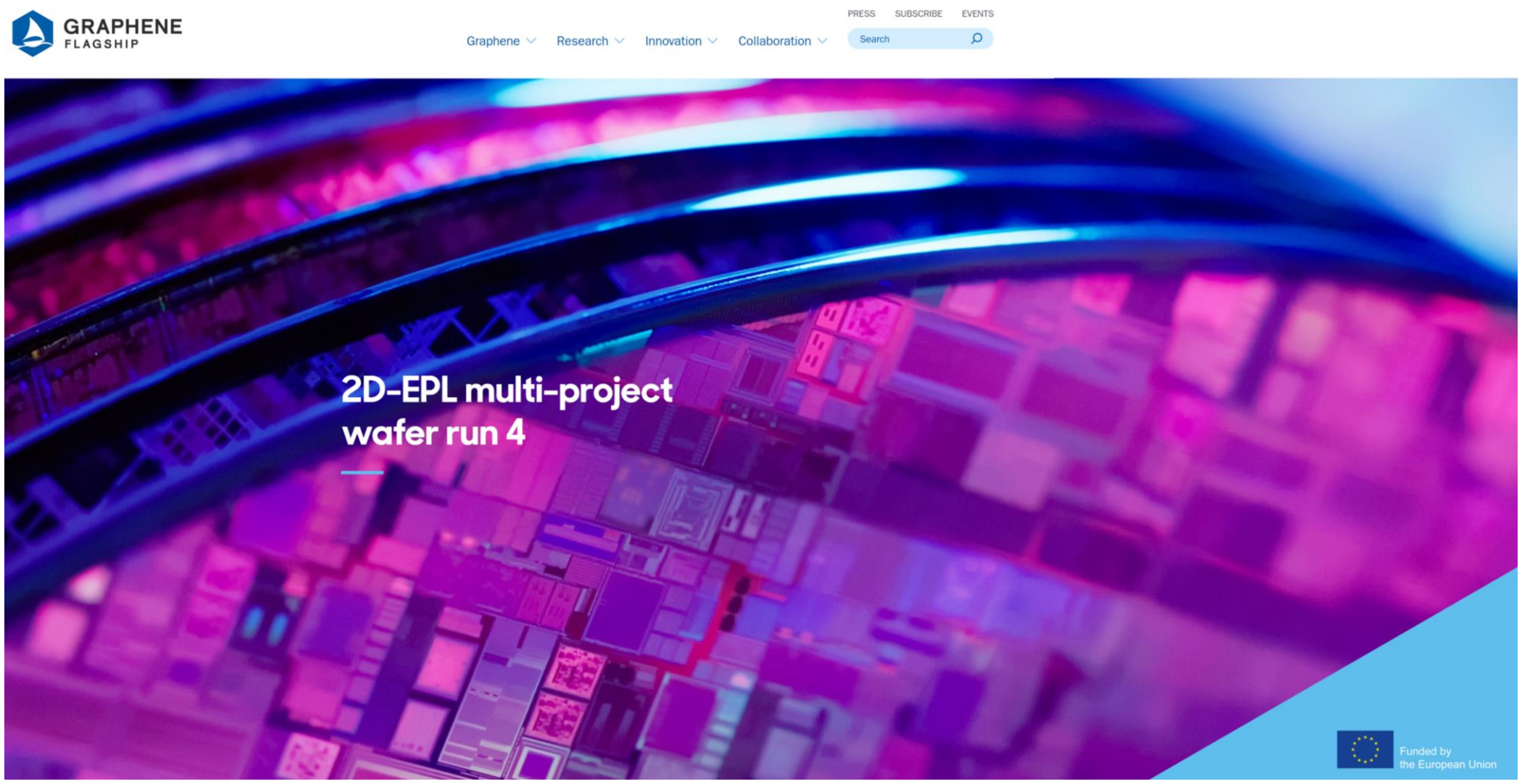
On Foil using Roll-To-Roll Process



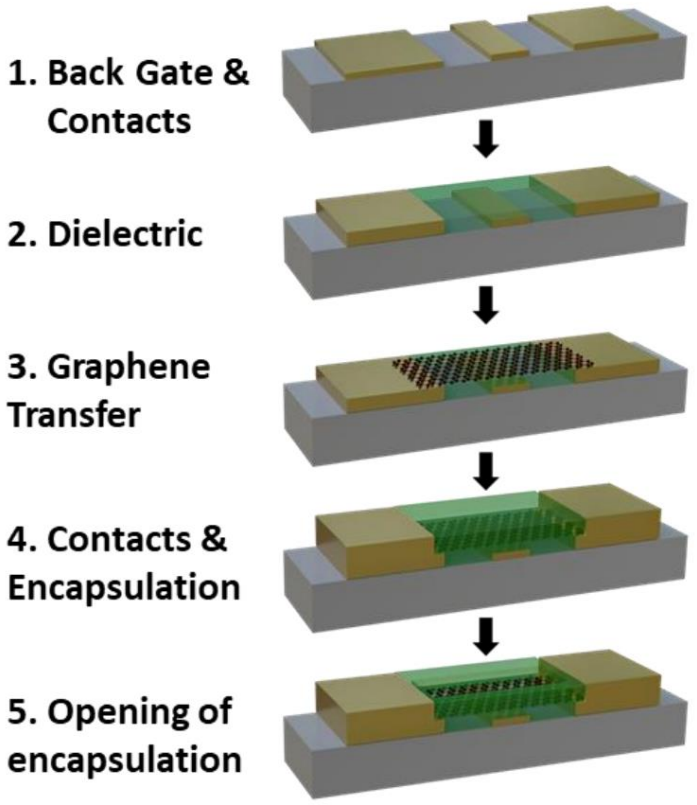
S. Bae et al. Nature Nano. 5, 571 (2010)

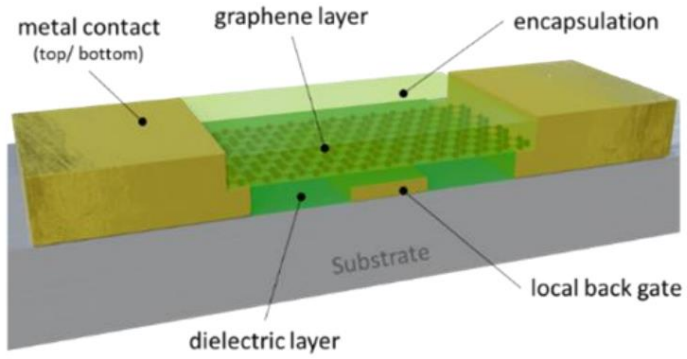
Transferable to nearly any surface!

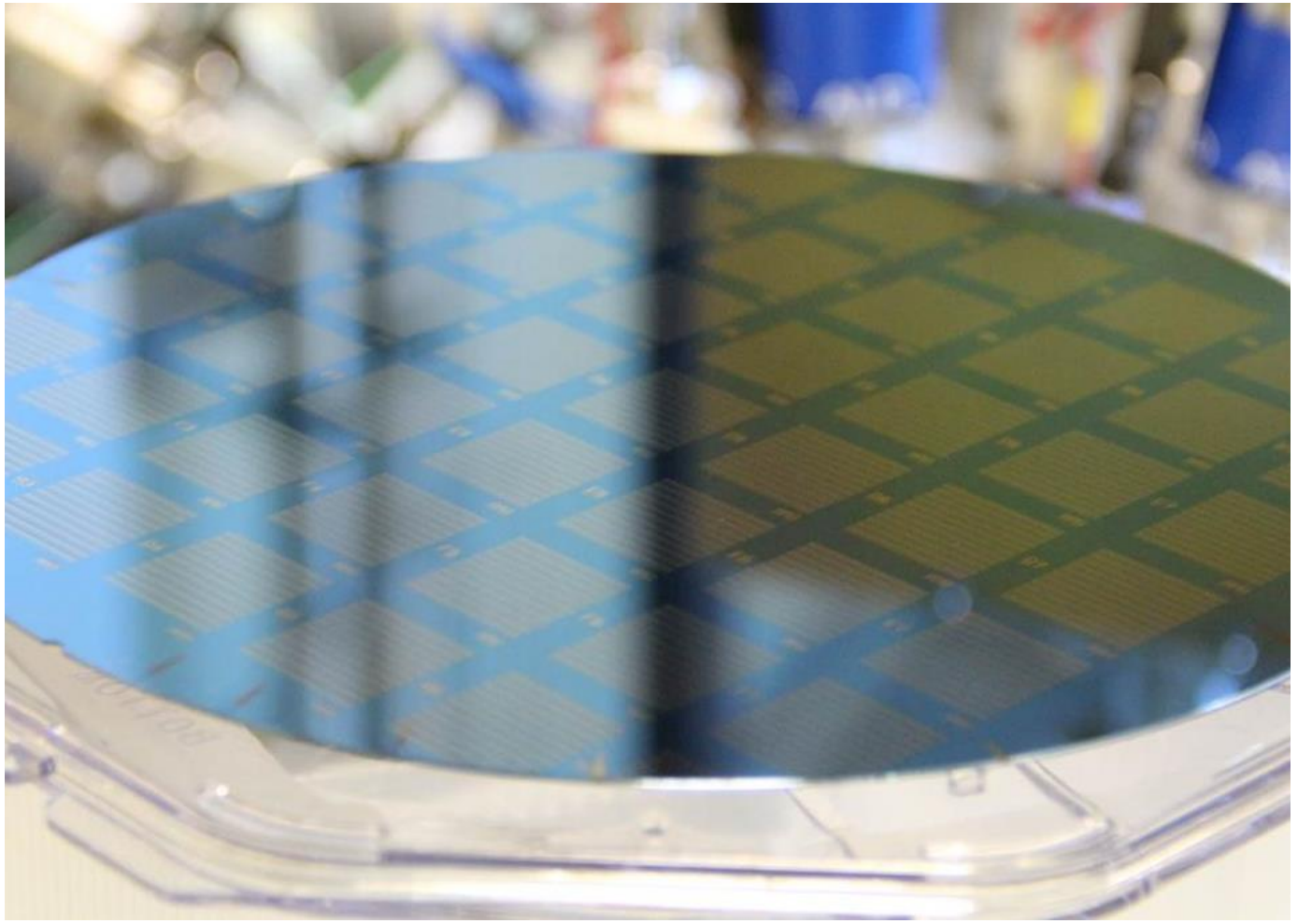
Graphene device production



Graphene device production







200 mm wafer

TMDC:

- Excellent material for ultra-scaled logic devices; but there are many challenges left.
- Also an ideal materials for flexible circuits; but there are many competitors out.

Graphene:

- Most production ready 2D material.
- Possible applications are sensors and flexible RF electronics.

Production:

- Key process steps are already at sufficient scale (8 inch)
- Pilot Line Process available through MPW runs

Thanks to…

Team members (AMO, BUW)

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Frank Koppens, ICFO
Andrei Vorobiev, Chalmers
Gianluca Fiori, Uni Pisa
Sanna Arpiainen, VTT
Thomas Müller, TU Wien

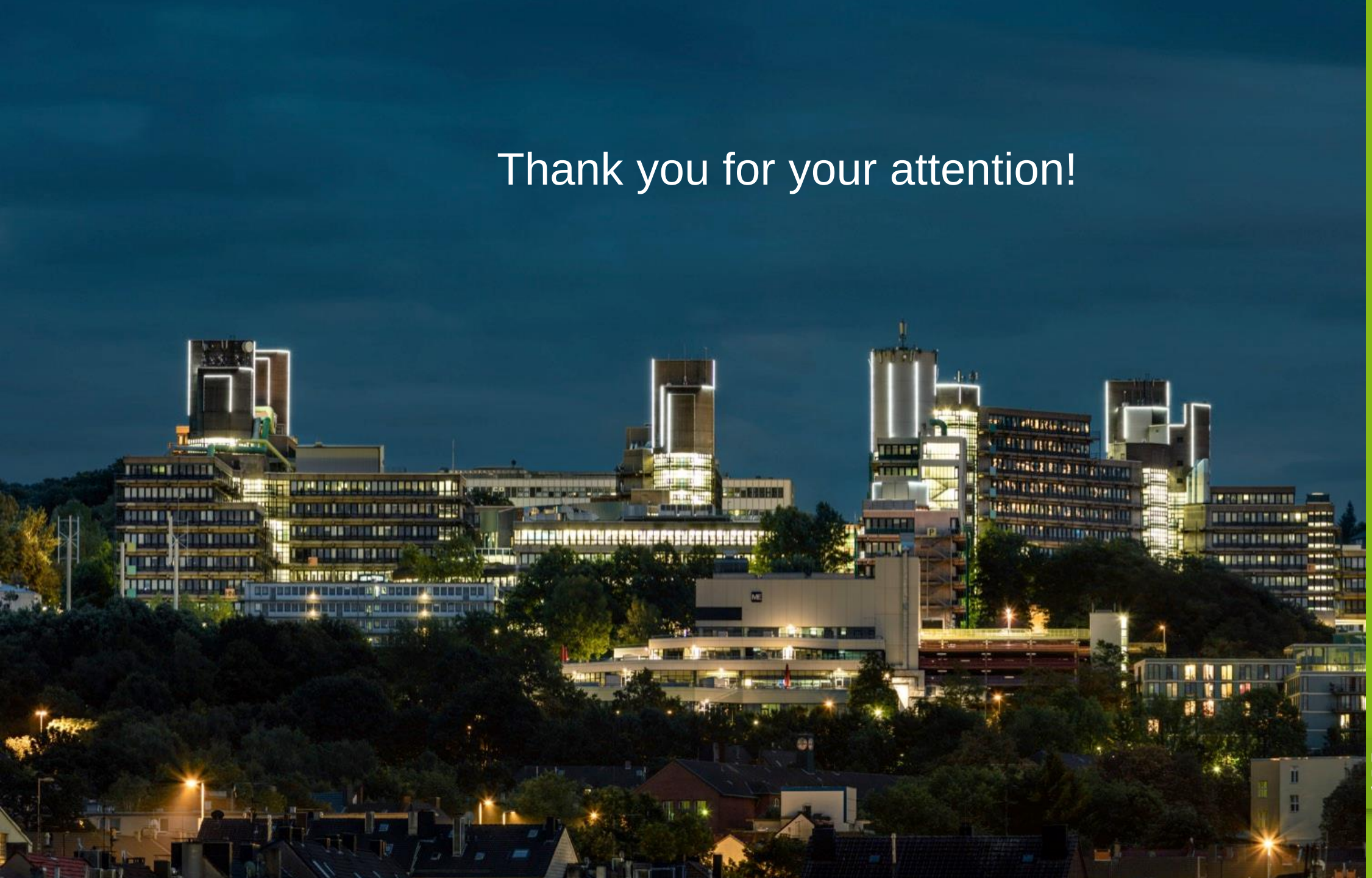
Aachen Graphene & 2D Materials Center

HORIZON 2020

Deutsche Forschungsgemeinschaft DFG

GRAPHENE FLAGSHIP

Thank you for your attention!



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