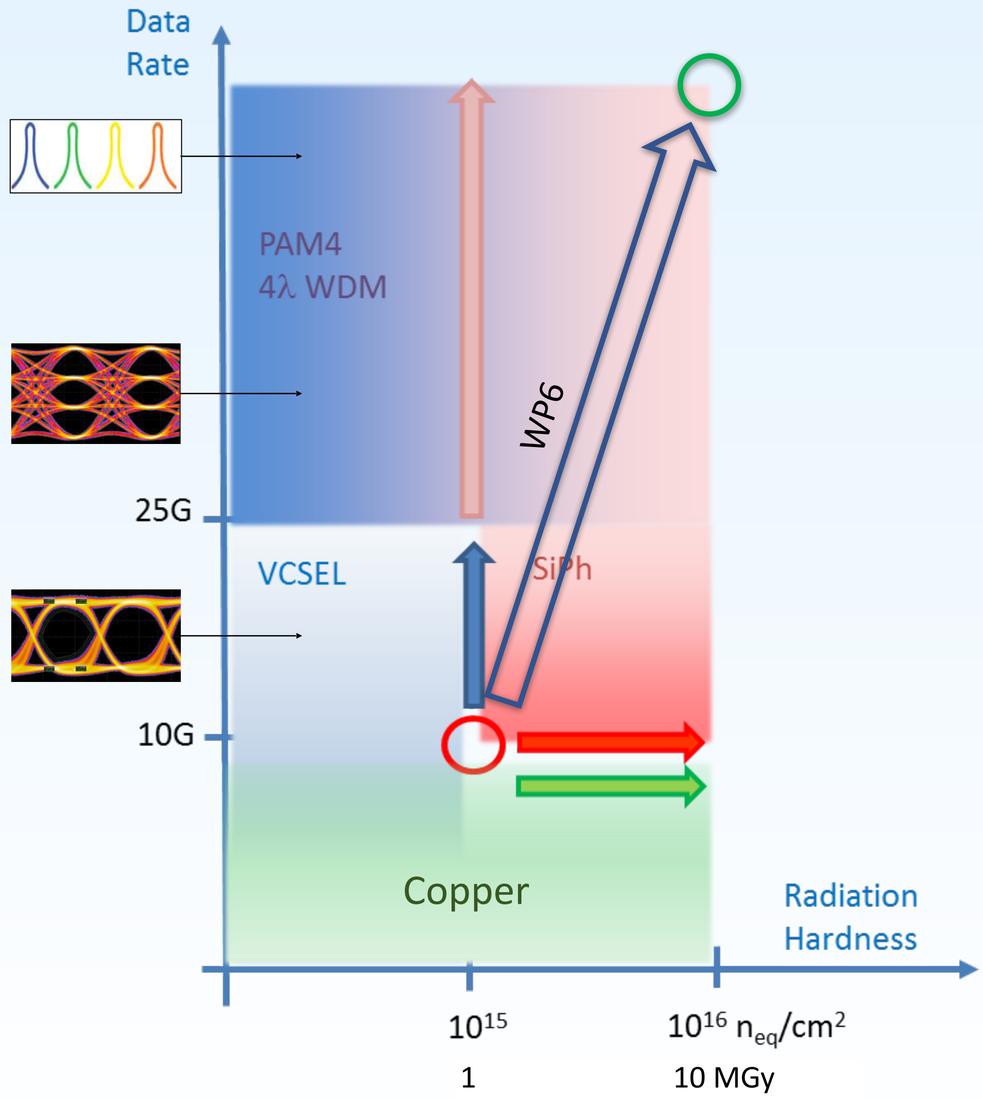
WP6 High Speed Links

- High Speed Link Project Goals recap
- Current Status
- Plans for 5-yr extension to EP R&D Programme

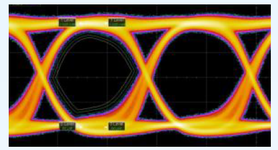
WP6 Goals

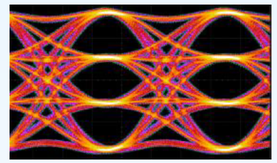
- Provide the future HEP systems with:
  - High bandwidths: ~25 Gbps / lane
  - High radiation tolerance *c.f. ECFA roadmap*
  - Low power, low mass
- FPGAs
  - Compatible with the state-of-the-art
- ASICS
  - Advanced technologies 28nm CMOS
  - High order modulation formats (PAM4)
  - Drivers for SiPh optoelectronics
- Optoelectronics
  - Silicon Photonics (SiPh)
  - External Modulators
    - Ring & MZ
- Wavelength Division Multiplexing (WDM)



New Technologies

- More advanced CMOS ASIC processes
  - Aligned with WP 5 – move to 28 nm CMOS
- Evolution of supported line rates in latest and future Optical Networking protocols, as supported by FPGAs
  - Two-level On-Off keying (NRZ) data rates up to 56 Gb/s
  - Four-Level Pulse Amplitude Modulation (PAM4) up to 112 or even 256 Gb/s

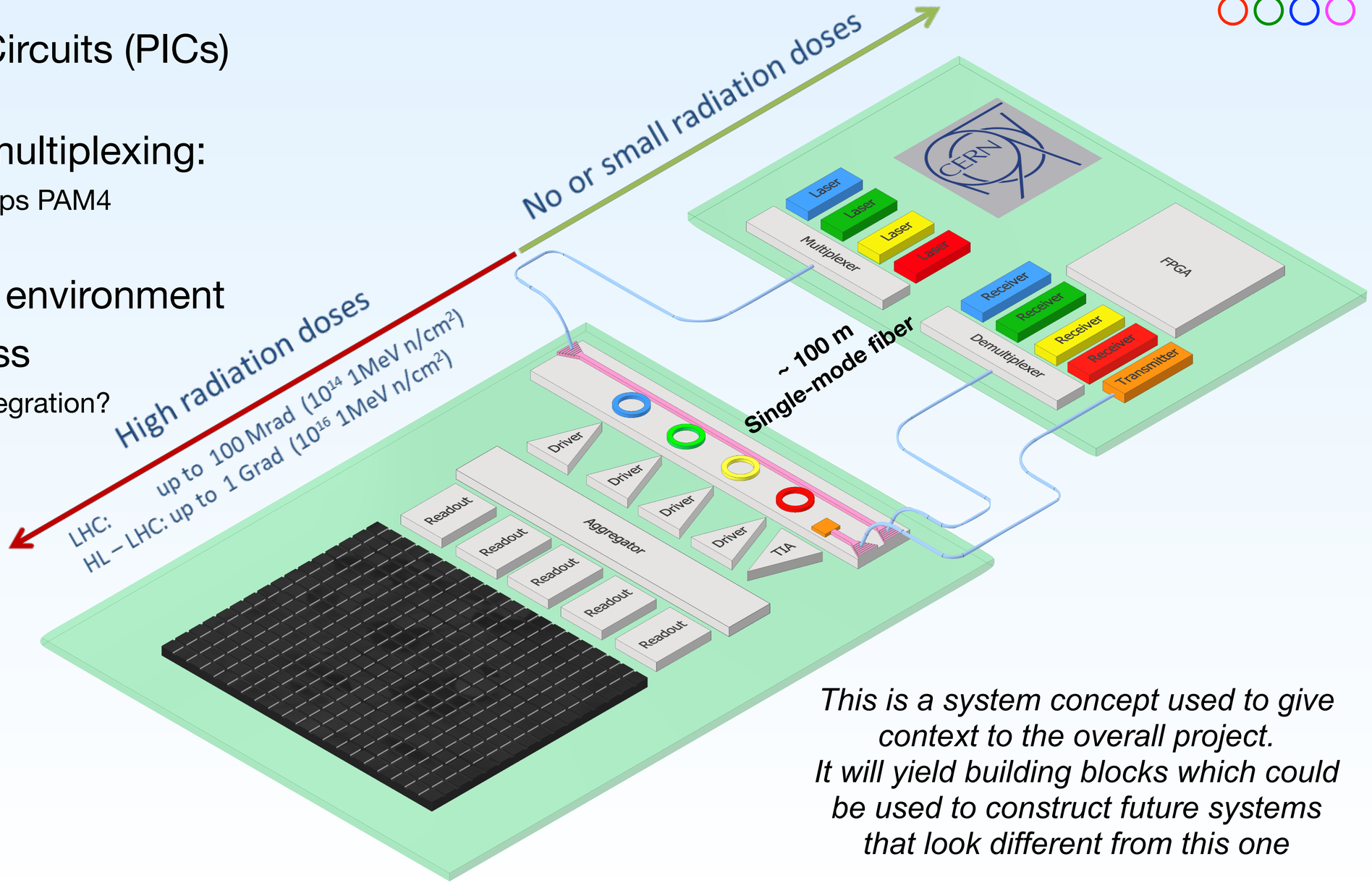




- Wavelength-Division Multiplexing (WDM)
  - using several wavelengths to send “parallel” data-streams down the same physical optical fibre
  - Most promising standard uses 4 distinct wavelengths
- Silicon Photonics
  - Using standard CMOS ASIC production techniques to build structures that manipulate light in optical waveguides on a silicon substrate
    - First-time in HEP that we can “design” our own optical link components!

Future HEP Link Architecture

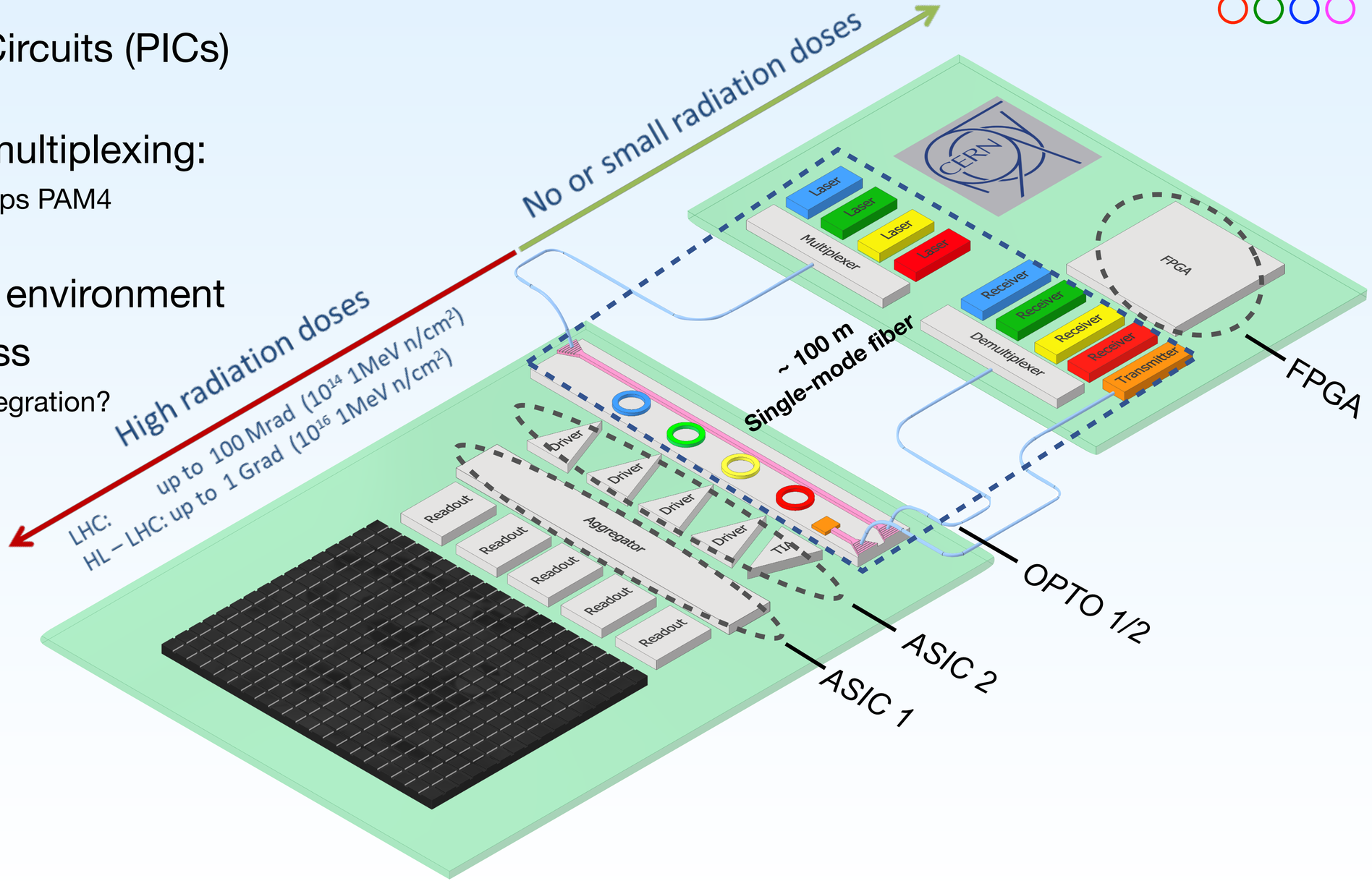
- Photonic Integrated Circuits (PICs)
  - RadHard “promise”
- Wavelength division multiplexing:
  - Lane: 25 Gbps NRZ / 50 Gbps PAM4
  - Fibre: 100 Gbps / 200 Gbps
- Laser out of radiation environment
- Low power / Low mass
  - How far can we push FE integration?



This is a system concept used to give context to the overall project.
It will yield building blocks which could be used to construct future systems that look different from this one

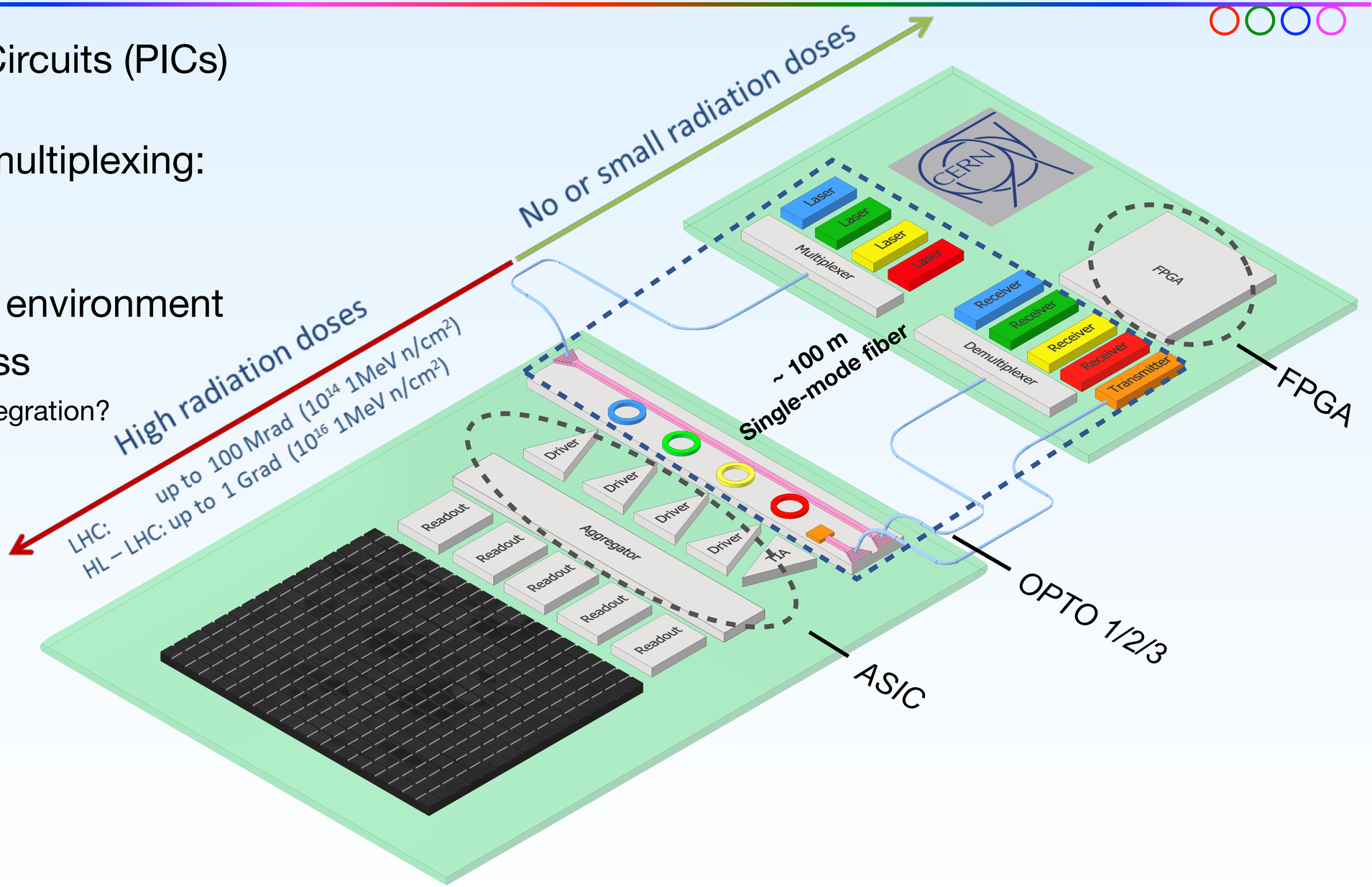
WP6 Project breakdown

- Photonic Integrated Circuits (PICs)
  - RadHard “promise”
- Wavelength division multiplexing:
  - Lane: 25 Gbps NRZ / 50 Gbps PAM4
  - Fibre: 100 Gbps / 200 Gbps
- Laser out of radiation environment
- Low power / Low mass
  - How far can we push FE integration?



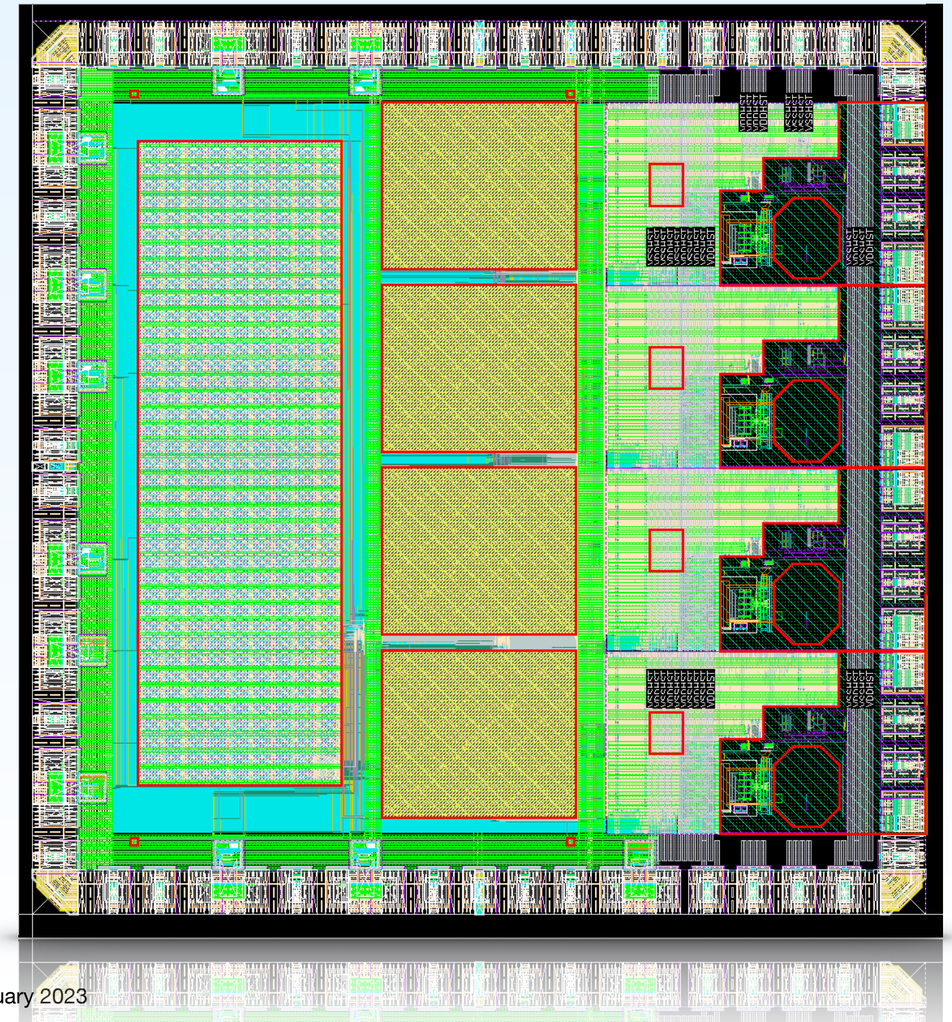
WP6 Project updated breakdown

- Photonic Integrated Circuits (PICs)
  - RadHard “promise”
- Wavelength division multiplexing:
  - Lane: 25 Gbps NRZ
  - Fibre: 100 Gbps
- Laser out of radiation environment
- Low power / Low mass
  - How far can we push FE integration?



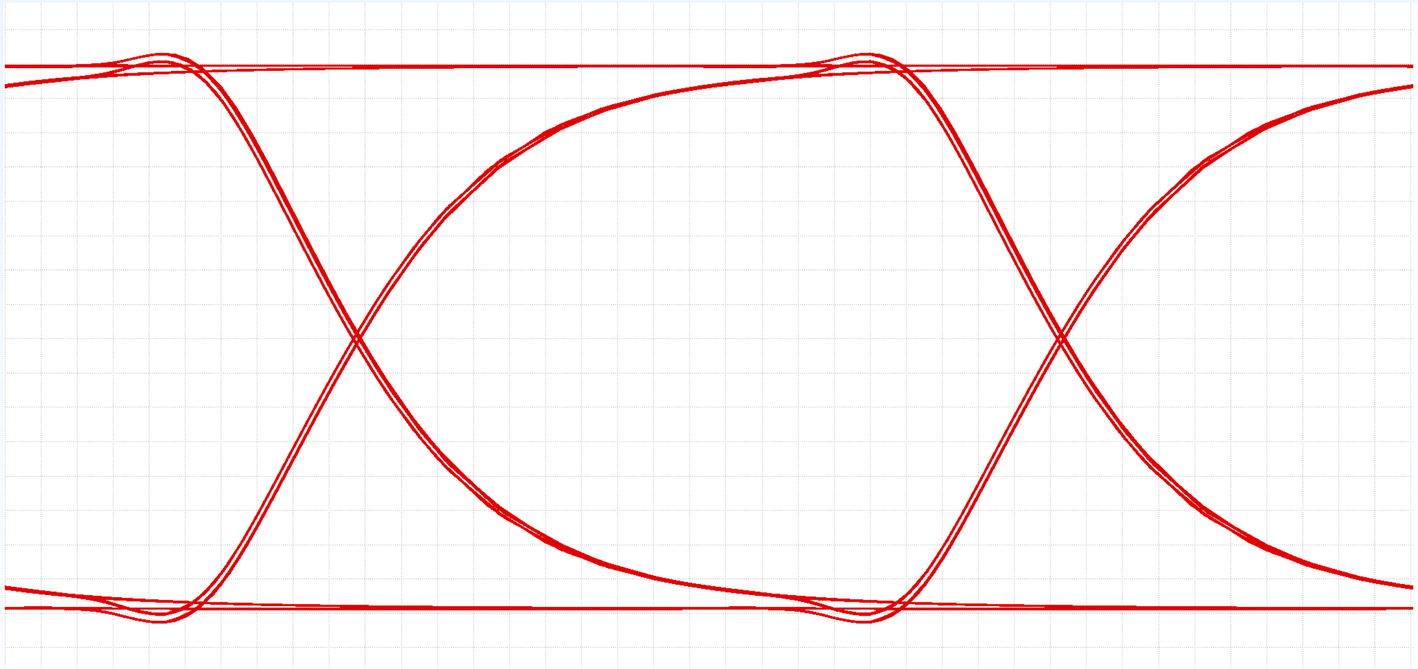
Status: ASIC – DART28NRZ

- DART28NRZ
  - **D**emonstrator **A**SIC for **R**adiation-Tolerant **T**ransmitter in **28** nm
- Goals
  - Demonstrate NRZ transmission at 25 Gb/s
    - Using embedded data generators
  - Evaluate the radiation hardness
  - Study co-integration with SiPh PICs
- Architecture
  - Four 25 Gbps channels
  - Dual Operation Mode Driver
    - Ring-Modulator Driver / Cable Driver
  - Low Jitter LC ADPLL
  - Data generators
  - Radiation test structures



Status: ASIC – DART28NRZ (2)

- Most major blocks designed
  - PLL / Clock generator / Serializer / Duty-Cycle correction circuit / Radiation tolerant data path / Data generators / Built-in test functionality
- Being finalised
  - Ring-Modulator/Cable driver
  - Radiation test structures
  - Chip level assembly started
- Submission
  - April 2023
- ASIC functional and TID testing
  - Q3 2023
- SEU testing
  - Q1 2024



Simulated Full-Swing 25.64 Gb/s Driver Output

Status: FPGA System investigations

- Understanding the High Speed link Market and Technology to answer technical (and existential) questions for the ASIC & Photonics activities:
  - Which Modulation format is most suited to achieving the overall goals of the Project?
    - NRZ, PAM4, …
  - Is Forward Error Correction (FEC) necessary and if so, what kind?
    - Standard vs Custom
  - What target data-rate (per lane, per link)?
    - At high data-rates, Clock and Data Recovery (CDR) circuits present in optical transceiver modules may prevent the use of ‘custom’ (beam synchronous) line rates
  - Which Module types?
    - e.g. QSFP28, QSFP-DD, …
    - Can we meet the optical power budget with custom front-end developments?
  - Which band/wavelengths for CWDM?
    - O-band (around 1310nm) vs C-band (around 1550 nm)
  - How will the Datacom Market evolve? What are the trends?
    - Crystal ball question to try to latch on to more long-lived link standards

Questions answered through:

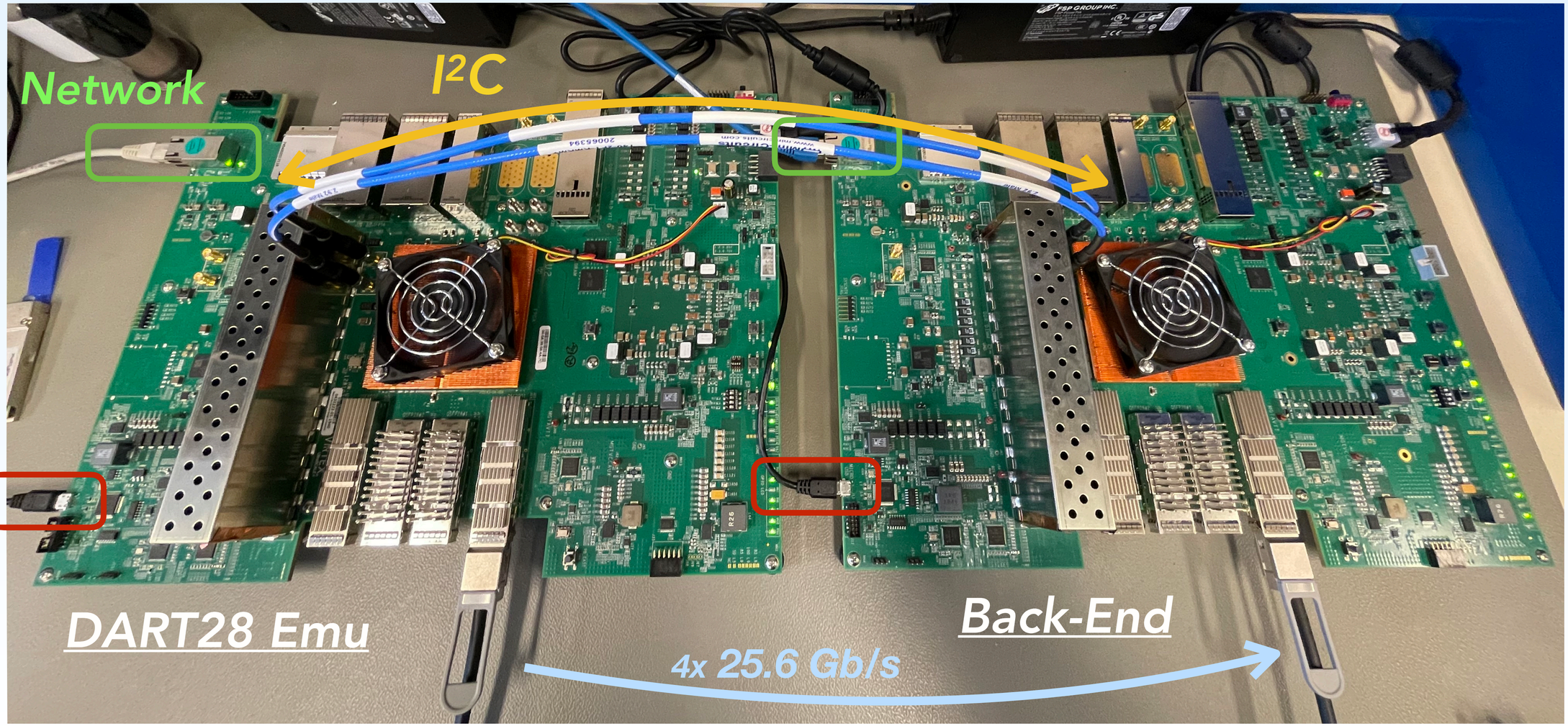
Rolling technology survey

Detailed studies as necessary (e.g. FEC)

See presentation at last EP R&D Days

Status: FPGA System investigations (2)

- Preparing for DART28 NRZ Testing
  - Emulation Test Bench (Firmware implemented on evaluation boards) being validated

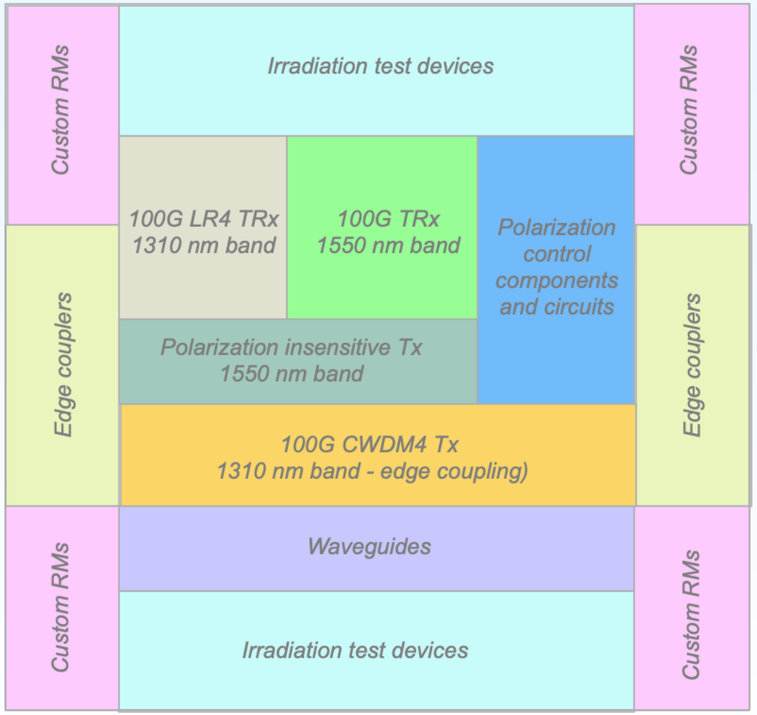


Status: Opto – Silicon Photonics

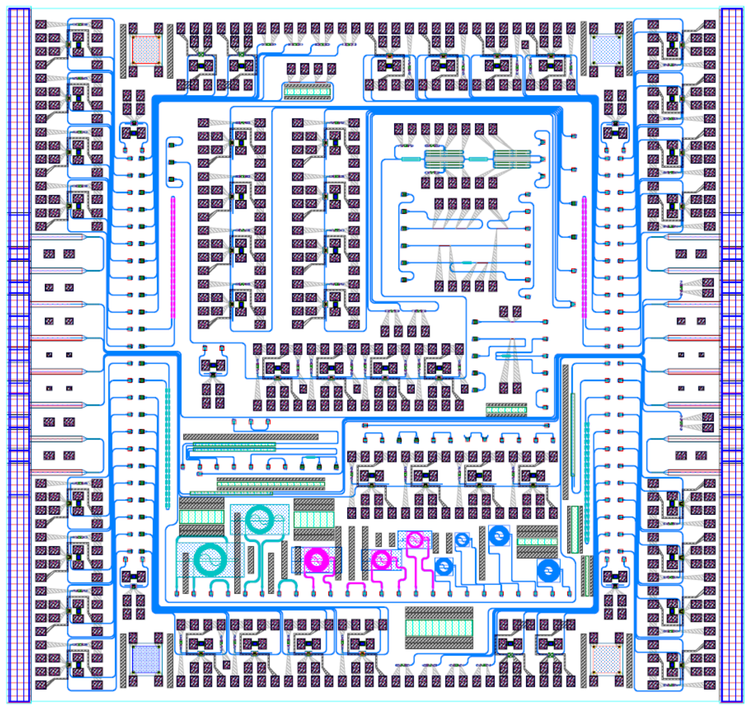
- System and Device Design
  - Implementation of Photonic Integrated Circuits (PICs)
  - Study of system operation (e.g. wavelength, temperature, polarisation effects)
- Radiation tolerance
  - Basic radiation tolerance studies of SiPh devices (X-ray TID, neutron fluence, proton SEE)
  - Study of impact of temperature on TID effects
- Packaging
  - Workpackage re-instated in 2022
  - Will invest in semi-automatic fibre alignment station in 2023
    - To enable PIC edge-coupling

Status: SiPh PIC design

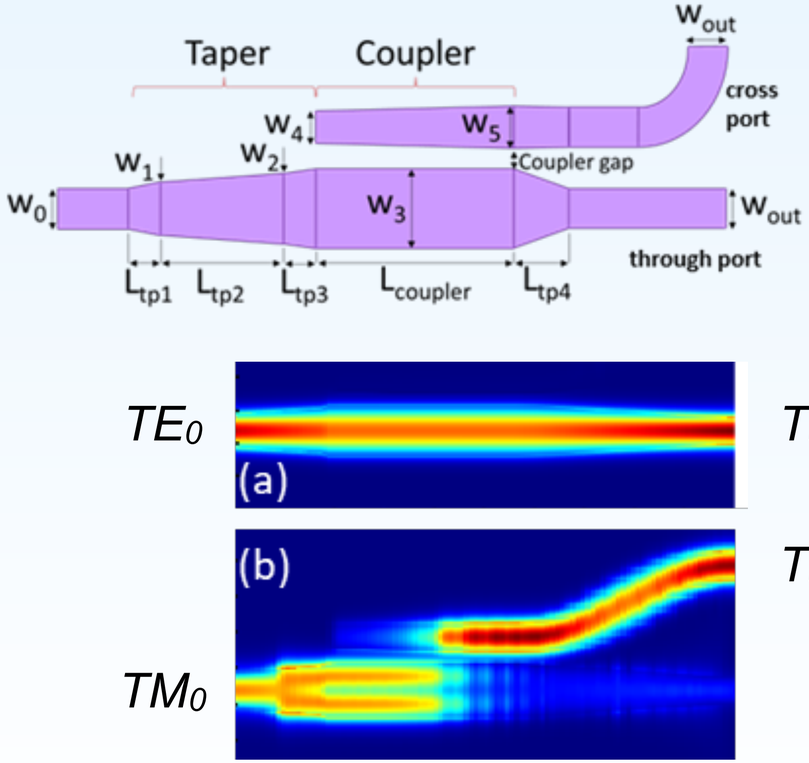
- Third CERN-designed PIC submitted for fabrication at imec using latest SiPh process
  - Study device performance in new process (functionality & radiation)
  - Included 4-channel Wavelength Division Multiplexing circuit operating around 1310 nm
  - Included novel structures for on-chip polarisation diversity



Floorplan



5 mm x 5 mm Layout

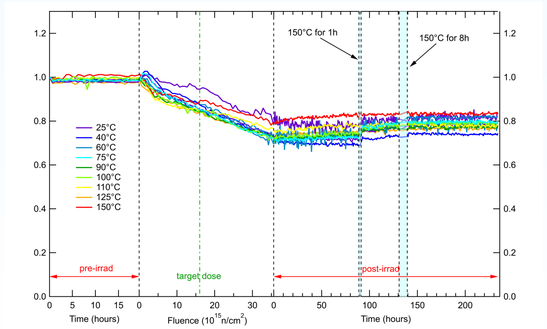


Polarisation Diversity Test Structure

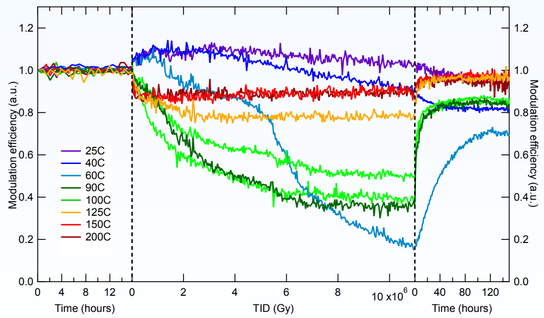
Status: SiPh Radiation Tolerance

- Carried out X-ray & neutron irradiation test with varying device temperatures
  - Neutron irradiation less damaging, independent of temperature
  - TID potentially more damaging, can be fully annealed with elevated temperature using on-chip heaters
- High-fluence proton irradiation of integrated Ge-photodiodes
  - Limited impact, appear more tolerant than current discrete devices
- Investigation of Single-Event Effects in SiPh devices started
  - Synergy with WP 1.4 – thanks to first tests with TPA-TCT laser emulating particle strikes

Silicon Photonics Ring Modulators

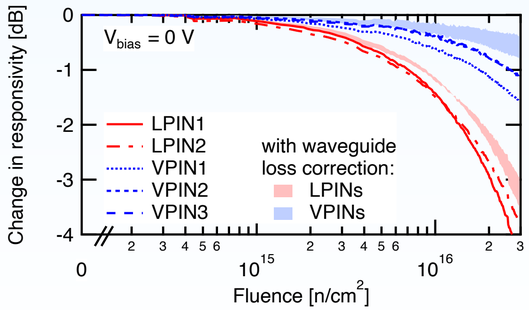


> 3.5x10^{16} n/cm^2



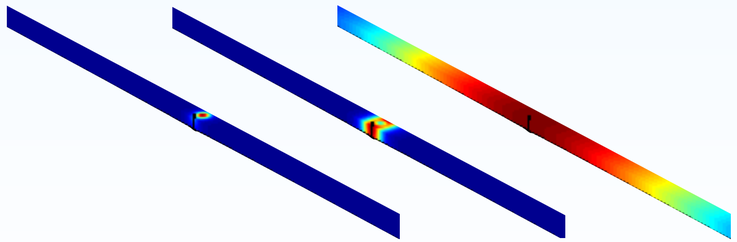
> 10 MGy

Integrated Ge-PD



> 2x10^{16} p/cm^2

Simulated Particle Strike



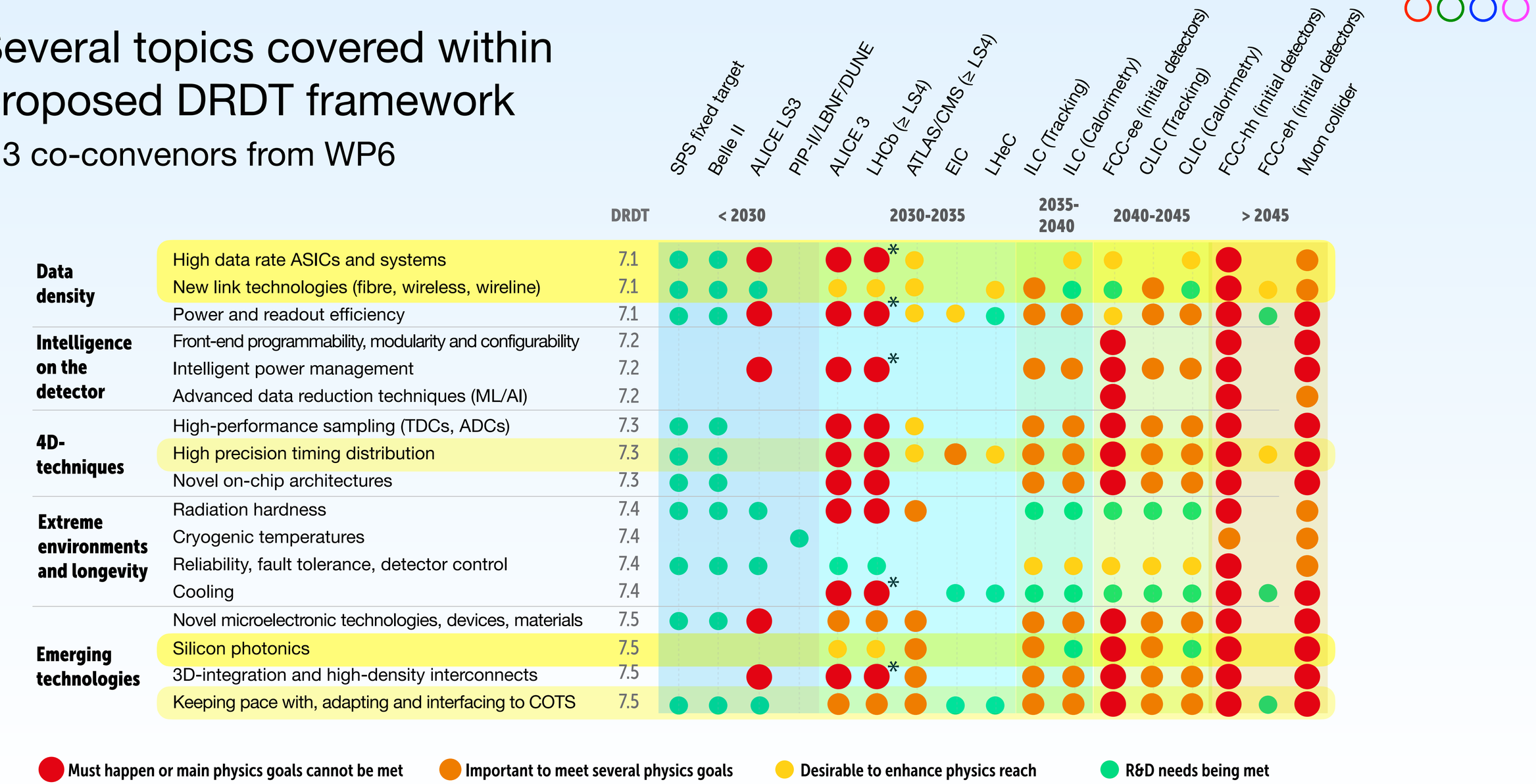
induces loss in waveguide
very small effect measured

Status Summary

- WP6 has produced much interesting R&D towards the implementation of future optical data transmission systems
  - Radiation tolerance
  - Higher line rate
  - COTS standards vs HEP
  - Async links
  - Low Mass, Low Power, Low Cost
- First link demonstrators have been operated
  - FPGA-based for line rate and FEC studies
  - Instrumentation-based for Silicon Photonics components
    - Including first thermal control of ring modulators, an important step to a robust system
- Work on providing building blocks for future application specific implementations is thus well advanced
  - Not a project goal to provide turn-key components for final applications

ECFA Roadmap & Implementation

- Several topics covered within proposed DRDT framework
  - 3 co-convenors from WP6



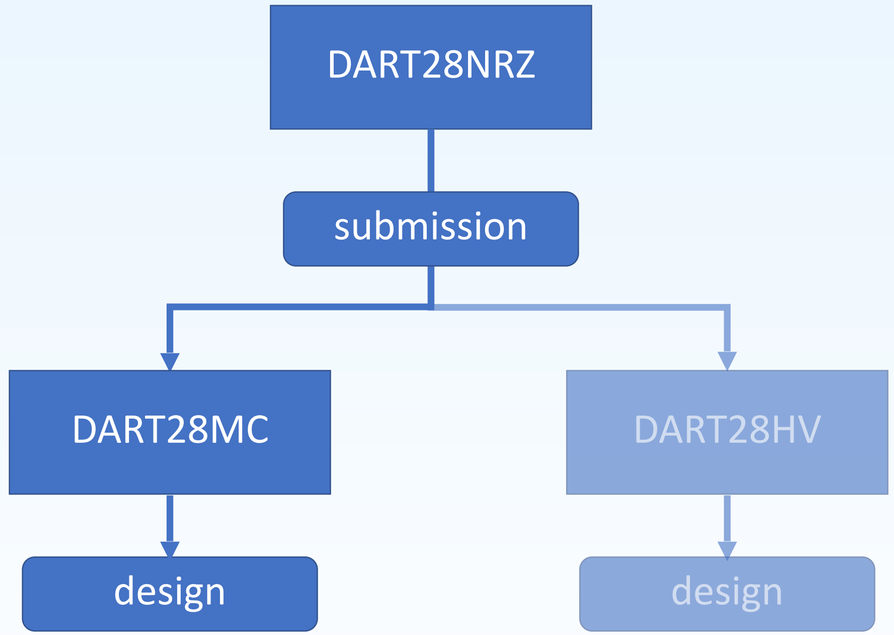
After: The 2021 ECFA detector research and development roadmap

Plans for EP R&D Extension

- Retain three major topics: ASIC, FPGA, and OPTO
- ASIC tasks
  - DART28NRZ extended to higher-voltage output driver – DART28HV
  - SiPh Demonstration ASIC – including system functionality
  - Rad-Hard FPGA – to enable (amongst others) future data concentrators to feed high-speed links
- FPGA tasks
  - System tests – including ASICs, SiPh PICs, commercial components
  - COTS & technology survey – to be able to adapt to commercial availability
  - Ethernet Link for Front-Ends – feasibility study
- OPTO tasks
  - SiPh System and Chip design
  - SiPh radiation hardness
  - SiPh packaging – including edge coupling that has not been investigated up to now

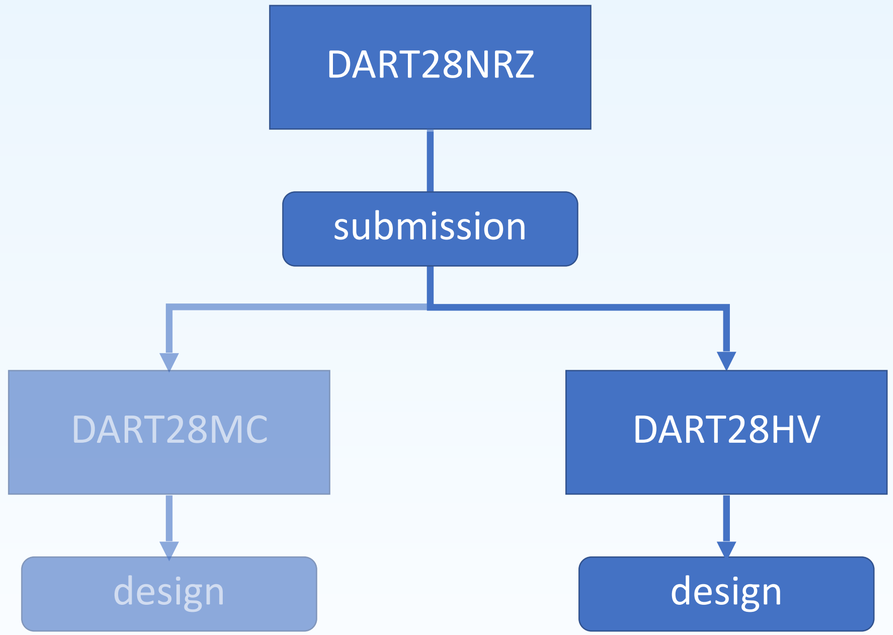
ASIC-1: DART28NRZ to Macro Cell

- Upon submission of the DART28 (April 2023)
  - “Transforming” DART28 core circuits into a Macro Cell (DART28MC)
  - Objective:
    - Facilitate the integration in ASIC for HEP detectors
    - Collaboration with LHCb in the VeloPix project
    - Bus interface under discussion with users to define
      - Data-rates / protocols / ...
  - The DART28MC will contain:
    - Layout
    - Schematics
    - Abstract
    - Timing model
    - Documentation



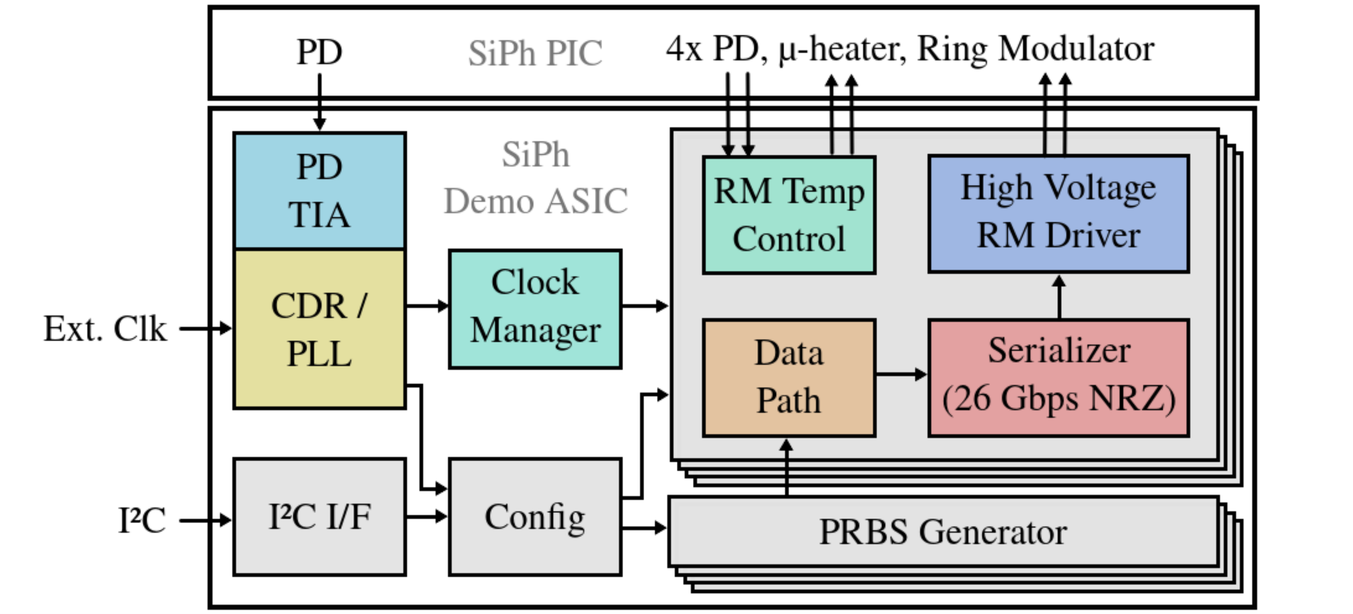
ASIC-1: DART28HV

- Efficient driving of SiPh ring modulators require voltages above standard ASIC supply voltages:
  - ≈ 1 V for the DART28 technology (CMOS 28 nm)
- In order to address that issue, a High-Voltage (HV) upgrade of the DART28, the DART28HV will be designed:
  - The Architecture, Functionality and Footprint will be kept the same
  - The output driver will be redesigned so that the output voltage swing will almost double
  - The major challenge is to achieve high-voltage driving while avoiding gate-oxide breakdown
  - The design work will start upon the DART28 submission



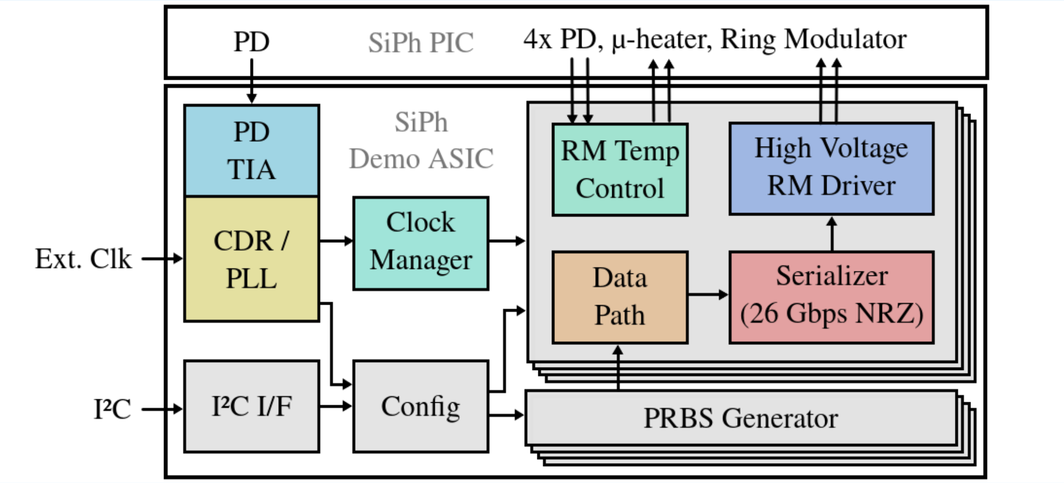
ASIC-2: SiPhDemo

- Development of a “fully” functional **SiPh** system **demo**nstrator ASIC (SiPhDemo)
- Objective
  - Demonstrate NRZ transmission at 100 Gbps (4 × 25 Gbps) with a SiPh system
- Down-link
  - Timing and control link
  - Single channel 2.5 Gbps
- Up-links
  - Data links
  - 4 × 25 Gbps NRZ



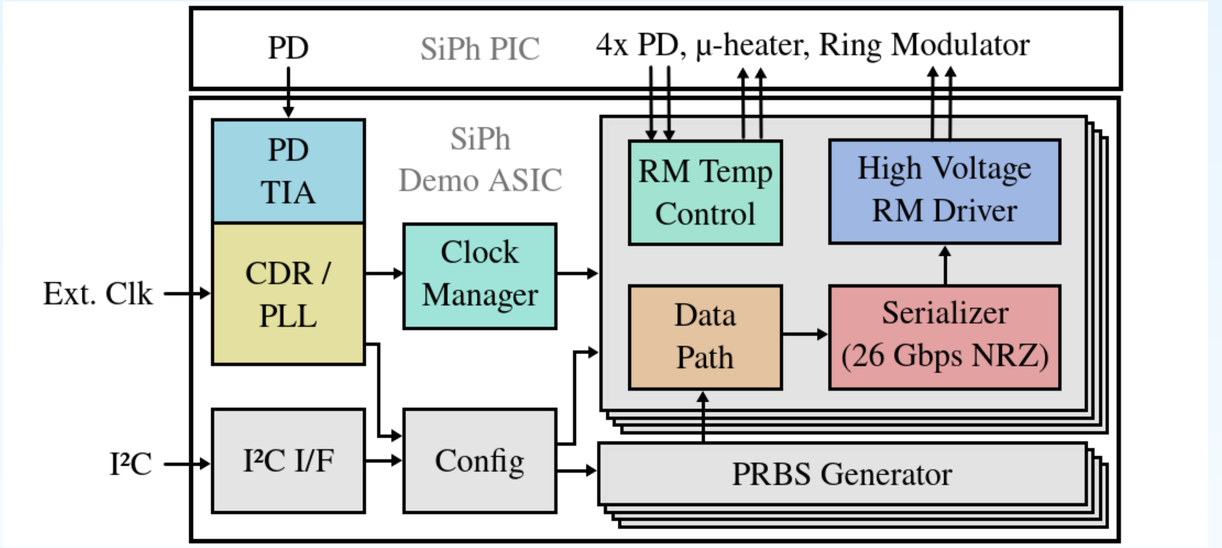
ASIC-2: SiPhDemo

- Designed in 28 nm CMOS
- Co-designed with the SiPh System and Chip Design task
- Matches the PIC footprint on the interconnect side
- Interfaces with a PIC containing:
  - “Down-link” photodiode (PD)
  - Four Ring-Modulators (RM)
  - Associated heaters (µ-heaters)
  - Average optical power monitoring photodiodes (PD)



ASIC-2: SiPhDemo Architecture

- Transimpedance amplifier:
  - Amplifies the down-link photocurrent
- Clock and Data Recovery (CDR)
  - Recovers the down-link bit clock and data
  - Generates the high-frequency clocks for the serializer
- RM Temperature Control
  - Monitors the average optical power on each ring-modulator drop-port (4 ×)
  - Individually controls the power fed to the µ-heaters to keep the optical power constant and thus the ring-modulator tuned to the set wavelength (4 ×)
- High-Voltage modulator drivers (4 ×)
- 25 Gbps serializers (4 ×)
- Self generated data (PRBS Generator) (4 ×)
- I2C port for testing and control



ASIC-3: RH FPGA

- FPGAs have been enablers of HEP off-detector systems
- Rad-Hard FPGAs that can be installed inside HEP detectors are not available
- Some on-detector functions would benefit from embedded programmable logic:
  - Data concentrators/aggregators
  - Trigger algorithms
- We propose to study the feasibility of developing a moderate complexity (realistic for our community) Radiation-Hard FPGA (RH-FPGA)
  - But, nonetheless, useful for embedded detector systems
- The study should answer questions like:
  - Which detector systems could benefit?
  - Which architectures are best suited for data concentrators, data compression and trigger algorithms?
- It will propose:
  - Architectures
  - Software and firmware tools
  - Minimum hardware set
- Depending on the study conclusions, a proposal for a demonstrator ASIC will be made

FPGA-1: System Testing

- Hardware emulation ahead of and during ASIC design
  - DART28NRZ
  - Temperature Control of the Ring Modulators in the PIC
- Algorithm investigations in order to guide future ASIC designs
  - FEC studies for 25Gbps NRZ links
- Support system demonstrators with “back-end” systems
  - Timepix + DART integrated demonstrators
- Preparation for ASIC testing and ASIC/PIC system testing
  - Hardware (the FE boards hosting the chips)
  - Firmware (the full test system and the BE counterpart of the tested chips)
  - Software (System test control)

FPGA-2: COTS & technology survey

- Rolling survey of availability and functionality evolution of commercial components
  - FPGAs
  - Optical Transceivers
- Validation with respect to our specific needs
  - 100G CWDM
  - LHC-synchronous links
  - specific FECs

FPGA-3: Ethernet Link for Front-Ends

- Streaming data directly from detector front-end to the DAQ processing farm is very attractive for trigger-less DAQ architectures
  - Would require sending output of FE datalink directly into a commodity network switch
- Propose to study the feasibility of implementing a standard-compliant 100G Ethernet link for on-detector deployment
  - Buffering
  - Asynchronous to LHC collisions
- To be carried out in close collaboration with future Back-End and DAQ developers

OPTO-1: SiPh System & Chip Design

- WDM system development
  - Multi-wavelength sources
  - Remote optical power supply: on-chip polarisation control vs PM fibre from source
  - Temperature control of rings: control stability, feedback, initial locking
- PIC evaluation
  - Polarisation control structures
  - WDM systems 1310 and 1550
  - Ring modulator performance: bandwidth & drive strength
- PIC design
  - two design iterations to integrate understanding from evaluation each previous PIC
    - 1st imec submission 2025
- Driver & Receiver ASIC evaluation
  - Commercial, DART28
- System integration & evaluation
  - Definition and testing of system evaluation metrics
  - Integration with integrated ROICs and Hybrids, integrated system setup methods

OPTO-2: SiPh Radiation Hardness

- Radiation Hardness testing
  - Benchmarking of PICv3 devices
  - Explore ultimate device limits in view of FCC-hh (irrad facility limitations TBC)
  - Explore radiation hardness of SiPh laser sources, understand limits to inform laser remoting requirement
  - Radiation testing of updated designs informed by earlier testing and modelling work
- Radiation effects modelling
  - Waveguides
  - Modulators
  - Photodiodes

OPTO-3: Silicon Photonics Packaging

- Market Watch
  - Follow industry development
  - Evaluate promising solutions
- Fibre attachment
  - Exploitation of alignment machine
  - Refinement of techniques, adapting to new industry solutions
- Co-packaging
  - Integration of driver and PIC: flip-chip vs wire-bond
  - Laser integration on-chip for low-radiation applications
  - Participation in full readout system Front-End integration on Hybrids
- Development of SiPh TRx module
  - Integrated standalone module to distribute in small quantities for user evaluations

WP6 Extension resources

- The realistic and ambitious plans outlined require resources
- The 5-yr request made for WP6 includes
  - 720k CHF consumables including 5 (2 ASIC, 3 PIC) chip submissions and radiation testing
  - 315k CHF investment in optoelectronic test equipment
  - 35.2 FTE split 1:4 between Students:Fellows

Collaboration Potential

- The DRDT 7 implementation will create opportunities to collaborate with interested institutions
  - DRDT 7.1
    - High data rate ASICs and systems
    - New link technologies (fibre, wireless, wireline)
  - DRDT 7.3
    - High precision timing distribution
  - DRDT 7.5
    - Silicon Photonics
    - Keeping pace with, adapting and interfacing to COTS
- We are in discussion with several institutions to find synergies
- The upcoming DRDT 7 Implementation Workshop (Mar. 14-15 2023) will provide the first open forum for defining these collaborations
  - We encourage attendance and discussion

https://indico.cern.ch/event/1214423/