EP-ESE
ELECTRONIC SYSTEMS FOR EXPERIMENTS

WP 5 – IC TECHNOLOGIES 2020 2023
ACTIVITIES OVERVIEW

D. CERESA on behalf of EP R&D Work Package 5

WP5 - IC TECHNOLOGY ACTIVITIES ORGANIZATION

WP 5 – *IC Technology* - *Leaders: K. Kloukinas, D. Ceresa (Deputy)*

WP 5.1 – *Technology Evaluation*

Team: G. Borghello, D. Ceresa, F. Piernas Diaz, R. Pejasinovic

WP 5.2 – *IP block development*

Team: R. Ballabriga, F. Bandi, M. Piller, T. Hoffman

WP 5.3 – *Rad-Tol SOC development*

Team: M. Andorno, A. Caratelli, D. Ceresa, J. Dhaliwal, K. Kloukinas, R. Pejasinovic.

WP 5.4 – *Powering solution*

Team: S. Michelis, G. Ripamonti, P. Antoszczuk, G. Bantemits, N. Van Der Blij

ASIC Support – *Technology support*

Team: M. Andorno, W. Bialas, A. Caratelli, K. Kloukinas,.

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ASIC SUPPORT – 28 NM HEP COMMON DESIGN PLATFORM

28nm Common Design Platform

CERN Design Kit

Design flows and scripts for digital design

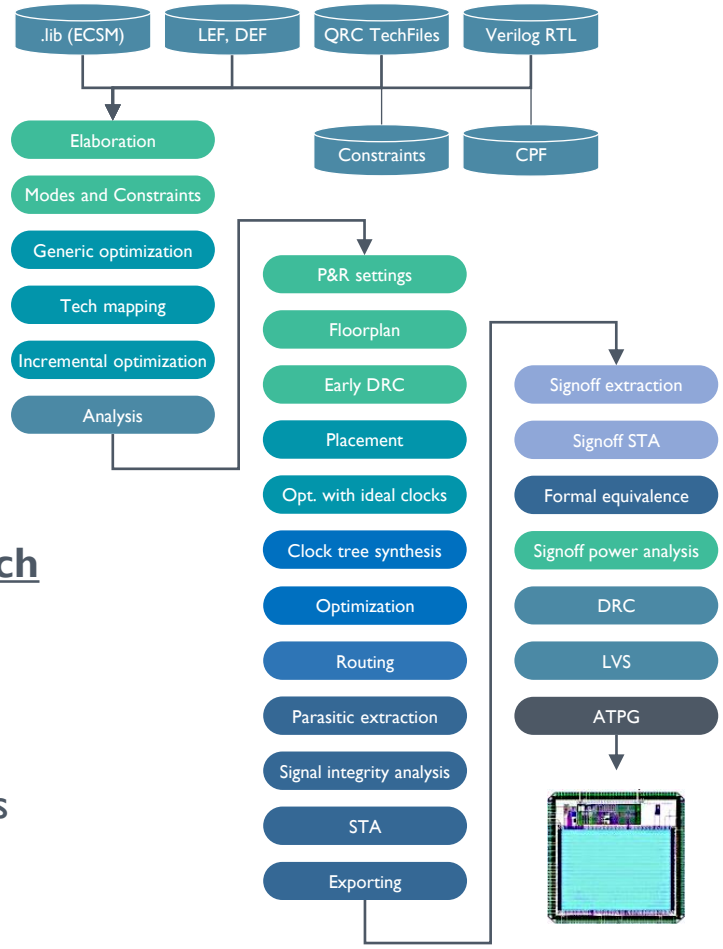
A growing radiation tolerant macro-cells library

System-On-Chip design enablers

NDAs
Commercial contract
Framework for collaborative design

Access via the CERN ASIC Support website:
https://asicsupport.web.cern.ch

Digital-on-top implementation design flow



- The CERN Design Kit is optimised to provide a **tested and reliable solution** that provide **Interoperability within the HEP community** avoiding incompatibilities across design teams
- Set of advanced scripts for synthesis and physical implementation:
  - Specific for radiation tolerant design

ASIC SUPPORT – TRAINING WORKSHOP

Program of the **5-days training workshop** on Mixed-Signal design in 28nm process

Designing in 28nm

Pilot session: Jan.30 – Feb.3, 2023
Next session: Mar.6 – Mar.10, 2023

DESIGN in 28nm

- Design in 28nm technology
- Introduction to the main concepts
- Technology specific requirements
- Radiation tolerant design techniques

ANALOG DESIGN:

- Schematic and layout
- Schematic simulation
- Extracted simulation
- IP block characterization (abstract and lib)
- Usage of the latest Cadence tools

DIGITAL-ON-TOP IMPLEMENTATION

- Digital IC introduction
- Timing constraints
- Synthesis and optimization
- Placement
- Static Timing Analysis
- Power analysis
- Optimizations
- Routing
- Signal Integrity
- Hierarchical analysis and sign-off
- Back-annotated simulation
- Block models generation
- Signoff STA in Tempus
- Signoff power and IR-drop in Voltus
- Signoff DRC and LVS

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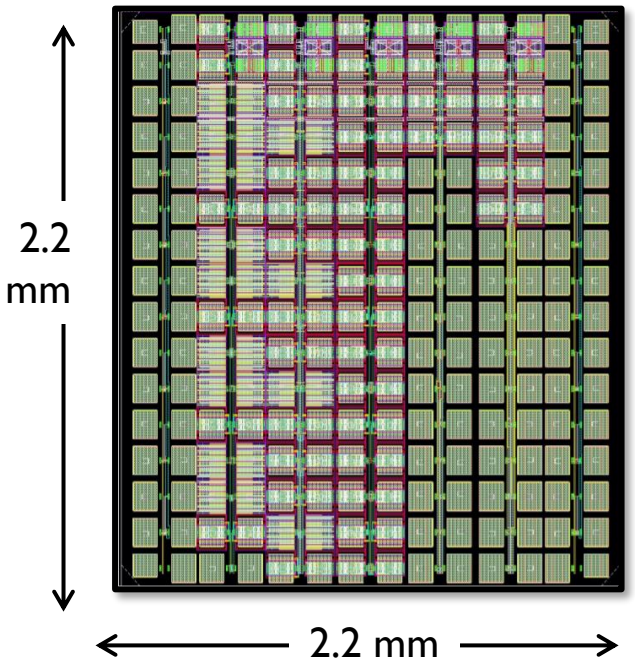
WP5.1 - TECHNOLOGY EVALUATION: TID28 & EXP28 TEST CHIPS

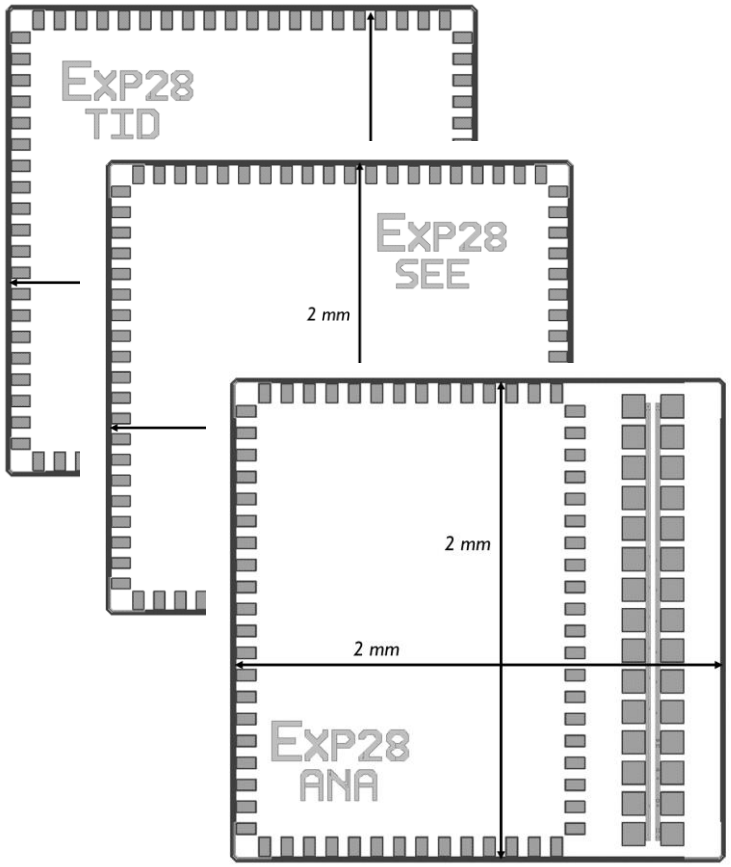
TID CHIP LAYOUT



SINGLE TRANSISTORS ARRAY

7x probing arrays
Different transistor flavors
Variability arrays
Design submitted in June 2021

EXP28 CHIP SUITE



TOTAL IONIZING DOSE (TID) STUDIES:

- Ring Oscillator for standard cells
- Built-In-Self-Test for SRAM memories

SINGLE EVENT EFFECT (SEE) STUDIES:

- Vernier Delay line for Single Event Transient (SET)
- Flip-Flop matrixes for Single Event Upset (SEU)
- Functional SRAM test for SEE on memories

IP BLOCKS CHARACHTERIZATION

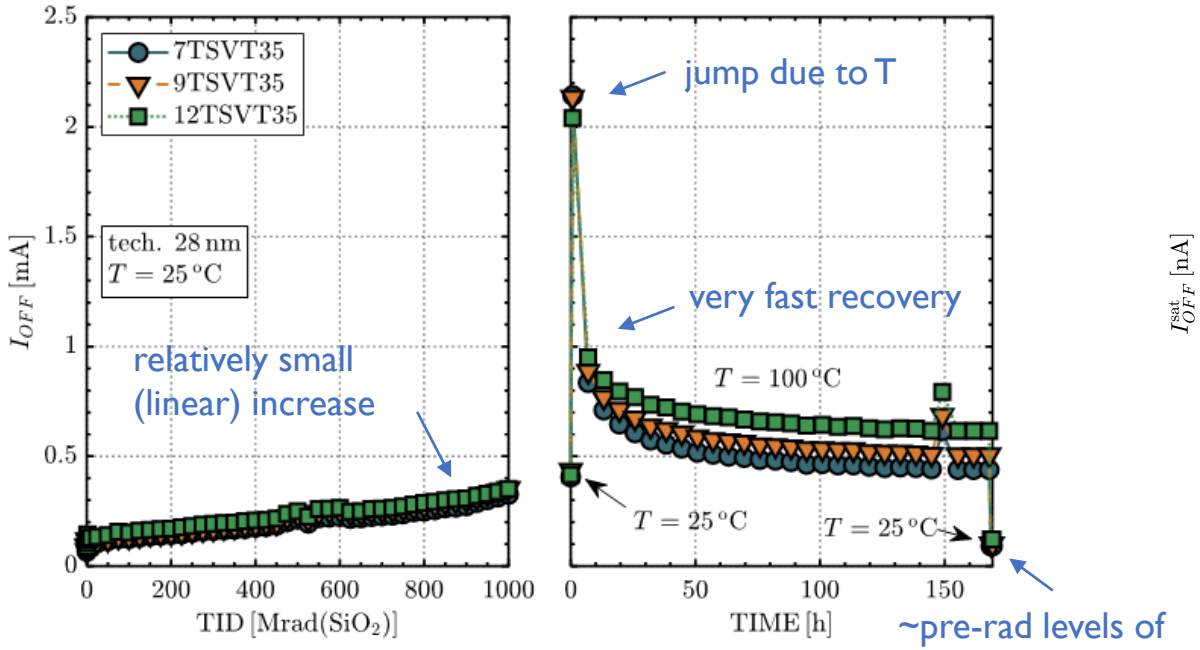
- Bandgap and Temperature sensor
- Digital-to- Analog Converted (DAC)
- Probe array for HV devices and resistors

SUBMITTED ON JANUARY 2022
RECEIVED IN MAY 2022

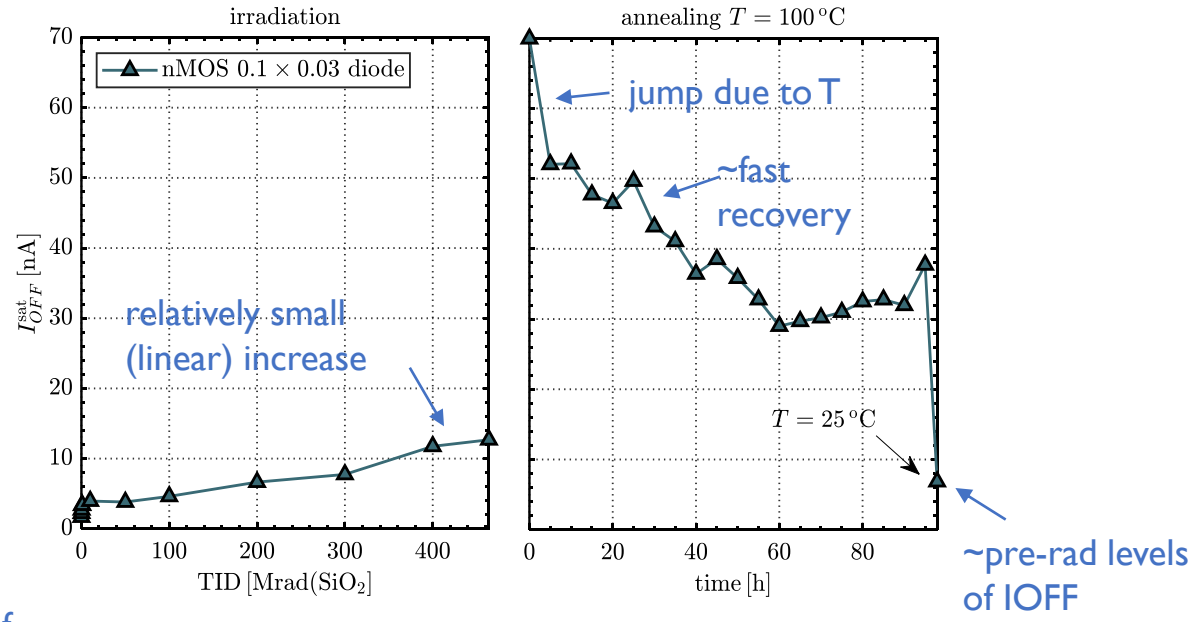
WP5.1 - 28 nm Total Ionizing Dose results
transistor & ring oscillators

Presented by G. Bergamin at TWEPP 2022:
https://indico.cern.ch/event/1127562/contributions/4904915/

EXP28 TID RESULTS



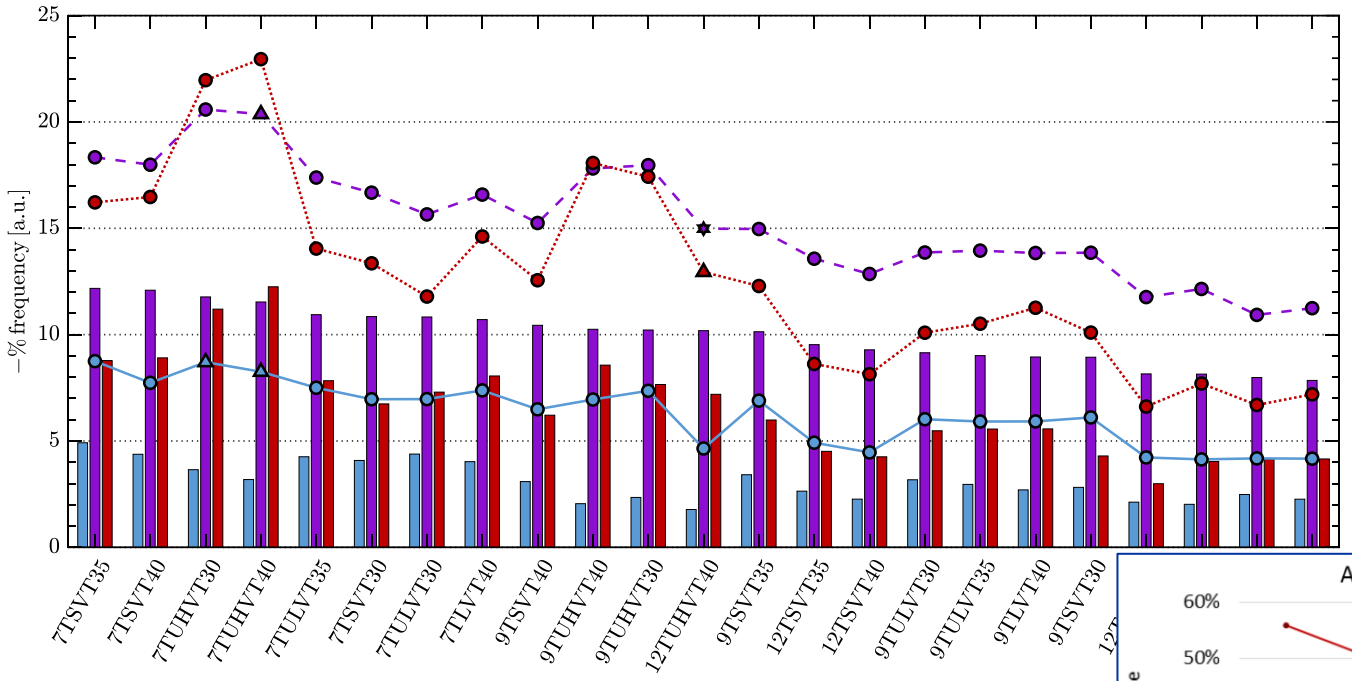
TID28 RESULTS

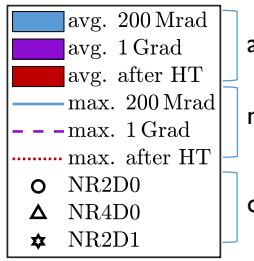


Results of test in single devices well predicted this behavior!

WP5.1 - 28 nm Total Ionizing Dose results

RING OSCILLATORS



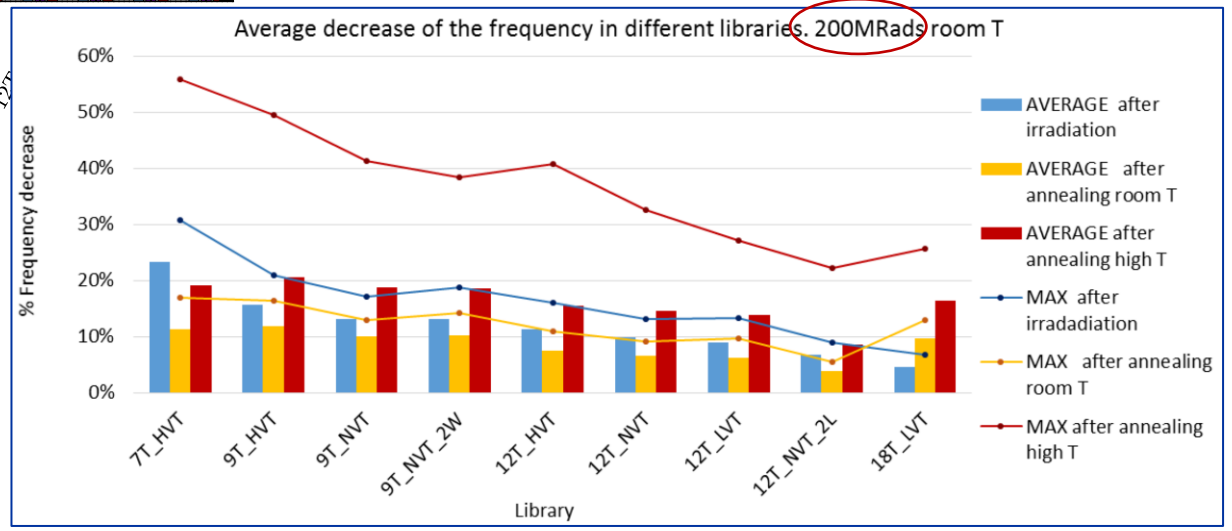


average among all cells of the same library

max degradation

cell with max degradation

much smaller degradation than 65nm technology!!

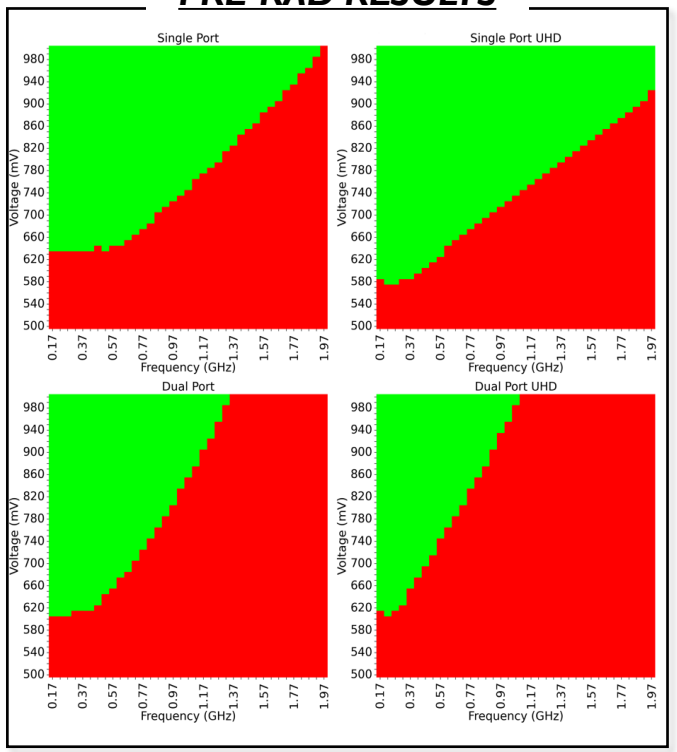


DRAD chip, 65nm tech.
https://cds.cern.ch/record/2725573/files/DRAD%20report.pdf

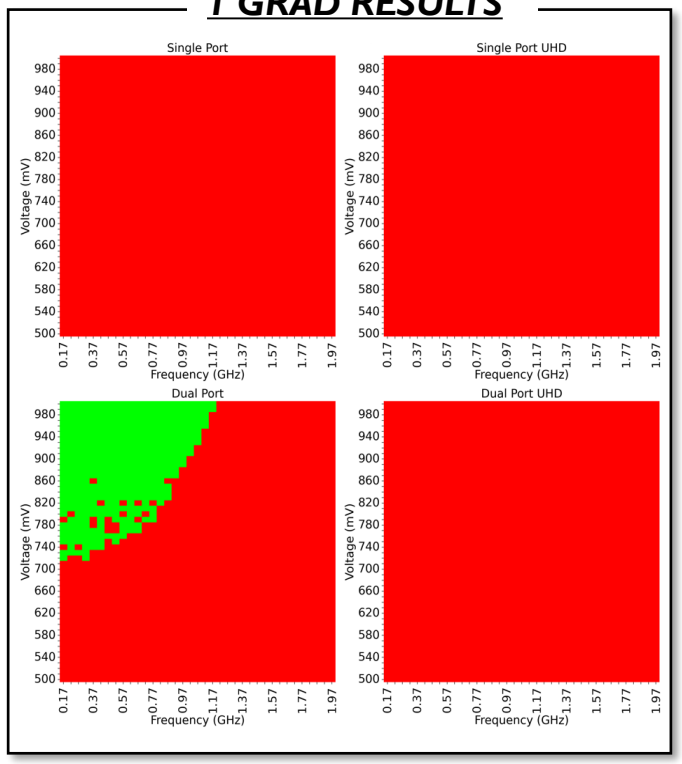
WP5.1 - 28 nm Total Ionizing Dose results
FOUNDRY SRAMS

Testing procedure: BIST logic kept fixed at 0.9V, frequency and voltage scan for SRAMs.

PRE-RAD RESULTS

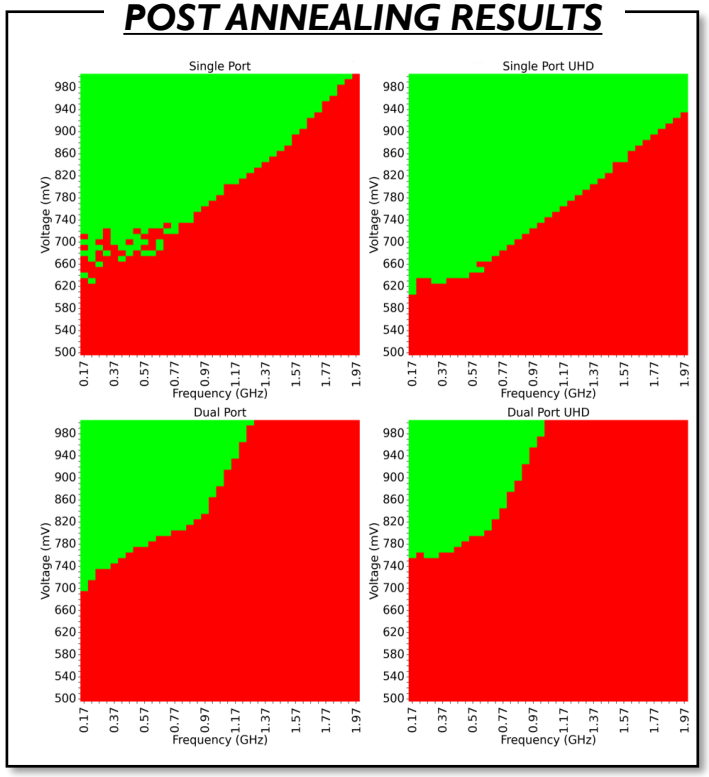


1 GRAD RESULTS



Dual-Port foundry SRAM survived (almost) to 1Grad

POST ANNEALING RESULTS



All SRAMs fully recover after annealing

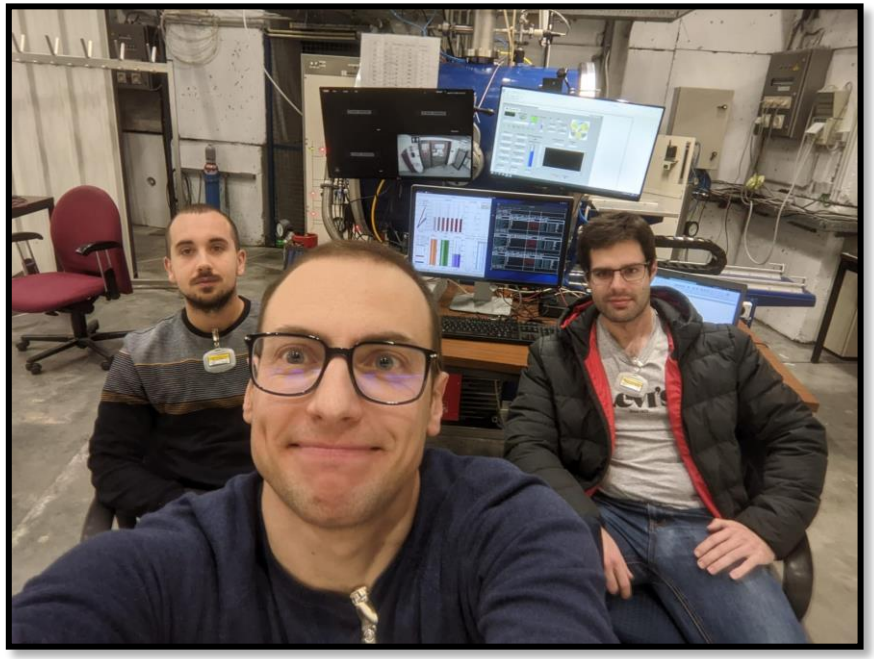
WP5.1 – TEST BEAM HIGHLIGHTS

16-hours Heavy Ion test run in UCL Louvain on 21st-22nd of November

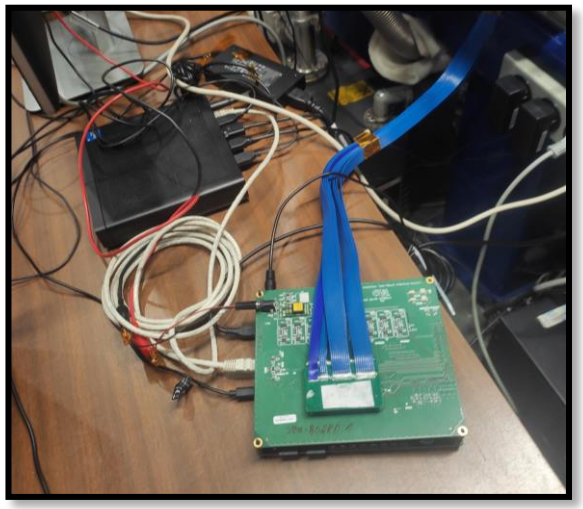
8-hours High-Energy Proton test at TRIUMF Canada on 7th of December

ACCESS TO FACILITY FUNDED BY:

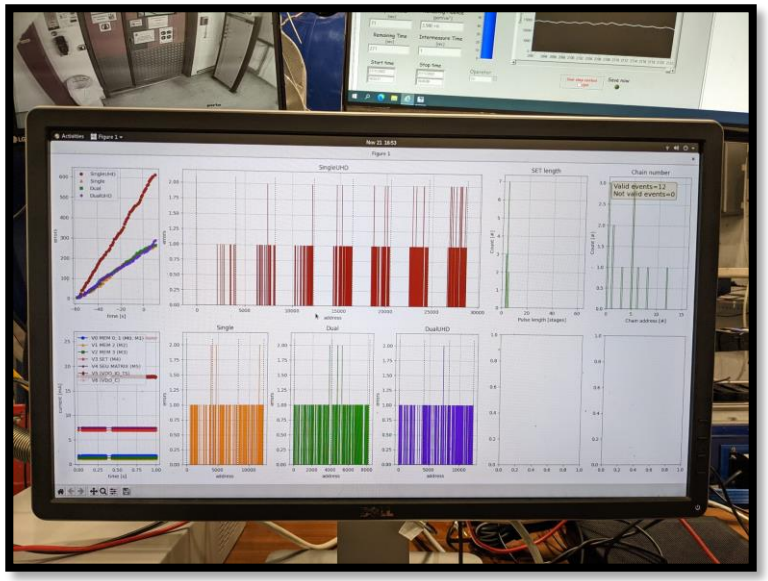
RADNEXT



A HAPPY TEST BEAM TEAM



A SUPER-COMPACT TEST-SYSTEM

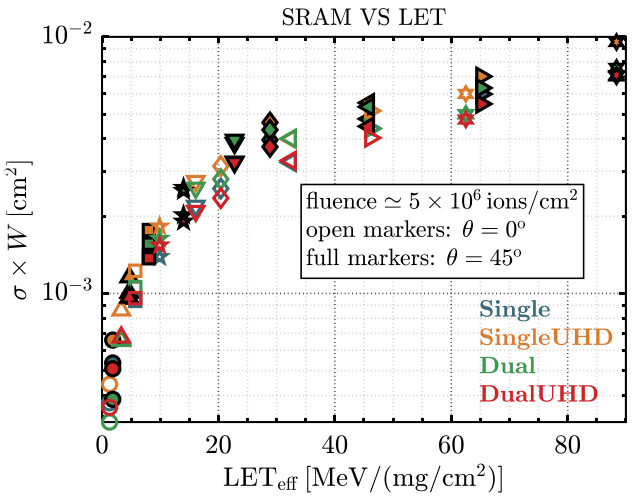


WITH FANCY ONLINE MONITORING

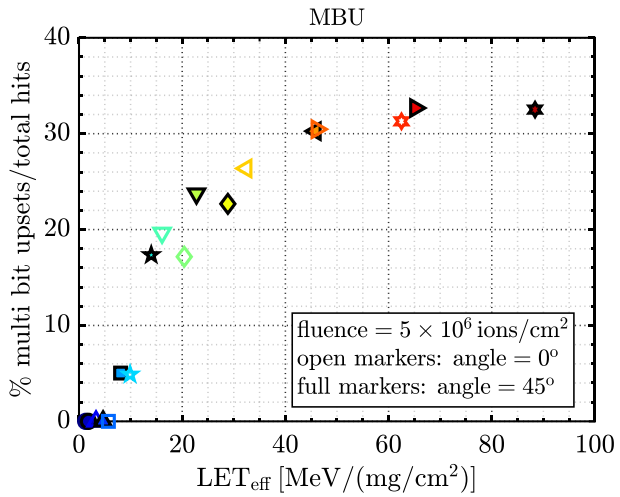
WP5.1 - 28 nm Single Event Effects results

EXAMPLE TEST RESULTS:

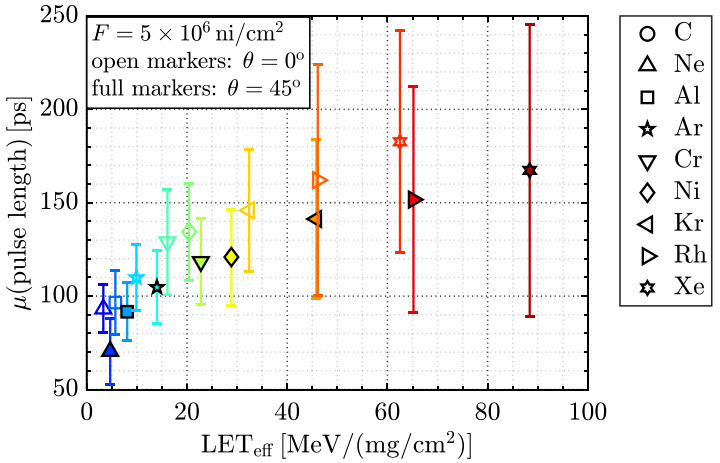
SRAM cross-section



FF multi-bit upset ratio



Single event transient pulse duration



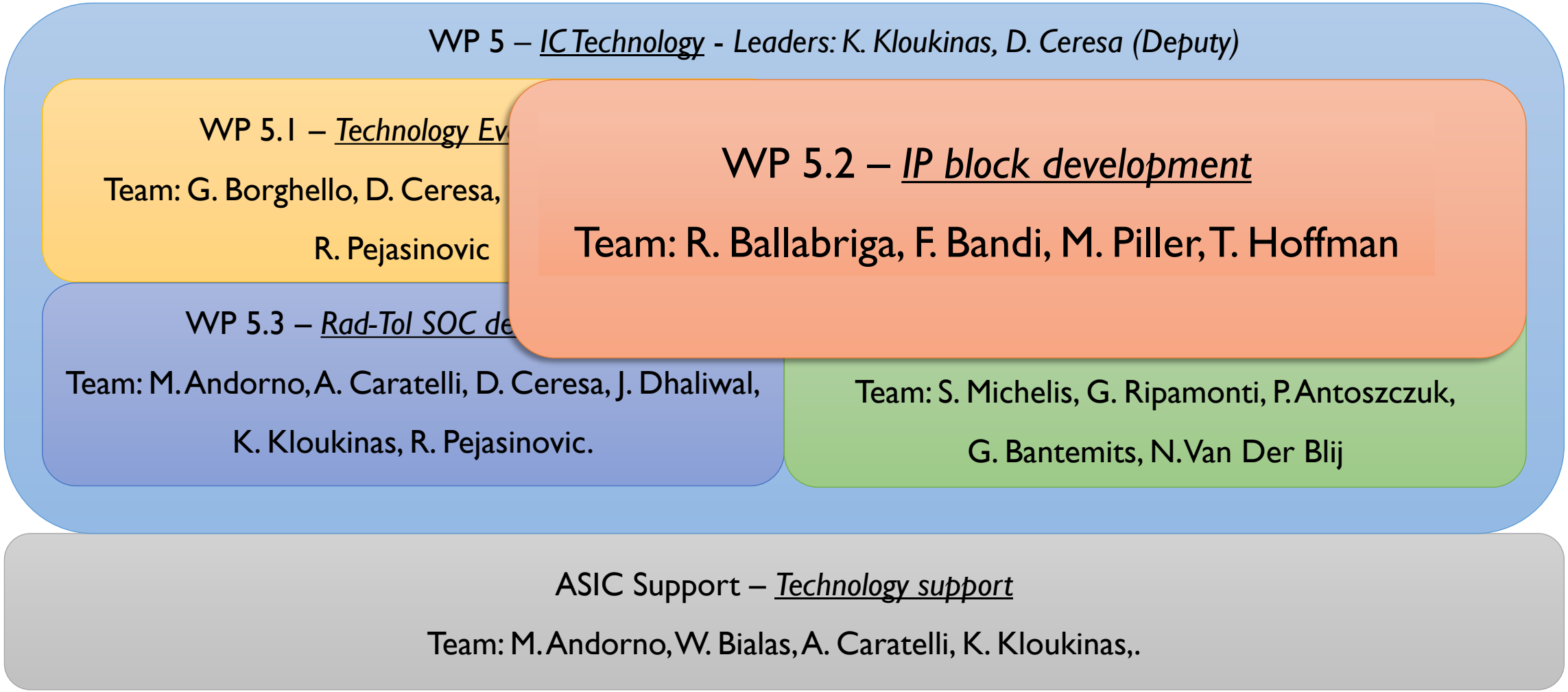
RAD-HARD DESIGN GUIDELINES:

Usability, refresh rate, data encoding scheme,…

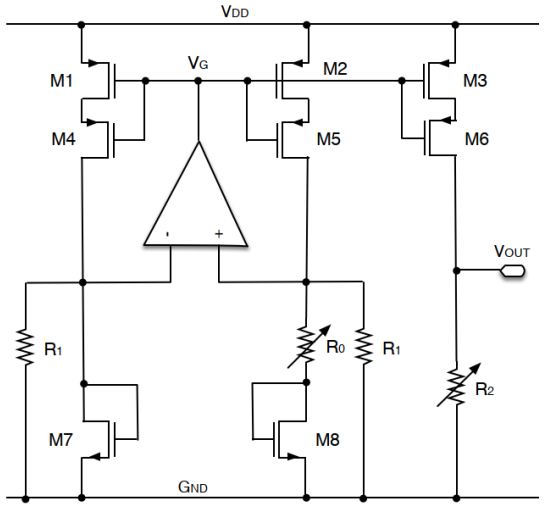
Tap distance, TMR distance, error probability, flavour choice, …,

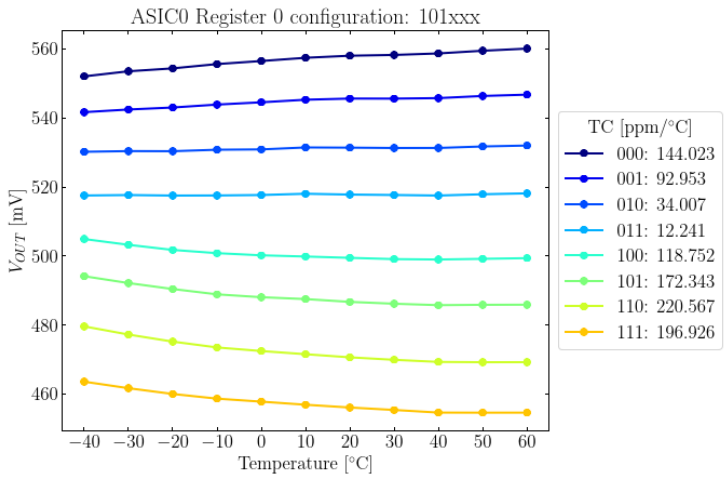
Max pulse length, glitch filtering, SET sensitivity, …,

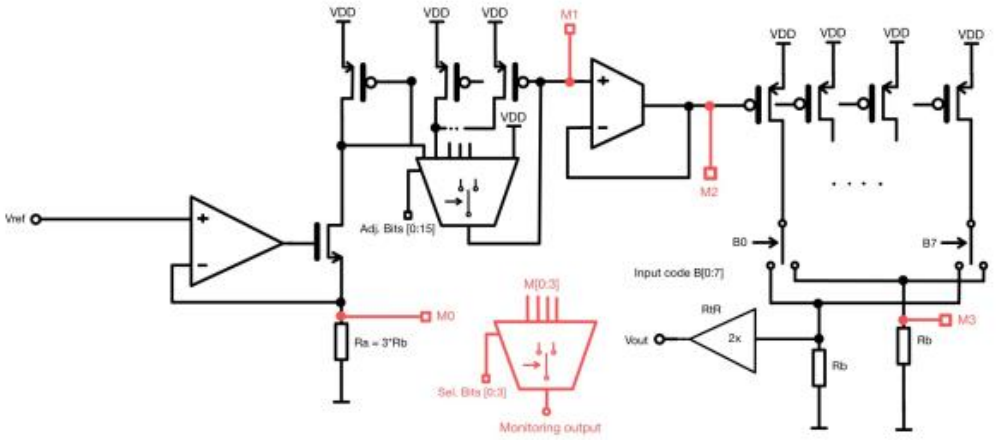
WP5 - IC Technology activities organization



WP5.2 – IP BLOCKS DEVELOPMENT – BANDGAP & 8-BIT DAC







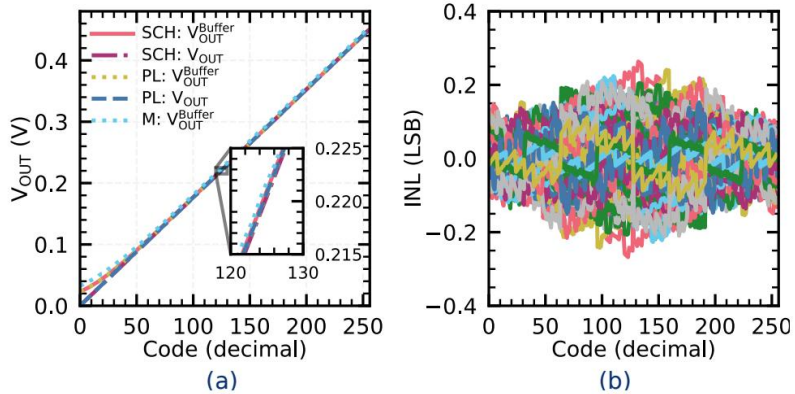


Figure: (a) DAC output voltage results from schematic and post layout (PL) simulations and measurements (M) (b) Calculated INL from Monte Carlo simulations[3]. Irradiation will start in the following weeks.

BANDGAP REFERENCE by G.TRAVERSI (INFN-BG)

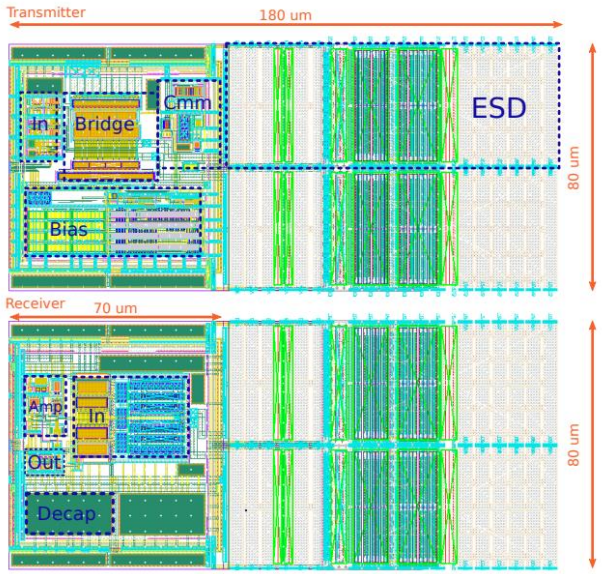
8-BIT DAC by M. PILLER

WP5.2 – IP Blocks development – SLVS transmitter & receiver

Specification

Parameter	Min	Typ	Max	Unit
IO voltage supply	1.08	1.2	1.32	V
Core voltage supply	0.72	0.9	0.99	V
Data rate	0		1.28	Gbps
Temperature	-40		80	°C
Area with ESD		180×80		μm^2
Metal stack		1-2-3(4 power)		metals

Horizontal Layout



Experimental results

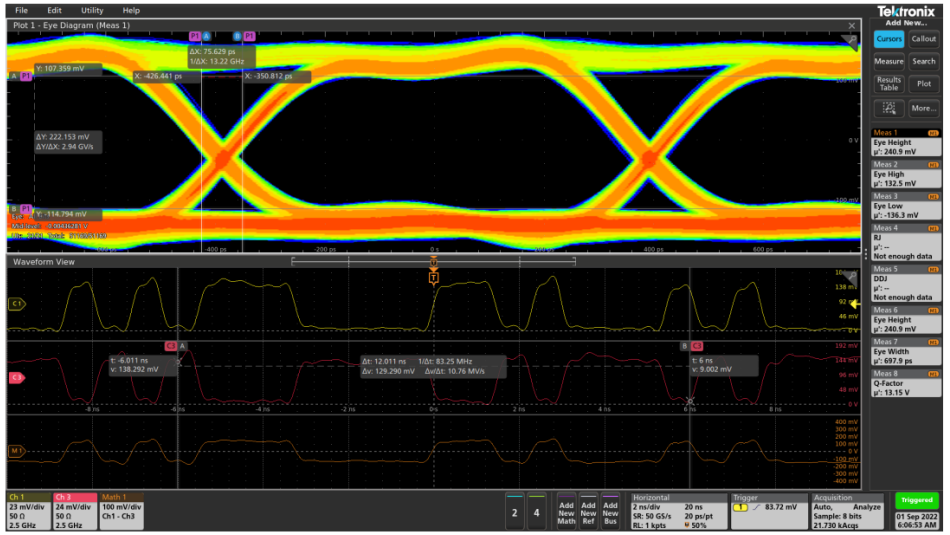
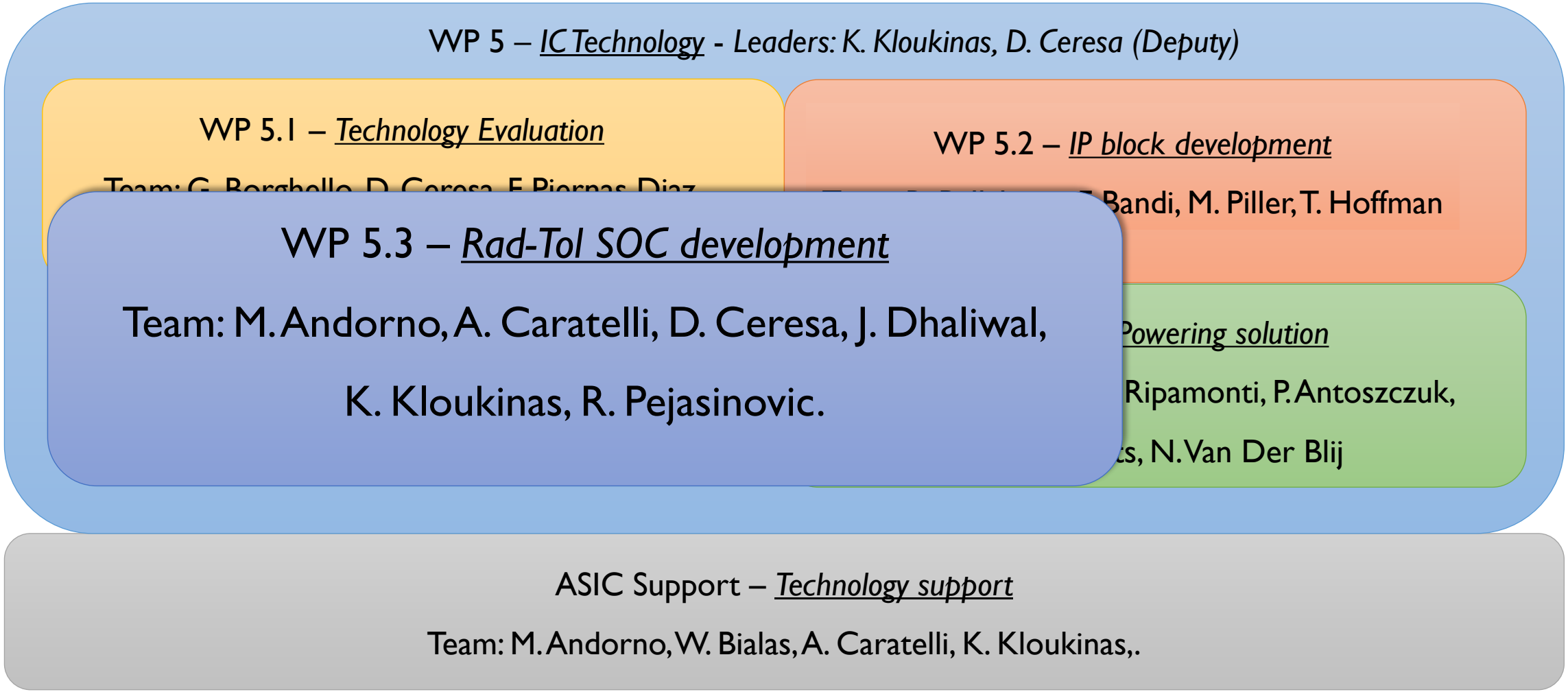


Figure: Eye diagram at 1.28 GHz with 100 Ω termination impedance (oscilloscope input impedance). Eye height, width and jitter are 240 mV, ∼ 700 ps and ∼ 80 ps, respectively. No significant degradation after 1Grad. Acknowledgment: G. Borghello, D. Ceresa, F. Piernas Díaz, R. Pejasinovic.

WP5 - IC Technology activities organization

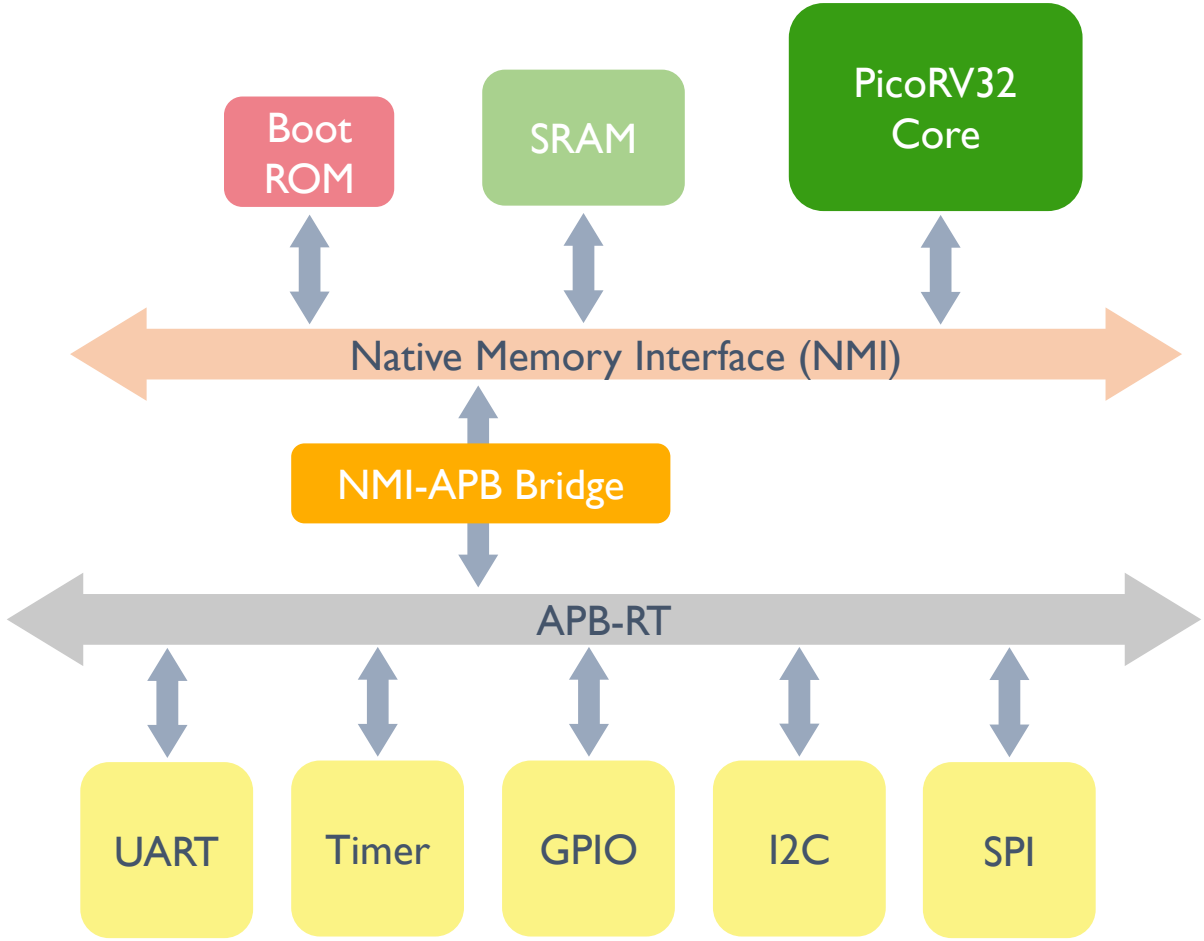


WP5.3 – System-On-Chip Radiation Tolerant Ecosystem

Specifications:

- Microcontroller-style (small, low power, low performance)
- RISC-V core (open-source)
- Radiation-tolerant
- APB-RT bus (from ARM AMBA) with a set of peripherals
- Simple programming interface

DEMONSTRATOR SUBMISSION FORESEEN IN Q3 2023



...OLERANT ECOSYSTEM

RADIATION TOLERANT APB (APB-RT) INTERCONNECT

Control signals are still fully triplicated

32-bit data and address buses are encoded by byte with Hamming(13,8), to permit byte access operations

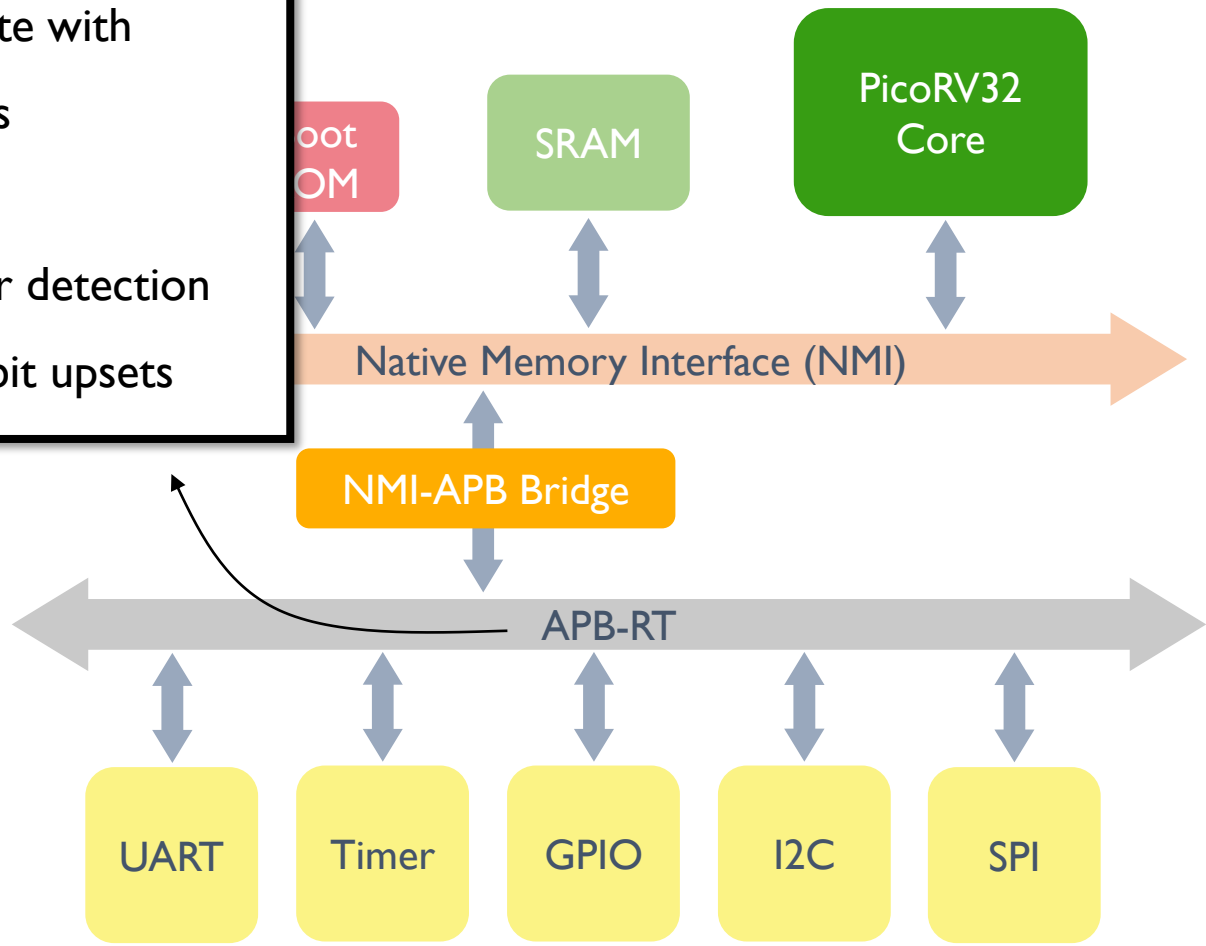
4 parity bits for single error correction

1 extra parity bit for additional double error detection

Placement constraints on buffers to avoid multi-bit upsets

- APB-RT bus (from ARM APBA) with a set of peripherals
- Simple programming interface

DEMONSTRATOR SUBMISSION FORESEEN IN Q3 2023

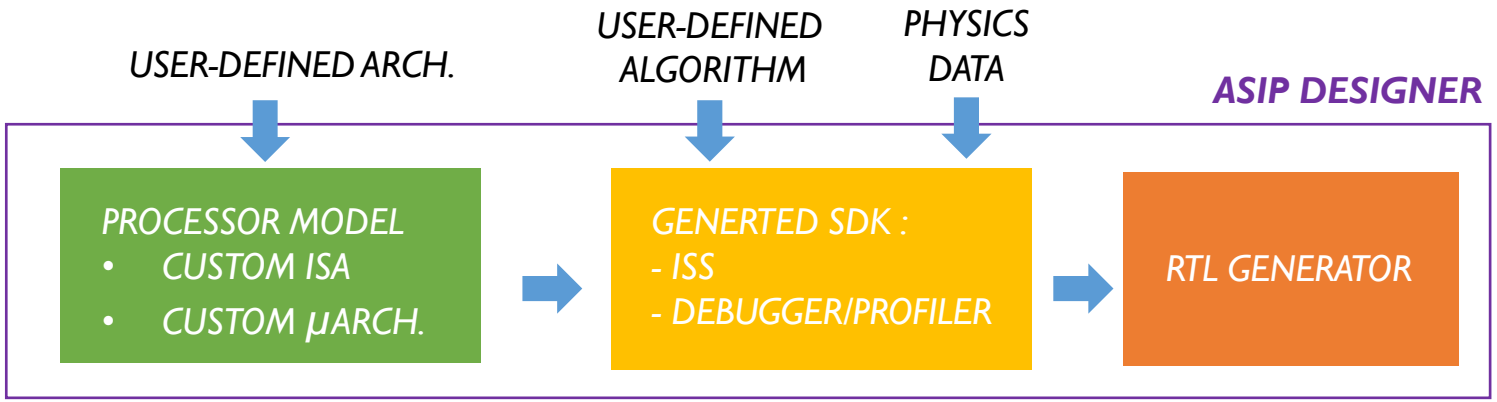


WP5.3 – On-Chip data processing study

Provide physics data and run existing algorithm on a customized processor.
Run on two different architectures:

- *TRV32P3:* 32-bit RV32IM, 3-stage pipeline, 32 registers
- *TMICRO:* 16-bit custom instructions, 3-stage pipeline, 8 registers

Results presented at TWEPP 2022 and Synopsis ASIP Designer University Day 2022



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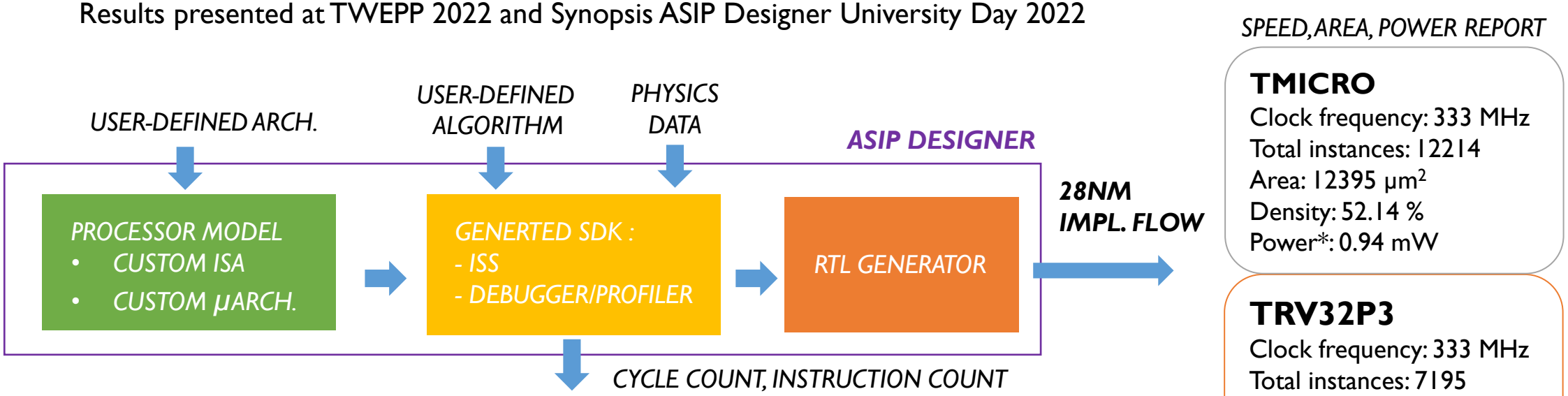


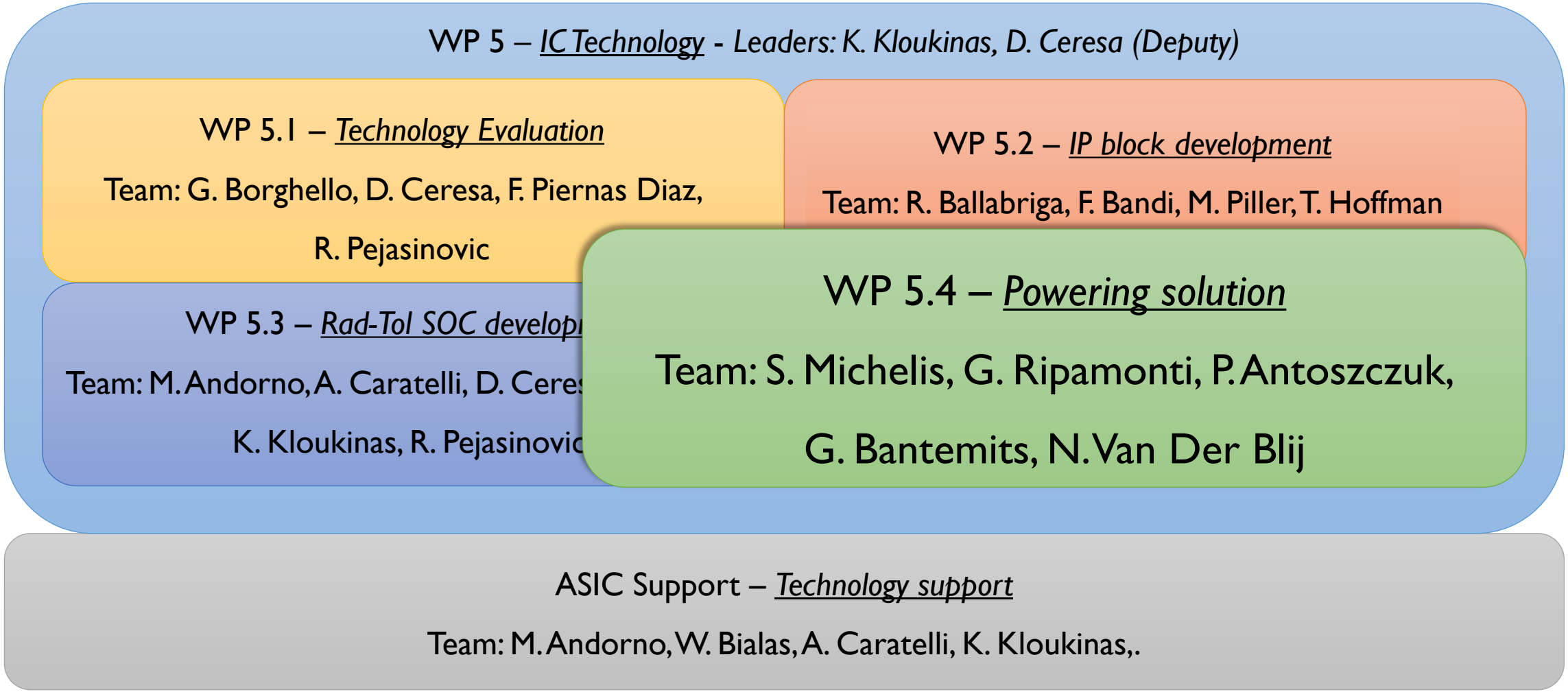
TRV32P3
Total cycle count: 2560
Total instruction count: 2144
Instruction coverage: 71.64 %

TMICRO
Total cycle count: 4284
Total instruction count: 3406
Instruction coverage: 69.50 %

TMICRO
Clock frequency: 333 MHz
Total instances: 12214
Area: 12395 µm^2
Density: 52.14 %
Power*: 0.94 mW

TRV32P3
Clock frequency: 333 MHz
Total instances: 7195
Area: 6147 µm^2
Density: 52.48 %
Power*: 0.50 mW

WP5 - IC TECHNOLOGY ACTIVITIES ORGANIZATION



WP5.4 – Powering Solutions

Existing solutions (in 2020)

Stage 1: $V_{in} = 5.5 - 12V$

bPOL12V
POL buck converter
(0.35 µm HV-CMOS)

$0.63 - 5V, 4A$

Stage 2: $V_{in} = 2.1 - 2.5V$

bPOL2V5
POL buck converter
(130 nm CMOS)

$0.6 - 1.5V, 3A$

Long-term solutions

Stage 1: $V_{in,max} = 48V$

GaN-based 48V DC-DC

Stage 2a: $V_{in} = 2.1 - 2.5V$

bPOL2V5
POL buck converter
(130 nm CMOS)

$0.6 - 1.5V, 3A$

Stage 2b: $V_{in} = 4.5 - 5V$

iPOL5V
Fully-integrated resonant converter
(28 nm CMOS)

$0.8V - 1V, 0.5A$

In production

R&D

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bPOL12V
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Long-term solutions

Stage 1: $V_{in,max} = 48V$

GaN-based 48V DC-DC

Available since 2022

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Stage 2b: $V_{in} = 4.5 - 5V$

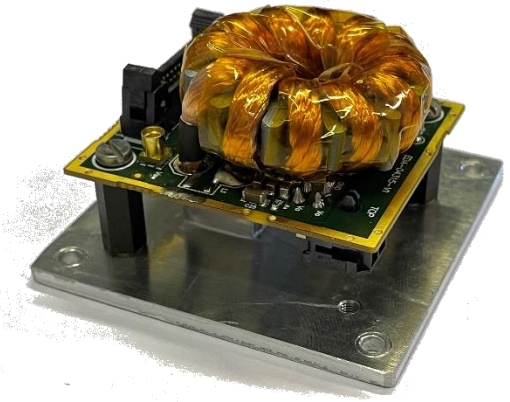
iPOL5V
Fully-integrated resonant converter
(28 nm CMOS)

$0.8V - 1V, 0.5A$

In production

R&D

WP5.4 – bPOL48V: 48V-INPUT BUCK DC-DC CONVERTER



Project started in early 2020. bPOL48V is composed by:

- a commercial Gallium Nitride (GaN) power stage EPC2152
- a rad-hard controller designed by CERN in the HV-CMOS OnSemi I3T80 technology

In production!
Current possible big customers:

- ATLAS Lar calorimeter (~20k reserved)
- Space industry

The OnSemi I3T80 fab is now closed!
>20k controllers remain available in stock.

⇩

R&D devoted to finding a HV technology for long-term availability of the controller

Specs	Vin	15-48V
	Vout	0.75-24V (Vout/Vin must be > 1/20, min switch on time 40 ns)
	Iout max	12A
Radiation tolerance	TID max	228 Mrad
	SEE max	88 MeV/(mg/cm²)
	DD max	4e14 n/cm2 2.23e14 p/cm2(30MeV)

TID=Total Ionizing Dose
SEE= Single Event Effect
DD= Displacement Damage

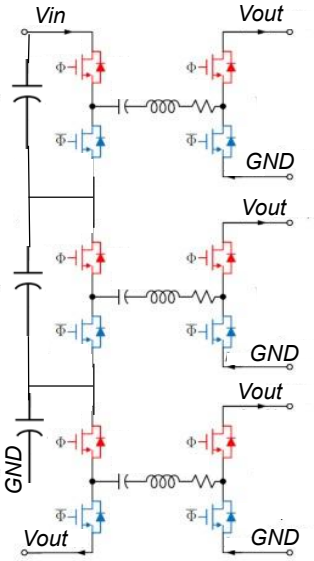
WP5.4 – iPOL5V: 5V-INPUT RESONANT DC-DC CONVERTER

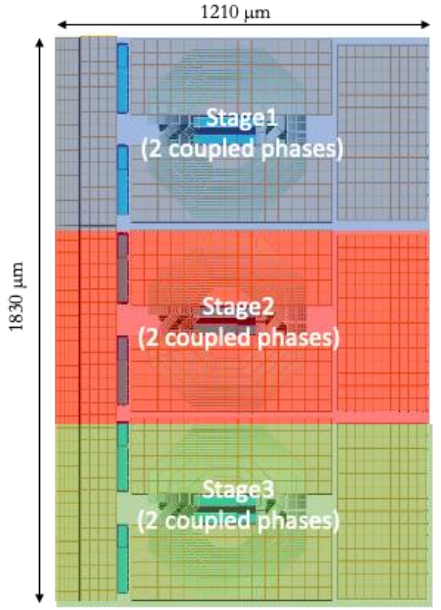
iPOL5V is a **fully integrated** resonant DC-DC converter developed in a 28 nm CMOS technology that can be integrated as a Macro Block in more complex ASICs (e.g. PicoPix).
R&D has started in Q4, 2021.

The target V_{out} is $0.9 - 1V$, with a tentative maximum current of $500\ mA$.

Added value:

- ultimate solution for low mass: no external components
- unprecedented radiation hardness for DC-DC converters: target TID tolerance is 1 Grad
- large reduction of input current (factor ≈ 4)
- a fully integrated solution relaxes the PCB design





Design started, submission of the first prototype in Q2 2023.
A full PicoPix could be powered by parallelizing several iPOL5V cells.

THANKS!

WP 5 – *IC Technology* - *Leaders: K. Kloukinas, D. Ceresa (Deputy)*

WP 5.1 – *Technology Evaluation*

Team: G. Borghello, D. Ceresa, F. Piernas Diaz, R. Pejasinovic

WP 5.2 – *IP block development*

Team: R. Ballabriga, F. Bandi, M. Piller, T. Hoffman

WP 5.3 – *Rad-Tol SOC development*

Team: M. Andorno, A. Caratelli, D. Ceresa, J. Dhaliwal, K. Kloukinas, R. Pejasinovic.

WP 5.4 – *Powering solution*

Team: S. Michelis, G. Ripamonti, P. Antoszczuk, G. Bantemits, N. Van Der Blij

ASIC Support – *Technology support*

Team: M. Andorno, W. Bialas, A. Caratelli, K. Kloukinas,.

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THANKS!

DAVIDE CERESA