EP R&D WP5
extension proposal

CERN EP R&D Day 2023

20 February 2023

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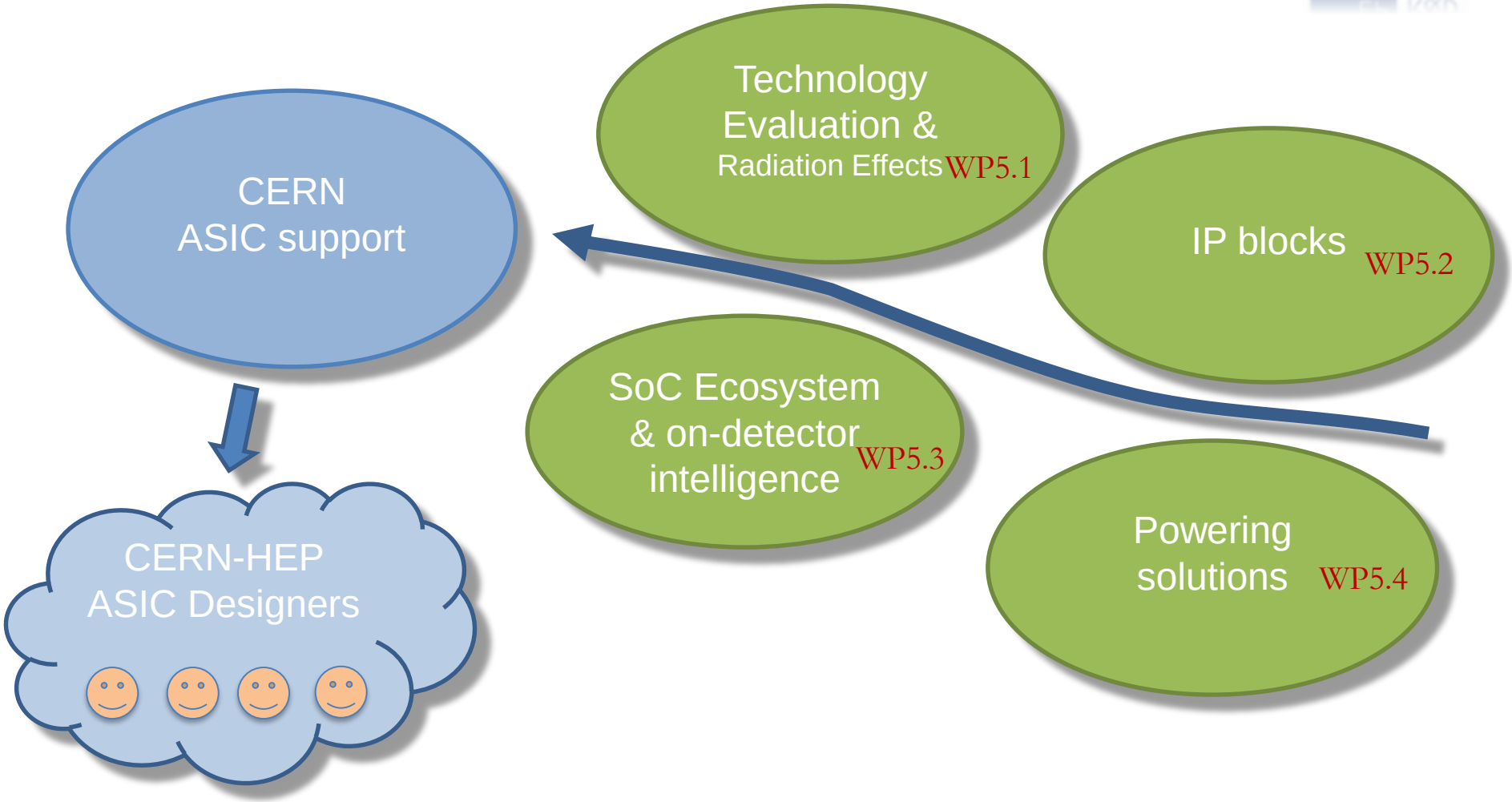
Davide Ceresa

on behalf of the EP R&D WP5

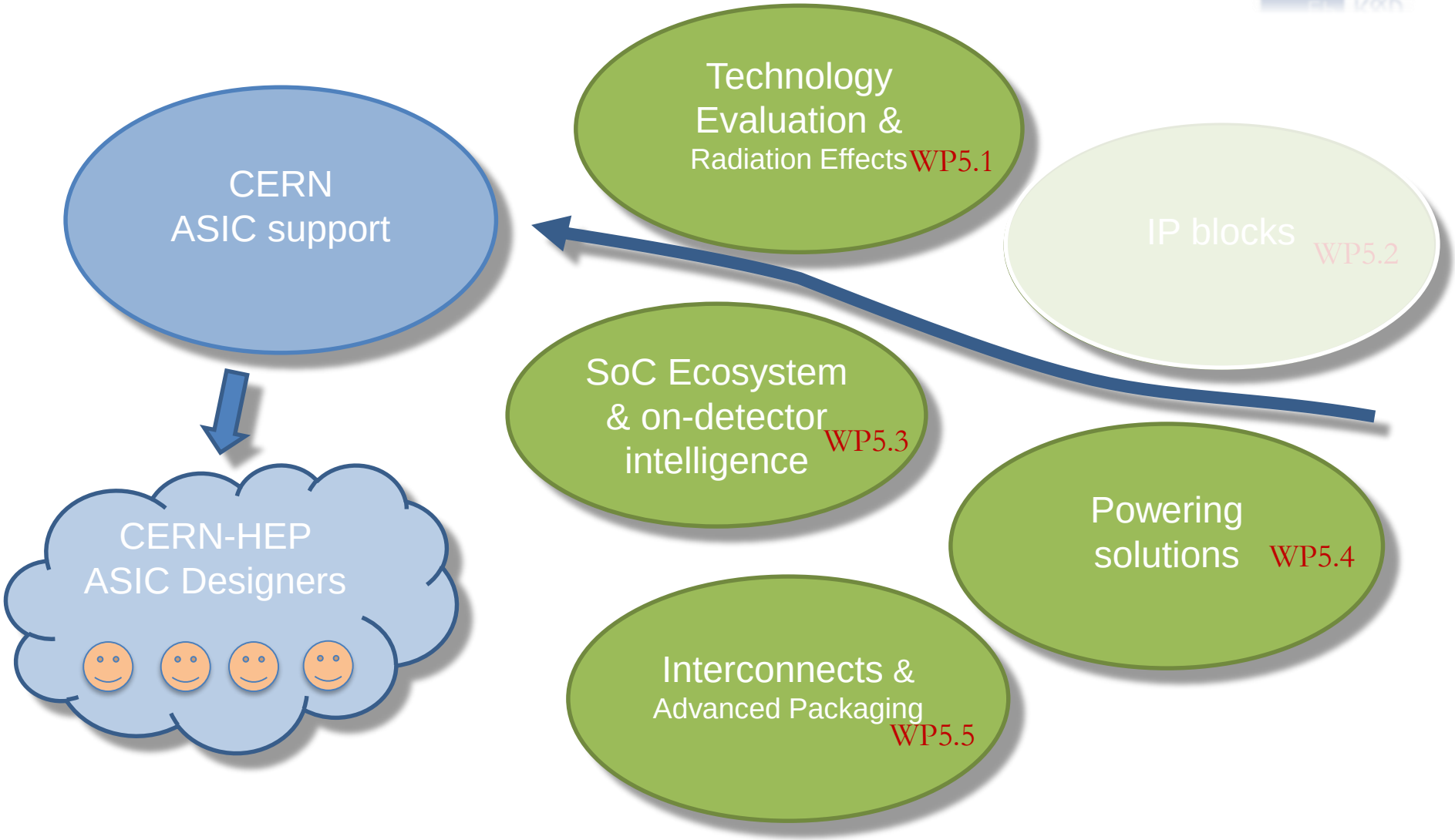
WP5 2020-2024

WP 5
EP R&D



WP5 2024-2028

WP 5
EP R&D



Technology Evaluation

- Technology survey and evaluation
  - Maintain activity but at a slower pace
  - Advanced processes; access and evaluation
    - FinFET (radiation evaluation)
    - FD-SOI (non Rad-Tol applications
      - Collaborating with external institute
  - Specialty Technologies; evaluation, customized developments
    - RRAM
    - MRAM
    - Ultra low leakage SRAM

Budget request: 120 kCHF
Recourses request

(FTE)	Fellows	Students
year 1	0	1
year 2	0	1
year 3	0	1
year 4	0	1
year 5	0	0

IP Blocks

- Rad-Tol IP blocks on 28nm bulk CMOS technology
  - Expect to complete and deliver all IP blocks by 2024-25
  - Maintain IP block repository by CERN ASIC support service
  - No further IP block development is foreseen within the EP R&D WP5
  - HEP community is invited to contribute with IP blocks

Budget request:
Recourses request

(FTE)	Fellows	Students
year 1	0	0
year 2	0	0
year 3	0	0
year 4	0	0
year 5	0	0

SoC & Data Processing

2024-2028 WP 5.3

WP 5 EP R&D

TWO COMPLEMENTARY R&D ACTIVITIES:

CONTROL & MONITORING

RISC-V BASED

- STANDARDIZED SOLUTION
- OPEN SOURCE
- FULLY RADIATION TOLERANT
- ECO SYSTEM OPEN TO HEP THE COMMUNITY
  - RT SOC IP BLOCKS
  - RT SOC INTERCONNECT

Stand alone applications of Control & Monitoring

IP blocks to support the implementation of Data Processing applications

DATA PROCESSING

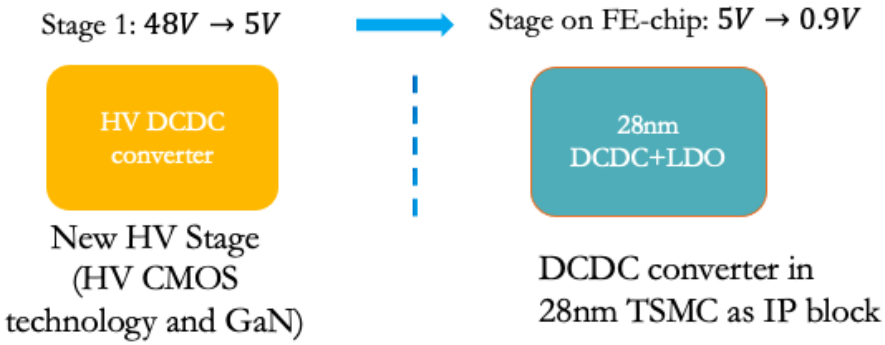
ASIP BASED

- APPLICATION SPECIFIC INSTRUCTION SET PROCESSOR
- COMMERCIAL TOOL – ASIP DESIGNER BY SYNOPSIS
- CUSTOM ISA
- CUSTOM MICROARCHITECTURE

Budget request: 500 kCHF
Recourses request

(FTE)	Fellows	Students
year 1	1	2
year 2	2	3
year 3	2	3
year 4	2	3
year 5	1	1

Powering Solutions



Slide by: S. Michelis

Stage 1: 48V → 5V

Find a new CMOS HV technology (old one no longer available)
Explore the new upcoming GaN commercial technologies
} Full radiation characterization (TID, DD, SEE)

Find a suitable architecture for this high conversion ratio with main specification
low volume, low noise, high efficiency, higher radiation hardness (bPOL48 only rated up to 5e14 n/cm2)

Power module design: provide to the experiment a small and optimized "brick"
with all active and passive elements included.

Stage 2: 5V → 0.9V

Continue the recently started R&D activity to:

- reach production readiness
- improve the design for a modular approach where designers can easily connect blocks for higher output current (>3A)
- design a linear regulator from 5V → 0.9V - 1.2V necessary for some I/O pads
- explore derived topologies for higher output voltages

Budget request: 340 kCHF

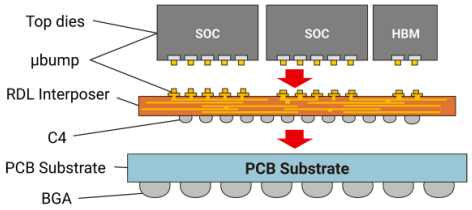
Recourses request

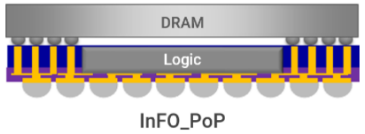
(FTE)	Fellows	Students
year 1	0	0
year 2	1.5	0
year 3	2	0
year 4	2	0
year 5	1	0

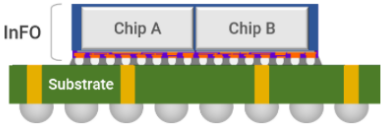
Interconnects & Packaging

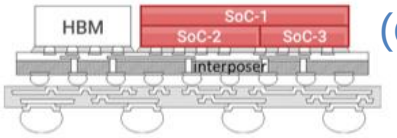
2024-2028 WP 5.5 EP R&D WP 5

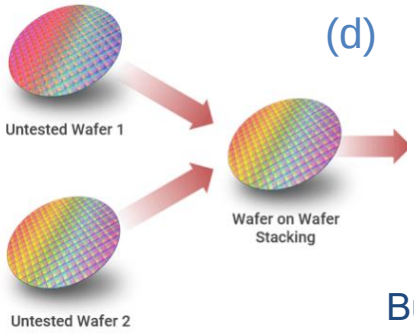
- Advanced packaging & 3D Interconnects
  - Technology survey, access and evaluation
    - Silicon Interposer (a)
    - Wafer Level Packaging & TSVs (b)
    - Chip on Wafer (c)
    - Wafer on Wafer (d)
  - Enabler for many applications
    - Hybrid detectors
    - Si Photonics
  - Timeline
    - Phase A
      - Identify industrial collaborators
      - Comparison between the 'third-party' and 'turn-key' approaches
    - Phase B
      - Invest R&D funds to test the viability of the technologies
      - Test vehicle ASICs (ex. TimePix4)











Budget request: 1'150 kCHF

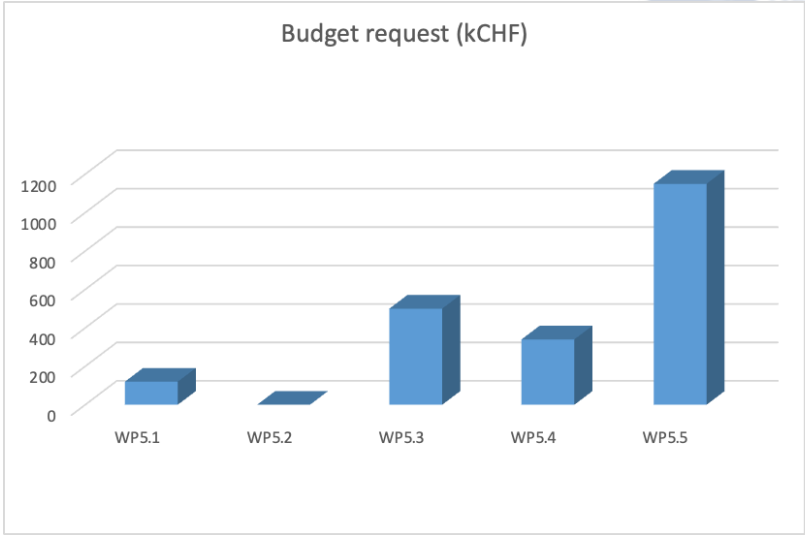
Recourses request

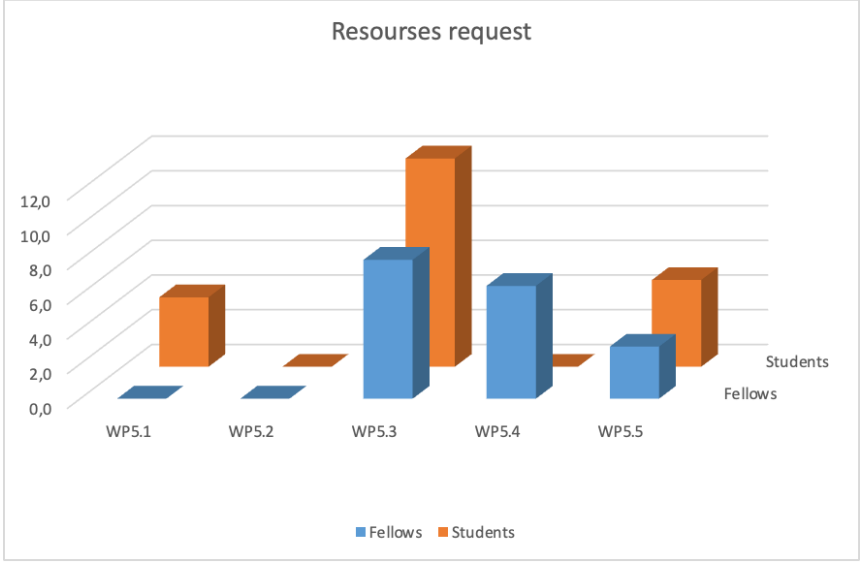
(FTE)	Fellows	Students
year 1	0	1
year 2	1	1
year 3	1	1
year 4	1	1
year 5	0	1

Budget & Resources

- Total Budget: 2,110 kCHF
- Total Recourses (2024-28)
  - Fellows: 16,5 (17,5)*
  - Students: 17 (21)*

** including 2024 top up*





Coherence with ECFA roadmap

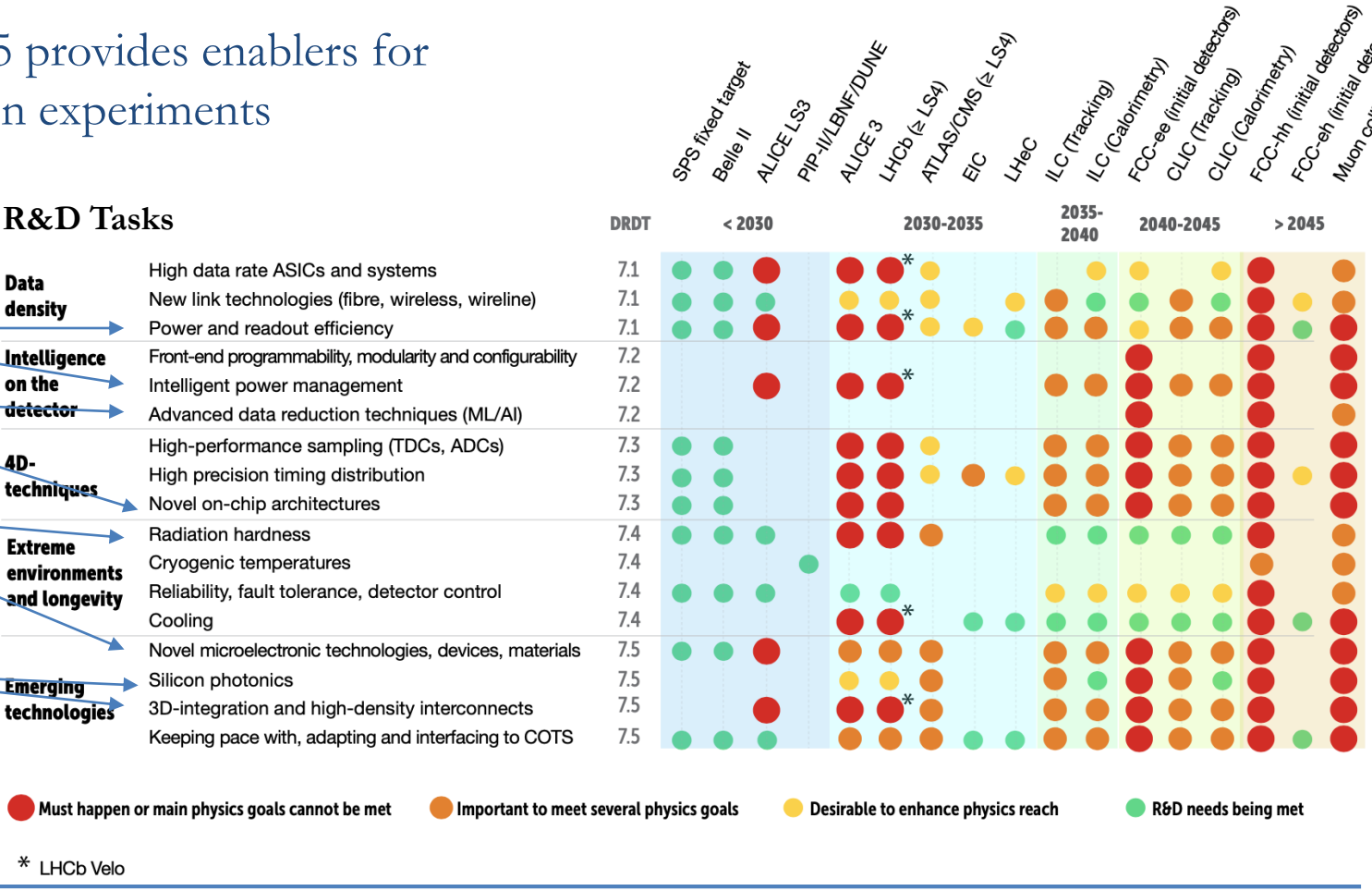
WP 5 EP R&D

2021 ECFA DETECTOR RESEARCH AND DEVELOPMENT ROADMAP
Chapter 7 Electronics and Data Processing

"near-future" experiments "further-future" colliders

EP R&D WP5 provides enablers for next generation experiments

WP5.4
WP5.3
WP5.1
WP5.5



Coherence with ECFA roadmap

- Technology Choice
  - The selection and adoption of the 28nm CMOS technology as a “mainstream” process will ”fuel” the developments of *”near-future”* experiments
  - *“Further-future”* collider experiments would require more advanced technologies offering the necessary combination of performance, power efficiency and radiation hardness
    - R&D on future state-of-the-art IC technologies would be necessary
- Infrastructure and Organizational issues
  - Common Design Platforms & Collaborative Framework
- ASICs evolution and front-end “intelligence”
  - Data processing adaptable to changing experimental conditions
  - Programmability to facilitate retargeting ASIC blocks to different applications
  - Present R&D on core-based SoC design topologies and methodologies will be applicable in “near-future” experiments as well as **pave the way** for the electronics of “further-future” colliders
- Power distribution
  - Stagged voltage conversion, multiple supply voltages, intelligent power management
- Advanced packaging and 3D interconnects
  - Emerging technologies in industry providing enablers in many applications for HEP detectors


Thank You

SoC developments

WP 5.3

WP 5 EP R&D

- System-on-Chip Radiation Tolerant Ecosystem (SoCRaTEs)
  - Rad-Tol open-source Risc-V based core & interconnect infrastructure
  - Rad-Tol peripherals
  - Rad-Tol embedded FPGA (eFPGA); commercial or open-source based
  - Rad-Tol non-volatile memories (NV-RAM); commercial or open-source based
- Control & Monitoring applications
  - Rad-Tol Microcontroller style implementations
- On-Detector data processing applications
  - Modeling & Simulation
    - Simulation Framework development; Front-End to Back-End
  - Application Specific Implementations
    - Rad-Tol processing Cores
    - Rad-Tol Network on Chip
    - Rad-Tol Neural Networks
- Radiation Tolerance evaluation of SoC components