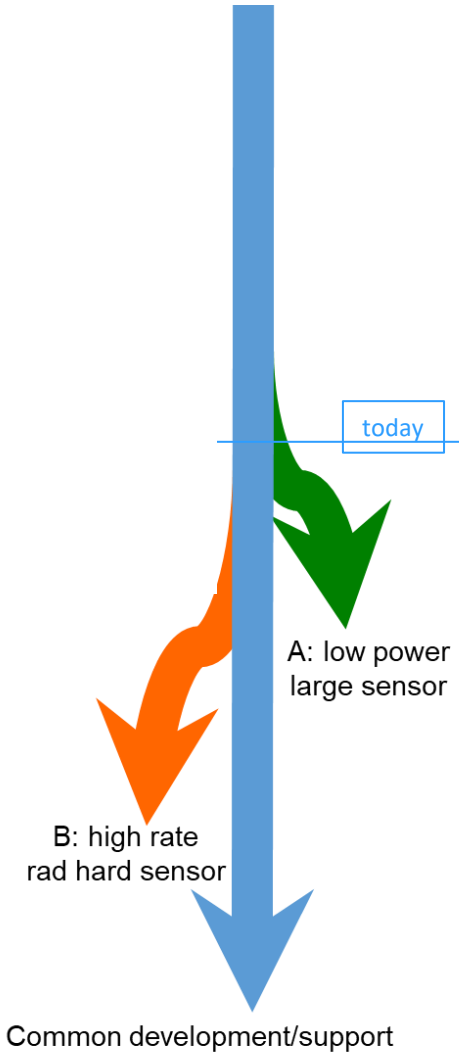
WP1.2 Monolithic Pixel Detectors

- Gianluca Aglieri, Federico Faccio, Walter Snoeys, Francois Vasey, Pedro Vicente Leitao on behalf of the EP R&D WP1.2 team

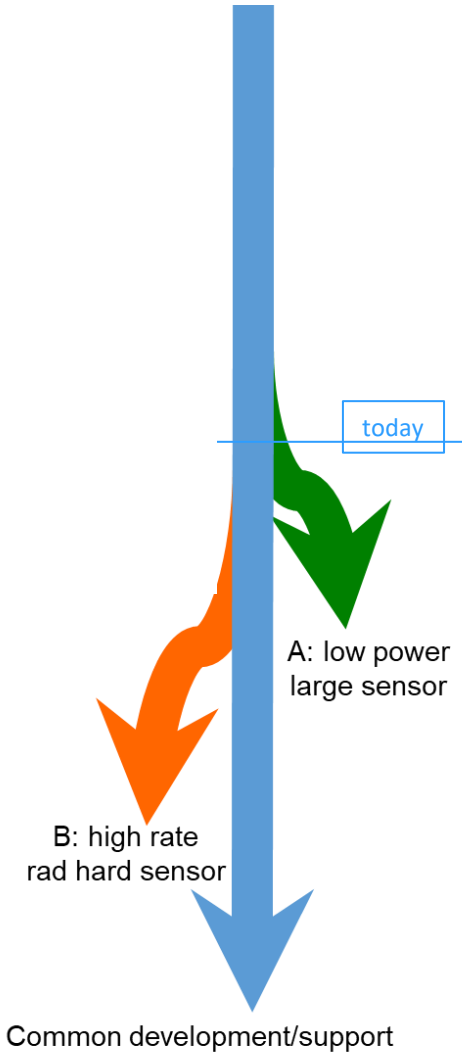
- The work presented here benefited from massive contributions from the ALICE and monolithic CMOS sensor communities

WP1.2 Timeline, Scope and Results



Time	*Scope*	*Submissions TPSCo ISC 65nm*
Phase I 2020-21	Technology Test structures Collaboration Framework	**MLR1** Dec20
Phase II 2021-22	Technology iterations Test demonstrators Dissemination	**ER1** Nov22
Phase III 2023-24	Technology iterations Full chips	**ER2** Exp. 2024
		MLR2

WP1.2 Timeline, Scope and Results



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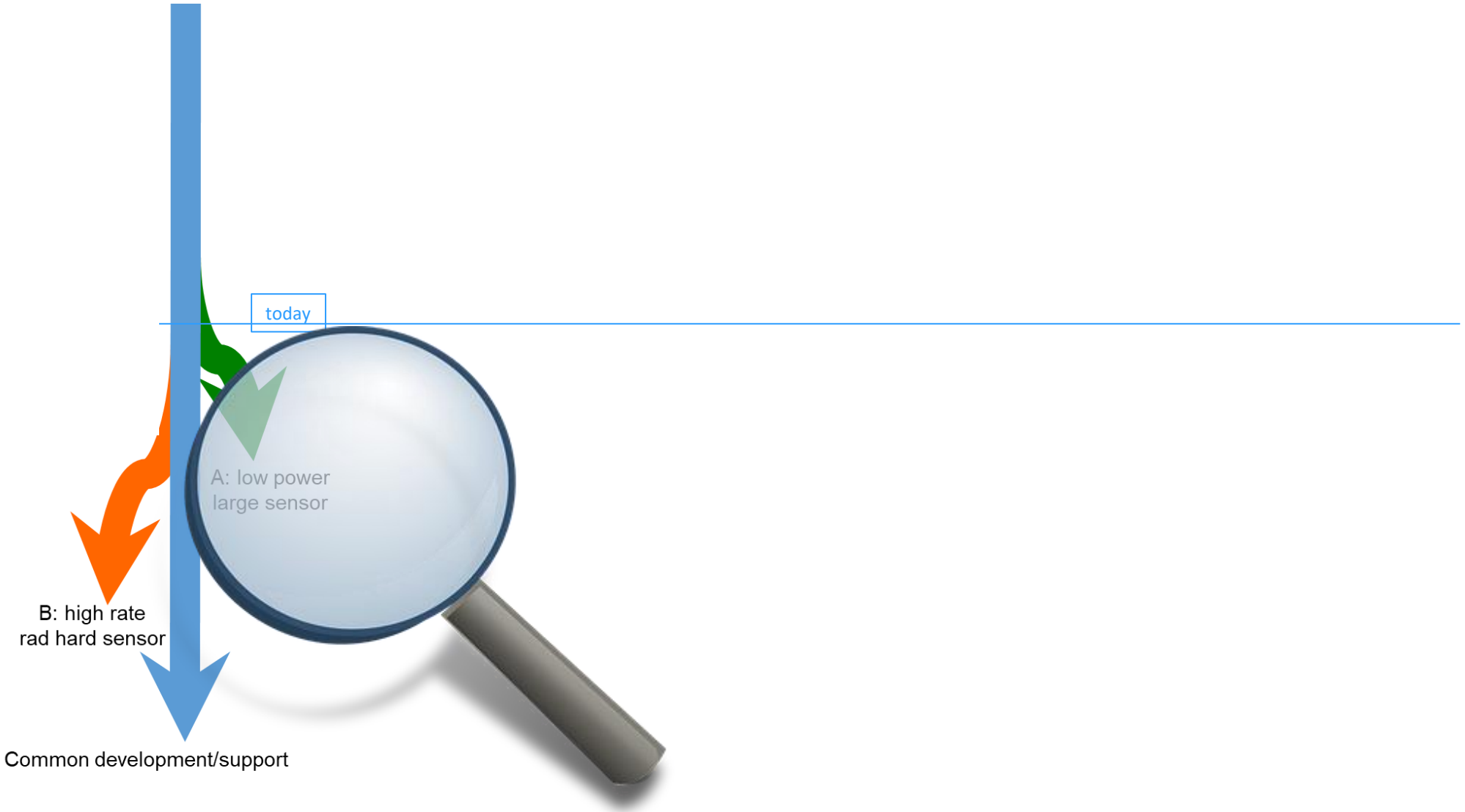
		MLR2

Walter: The ISC65 technology promise

Pedro: Getting ready for ER1-Silicon

Francois: Addendum to WP1.2 project workplan

WP1.2 Moving beyond Phase II



EP R&D WP1.2

ALICE ITS3

2022

Sensor A (Alice ITS3) | **Common Development / Support**

Design

MOSS → ER1 ← MOST Chiplets (H2M, MacroBlocks, Others)

Design

WP1.2 Phase II

WP1.2 Phase III.A

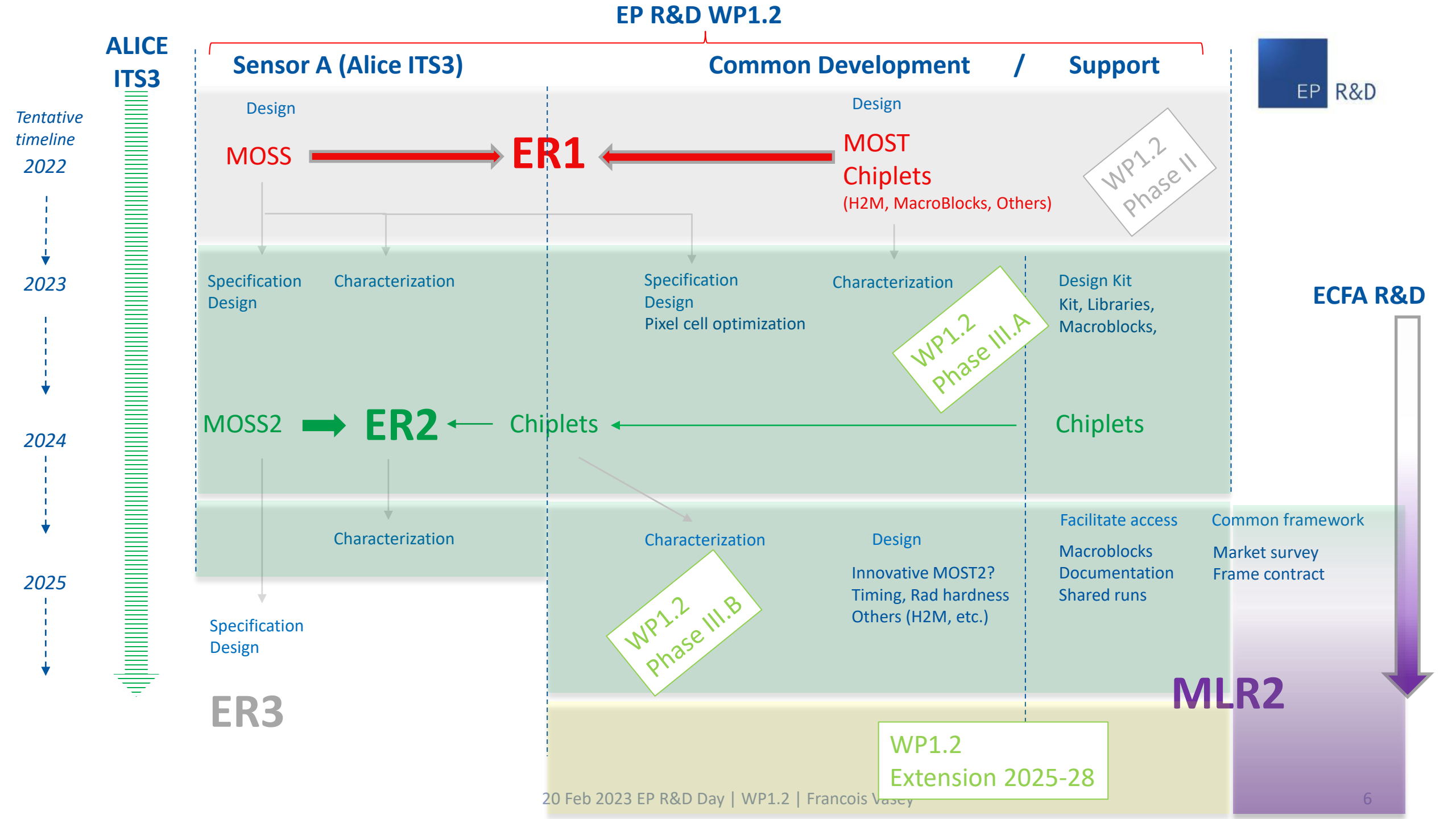
Must focus effort on

- *Characterization of ER1 chips*
- *One single design and submission (Alice ITS3) within ~12-18 months: ER2*
  - *Develop design flow and libraries*
  - *Implement 2D stitching, pixel cell optimization, digital periphery, clock & power distribution*
  - *Fully functional wafer-scale chip*

WP1.2 Phase III.B

Must focus effort on

- *Characterization of ER2 chips and harness results from ER1*
- *Implementing framework for future shared run*
- *Designing and submitting chiplets on shared run: MLR2*
- *Aligning with ECFA*


EP R&D WP1.2
ALICE ITS3
Sensor A (Alice ITS3)
Common Development / Support
EP R&D
Tentative timeline
2022
2023
2024
2025
Design
MOSS
ER1
Design
MOST Chiplets
(H2M, MacroBlocks, Others)
WP1.2 Phase II
Specification
Design
Characterization
Specification
Design
Pixel cell optimization
Characterization
WP1.2 Phase III.A
Design Kit
Kit, Libraries,
Macroblocks,
ECFA R&D
MOSS2
ER2
Chiplets
Chiplets
Characterization
Characterization
Design
Innovative MOST2?
Timing, Rad hardness
Others (H2M, etc.)
Facilitate access
Macroblocks
Documentation
Shared runs
Common framework
Market survey
Frame contract
WP1.2 Phase III.B
Specification
Design
ER3
MLR2
WP1.2
Extension 2025-28

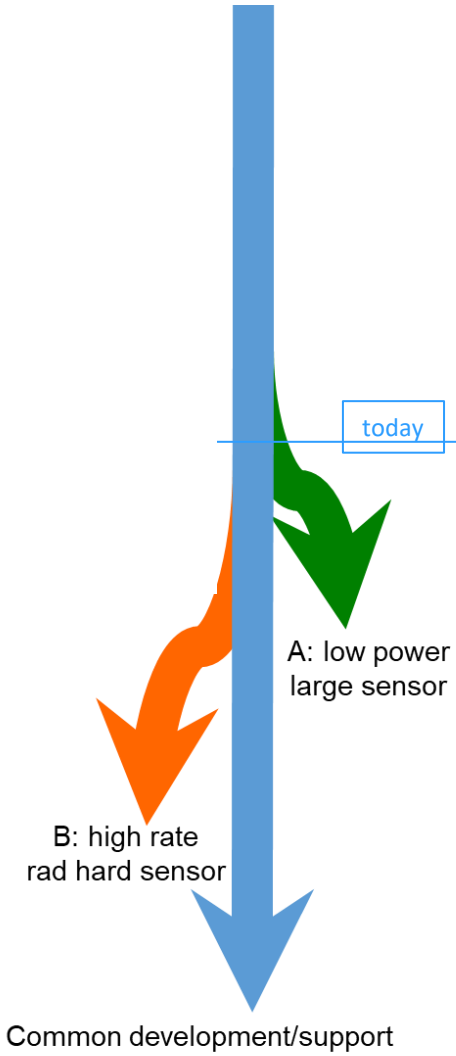
WP1.2 Extension beyond Phase III: 2025-2028

- Draft proposal in progress

- Baseline programme:
  - Test
    - Comprehensive test of all material from ER2 and successive MLR runs
    - In tight collaboration with Alice, community and EP R&D WP1.4
  - Design
    - Two MLR shared runs in 2025 and 2027 (MLR2 and MLR3)
    - Explore radiation resistance limits, power efficient designs, scalability to large detector surfaces, …
  - Establish a common framework in one technology (TPSCo-ISC65)
    - Frame contract, PDK and libraries, MPW runs, Macroblocks

- Coordination with ECFA Detector R&D Theme (DRDT) on monolithic detectors
  - EP R&D WP1.2 will contribute:
    - With relevant parts of the baseline program highlighted above
    - By possibly joining, as an opportunity to diversify, DRDT collaboration active in other promising areas

WP1.2 Timeline, Scope and Results



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Walter: The ISC65 technology promise

Pedro: Getting ready for ER1 S...icon

Submissions

TPSCo ISC 65nm

MLR1 Dec20

ER1 Nov22

ER2 Exp. Q1-2024

MLR2

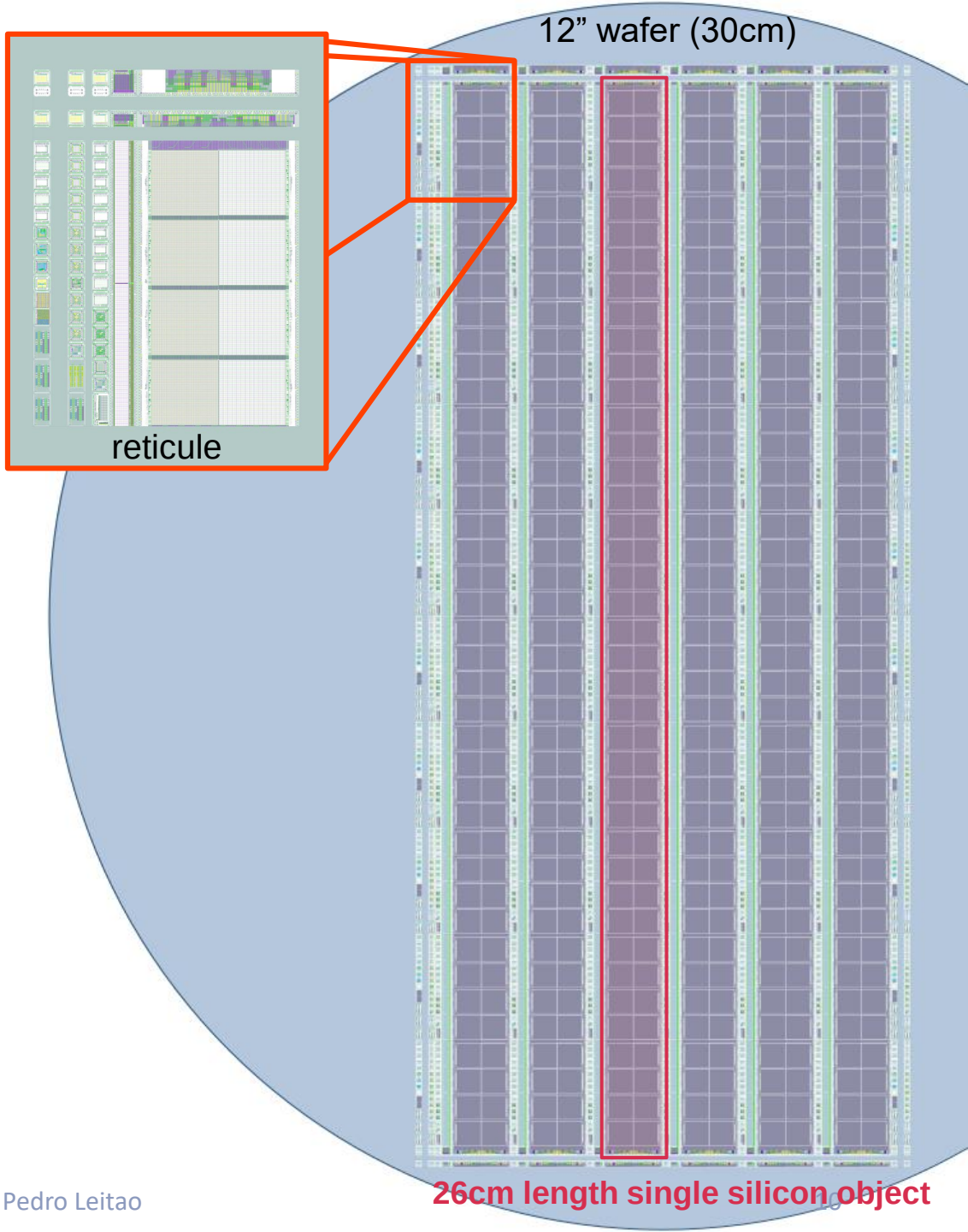
MLR1 & ER1 Executive summary

- MLR1 submission (tapeout December 2020)
  - All chips and pixel prototypes are functional
  - Technology characterized for HEP
    - Similar performance & radiation hardness for the transistors and CMOS circuitry as other 65nm techs
  - Pixel prototypes are being characterized in detailed (Walter will discuss selected results)
- ER1 submission
  - Shift of focus towards stitching
  - Tapeout in November 2022
  - Expecting 24 wafers to arrive end of April 2023
- Next
  - Thinning, dicing and assembly of stitched chips and chiplets on carriers / test systems
  - Development of HW/FW/SW for testing
  - Design for ER2 submission

MLR1 & ER1 already introduced in the last EP R&D Day, https://indico.cern.ch/event/1156197

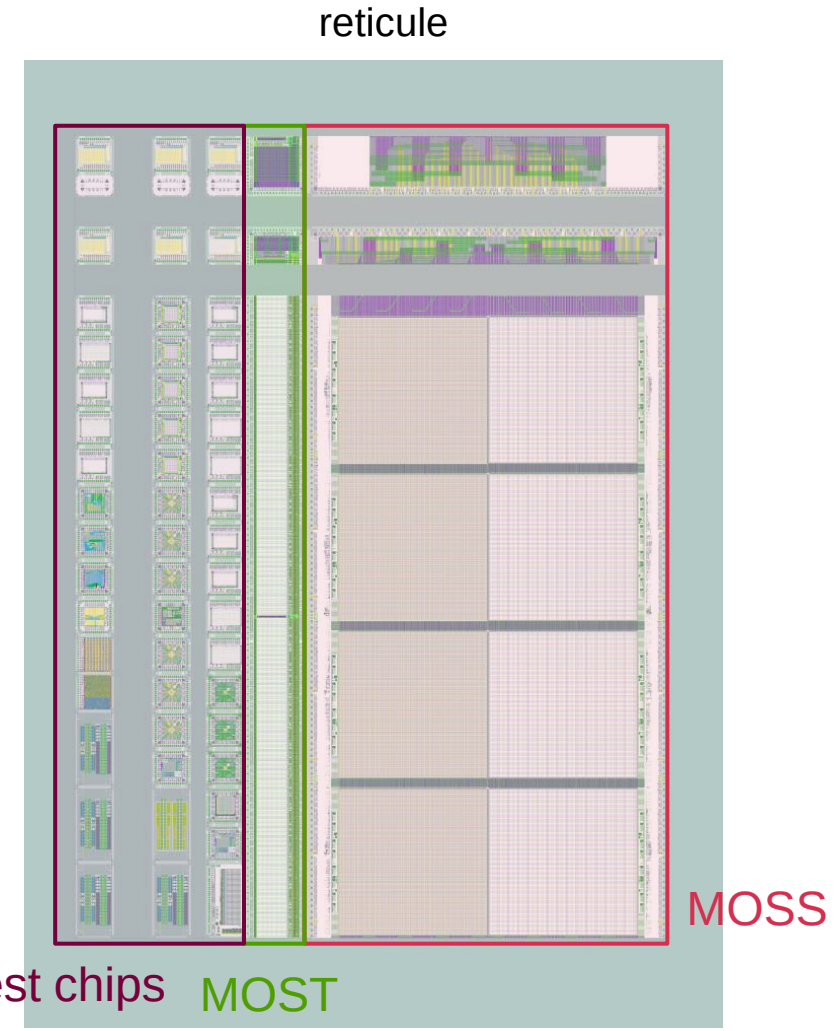
ER1 summary

- What is the ER1 submission objective?
  - The goal is to prove that we can design wafer scale pixel detectors
    - Learn stitching techniques
    - Interconnects
    - Learn about yield, design for manufacturing (DFM) and defects masking
    - Study power schemes, leakage, spread, noise and speed
    - Develop methodology



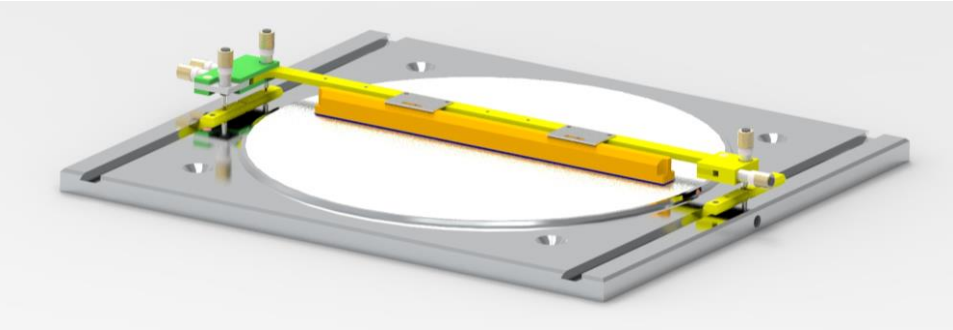
ER1 Executive summary

- Features two stitched sensor chips
  - MOSS chip (1.4 x 26 cm, 6x per wafer)
    - Conservative layout (DFM rules), Alpide-like readout scheme with 1/20 power segmentation
  - MOST chip (0.25 x 26 cm, 6x per wafer)
    - High local density with higher power gating granularity to mitigate faults, async hit driven readout
- Features 51/reticule chiplets for prototyping
  - PLL, pixel prototypes, fast serial links, SEU test chips, ...
- Technology and support development
  - New metal stack: new I/Os, PDK, DDK, DRC deck
  - Custom DRC/LVS rule deck
  - Custom DFM standard cell library implemented
  - Setup of a legal and contractual framework
  - Develop wafer assembly and signoff methodology



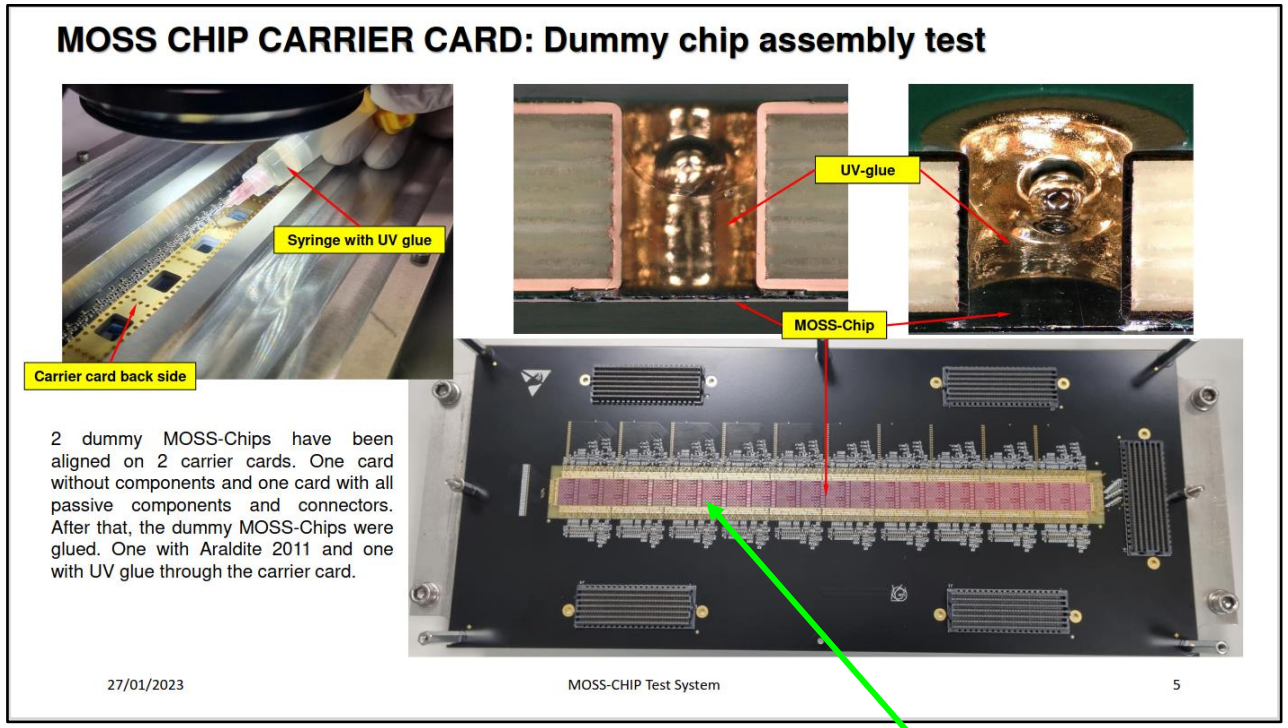
ER1 testing preparation

- Significant effort by ALICE and other groups
- Testing developments ongoing for both stitched chips
  - MOSS: dummy chip assembly tests
  - MOST: hardware and mechanical handling
- Most chiplets are tested by their home institutes



R. Barthel/M. Rossewij
MOST testing preparation

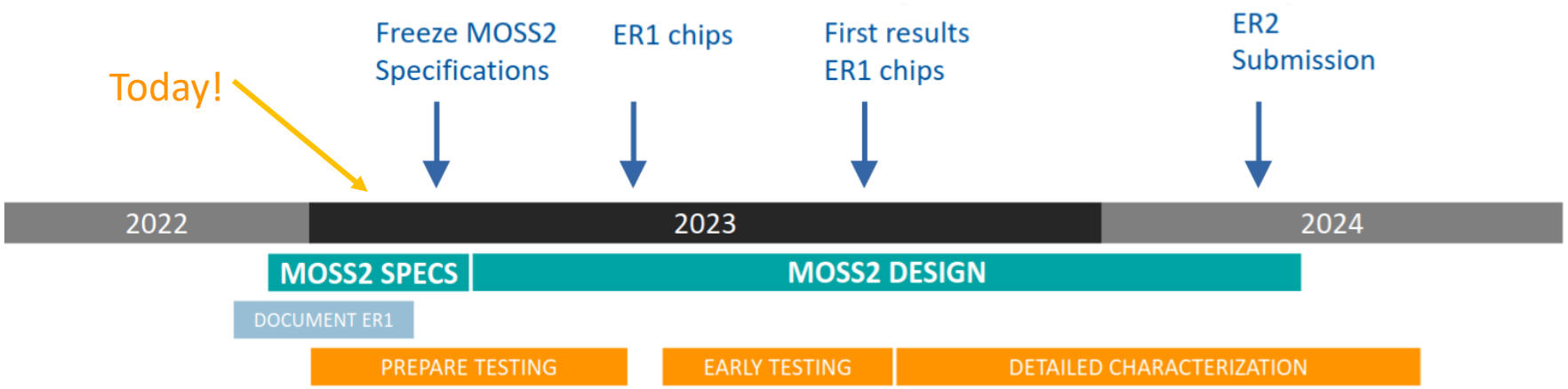
A. Junique
https://indico.cern.ch/event/1244919



Single 1.4 x 26 cm silicon die glued and bonded on carrier

Towards ER2 submission

- ER2 submission will focus on a large area stitch sensor that targets the ALICE ITS3 requirements
  - Build on ER1 learned lessons
  - Increased dimensions (1.8 x 26 cm)
  - Decreased dead area (between 6.7% - 9.5%)
  - Increased readout speed (between 25.6 Gbps – 51.2 Gbps)
  - On chip power regulation for power segmentation and IRdrop compensation (~0.6% active area granularity)
- Design specifications are ongoing



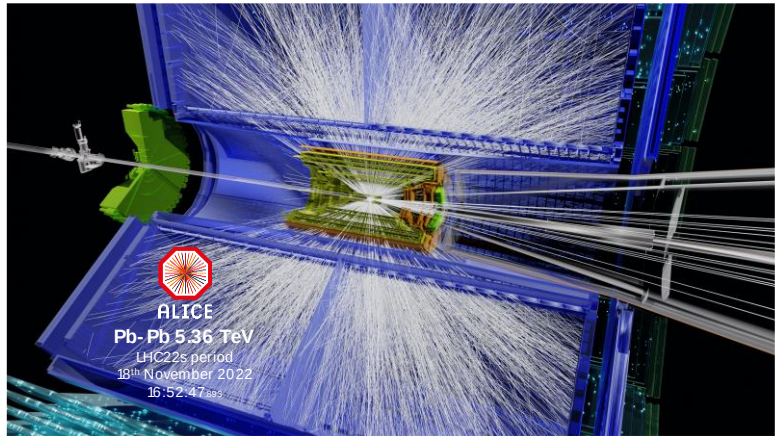
Test results in 65 nm TPSCo

Summary and outlook

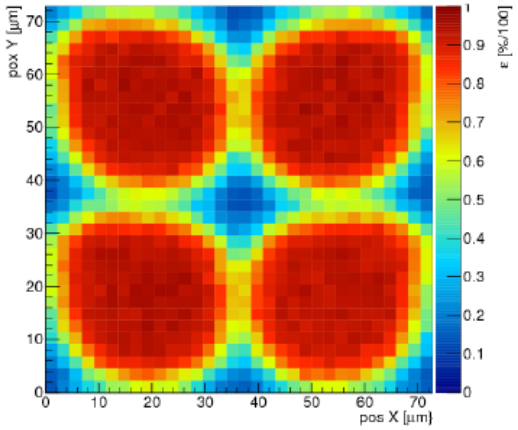
Massive effort from many people

Pixel optimization in 180 nm (started in 2012)

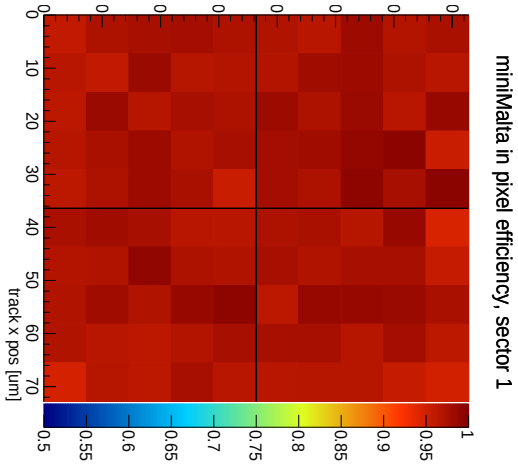
efficiency loss at ~ 10^{15} 1 MeV n_{eq}/cm^2



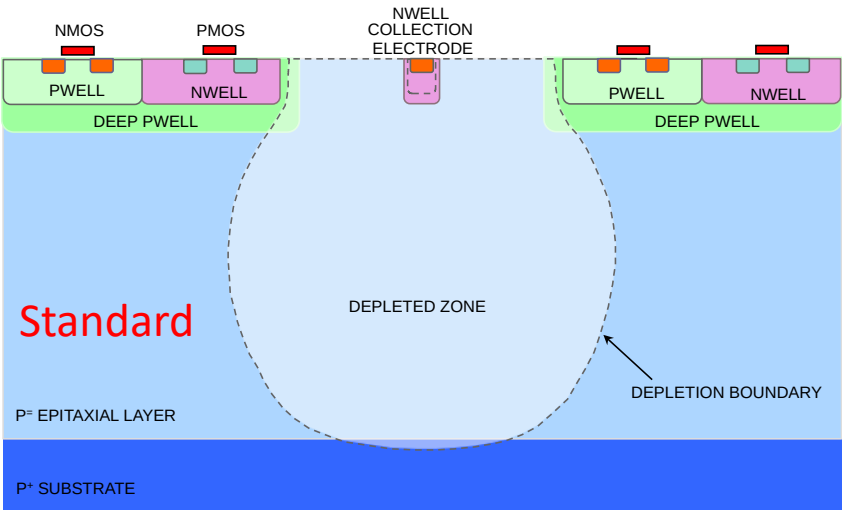
ALPIDE and ITS2 in ALICE (10 m^2)

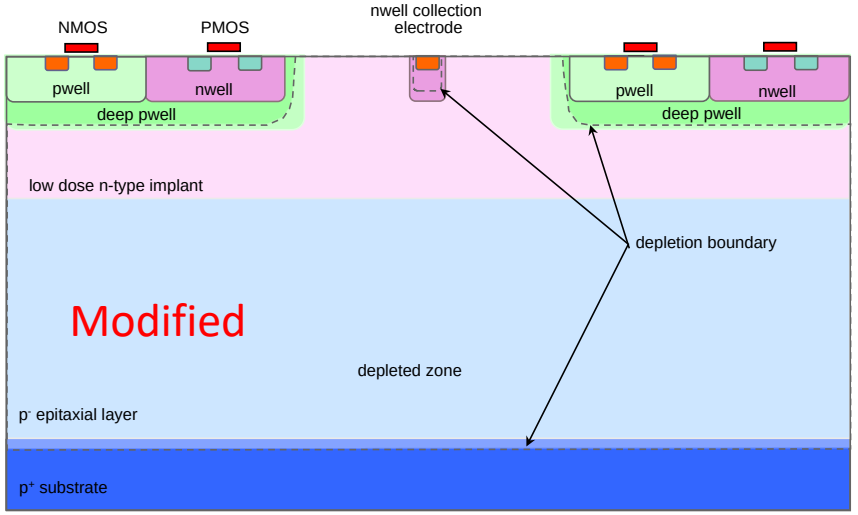


E. Schioppa et al, VCI 2019

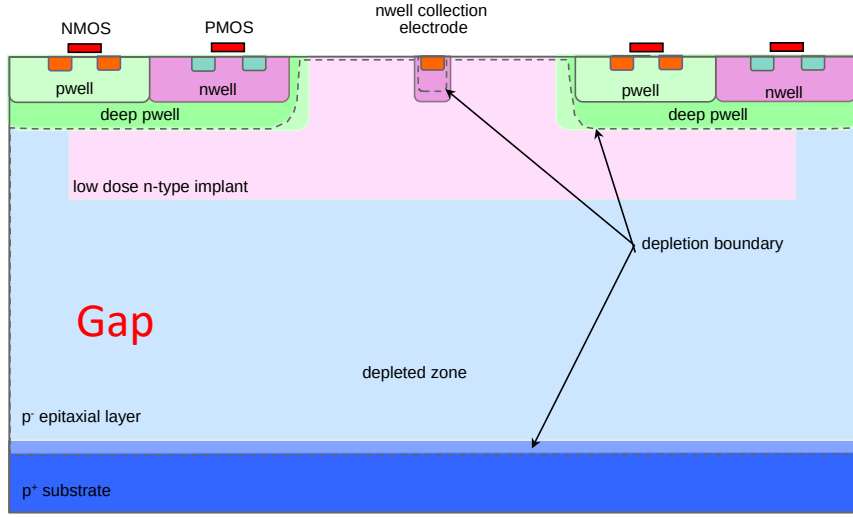


H. Pernegger et al., Hiroshima 2019, M. Dyndal *et al* 2020 *JINST* **15** P0200





https://doi.org/10.1016/j.nima.2017.07.046 (180nm)



https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013 (180nm)

Charge collection speed

Charge sharing

Moving to deeper submicron CMOS

First technology selected: TPSCo 65 nm ISC

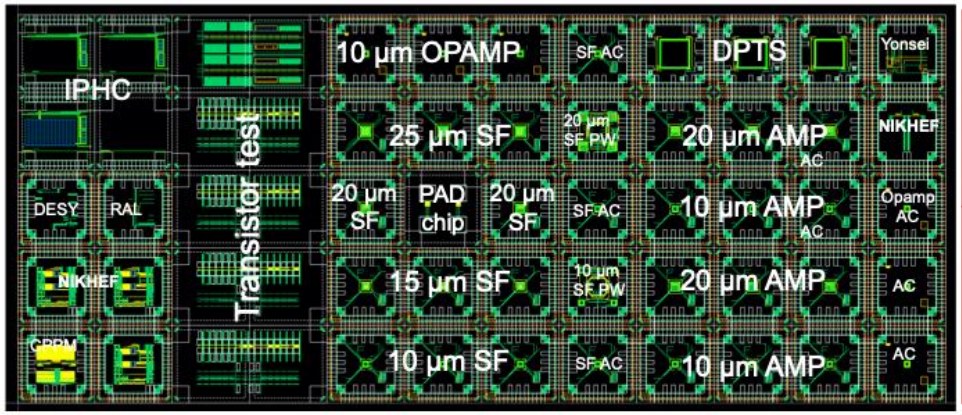
- TPSCo (joint venture TJ & Panasonic): several 65 nm flavors: high density logic, RF, and imaging (ISC)
- ISC preferred: 2D stitching experience, special sensor features, different starting materials, lower defect densities, etc
- Initially 5 metal layers, now 7 metals

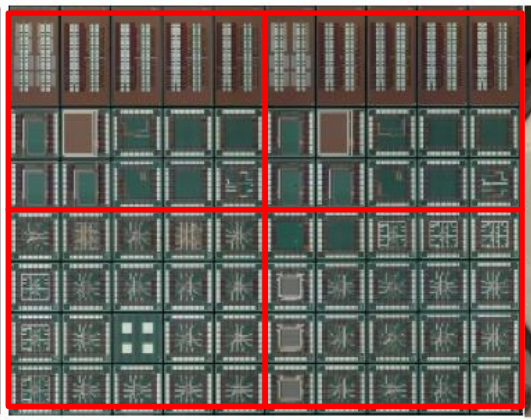
First submission: Multi Layer per Reticle MLR1

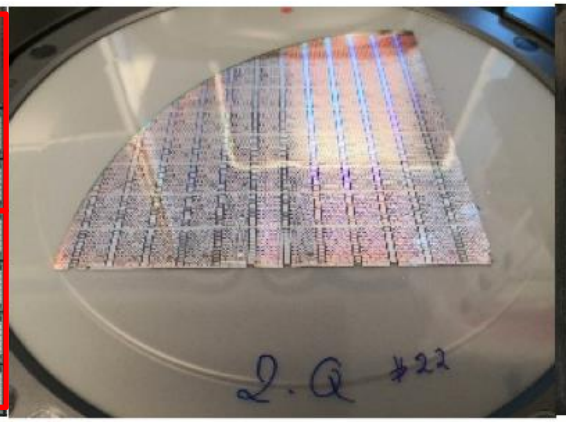
- Significant contribution from outside groups (from ALICE but not only) to design and test (!), also financially
- Many test chips of 1.5 x 1.5 cm^2 or twice that size.
- GDS submitted Dec 1, 2020, chips ready to test, Sept, 2021

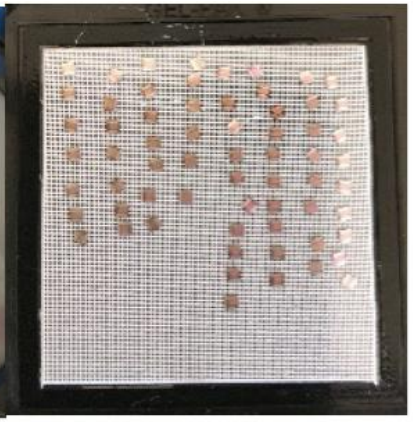
Second submission: Stitched engineering run ER1 see Pedro's presentation

- Two stitched sensors, MOSS and MOST and many test chips of 1.5 x 1.5 cm^2 or twice that size
- Back end of April

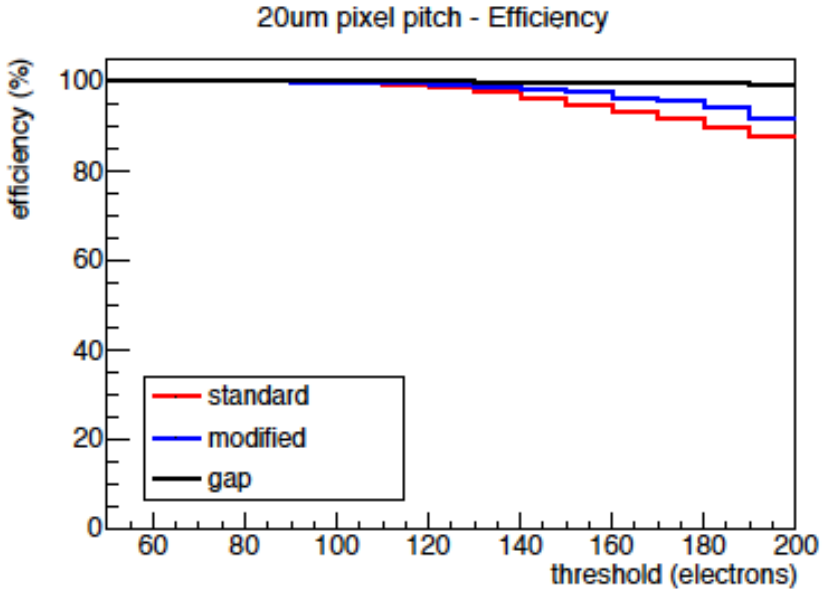


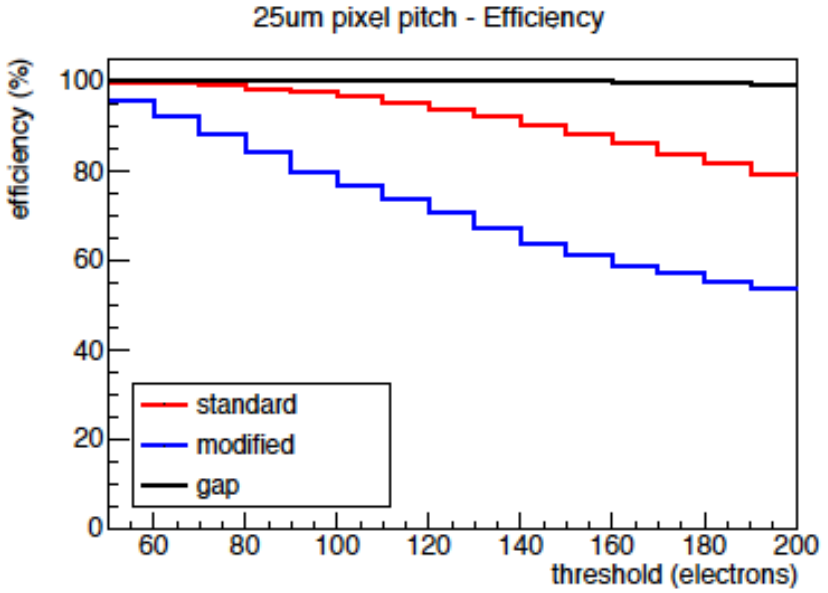


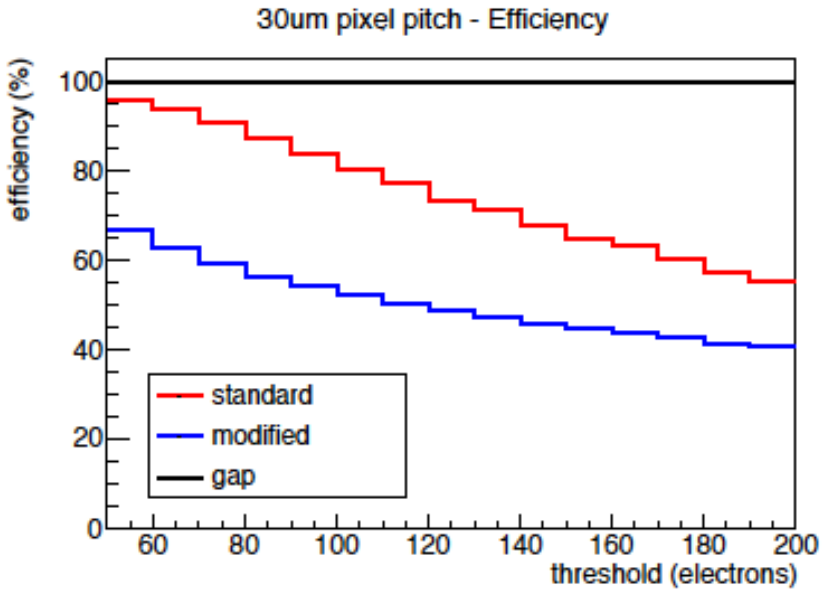


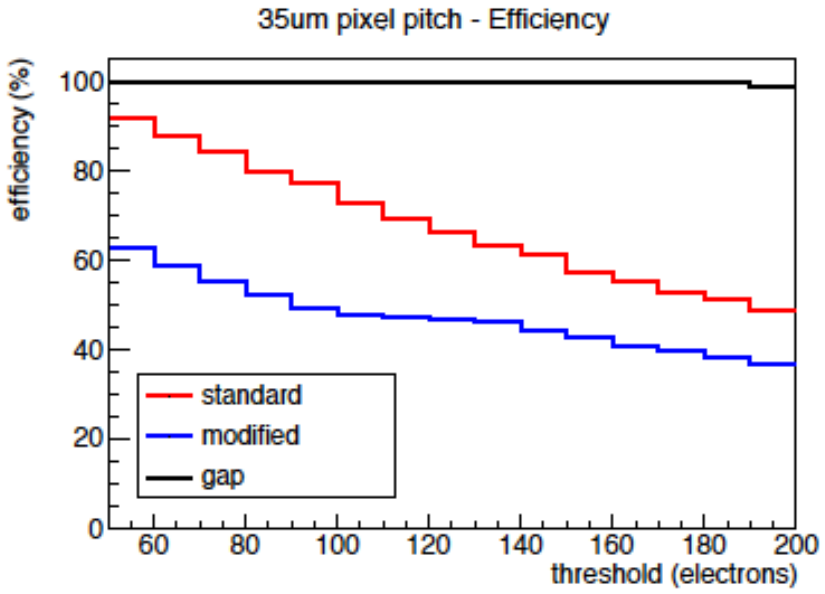


Moving to 65 nm: apply same principles as in 180 nm









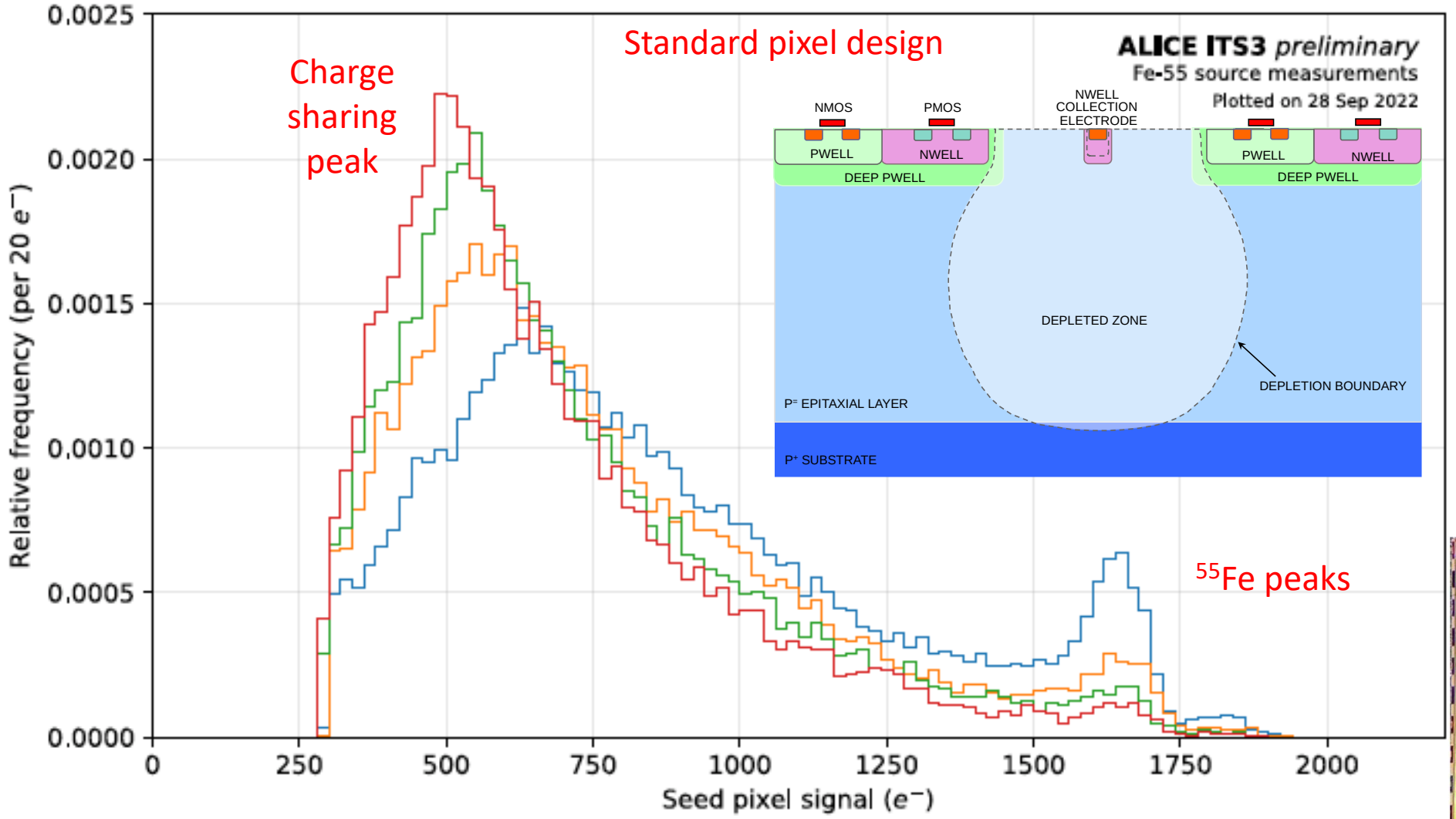
Simulations by J. Hasenbichler

Different pixel flavors varying the pixel pitches also to larger values

Only gap maintains reasonable efficiency

^{55}Fe: pitch dependence for different variants

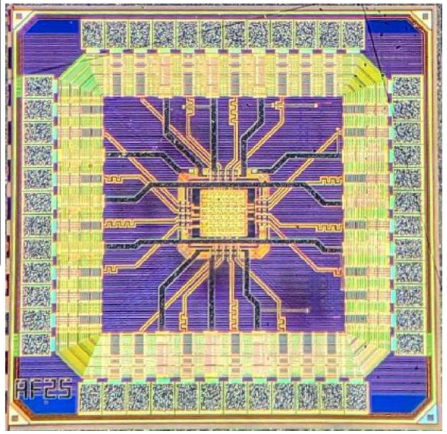
See also: I. Sanna IEEE NSS 2022



APTS SF
type: standard
split: 4
$V_{sub} = V_{pwell} = -1.2$ V
$I_{reset} = 100$ pA
$I_{biasn} = 5$ µA
$I_{biasp} = 0.5$ µA
$I_{bias4} = 150$ µA
$I_{bias3} = 200$ µA
$V_{reset} = 500$ mV

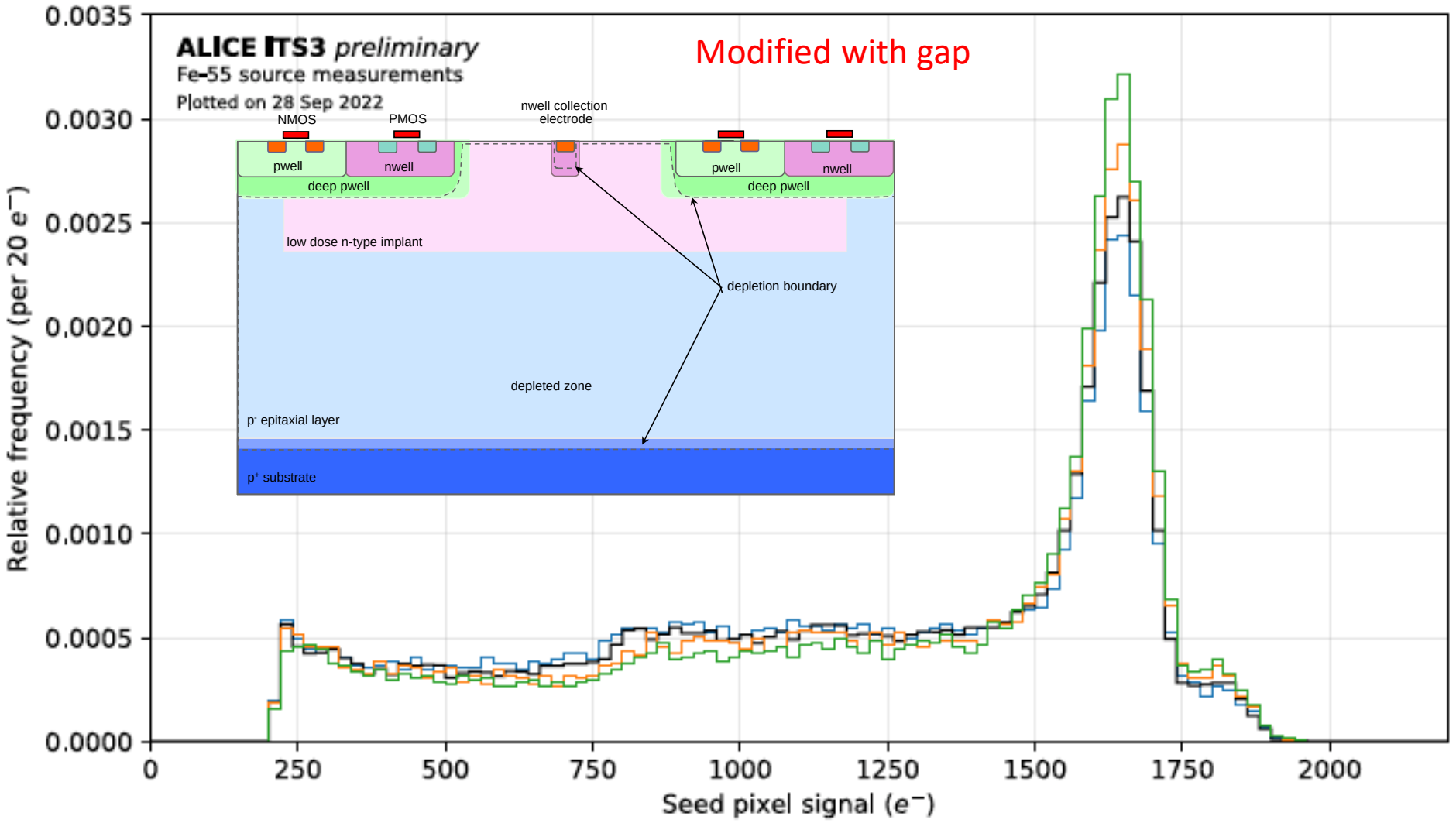
pitch = 10 µm
pitch = 15 µm
pitch = 20 µm
pitch = 25 µm

APTS SF



^{55}Fe: pitch dependence for different variants

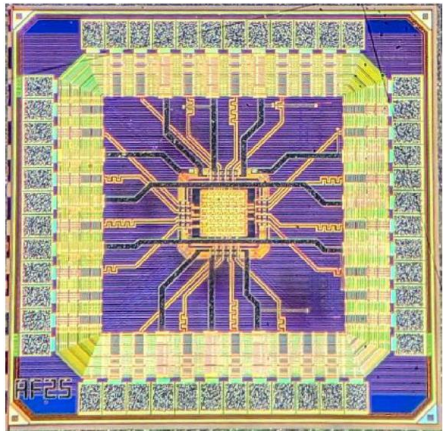
See also: I. Sanna IEEE NSS 2022



APTS SF
type: modified with gap
split: 4
$V_{sub} = V_{pwell} = -1.2\,V$
$I_{reset} = 100\,pA$
$I_{biasn} = 5\,\mu A$
$I_{biasp} = 0.5\,\mu A$
$I_{bias4} = 150\,\mu A$
$I_{bias3} = 200\,\mu A$
$V_{reset} = 500\,mV$

pitch = 10 µm
pitch = 15 µm
pitch = 20 µm
pitch = 25 µm

APTS SF



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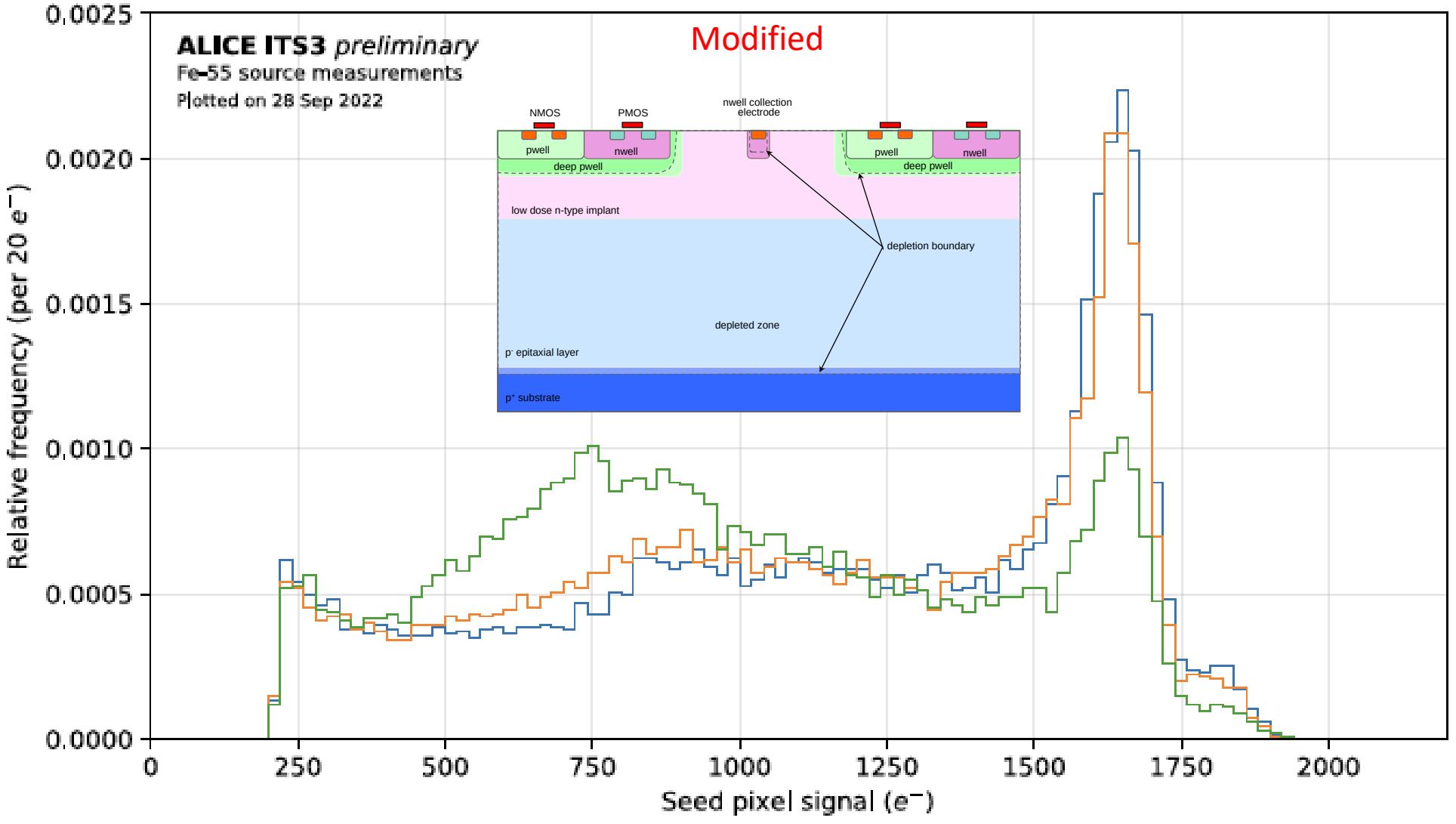
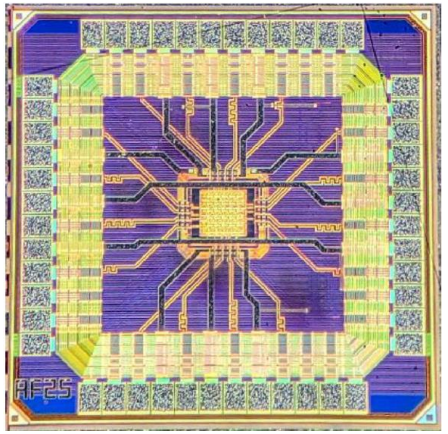


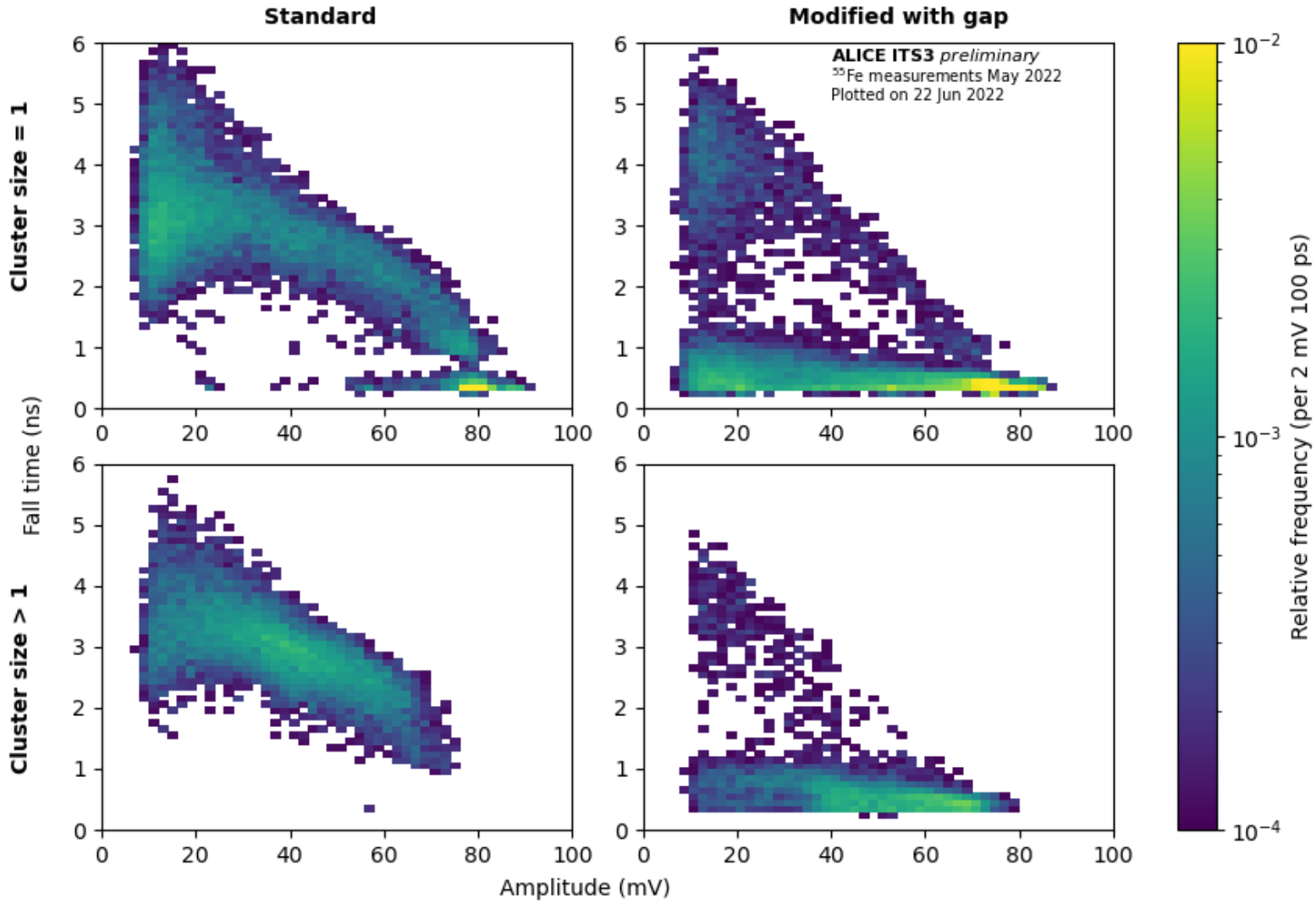
APTS SF
type: modified
split: 4
$V_{sub} = V_{pwell} = -1.2$ V
$I_{reset} = 100$ pA
$I_{biasn} = 5$ µA
$I_{biasp} = 0.5$ µA
$I_{bias4} = 150$ µA
$I_{bias3} = 200$ µA
$V_{reset} = 500$ mV

pitch = 10 µm
pitch = 15 µm
pitch = 25 µm

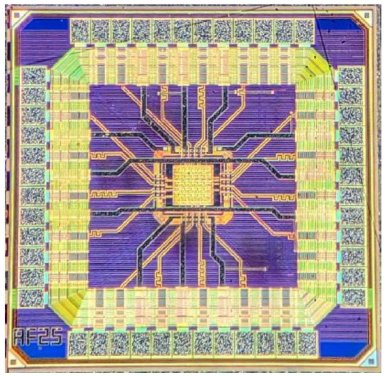
APTS SF



^{55}Fe measurements on Analog Pixel Test Structure Opamp



APTS OPAMP
pitch: 10 um
version: modified with gap
split: 4 (opt.)
$I_{biasp} = 10$ uA
$I_{biasn} = 75$ uA
$I_{bias3} = 200$ uA
$I_{bias4} = 2.5$ mA
$I_{reset} = 100$ pA
$V_{reset} = 350$ mV
$V_{casp} = 300$ mV
$V_{casn} = 750$ mV
$V_{pwell} = V_{sub} = -4$ V
T = ambient



Clusters of various sizes show distinct time and charge distributions

Illustrates impact of pixel design and process modifications on the charge collection

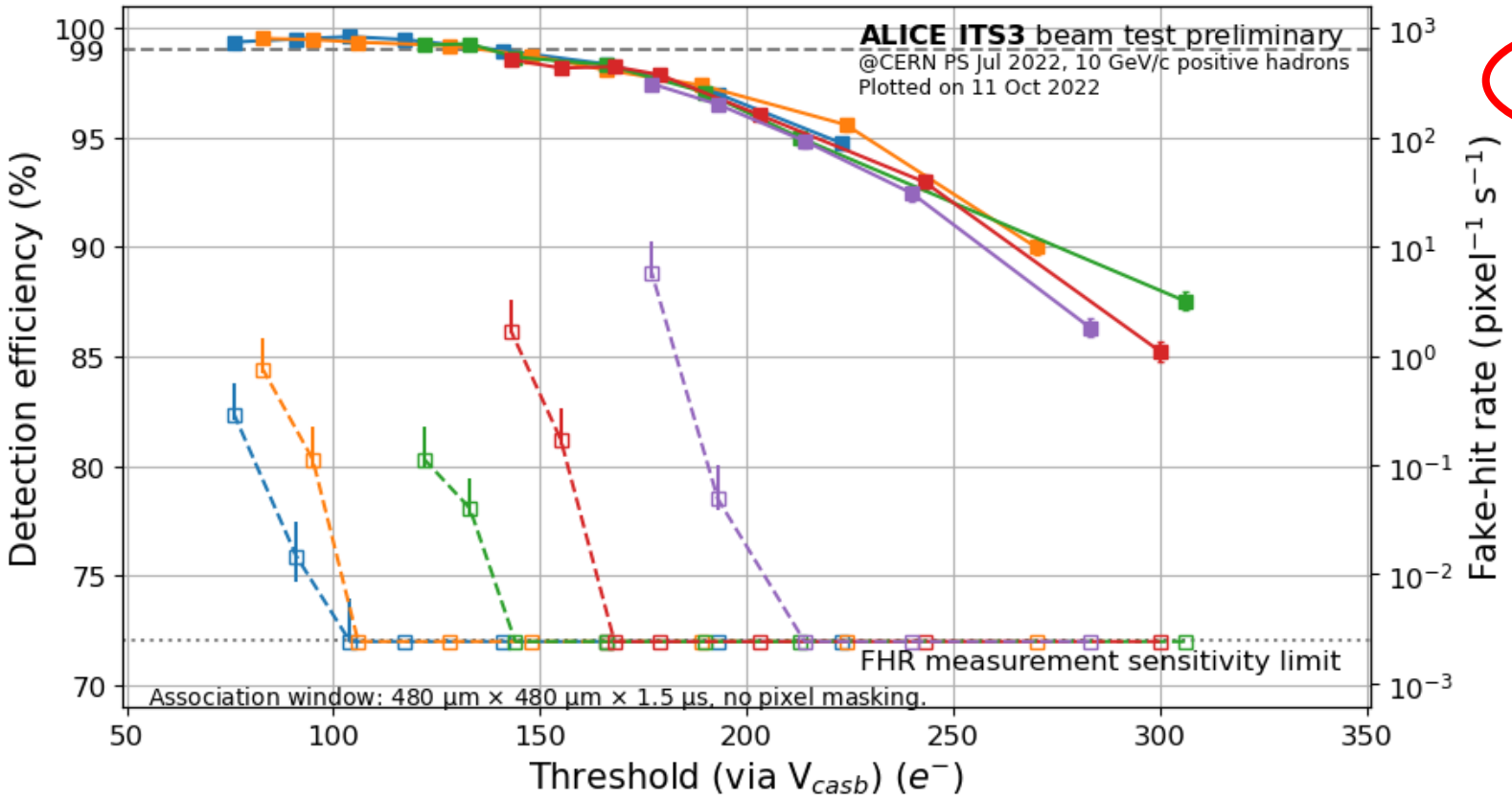
Sensor timing is at present under study with two APTSOA in coincidence (!).

In 180nm better than 150 ps*, expect improvement in 65 nm

*Fastpix :https://www.mdpi.com/2410-390X/6/1/13
J. Braach, E. Buschmann, D. Dannheim et al.

C. Ferrero et al

Detection efficiency/Fake hits for ITS3

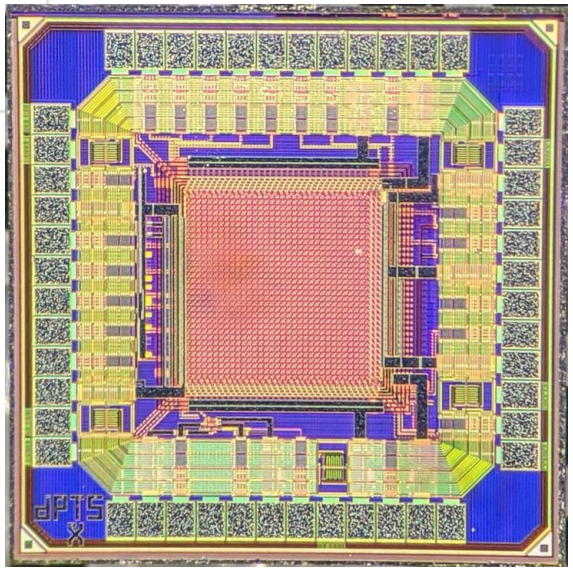


DPTSOW22B3
TID + NIEL,
10 kGy + 10^{13} 1MeV n_{eq} cm^{-2}
version: O
split: 4 (opt.)
I_{reset} = 35 pA
I_{bias} = 100 nA
I_{biasn} = 10 nA
I_{db} = 50 nA
V_{casn} = *variable*
V_{casb} = *variable*
V_{pwell} = V_{sub} = *variable*
T = 20 °C

Detection efficiency
Fake-hit rate
V_{sub}=-3.0 V
V_{sub}=-2.4 V
V_{sub}=-1.8 V
V_{sub}=-1.2 V
V_{sub}=-0.6 V

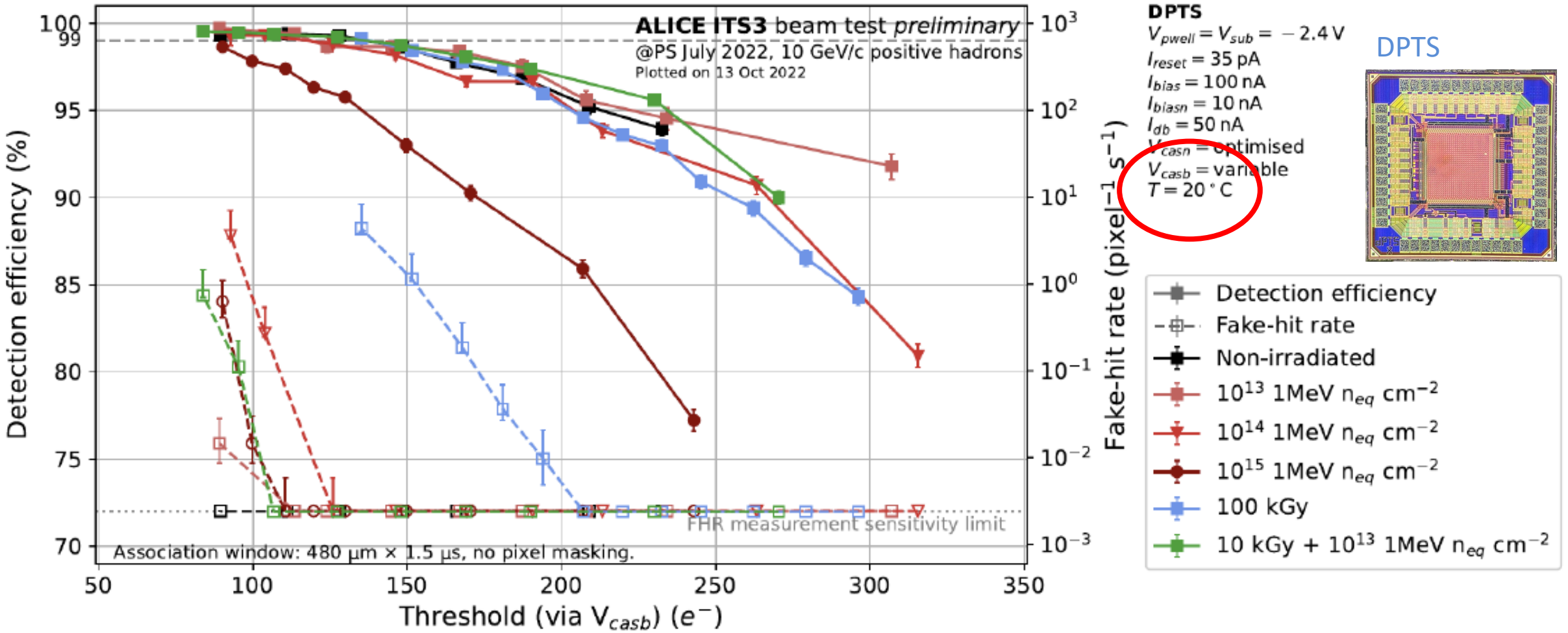
ITS3 specification

DPTS



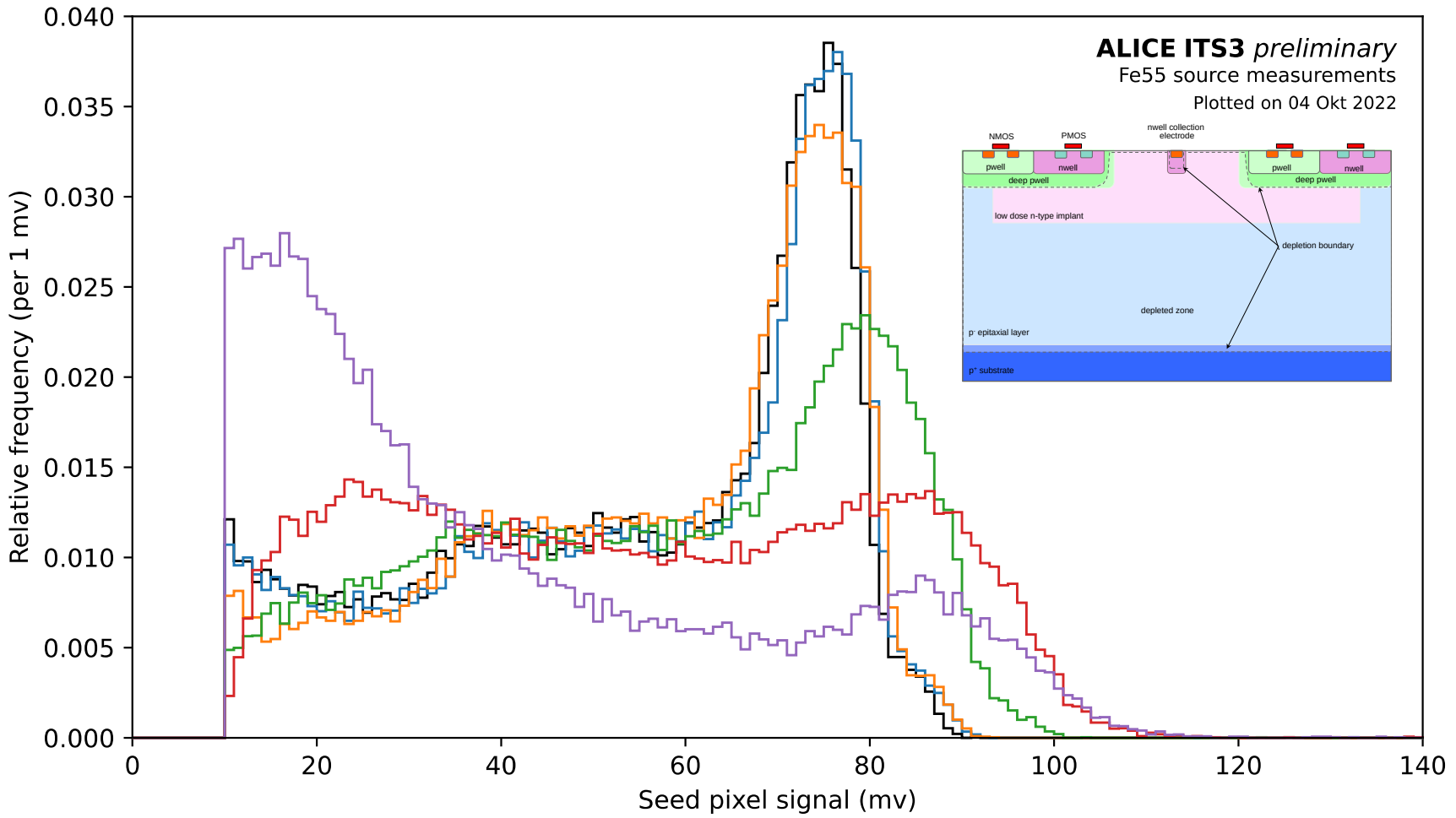
- Fully efficient chain of optimized sensor, analog front end, digital readout in 15 x 15 µm^2 pixel (DPTS)

~ 99 % efficiency at 10^{15} n_{eq}/cm^2 … at room temperature



- Fully efficient sensor, analog front end, digital readout chain in 15 x 15 µm^2 pixel (DPTS) including sensor optimization
- Circuit radiation tolerance TID in line with other 65 nm technologies (ringoscillators up to 25 % frequency degradation after ~800 Mrad)

Higher fluences (modified with gap)

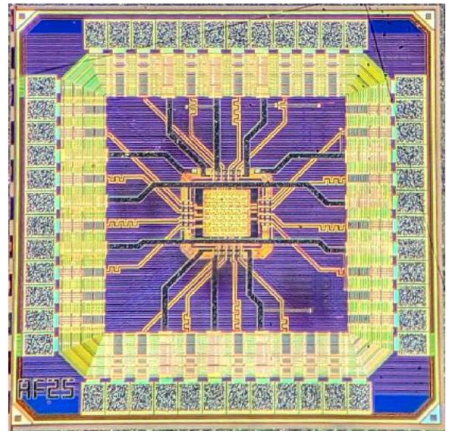


APTS SF
pitch: 15 µm
type: modified with gap
split: 4
$V_{sub} = V_{pwell} = -1.2\,V$
$I_{reset} = 250\,pA$
$I_{biasn} = 5\,\mu A$
$I_{biasp} = 0.5\,\mu A$
$I_{bias4} = 150\,\mu A$
$I_{bias3} = 200\,\mu A$
$V_{reset} = 500\,mV$
temperature = 14 °C

- Not irradiated
- 1e13
- 1e14
- 1e15
- 2e15
- 1e16

DPTS still efficient

Chips:
- AF15P_W22B2
- AF15P_W22B9
- AF15P_W22B12
- AF15P_W22B16
- AF15P_W22B34
- AF15P_W22B18



- Measuring devices up to 10^{16} n_{eq}/cm^2 also for higher n-type implant doses, work in progress
- Studies with TCAD (C. Lemoine)

APTS SF

Results fully in line with ECFA RD Goals

Multiple strands for R&D on MAPS:

- MAPS for small-pixel trackers in sub-micron node(s) for smaller pixels pitch and stitching process for large area sensors to reach ultimate precision and radiation length in vertex detectors;

  DPTS 15 µm pixel pitch, stitched devices in ER1 18 µm and 22.5 µm

- MAPS for small-pixel trackers with radiation-hard cell designs and high hit-rate capability (sufficient charge collection after 10^{15} n_{eq}/cm^2 to 10^{16} n_{eq}/cm^2 non-ionising energy loss (NIEL), single event upsets (SEU) and single event effects (SEE) tolerant and power-optimised logic, concepts for high data volumes handling on a sensor;

  DPTS 10^{15} n_{eq}/cm^2 at room temperature, investigating paths to 10^{16} n_{eq}/cm^2

  circuit total ionizing radiation tolerance and SEU cross-sections in line with other deep submicron CMOS

- MAPS designs to reach ultimate timing precision in different processes;

  FASTPIX < 150 ps with small collection electrode in 180nm, studies ongoing in 65nm

- MAPS with reduced granularity and very low power consumption in very large area detectors for tracking and calorimetry applications.

  DPTS 10 – 1000 nA, sensor variant with gap designed to maintain efficiency for larger pixel pitches

Technology features

Building knowledge about this technology for general interest

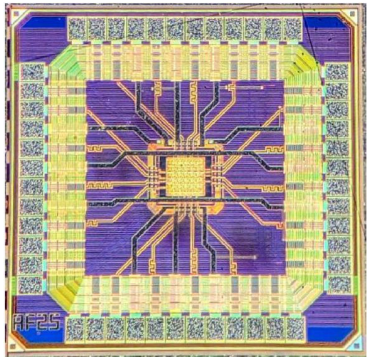
- Very significant contribution from the ALICE experiment
- Building on 10 year experience with 180 nm in the entire community (ALICE, ATLAS, CLIC, …)
- Towards full technology validation for our applications: full efficiency and SEU, TID according to expectations, further studies on sensor timing and NIEL:

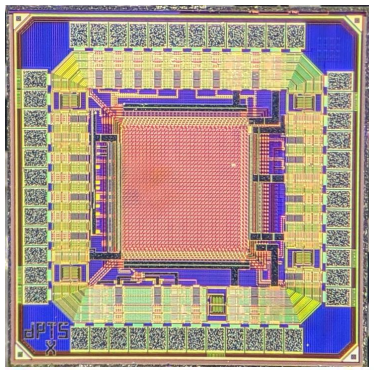
  NIEL: 10^{15} n_{eq}/cm^2 at room temperature, investigating path to 10^{16} n_{eq}/cm^2

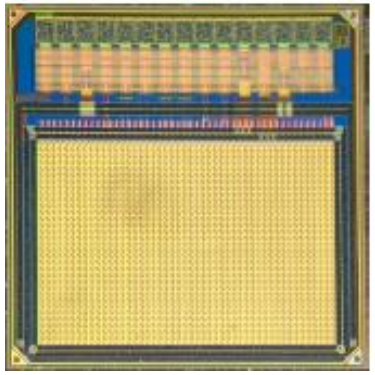
Features

- Significantly more dense than 180 nm
- Specific imaging sensor features could still open further possibilities

  (only explored our 'standard sensor'):
  - stacked photodiode
  - gain in the pixel
  - …
- Possibility of wafer stacking
- Good relationship with the foundry with excellent support, results oriented.


APTS


DPTS


CE65

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