EP R&D Days
WP1.1 Silicon Hybrid Detector

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…. and a big thanks to collaborating institutes PSI, Nikhef, CNM, IGFAE-USC, CPPM, University of Oxford, …

Motivations

MIP detection in next generation of collider experiments

from the CERN Strategic R&D Programme on Technologies for Future Experiments [CERN-OPEN-2018-006]

[fineprint in CERN-OPEN-2018-006]	HL-LHC	SPS	FCC-ee	FCC-hh
Total fluence [$n_{eq} cm^{-2} s^{-1}$]	$5x10^{16}$	10^{17}	10^{10}	10^{17}
Max Hit rate [$cm^{-2} s^{-1}$]	2-4G	8G	20M	20G
Material budget per layer [X_0]	0.1-2%	2%	0.3%	1%
Pixel size [μm^2] inner trackers	50x50	50x50	25x25	25x25
Temporal hit resolution [ps] inner trackers	~50	~40	-	~10

- **Time resolution 10 - 50 ps**
- **Pixel pitches down to 25µm**
- **Fluences up to $10^{17} n_{eq}/cm^2/y$**
- **Max hit rate up 20G/cm^2/s**

Challenges for sensor
Challenges for front-end electronics

Workplan

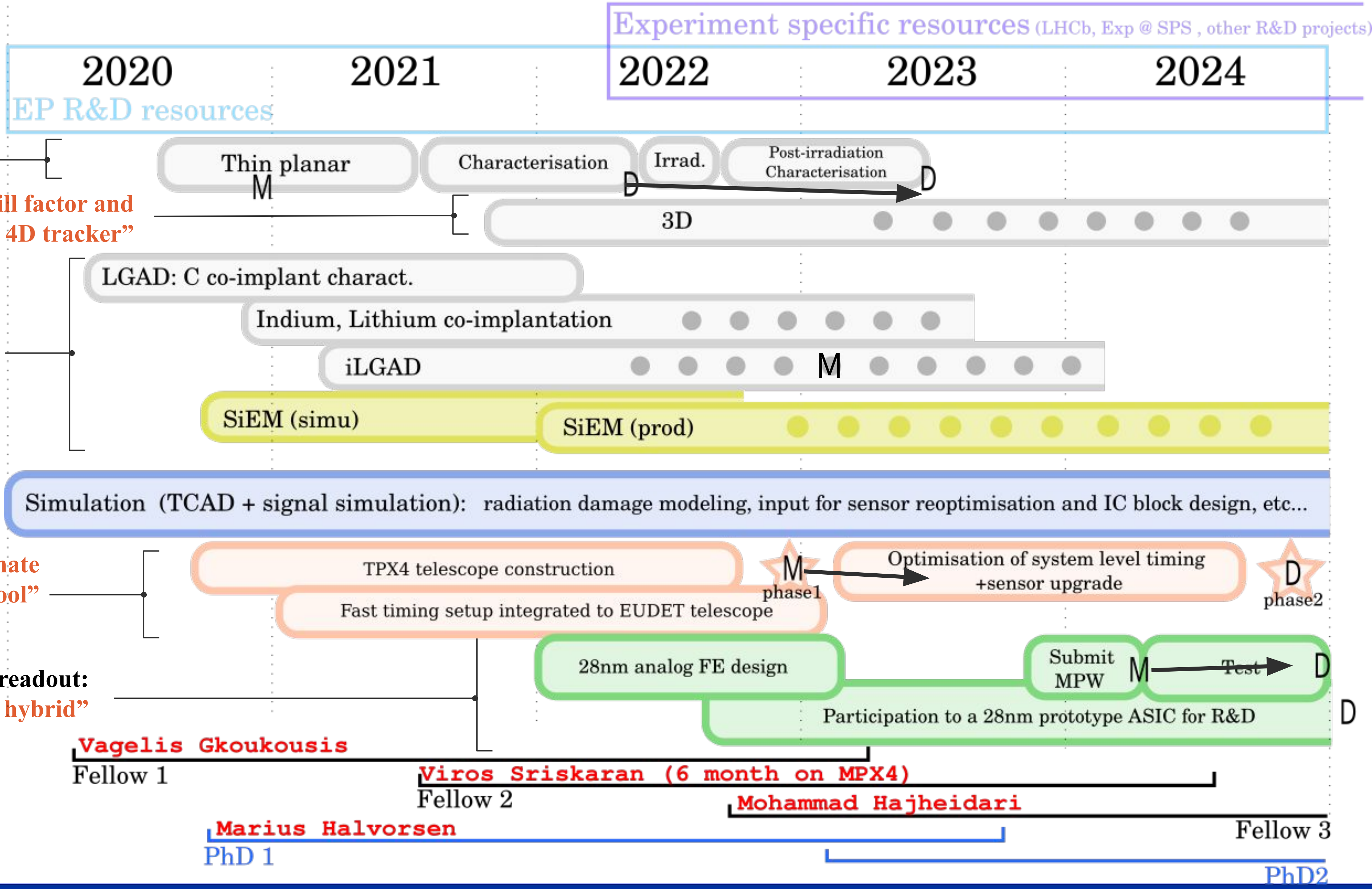
Planar: **“the reference”**

3D technology: **“improve fill factor and characterise toward 4D tracker”**

Sensor with internal gain: **“make them radiation hard and small pitch”**

Fast timing telescope: **“ultimate sensor characterisation tool”**

ROC for fast readout: **“The second key part of the hybrid”**



WP1.1 from phase 1 (2020-2024) to phase 2 (2024-2028)

- **Key point of the program is the characterisation of sensor hybridised to the ROC developed in phase 1**
  - limitation of testing sensor “by themselves” (see study for 3D specs later in the talk)
  - quick hybridization turn around made possible thanks to the work in WP1.3 on ACF
  - O(50ps) / O(40-50um) ROC expected end of phase 1 thanks to the work WP5, WP1.1, EP-ESE and Nikhef [Picopix]
- **Sensor**
  - Test of phase 1 sensors hybridised to the picopix
  - Evolution and production of sensors (3D / small pitch LGADs)
  - Blue-sky R&D projects : evaluation of the SiEM scalability / support of new ideas
- **ROC**
  - Need readout/DAQ for test and sensor characterisation
  - Qualification with sensor / under irradiation / under cold temperature
  - Second submission with evolution [application to other targets, operation at low temperature, on ASIC logic]
- **Characterisation setup**
  - Request from several body (AIDA innove WP6) to have access to the TPX4 telescope to test fast sensor
  - In Phase 1, DUT readout based on TPX4, to be extended in Phase 2 to PicoPix / external readout (ex. 16ch board)
  - Documentation and support of internal/external user
- **Collaboration with ECFA DRD3 – R&D on Solid State Detectors**

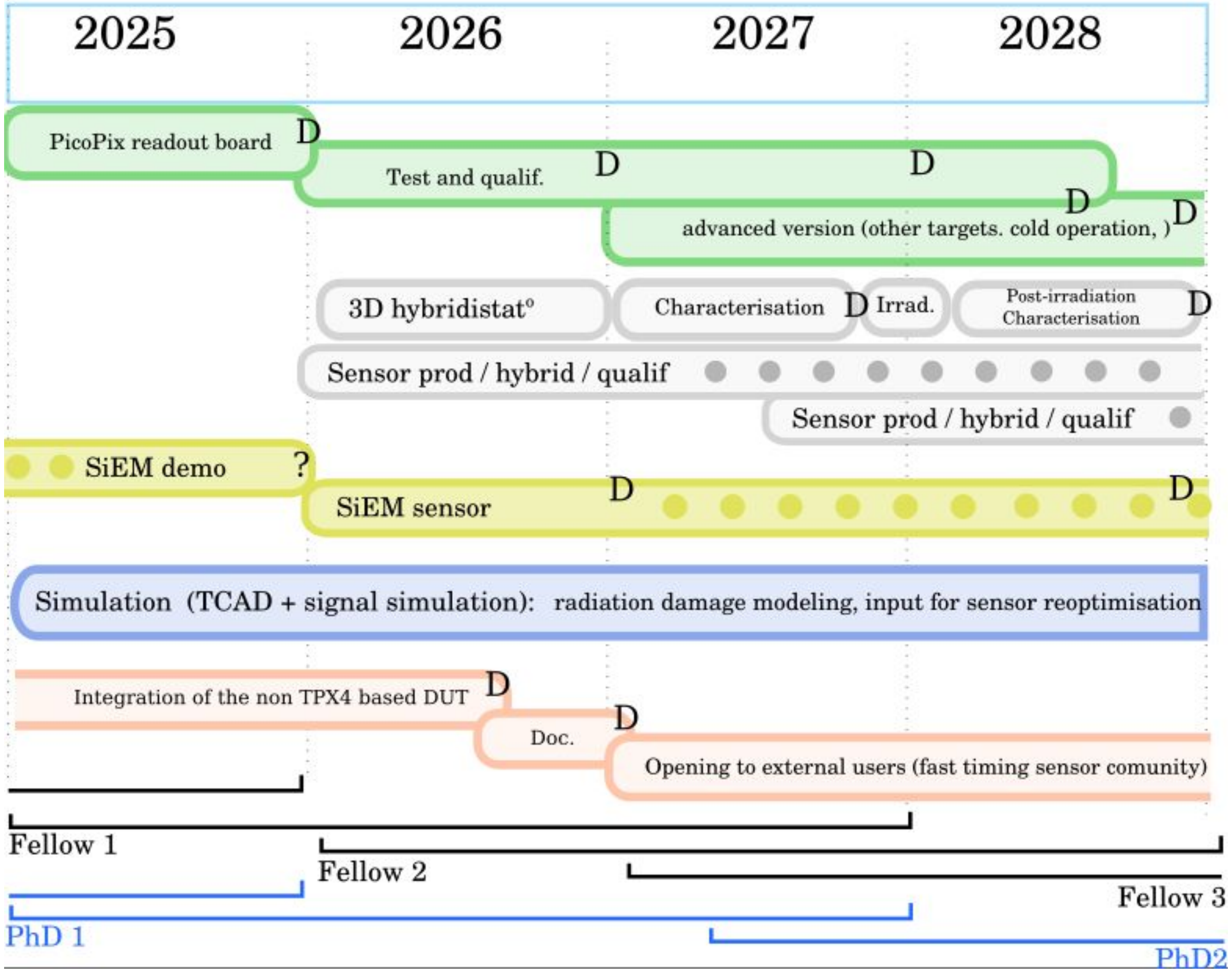
Workplan 2025-2028

ROC for fast readout
⇒characterisation and evolution

Fast sensor:
⇒ hybridised characterisation
+ design evolution

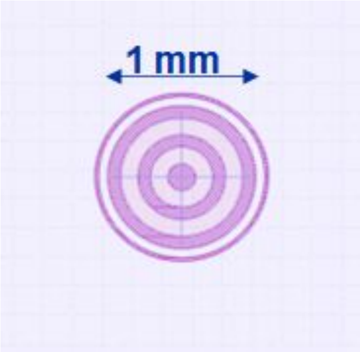
SiEM: ⇒scaling up?

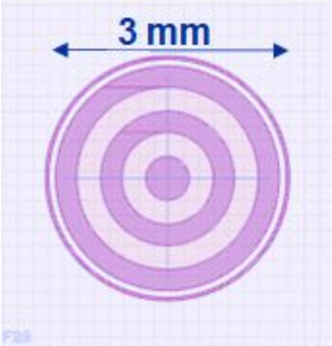
Fast timing telescope:
⇒extending the usage beyond TPX4 and



SENSORS

Planars & 3D Irradiation campaign

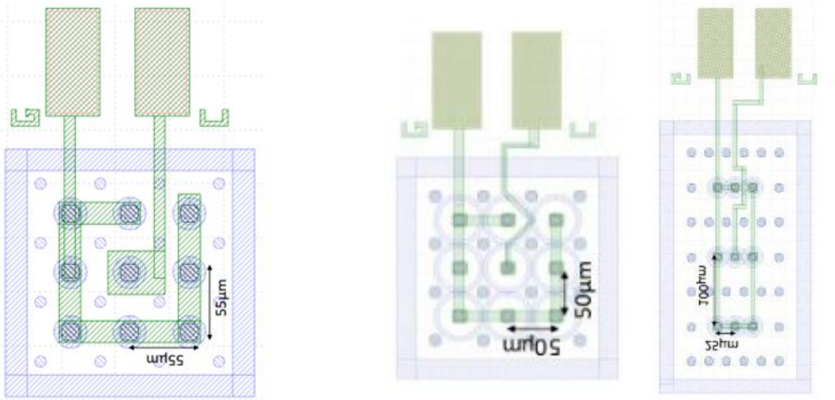




Study of radiation hardness up to fleunce of $1x10^{17}$ n_{eq}/cm^2 with proton and neutron

Planar production by ADVACAM:

- n on p planar test structures with 50,100,200 and 300 µm thickness
- Test structures:
  - **Small diodes** (1 mm diameter)for timing study due to lower capacitance
  - **Big diodes** (3 mm diameter) for radiation damage study and benchmarking the simulation



3D production by CNM:

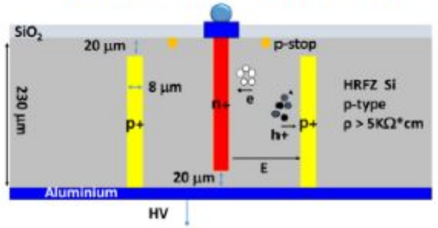
- Test field uniformity and timing with respect ot generated charge (thickness)
- **Double Sided** n-in-n: 230 µm thick, 55 x 55 µm single cell structures
- **Single Sided** n-in-p: 150 µm active thickness, 50 x 50 µm & 25 x 100 µm single cell structures

Irradiations:

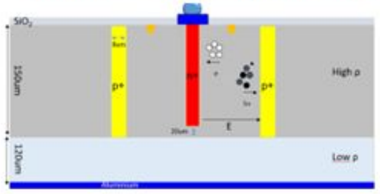
- Fast Neutrons at JSI (Ljubljana)
- 25 GeV Protons a@ CERN PS
- 4 points in fluence for each irradiation type

Fluence [n_{eq} /cm^2]	Small Diodes	Big Diodes
$1x10^{15}$	8	8
$8x10^{15}$	8	8
$6x10^{16}$	8	8
$1x10^{17}$	8	8

Double Sided
(thicker, more expensive)



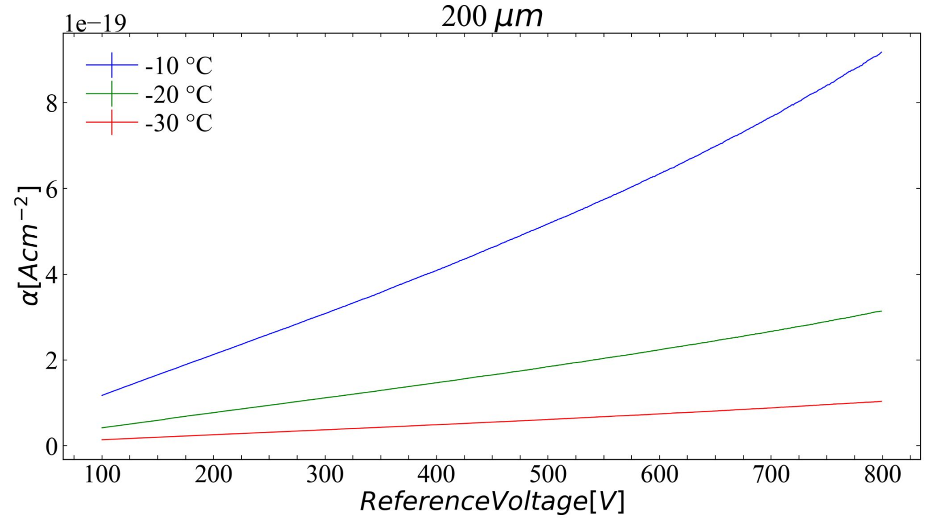
Single Sided
(thinner, simpler process)



Planar sensors
IV measurements (Alpha factor)

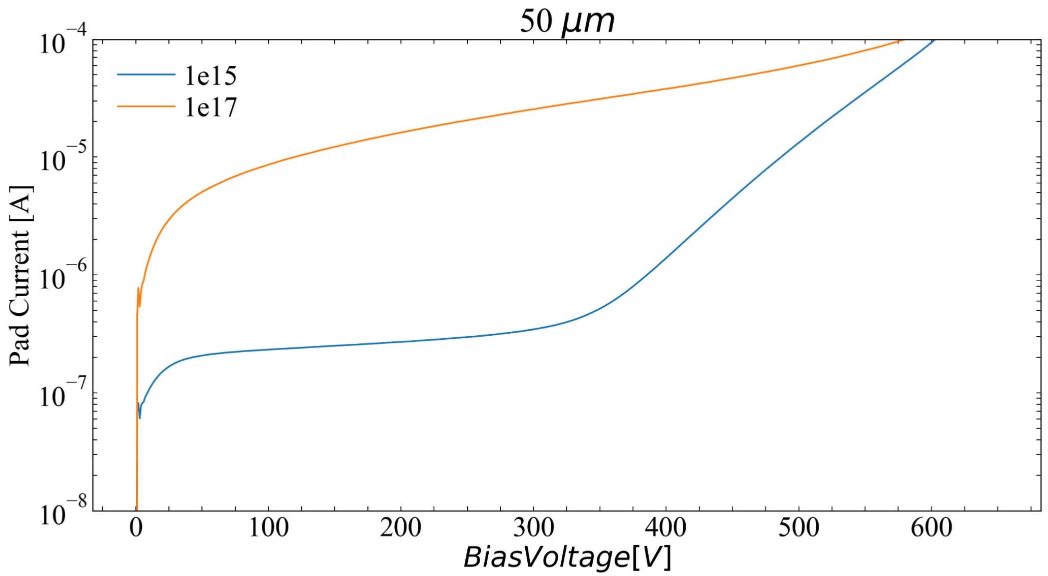
- All sample are annealed for 60 min at 80°C
- Alpha factor depends strongly on voltage point used for calculation
- Depleted volume unknown

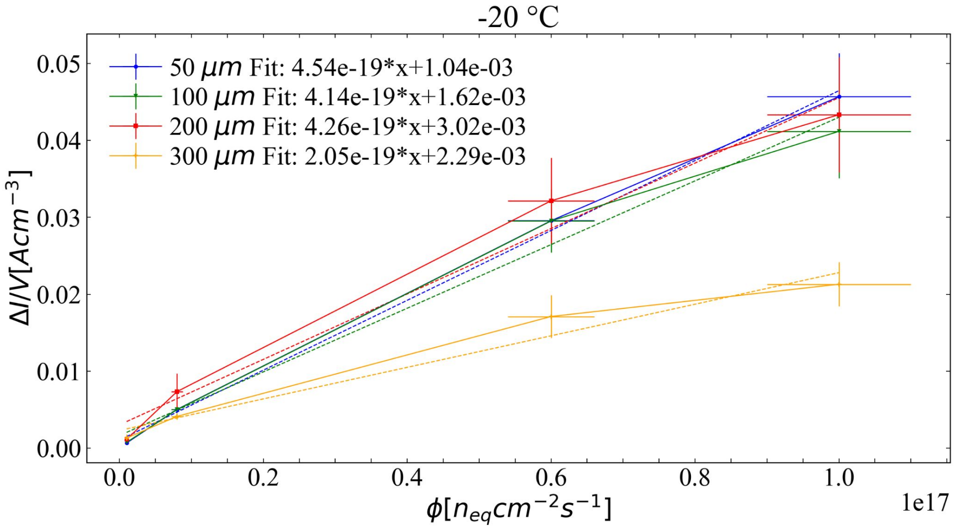
$$\Delta I/V = \alpha \Phi_{eq},$$



Alpha factor change as function of calculation point.

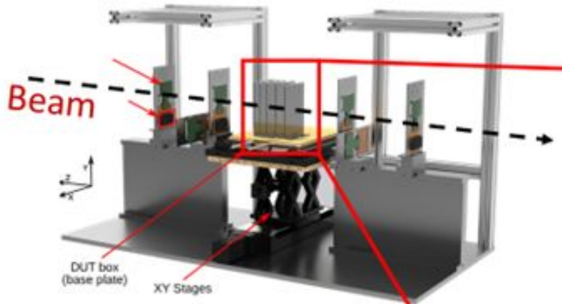
No signs of current saturation at high fluences.

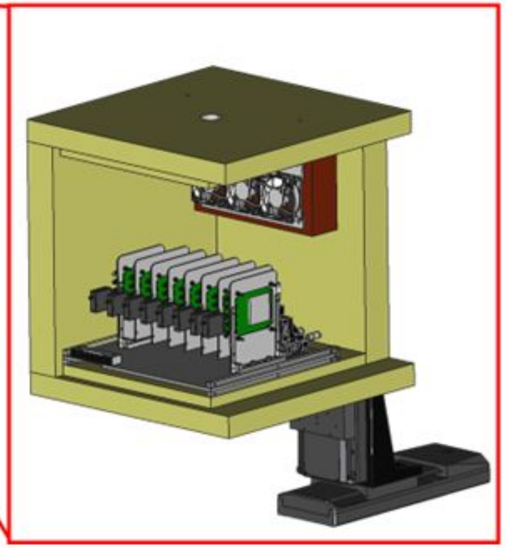




Alpha factor calculation for quadratic scaling of calculator point with thickness

3Ds & Planar characterisation in Testbeams

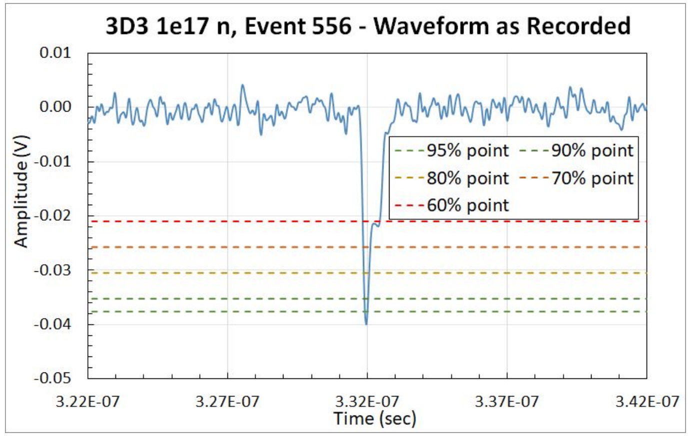




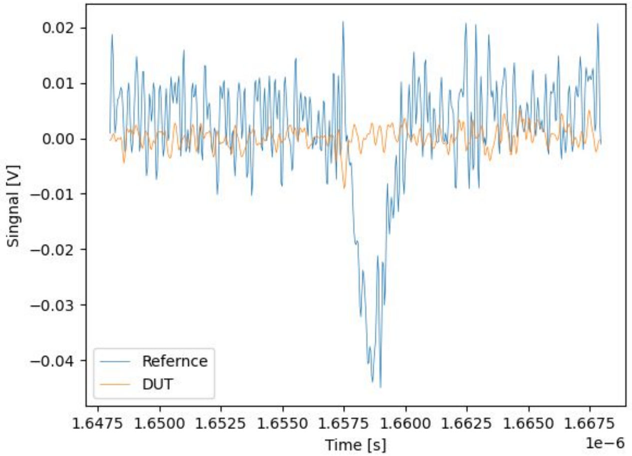
The Setup

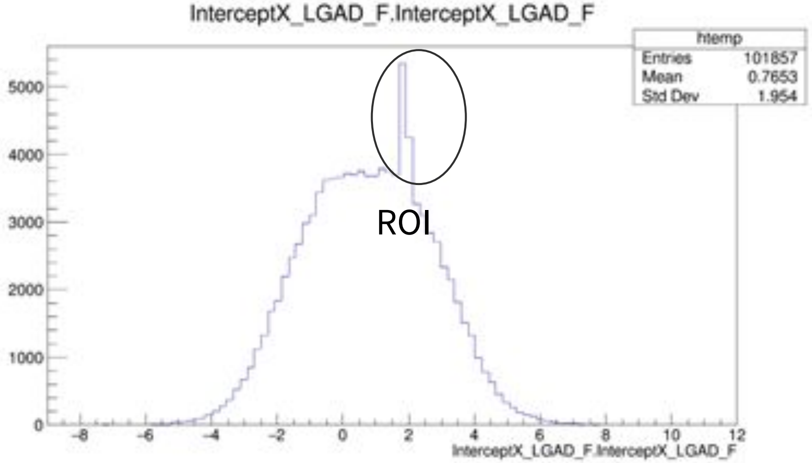
- MIMOSA based AIDA Telescope
- Custom Cold Box
- DUTs on individual motorized motorized individual stages
- Pixelated alignment & ROI plane

- Remove DUT from trigger
- Reconstruction finished
- Waveform analysis ongoing



Event for unirradiated 50μm





Aim for this measurements: time resolution measurements as function of irradiation.

Current status: Finalising the waveform analysis

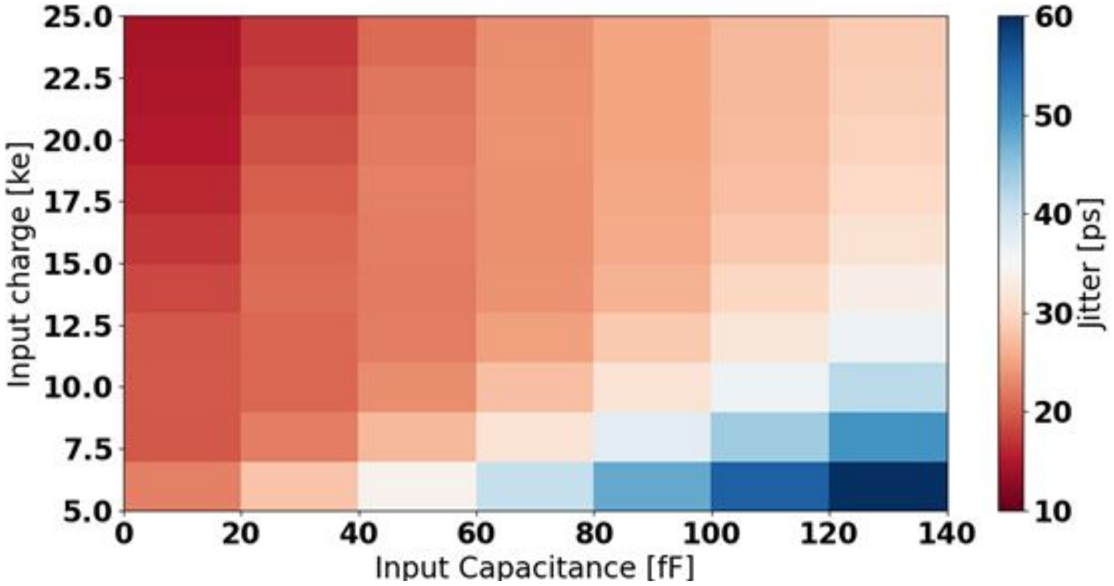
ASIC Jitter as a function of input charger and capacitance

Simulation results of an analog front-end (see ASIC part)

More about this in j.nima.2022.167489

Two important features from these data:

- ❑ Larger the capacitance, larger the jitter
- ❑ Larger the input charge, smaller the jitter



These results put a strong restrictions on type of the sensors that can be used for high precision timing measurements (less than 30 ps).

Need to be taken into account in the design

Calculation of charge and capacitance of a 3D sensor

The capacitance of a single pixel is calculated as:

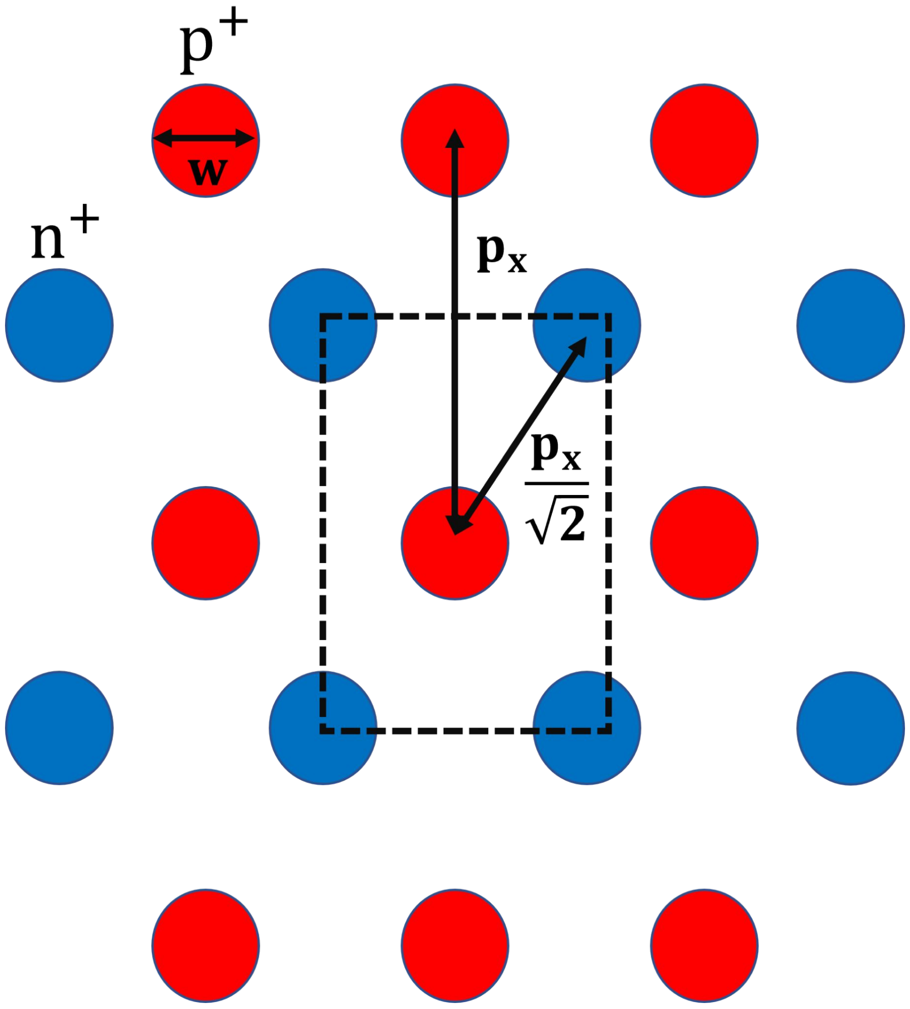
$$C_{pix} = 2C_{p^+p^+} + C_{p^+n^+}$$

Where $C_{p^+p^+}$ an$C_{p^+n^+}$ depends on column width (w) and the aspect ratio of the sensor (A.R).

The deposited charge of a single pixel is calculated as:

$$Q_{in} = 0.072\ \text{ke} \times \text{AR} \times \text{w}$$

Using these equation one can calculate the parameters of a sensor which correspond to a certain time resolution (e.g. 30 ps).



Acceptance region in w-A.R phase space

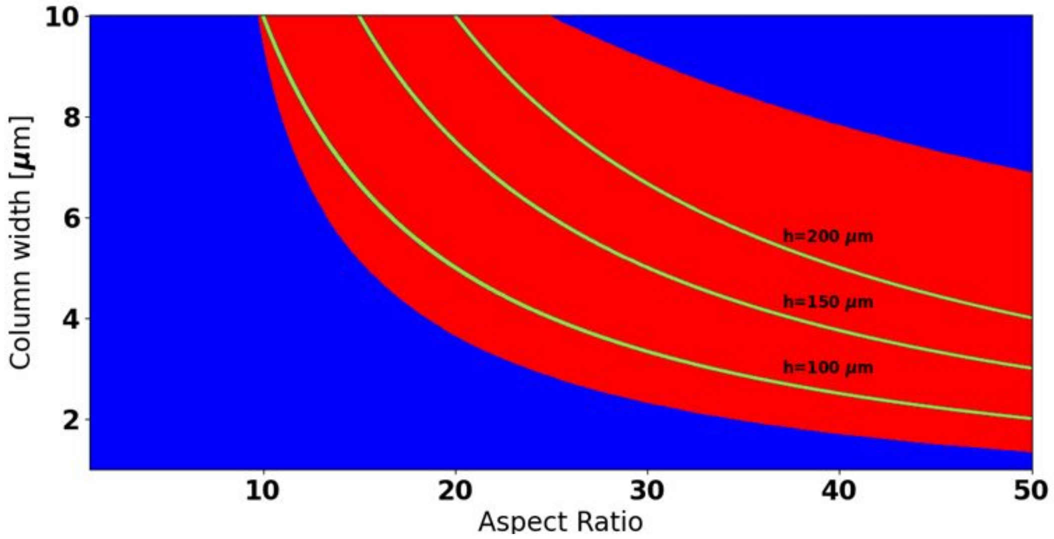
By combining the capacitance and charge calculations with results of the jitter simulation, the acceptance region in w-A.R space is found.

Such plots can be used in tendering letter for sensor production.

$$\theta = 0°, \sigma_t < 30 \text{ ps}$$

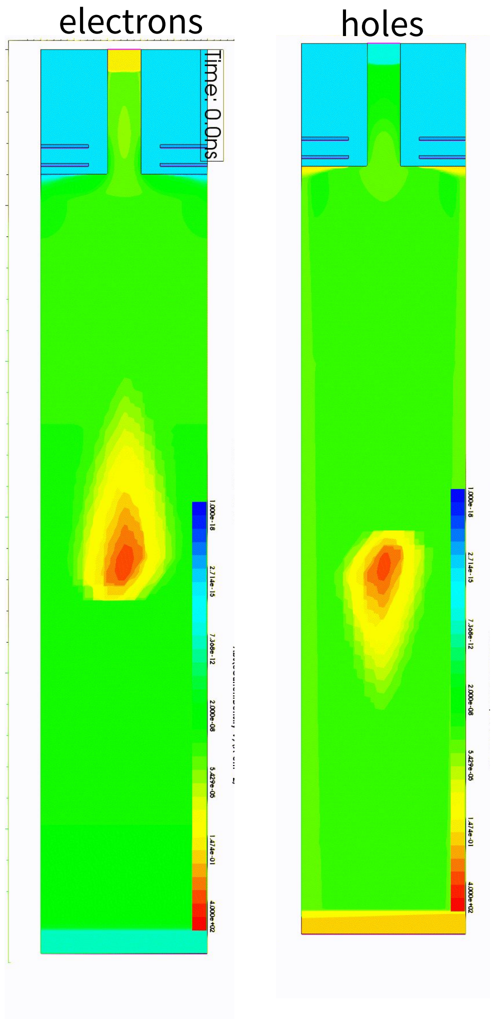
This pictures becomes more complicated if the tracks are not parallel, $\theta \neq 0°$, and fill factor considerations are taken into account.

Angle often use to recover geometrical fill factor, but angle adds charge sharing that reduce the minimal charge



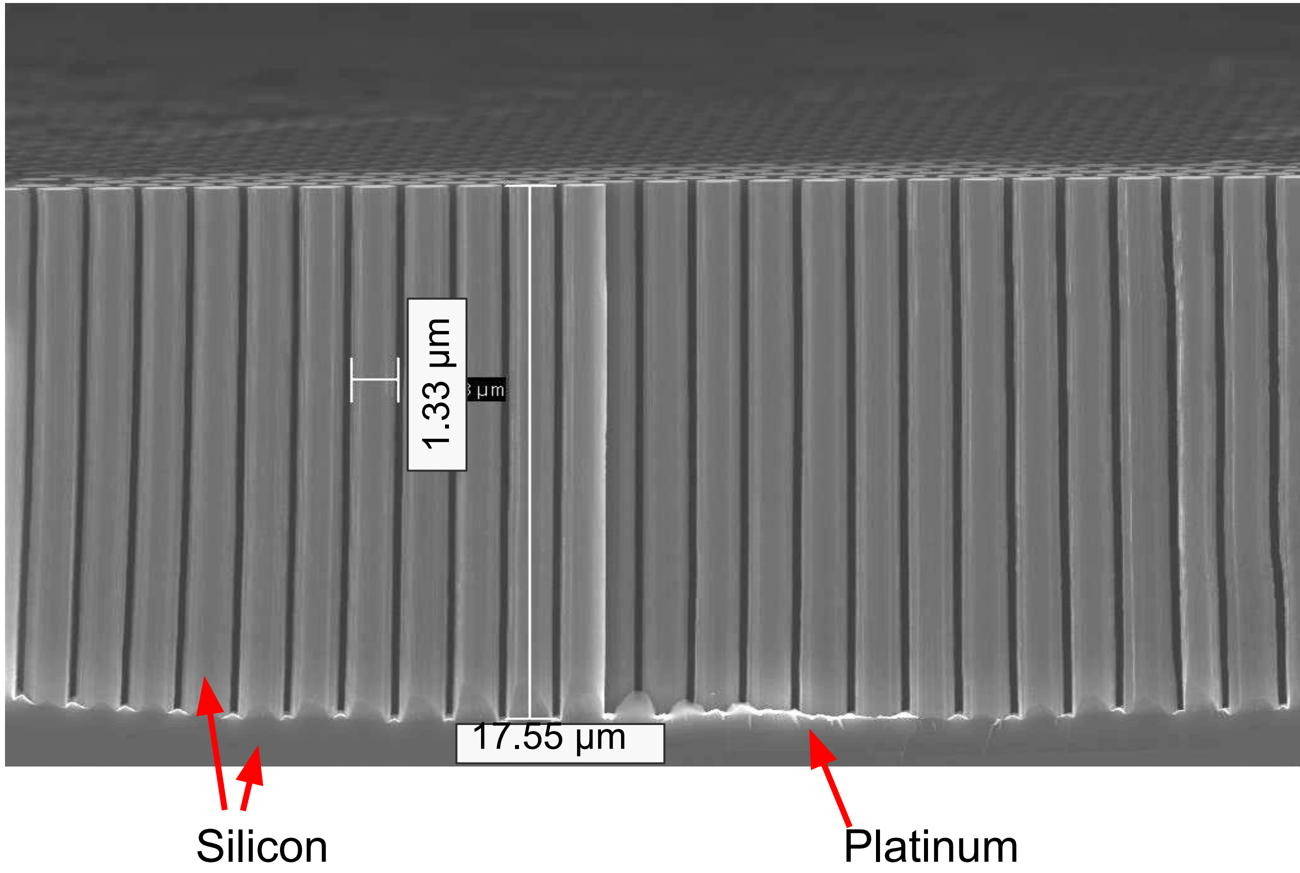
SiEM

- **Silicon Electron Multiplier Sensor**
  - Electrodes embedded into the sensor substrate to promote charge multiplication
  - Good temporal and spatial resolution, gain not to degrade by acceptor removal
  - Article on simulations: https://doi.org/10.1016/j.nima.2022.167325
  - Fabrication projects
    - Metal Assisted Chemical Etching (MacEtch)
    - Deep Reactive Ion Etching (DRIE)



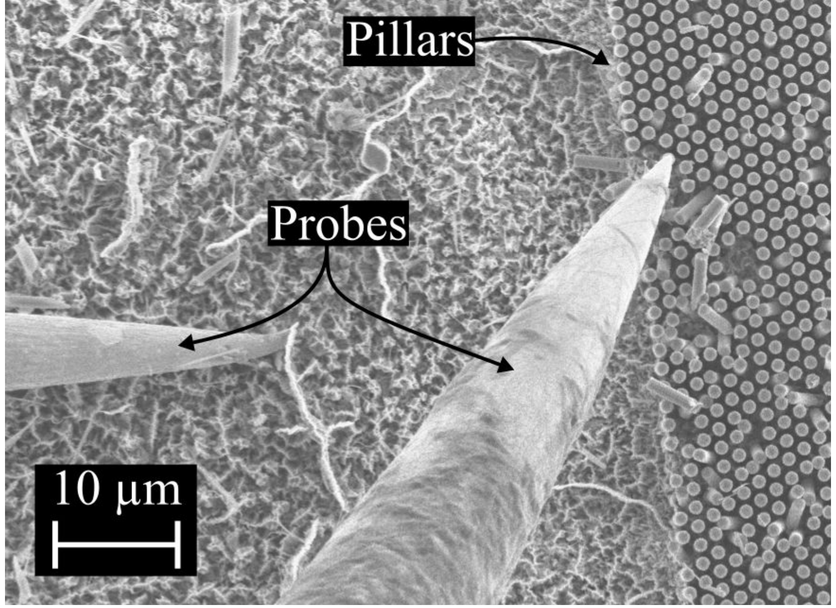
SiEM MacEtch

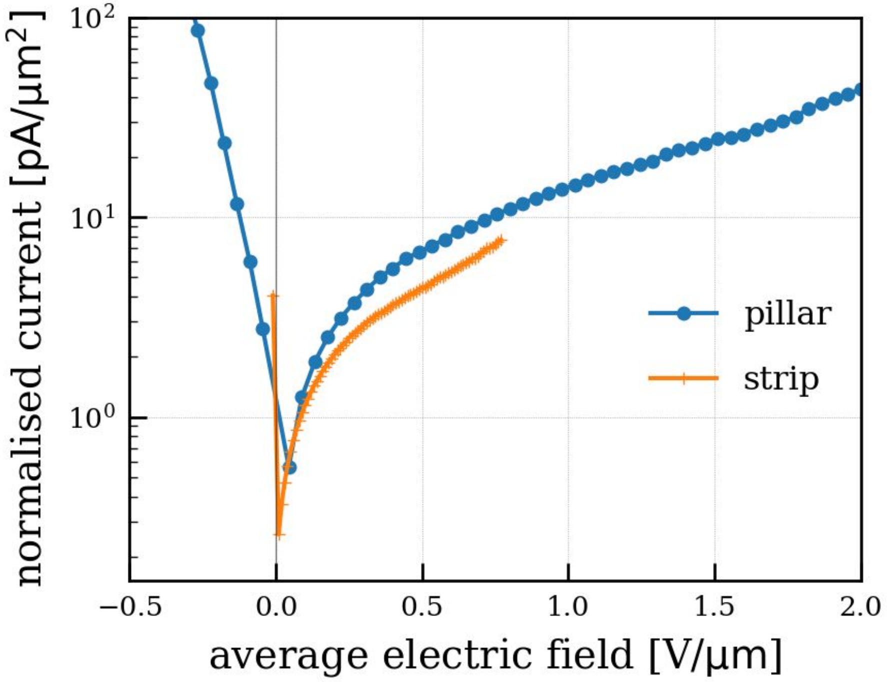
- **Fabrication using Metal Assisted Chemical Etching (MacEtch)**
  - Metal catalyst for etching is also used for sensor operation
  - Allows extreme aspect ratios
  - Can make structures in 10s of nanometer range
  - Not until now applied on active media
- **Recipe tuning**
  - Target pillars with
    - Diameter 1um
    - Height 10um
    - Hexagonal lattice pitch 1.5um
  - Metallisation



SiEM MacEtch

- **Electrical characterisation**
  - Probe station inside Scanning Electron Microscope
  - Sub-micrometer needles
  - Single pillar characterisation
- **Diode characteristics preserved after fabrication**
  - Similar normalised current for strips and pillars
- **Next steps:**
  - Finish IV characterisation
  - IR-laser and beta measurements
  - Second production
    - Tune metallisation procedure
    - Reduce defects

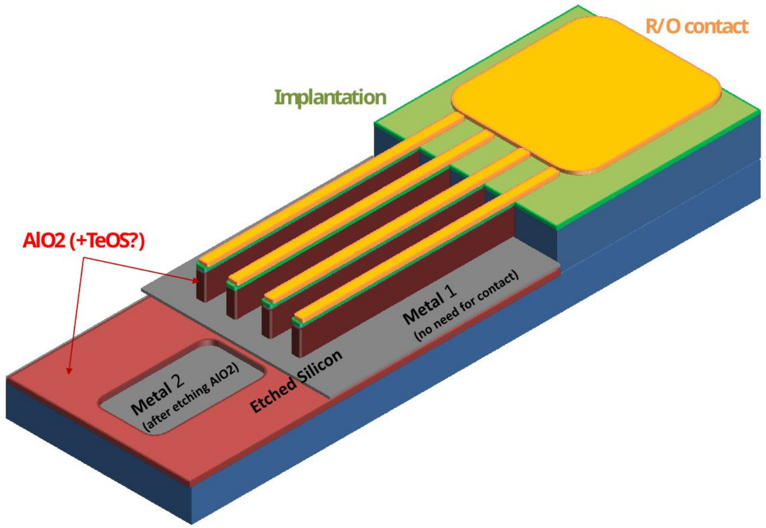




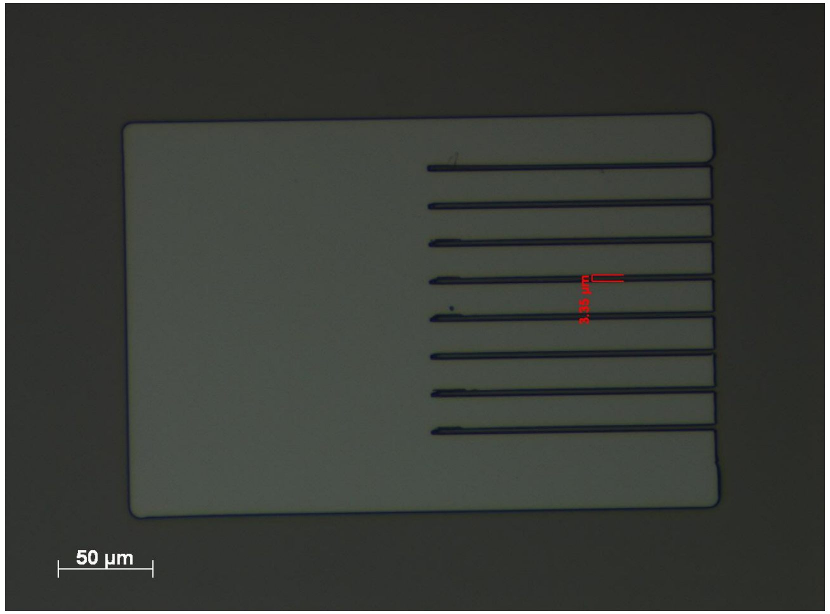
SiEM DRIE

- **Project lead by CERN and CNM**
- **Aim at demonstrating the concept of SiEM described in** NIM A 1041 [2022] 167325
- **Project organised in several phases**
    - [1] Definition of the process (technics, marterial etc…)
    - [2] TCAD simulation and design of the chosen process
    - [3] Production
    - [4] Characterisation
    - [5] Investigation of alternative approach (different available tech., materials)
- **Proposed process based on DRIE.**
- **Study of geometrical constraints [1]**
    - On-going investigation on the minimal pillar width achievable with laser photo-lithography
    - Rest of the process test to be carried on in 2023

First process proposal (Sept 2022)



Photolithography test (3um)



CHARACTERISATION SETUPS

TPX4 Telescope Status

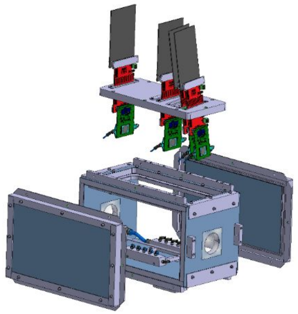
Timepix4 chip ideal for telescopes: large area, simultaneous ToA and ToT, high resolution timσestamp (195 ps TDC), high rates achievable *(JINST* **18** P02011).

Telescope Autumn Campaign: Timepix4v1 bonded to n-on-p 300 um and 100 um thick sensors

(Known issue of v1: Voltage Controlled Oscillator running 25% too fast and not properly locked to reference oscillator, so the best performance not yet expected)

Half Telescope demonstrator:

- tilted planes for σ_{xy}
- perpendicular planes for σ_t

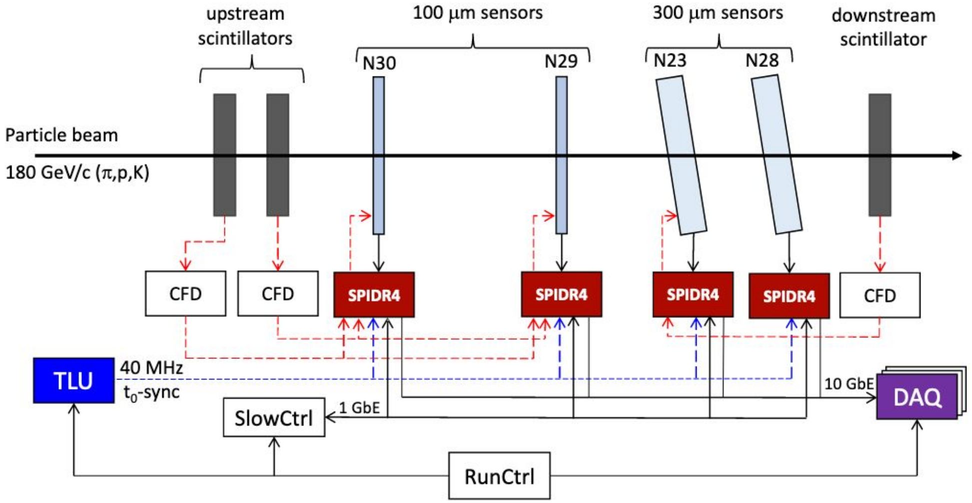


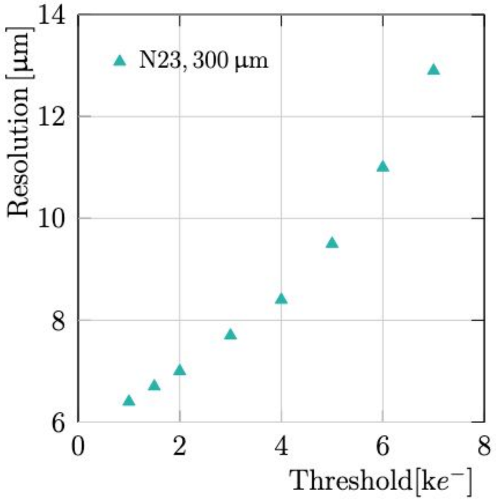
Spatial resolution

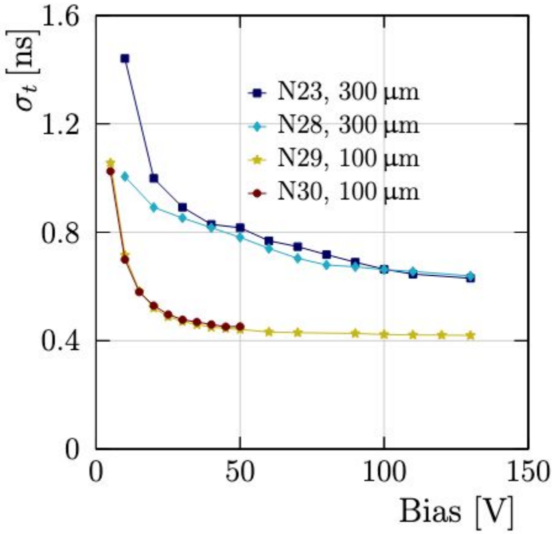
- in agreement with predictions
- benefits from operating at low threshold

Temporal Resolution

- corrections for timewalk + track topology + per pixel offsets applied
- Sensor bias is limiting
- Low threshold beneficial
- Track time resolution 340 ps







TPX4 telescope: next steps

Track time resolution improvements expected from:

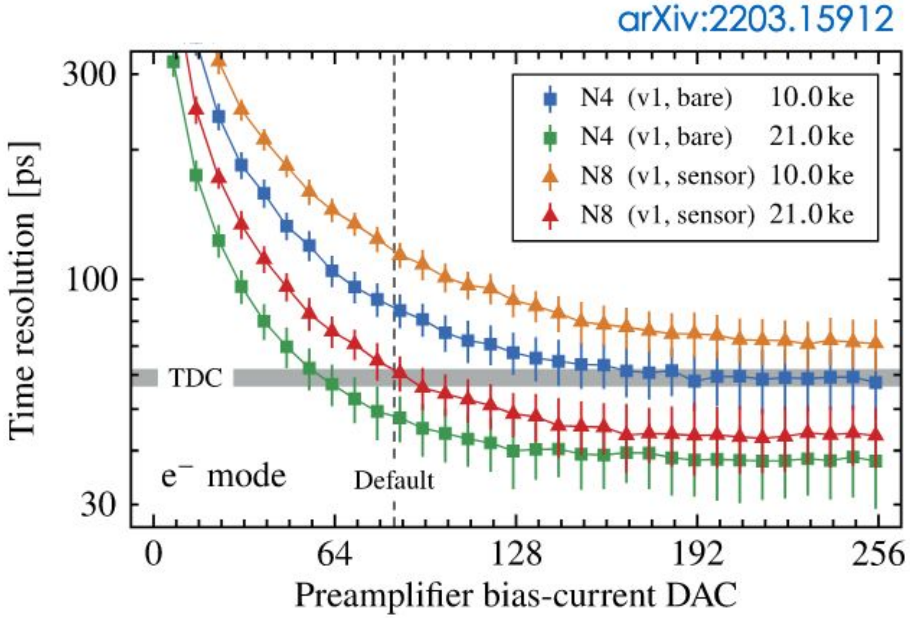
- more layers
- higher bias voltages
- Timepix4v2
- higher preamplifier current
- additional corrections (currently limited by statistics)
- faster sensors

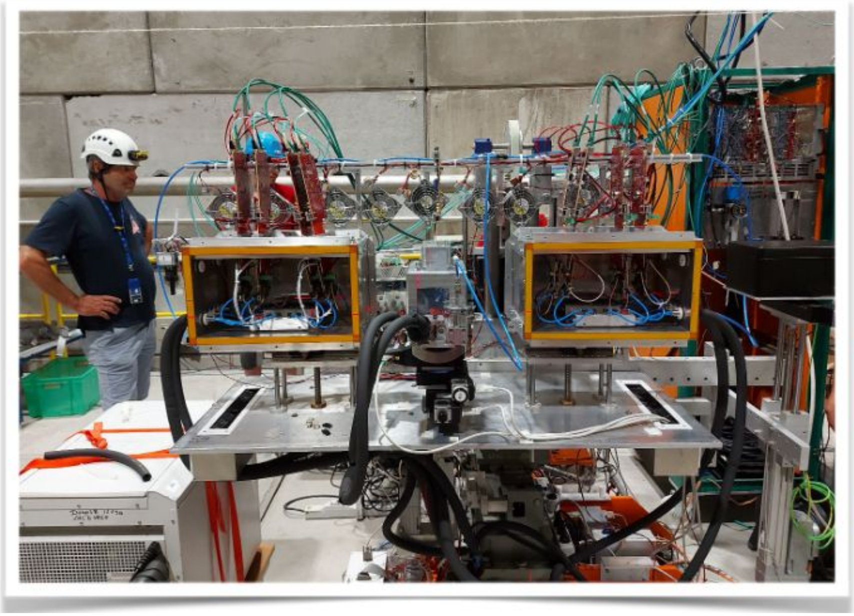
Second iteration of telescope in 2022

- up to 8 layers
- combination of Timepix4v2 and Timepix4v1
- various planes configurations
- quartz + MicroChannelPlate-PMT in outer stage

Current status: Commissioning and analysis of 2022 data ongoing!

Next step equip with fast sensor (iLGAD/timespot/TI-LGAD…)





Integration to TPX4 telescope

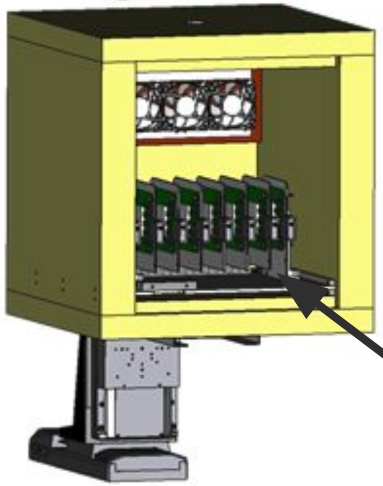
- Consolidate the system in a 3-object setup:
  - Rack containing power supplies, AIDA TLU, readout board and support electronics
  - Cold box with stages, mechanics, front-end boards and heat exchanger
  - Chiller and relevant controls

Integrated at the end of TimePix 4 Telescope

18U Rack Cabinet

\+

Cold box with motorized stages and ROI



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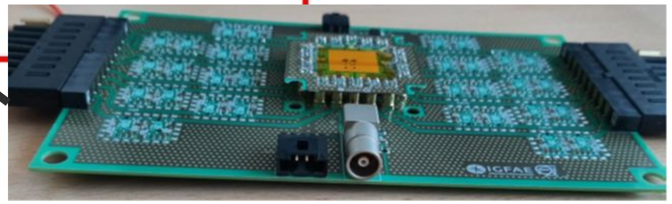
Chiller with control



Transport as a pre-assembled pre-configured integrated system

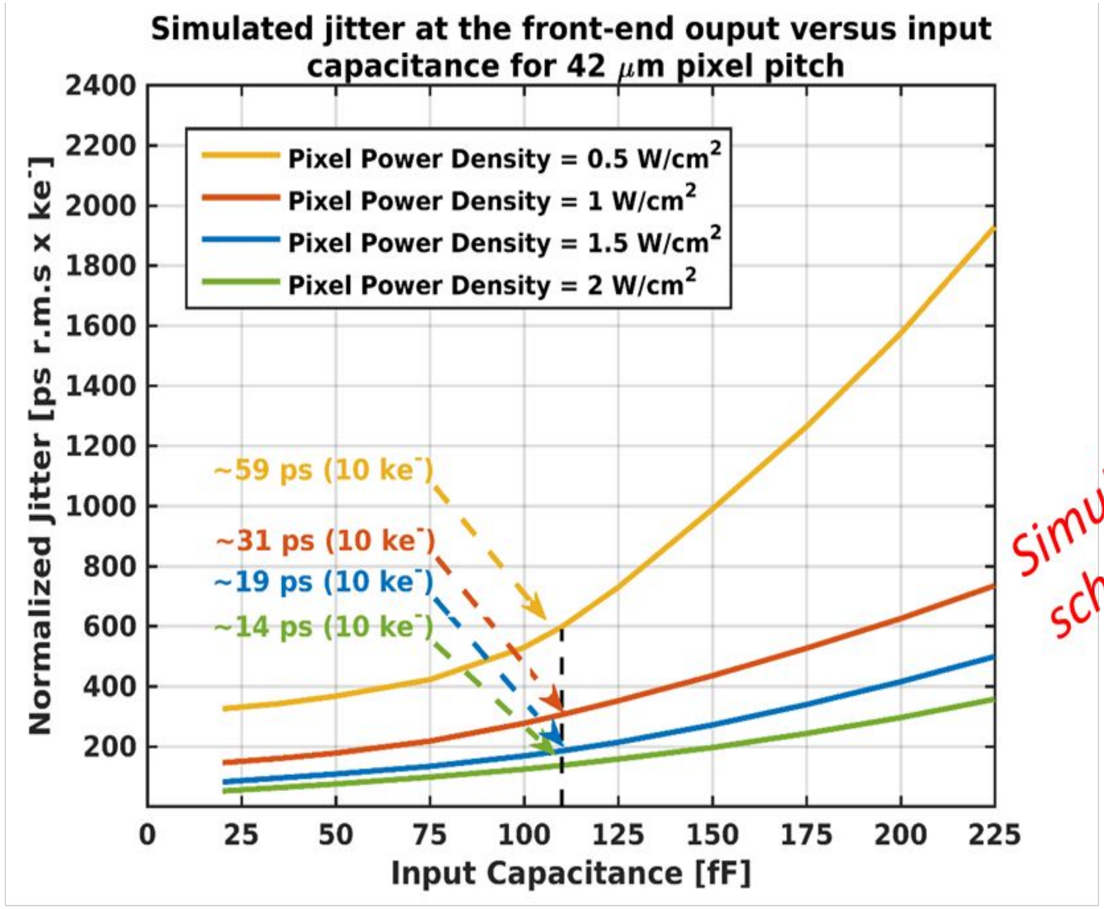
READOUT ASIC

V. Sriskaran, on behalf of the PicoPix design team

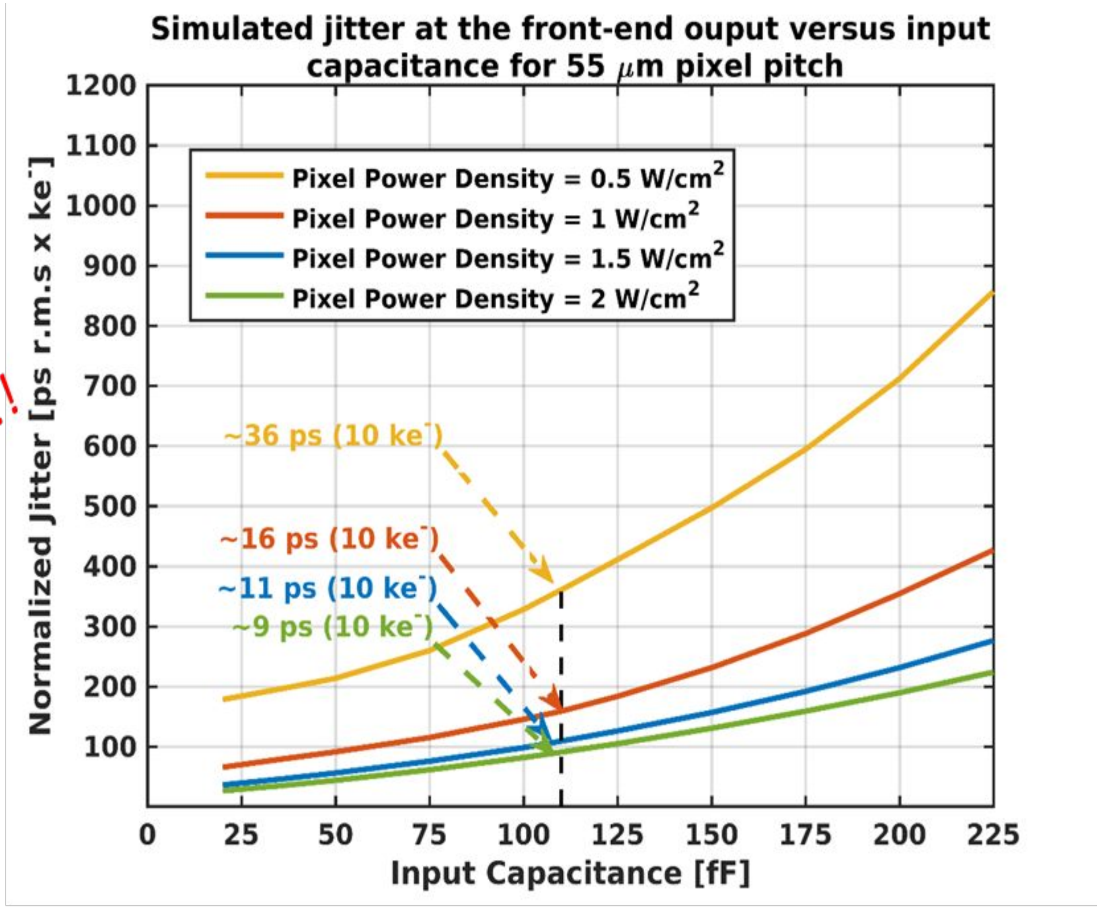
Towards sub-30ps time resolution: PicoPix demo chip

- Designed as a “real” small scale prototype:
  - Analog FE
  - Local VCO
  - Pixel data clustering
  - Pixel readout
  - SEE robust architecture
  - Clock distribution using dDLL approach (as in Timepix4)
  - High-speed links
  - On-chip Bandgap and biasing DACs
  - UVM Functional verification
- Chip should be ready to be bump bonded to different sensor types:
  - ACF Anisotropic Conductive Film
- Slow Control protocol can be simplified → reused from Medipix4/Timepix4?
- Why?
  - CMOS 28nm technology is most certainly the choice for this project given the time scale and experience
  - Avoid to get false expectations on final design
  - If this design is successful the large scale chip should be simple and minimizes risk (time and money)
  - Required ASIC for future sensor developments

Analog FE pixel for PicoPix

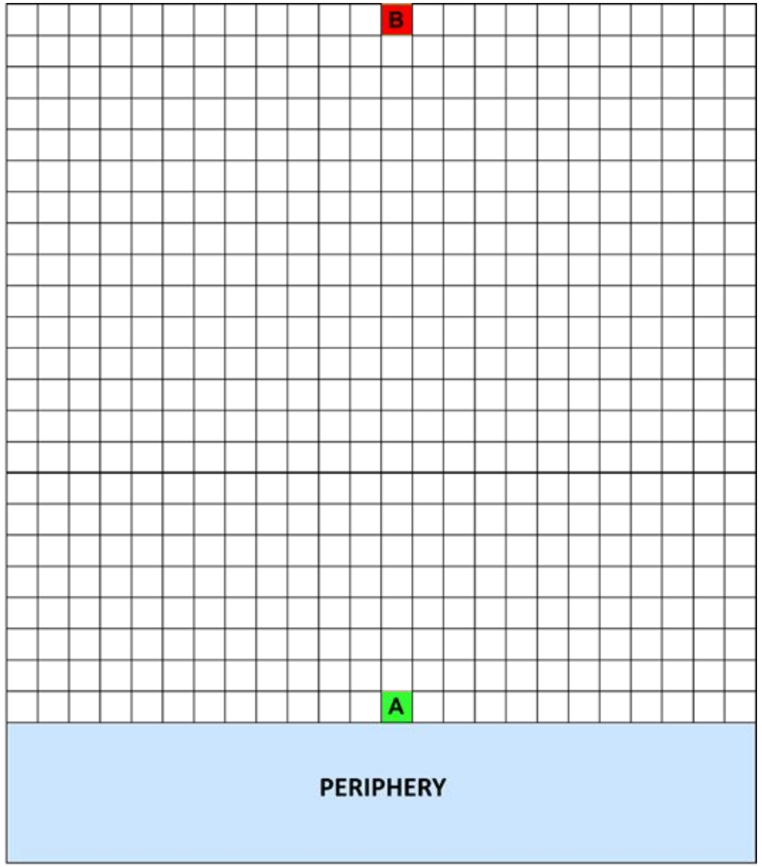


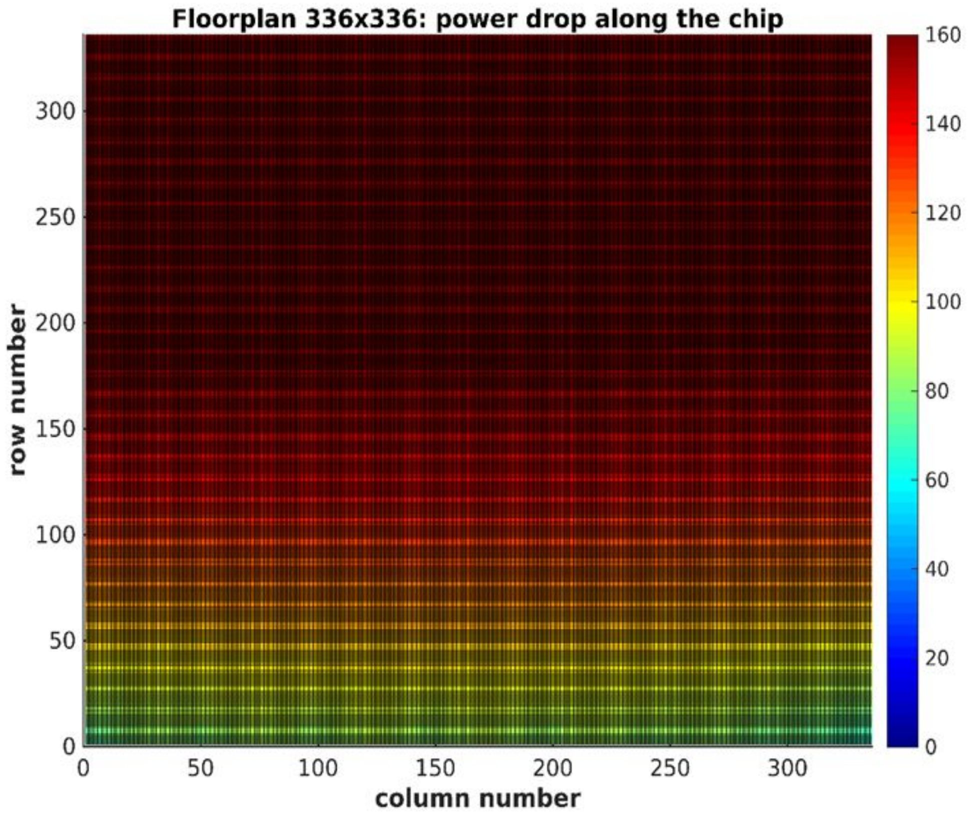
Simulation using schematic view!!



NB: 110 fF is the total pixel capacitance obtained with 3D-trench sensor.
DOI: 10.1088/1748-0221/15/09/P09029

Power drop in a 336 x 336 array of 42 µm pixels



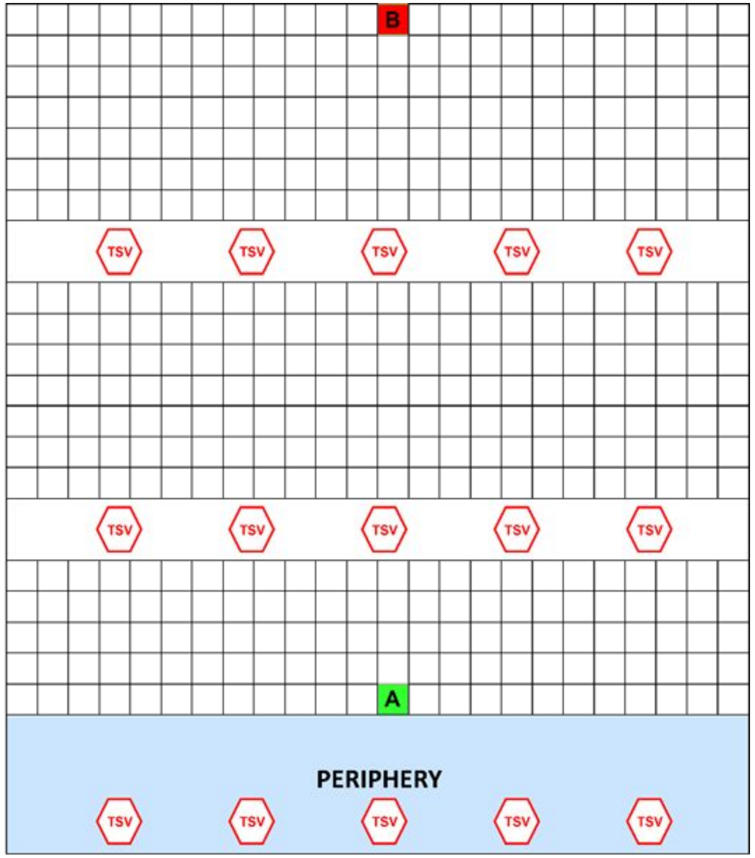


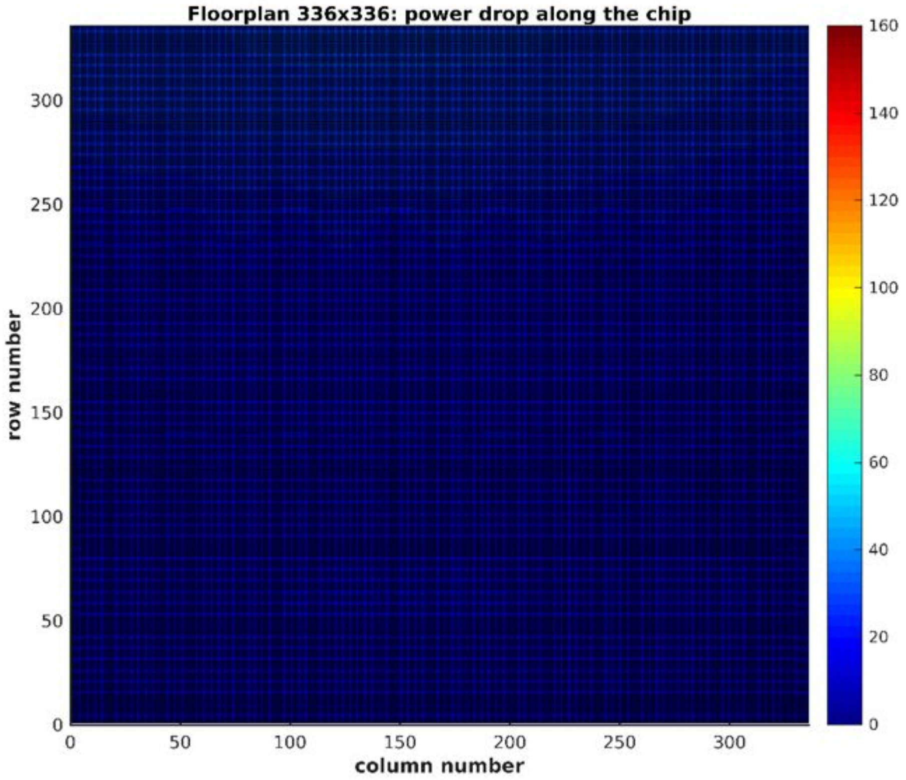
	Pixel A	Pixel B
V_{GND} [mV]	45	90
V_{GND_KRUM} [mV]	45	61
Peaking time [ns]	1.71	2.27
$I_{DS}(M_{INPUT})$ [µA]	17.3	11.9
σ_{TOA} (ps r.m.s)	12	24
I_{KRUM} [nA]	98	69
ToT [ns]	42	68

→ The power drop along the pixel must be minimized to avoid top-down effect!

→ Systematic I_{KRUM} mismatch: ToT mismatch and gain mismatch!

Power drop in a 336 x 336 array of 42 µm pixels





	Pixel A	Pixel B
V_{GND} [mV]	8	14
V_{GND_KRUM} [mV]	8	14
Peaking time [ns]	2.06	2.1
$I_{DS}(M_{INPUT})$ [µA]	17.3	16.5
σ_{TOA} (ps r.m.s)	9	11.5
I_{KRUM} [nA]	98	82.6
ToT [ns]	42	49

Advantages of using TSVs:

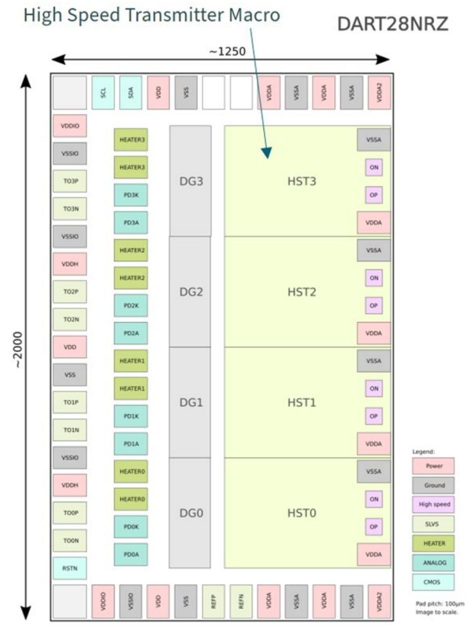
- Improved Analog & digital power distribution → Better uniformity in pixel performances
- Improved readout bandwidth
- Minimized top-down radiation mismatch

Status of the PicoPix

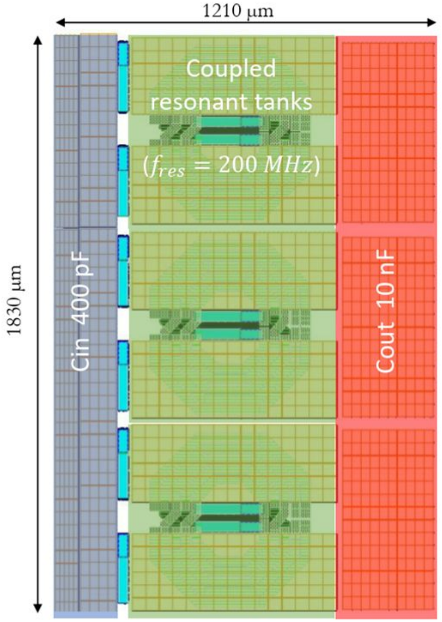
- Status → "exploration phase" of the specs limitations for a large 30 ps r.m.s target ASIC:
  - Front-end limits and optimization
  - On-pixel clustering
  - On-pixel TDC
  - dDLL reference clock distribution
  - On-pixel clock-cleaning PLL (Nikhef)
  - 1st full column RTL exists

- Project organization:
  - Design meetings every two weeks have been organized
  - Design team: CERN and Nikhef
  - Close collaboration with EP R&D WP:
    - 8-bit biasing DACs (**WP1.1**)
    - High speed links 26 Gbps (**WP6**)
    - On-chip DC-DC converter (**WP5.2**)

- Expected submission ~ Q1 2024- Q2 2024



S.Bieregel (CERN-ESE-ME)
https://indico.cern.ch/event/1138500/

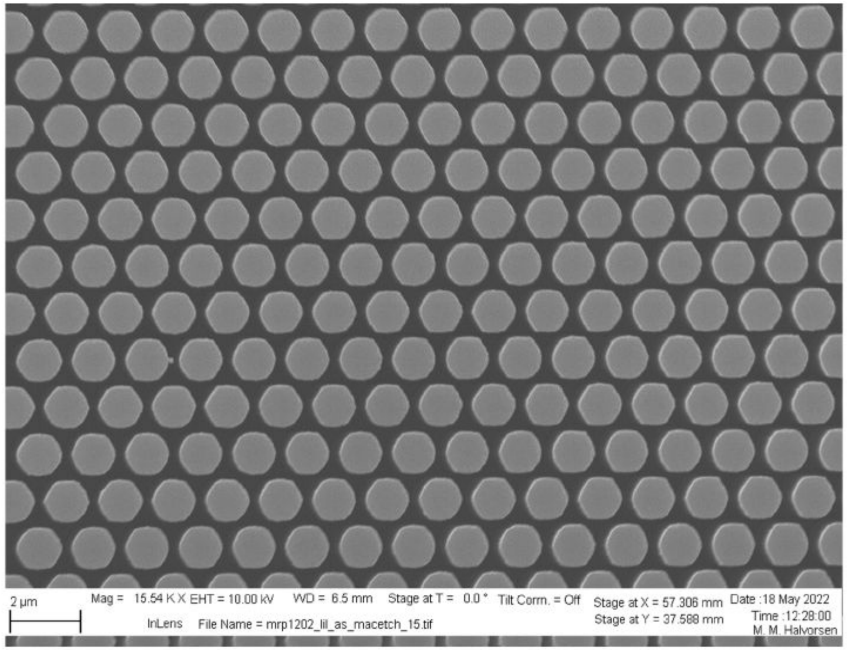


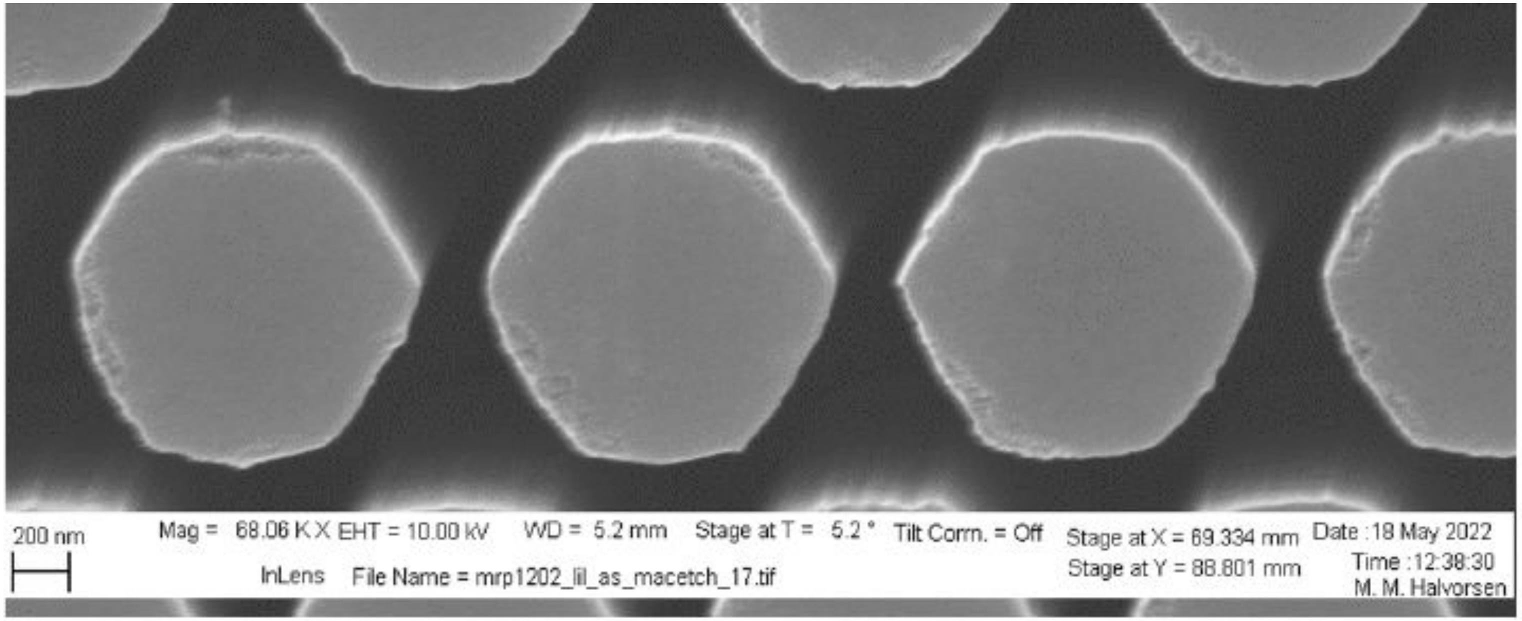
G. Ripamonti (CERN-ESE-ME)
https://indico.cern.ch/event/1138502/

Conclusion

- Advances on the ASIC design allows to integrate the requirements to the next generation of sensor
- Several sensor productions under study (planar, 3D, soon new 3D and iLGAD production)
- SiEM MacEtch based fabrication being tested, DRIE test structure by end of 2023.
- TPX4 telescope close to completion
- Phase 2 program will build on what was developed in phase 1 (ASIC,sensor and charact. tools)

SiEM pillar array from MacEtch process





Backups

3D Sensors

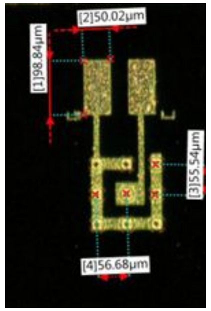
3D Sensors: Decoupling of charge generation and drift volume

Pros

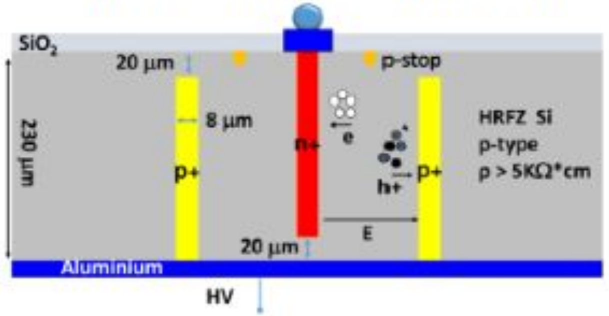
- High radiation tolerance up to several times $10^{17}\ n_{eq}/cm^2$
- Short drift distance with fast rise time
- Reduced Landau fluctuation, practically non-existent for perpendicular tracks

Cons

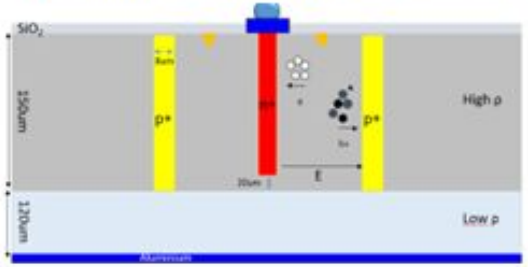
- Non-uniform field geometry
- High cost (depending on process)
- Increased cell capacitance



Double Sided
(thicker, more expensive)



Single Sided
(thinner, simpler process)

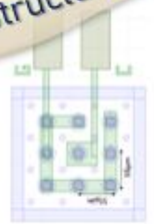


Irradiation Campaign

✓ *Irradiated with protons and neutrons up to $1 \times 10^{17}\ n_{eq}/cm^2$*
- ➢ *25 GeV p^+ @ CERN PS*
- ➢ *JSI fast neutrons @ TIGRA Reactor*

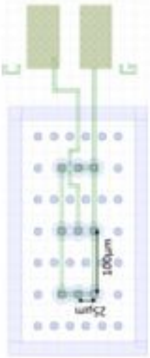
Tested Structures

ATLAS IBL Type

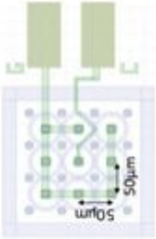


- ✓ Double sided n-on-p process
- ✓ Pixel Size $55 \times 55\ \mu m^2$
- ✓ Active thickness 230 μm
- ✓ High Resistivity (> 2 kΩm × cm) Fz silicon

ATLeS Pre-Production type



- ✓ Single sided n-on-p process
- ✓ Pixel Size $25 \times 100\ \mu m^2$
- ✓ Active thickness 150 μm
- ✓ High Resistivity (> 2 kΩm × cm) Fz silicon



- ✓ Single sided n-on-p process
- ✓ Pixel Size $50 \times 50\ \mu m^2$
- ✓ Active thickness 150 μm
- ✓ High Resistivity (> 2 kΩm × cm) Fz silicon

Planars
Irradiation campaign

what struct

Goal: Study of radiation hardness and timing in planar sensors as a function of irradiation and thickness up to $1x10^{17}$ n_{eq}/cm^2 with proton and neutron

N on p planar sensor test structure run done by ADVACAM

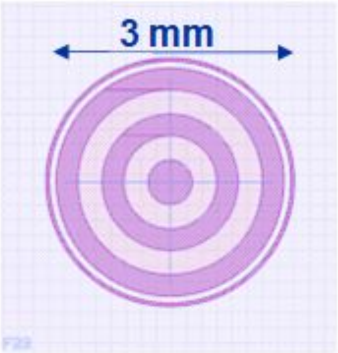
Test structures were produced in the following thickness:

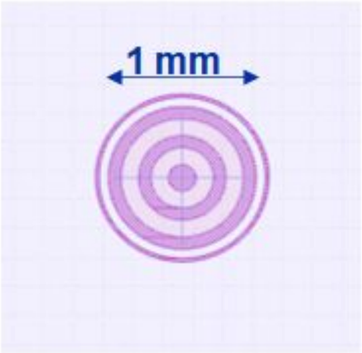
50, 100, 200 and **300** µm

Circular diodes to avoid edge effects

Test structures:

- **Small diodes** (3.14 mm^2 active area)for timing study due to lower capacitance
- **Big diodes** (28.27 mm^2 active area) for study of radiation damage and benchmarking the simulation





Fluence [n_{eq} /cm^2]	Small Diodes	Big Diodes
$1x10^{15}$	8	8
$8x10^{15}$	8	8
$6x10^{16}$	8	8
$1x10^{17}$	8	8

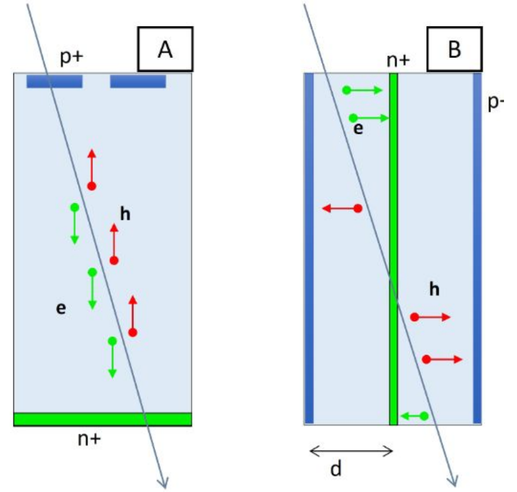
3D sensor for high precision timing measurements

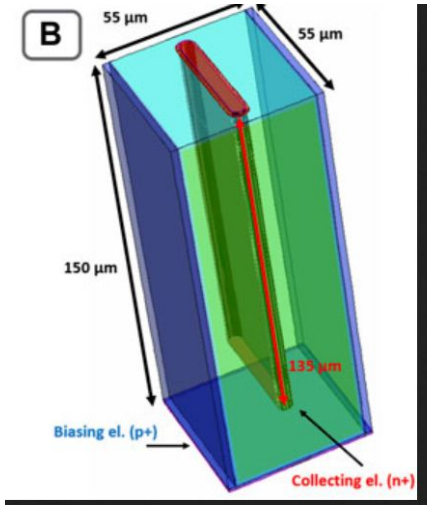
3D sensors are a good candidate for timing measurements:

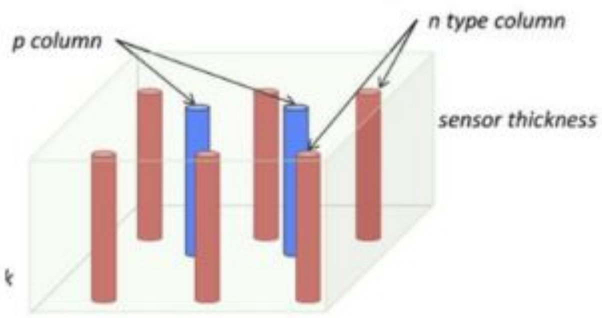
- ❑ Smaller drift distances, larger induced charge
- ❑ Low leakage current and full depletion voltage
- ❑ Radiation tolerant

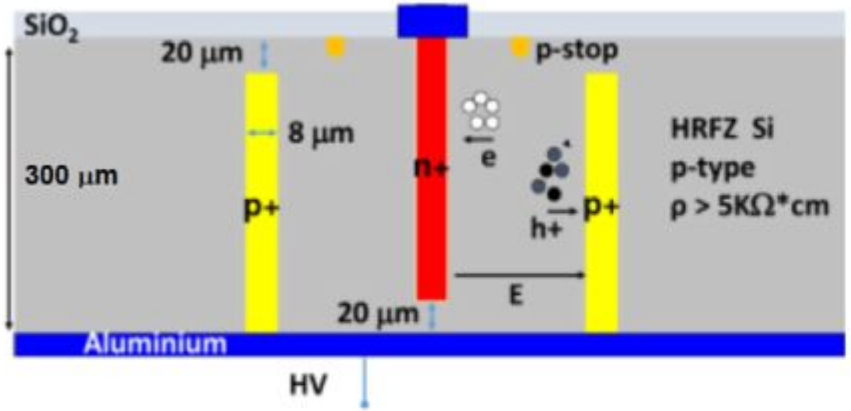
Different designs for 3D sensors:

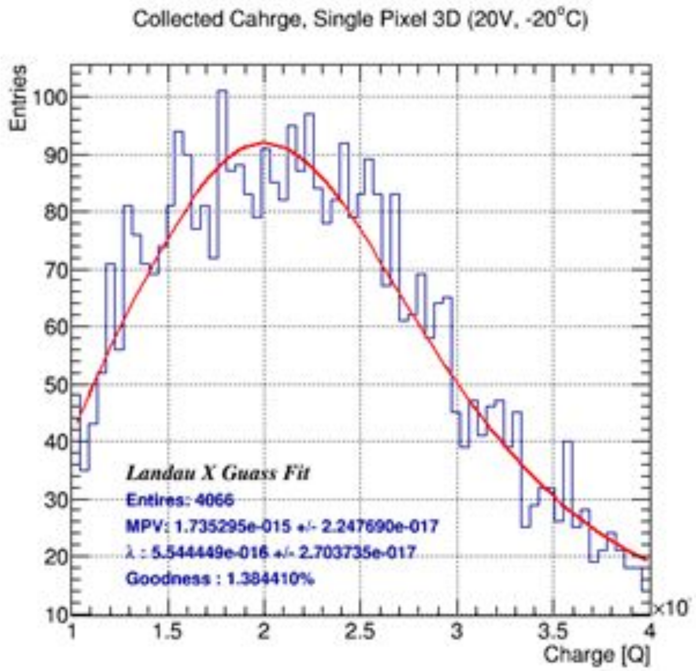
- ❑ Column-based and Trench-based designs

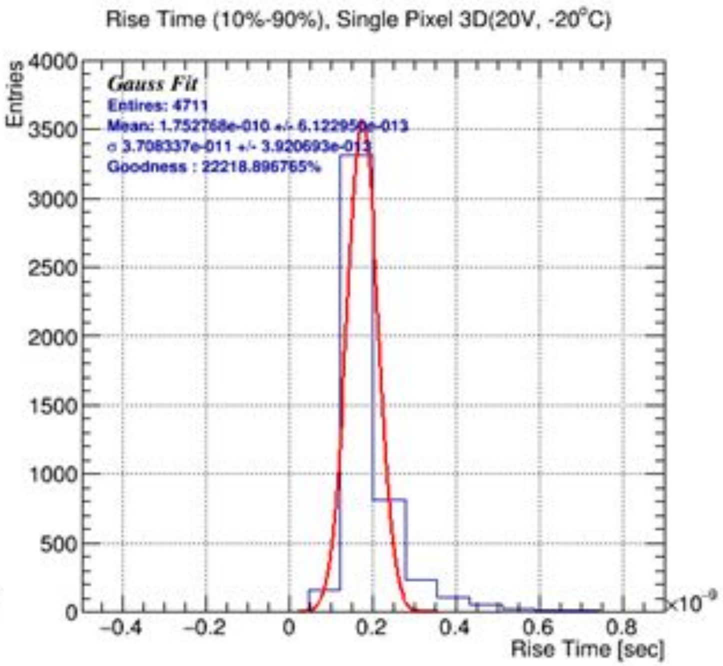


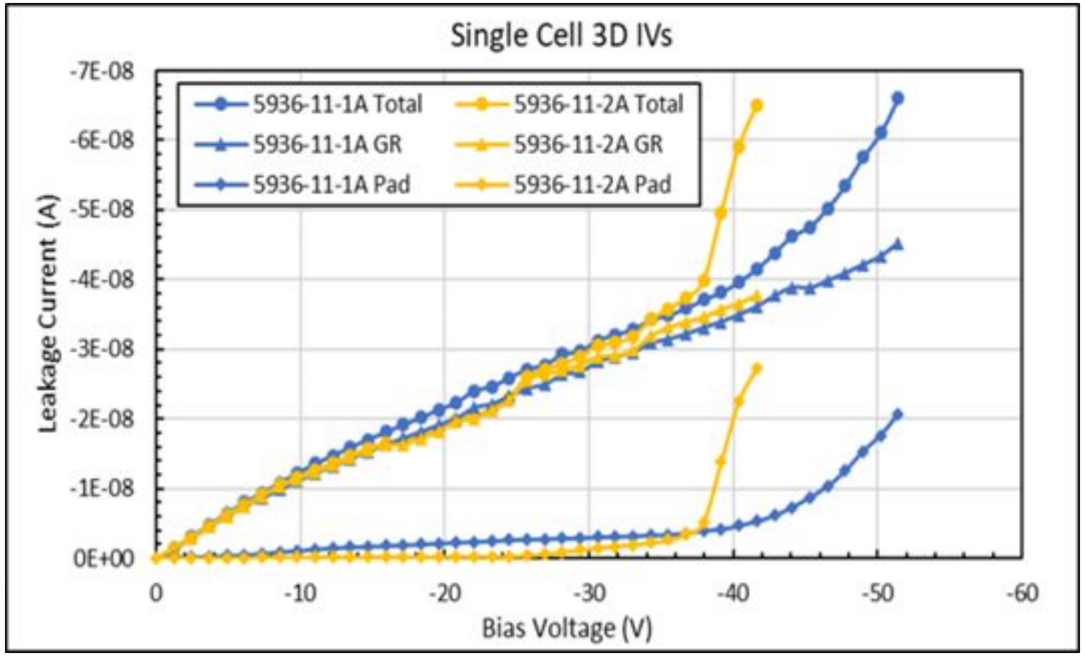






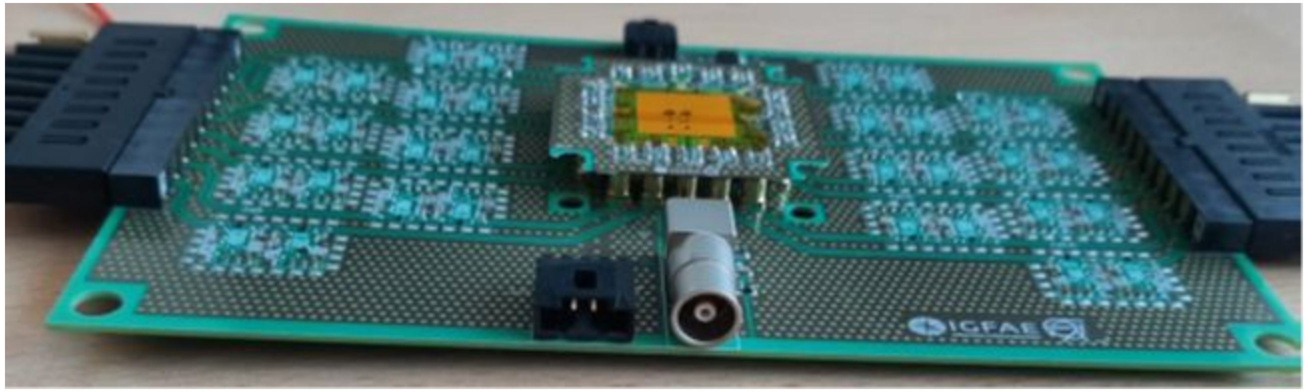

Collected Cahrge, Single Pixel 3D (20V, -20°C)
Entries
Landau X Guass Fit
Entries: 4066
MPV: 1.735295e-015 +/- 2.247690e-017
λ : 5.544449e-016 +/- 2.703735e-017
Goodness : 1.384410%
Charge [Q]

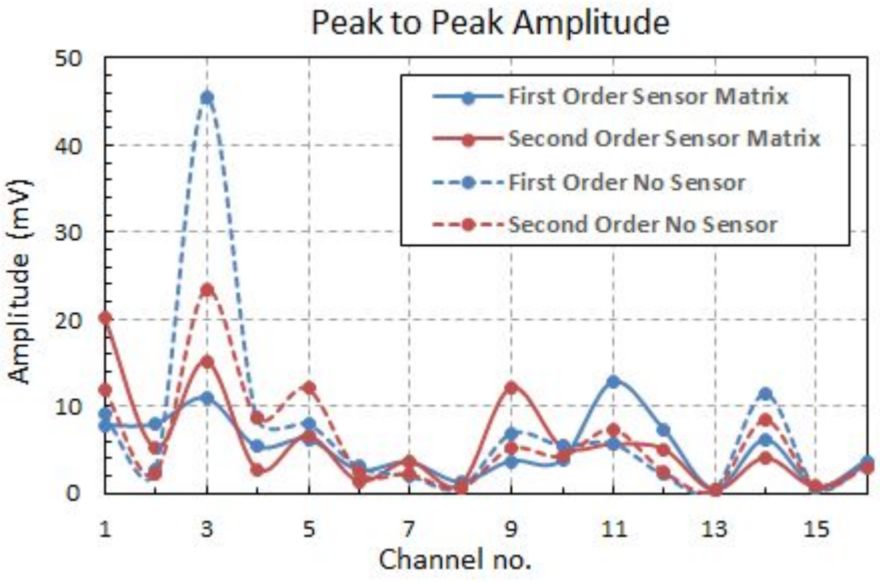

Rise Time (10%-90%), Single Pixel 3D(20V, -20°C)
Entries
Gauss Fit
Entires: 4711
Mean: 1.752768e-010 +/- 6.122950e-013
σ 3.708337e-011 +/- 3.920693e-013
Goodness : 22218.896765%
Rise Time [sec]


Single Cell 3D IVs
5936-11-1A Total
5936-11-1A GR
5936-11-1A Pad
5936-11-2A Total
5936-11-2A GR
5936-11-2A Pad
Leakage Current (A)
Bias Voltage (V)

16ch board tests
ADD ALSO A PLOT FROM ANTONIO

- High Frequency SiGe discreate electronics @ 12 GHz bandwidth
- 2 Stage configuration with a transimpedance followed by a voltage stage
- Low max current (~10mA) with well behaved gain linearity vs V_{DD}
- Ruggers 3000 High Frequency substrate
- Pre-assembled miniaturized coaxial edge connectors with panel-mounted SMA plugs (1m cable length)
- 140 x140 mm outer dimensions





Modified –Uniform design