Experience with the HGCROC from the HGCAL silicon module beam tests

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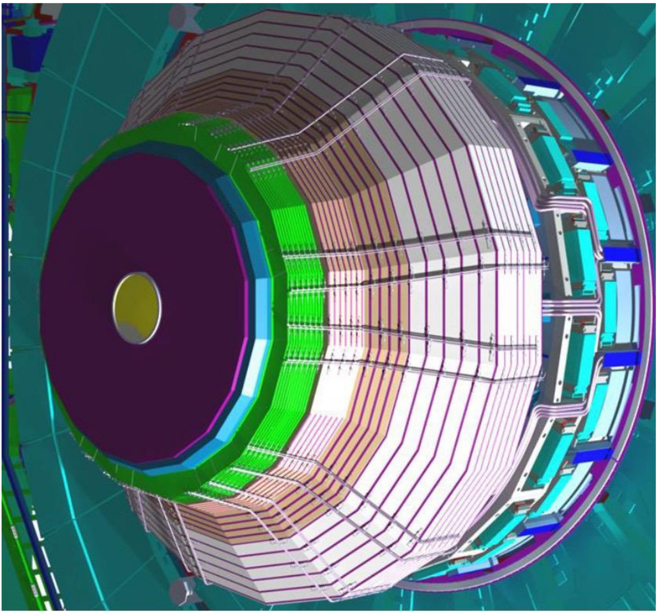
Outlines

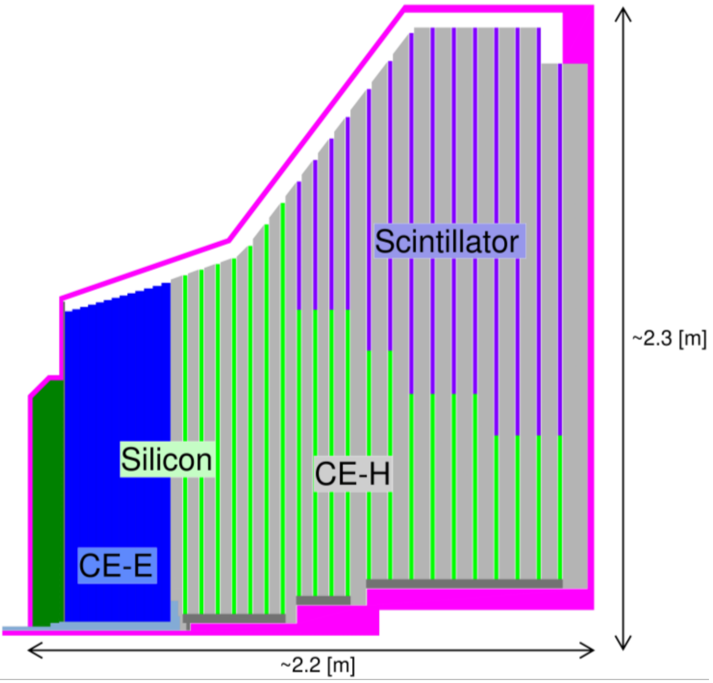
- The silicon module and electronics at the HGCAL
- The silicon module beam test 2021 and 2022
- Studies from the beam test 2021
- Studies from the beam test 2022

The HGCAL and the silicon module



As part of the phase-II upgrade of the CMS detector, **the High Granularity Calorimeter (HGCAL)** will replace the existing endcap calorimeters, to satisfy the stringent requirements from the **high irradiation and pileup** during the **High Luminosity Large Hadron Collider (HL-LHC)**.

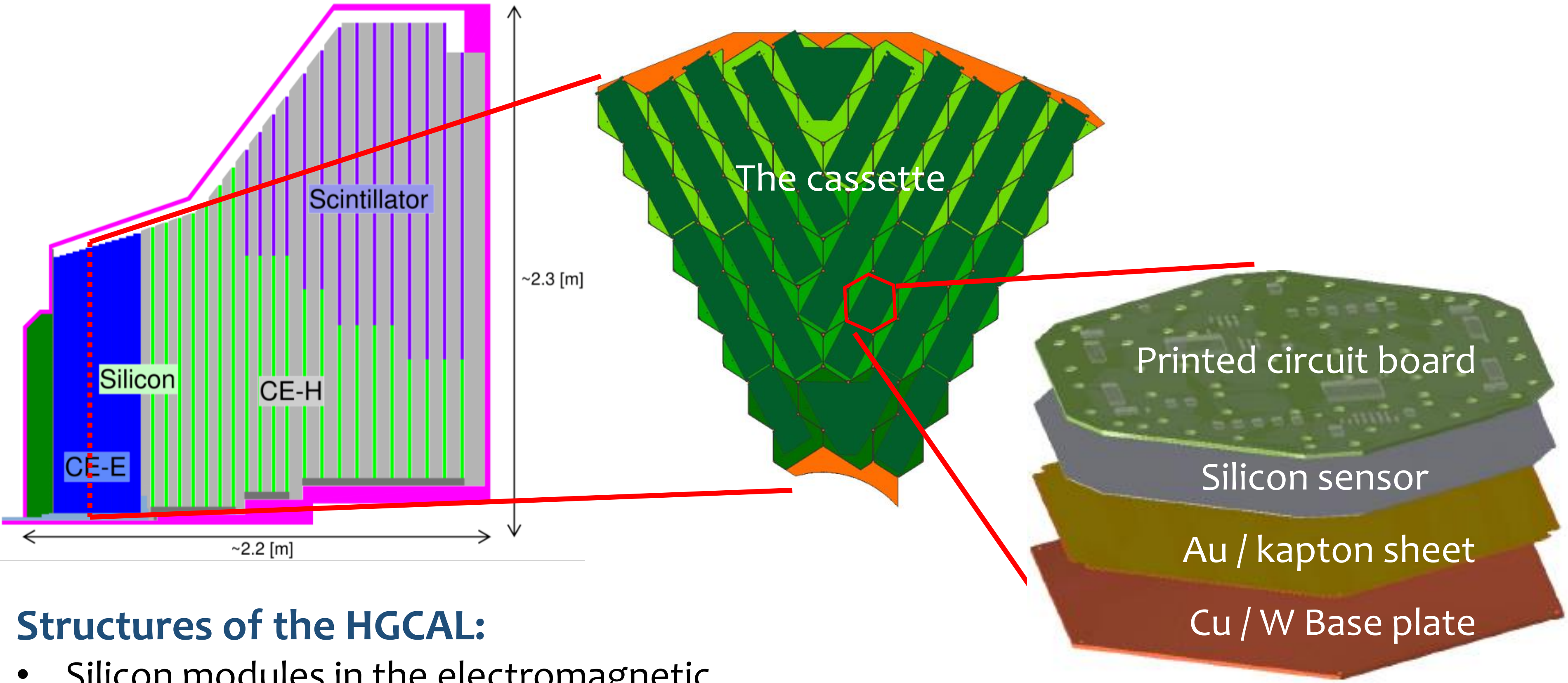
The HGCAL and the silicon module



Structures of the HGCAL:

- Silicon modules in the electromagnetic section (**CE-E**).
- Mixture of silicon modules and scintillator tile-modules in the hadronic section (**CE-H**).

The HGCAL and the silicon module



Structures of the HGCAL:

- Silicon modules in the electromagnetic section (**CE-E**).
- Mixture of silicon modules and scintillator tile-modules in the hadronic section (**CE-H**).

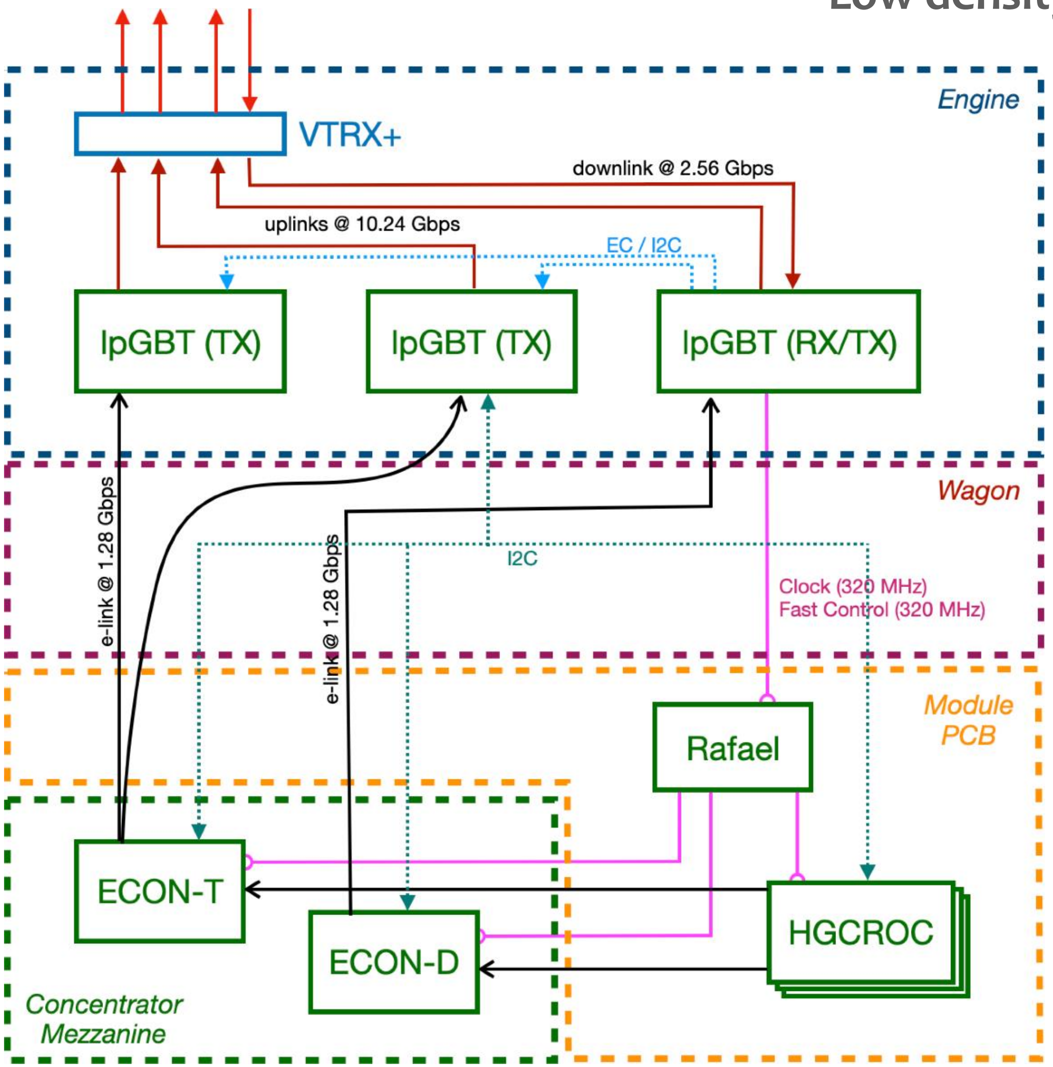
The HGCAL front-end electronics [presentation by N. Strobbe]

- **HGCROC-Si**: frontend readout chip, receives and digitizes signals from the Si sensors
- **ECON-T**: frontend concentrator chip for trigger path, concentrates trigger channel data via one of 4 trigger algorithms
- **ECON-D**: frontend concentrator chip for DAQ path, performs channel alignment and zero suppression after L1Accept
- **Rafael** chip for clock and fast control fanout
- CERN **lpGBT** for sending/receiving data/clock/control signals via optical link (and **VTRX+**)

HGCAL-specific
CMS-specific
LHC-wide

The HGCAL front-end architecture [presentation by N. Strobbe]

Low density region



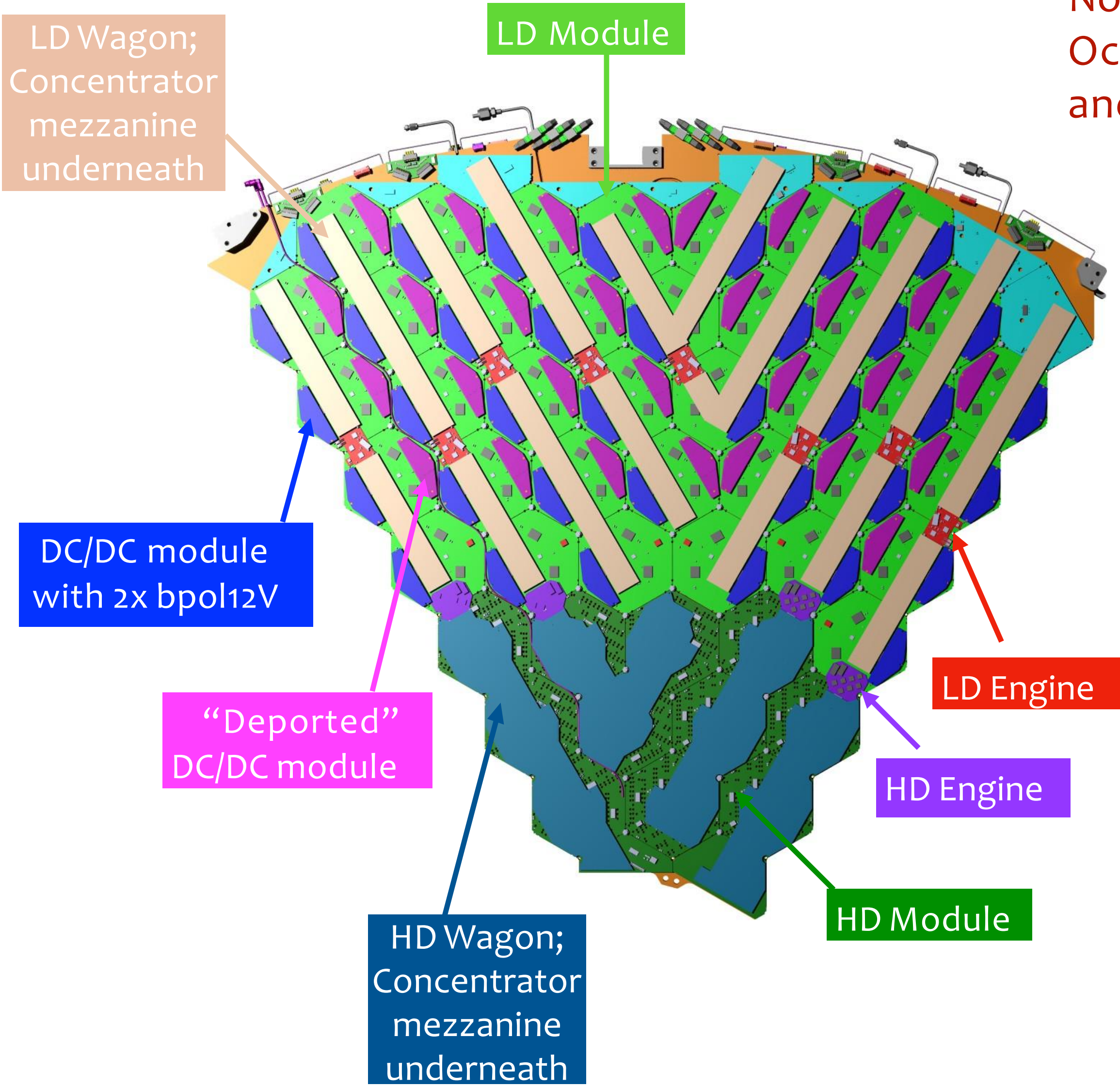
Engine board is connected to 2 Wagon boards

Passive Wagon board is connected to 1 - 4 Modules

Module is composed of the Si sensor and hexaboard PCB

HGCROC and ECONs are custom for this project, all other chips and components are common developments!

The modular implementation [presentation by N. Strobbe]



Note: each layer is different! Occupancies vary greatly within and between layers

Low density (LD) region

- Si sensor 200 or 300 μm thickness
- 192 channels (3 HGCROC) per 8” hexagonal module

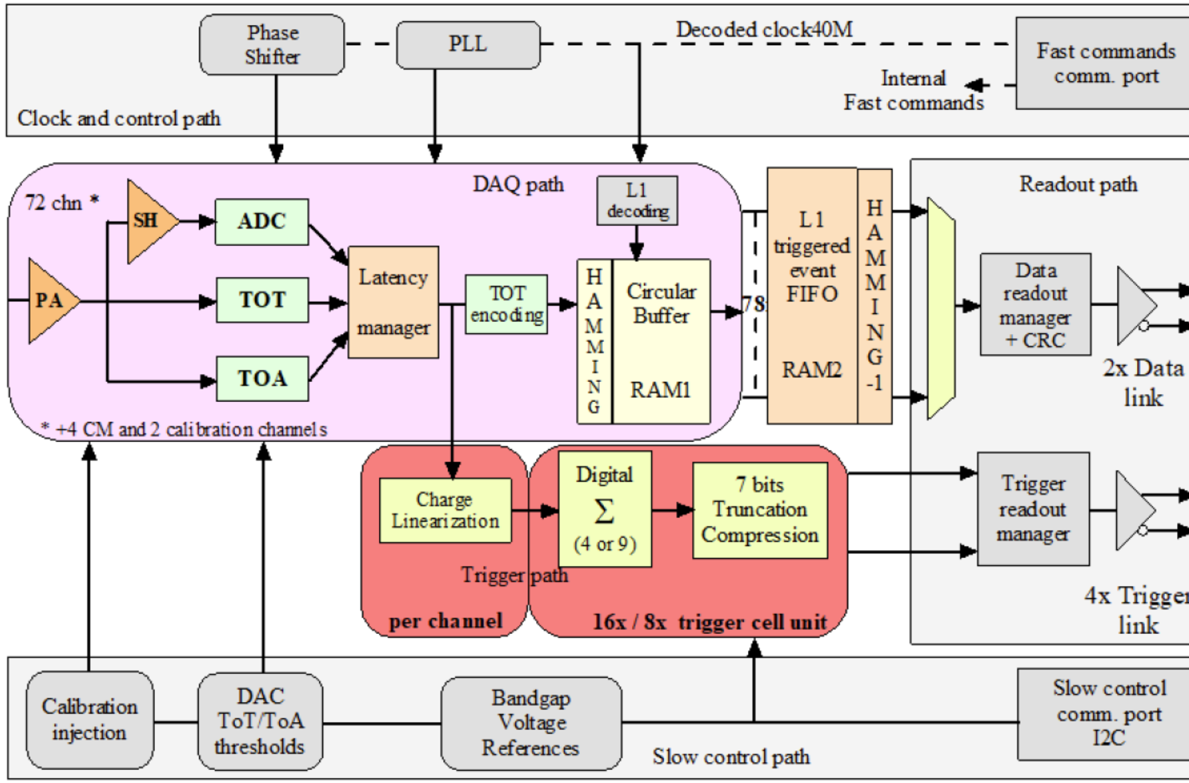
High density (HD) region

- Si sensor 120 μm active thickness
- 432 channels (6 HGCROC) per 8” hexagonal module

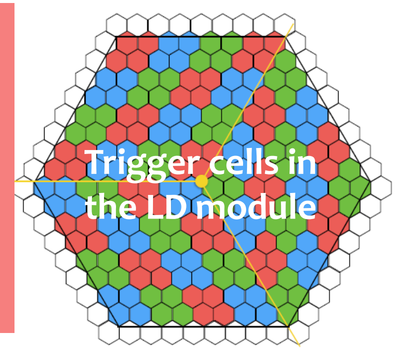
The HGCROC at the HGCAL

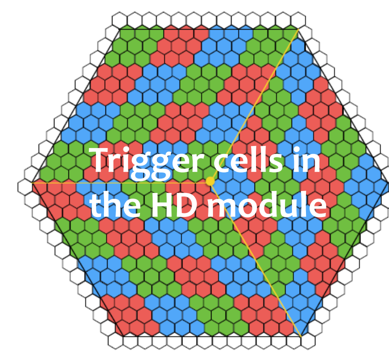
HGCROCv3 as the front-end readout ASIC on the hexaboards

- 40 MHz clock in phase with the 25ns bunching crossing (BX) at the LHC
- Precise measurements of the collected charges in the silicon sensor (**ADC** + **TOT**) and time (**TOA**).
- Two identical halves in one chip. In each half:
  - 36 readout standard channels
  - 1 readout calibration channel
  - 2 common mode channels (coherent noise estimation)
- Two DAQ 1.28 Gbps CLPS output links



- Compressed data of the charge @ 40 MHZ for **L1 trigger**.
  - **Charge linearisation** over ADC / TOT range
  - **Reduced granularity**: 48 trigger cells per module
  - **Charge encoded** in 7 bits for bandwidth (4b exponent + 3b mantissa)
- Four trigger 1.28 Gbps CLPS output links (2 for HD)





The ECON at the HGCAL

The ECON (Endcap Concentrator ASIC) concentrates data to reduce #links to backend

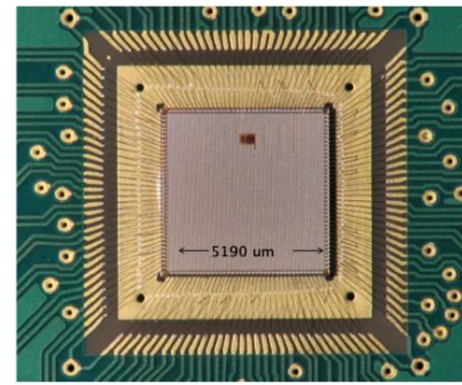
ECON-D: performs most digital processing of sensor data for events passing L1 trigger at 750 kHz

- zero suppression with programmable corrections
- time-analysis of error conditions to generate reset requests

ECON-T: select or compress HGCROC trigger data for transmission off detector at 40 MHz

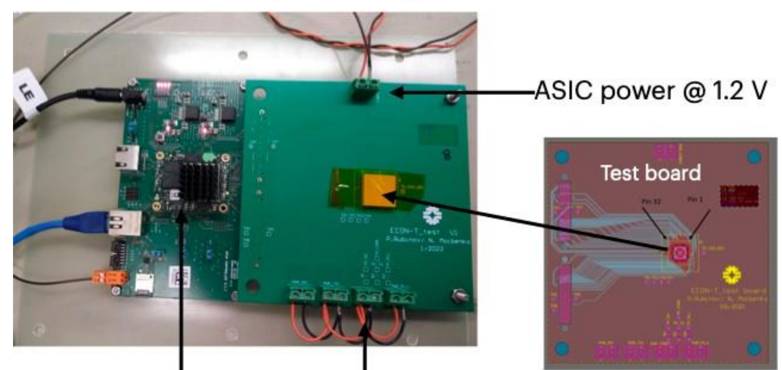
Starting from 48 Trigger Cells (TC)

Threshold-Sum	Best-Choice	Super-Trigger-Cell	Encoder
Variable-latency Chooses TC above threshold	Fixed-latency Sorts TC by charge Q, sends N with largest Q	Fixed-latency Groups TC and forms larger STCs	Fixed-latency Fully reconfigurable Encodes with CNN



ECON-T-P1 die mounted directly on PCB and wirebonded

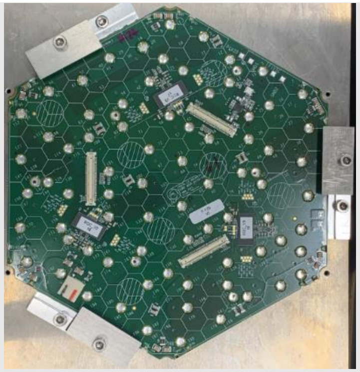
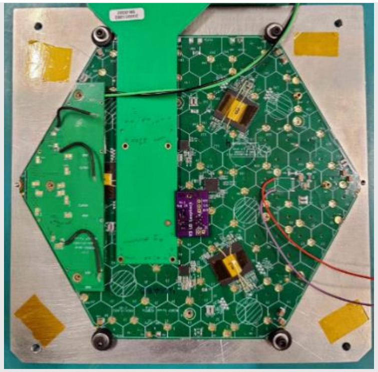
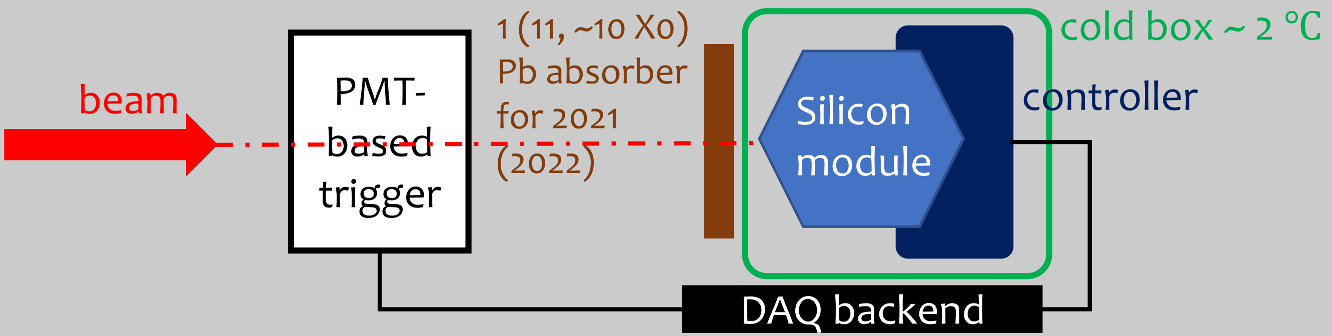
Chip-on-board @ bench



First ECON-T-P1 chips received, ~ 80% functionality tested, no major issues found

First SEE test campaigns completed: Preliminary results indicate excellent performance of configuration registers, no issues requiring human intervention

The HGCAL beam test 2021 and 2022

	Beam test 2021	Beam test 2022
Time / location	6th – 13th Oct. 2021, SPS H2 beamline	5th – 12th Oct. 2022, SPS H2 beamline
The silicon module	**NSH** LD module assembled by IHEP; 300 μm silicon sensor with 250 V bias voltage (BV) 	**V3** LD module assembled by UCSB; 300 μm sensor with 270 V BV; **LD HGCROCv3 packages**; **Expect low coherent noise** 
Setup		
Beam	20 - 100 GeV electron	20 – 250 GeV electron; 150 GeV pion
Preamplifier gain	Higher (ADC range 80fC), Default (160 fC), Lower (320 fC)	
Variables	**Trigger phase** with respect to the 40 MHz clock √	
	ADC values in the current bunch crossing (BX) (**ADC**) and previous BX (**ADCm**) √	
	TOA, TOT, trigger primitive ×	**TOA, TOT, trigger primitive** √

The HGCAL beam test DAQ system

Hexaboard interface (95 IO)

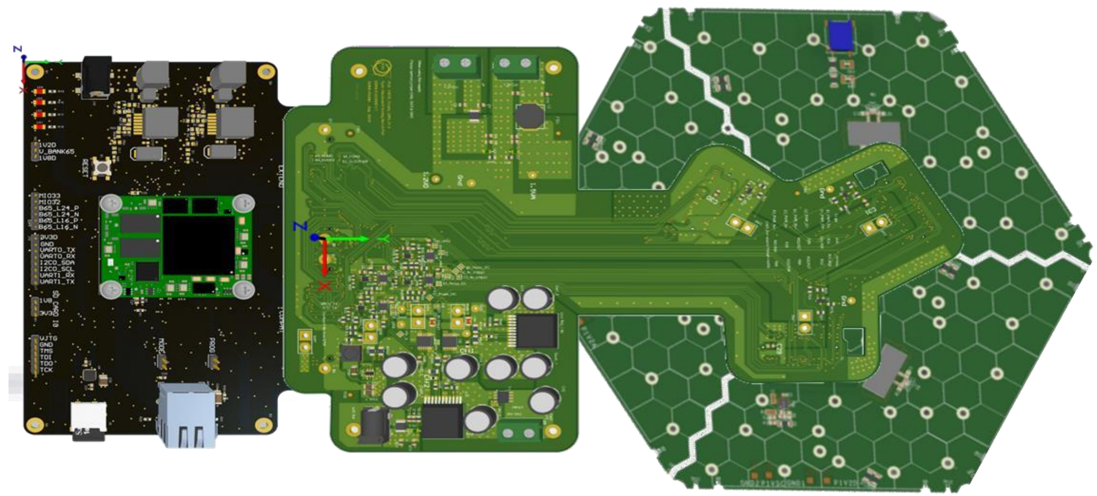
- 21 low speed control lines (used by the hexaboard)
- 5 I2C lines (clock, data)
- 4 low speed control lines (used for ADC Ready signals)
- 30 high speed differential lines (3x4 data + 3x4 trg + 3 clk320 +3 fcmd)

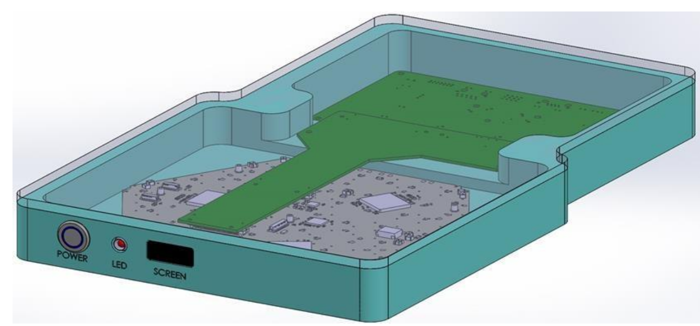
Trigger interface (8 IO)

- 4x Differential signal on RJ45 connector.

Processing system side

- 2 x userIO
- 1 x Serial
- 1 x I2C





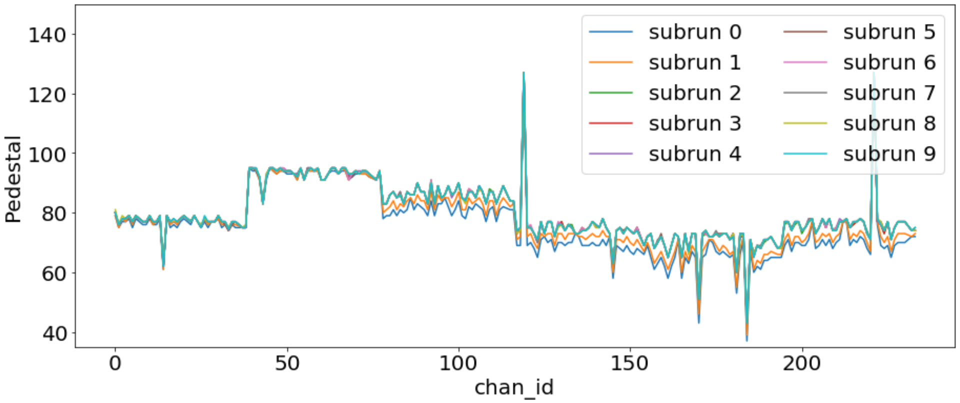
Results of the HGCAL silicon module beam test 2021

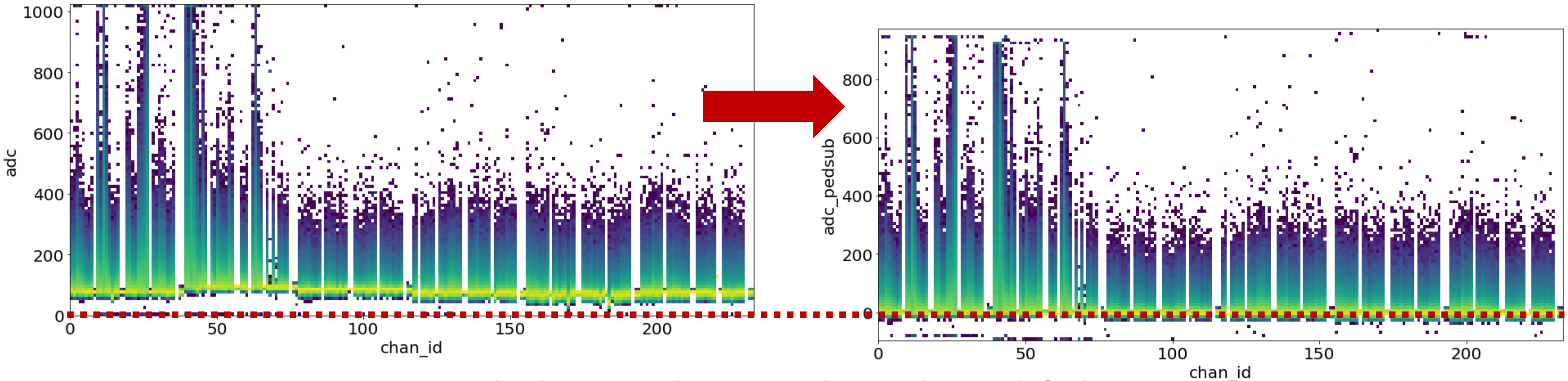
Pedestal subtraction

- Pedestals in each channel are equalized and trimmed to use the full dynamic range of the ADC values.

➢ Pedestal subtraction method

- Can't use pedestal runs to do pedestal subtraction reliably.
- Pedestal is computed from ADCm in the beam runs since it lacks signals
- The ADC in all events should be subtracted by the pedestal as a function of channel

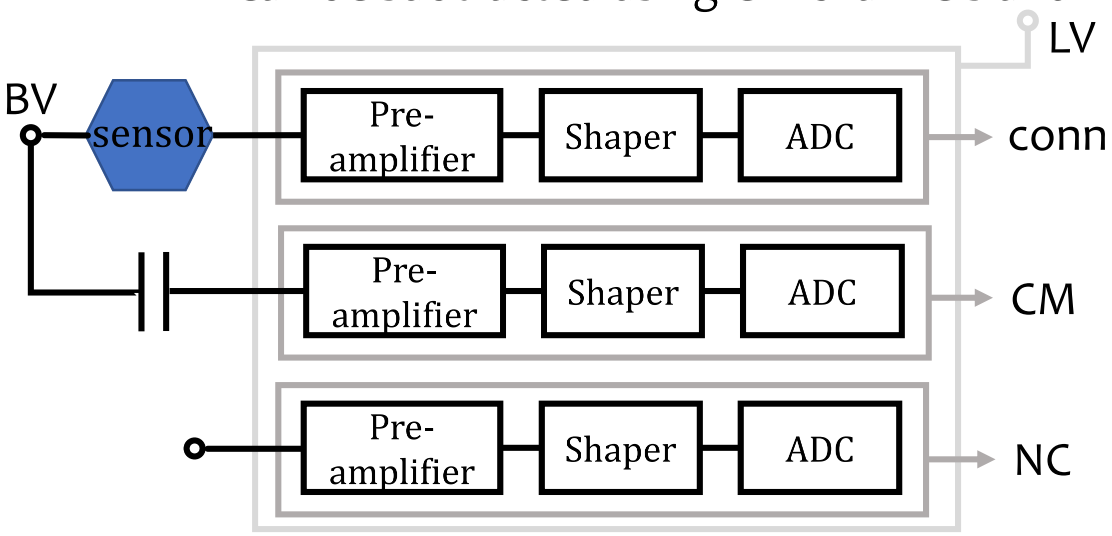




Example: dataset with 100 GeV electron beam, default gain

Common mode noise subtraction

- **Intrinsic noise:**
  - Noise generated by the channel
  - Can do nothing with it
- **Common mode (CM) noise:**
  - Caused by the variation of bias voltage (BV) and low voltage (LV, power supply of the chip)
  - Correlated in different channels
  - Can be subtracted using CM channels and non-connected (NC) channels

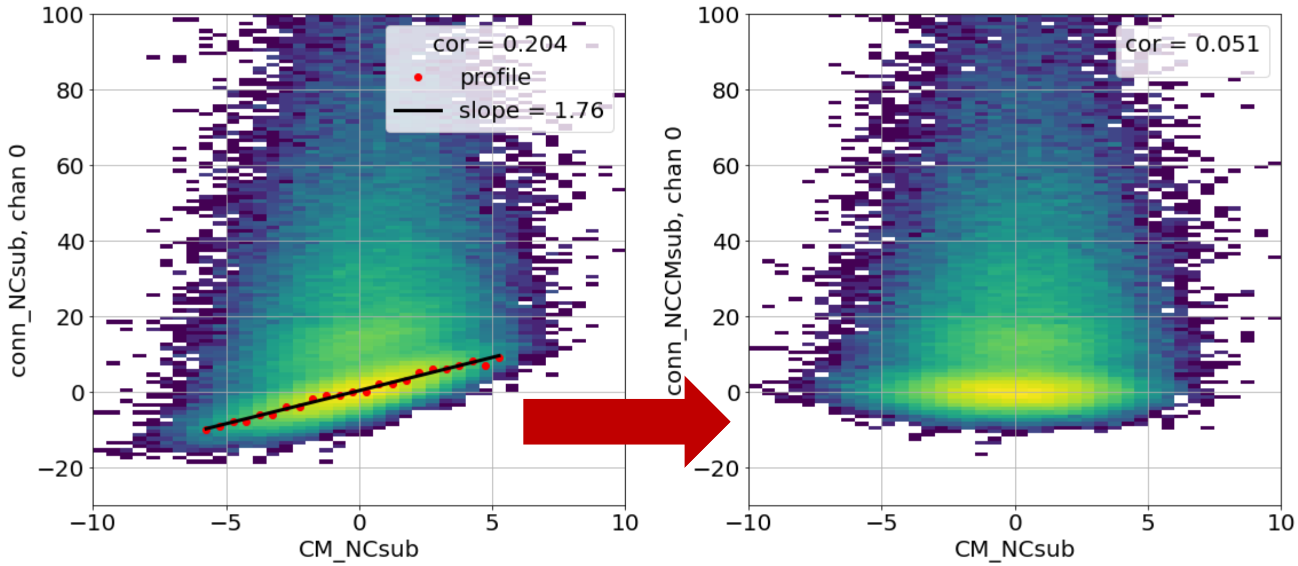


	Beam	BV	LV
conn	√	√ 3	√ 2
CM	×	√	√ 1
NC	×	×	√

- **Noise subtraction method**
  - ADC_NCsub(CM) = ADC(CM) – k1·ADC(NC) – b1 (1)
  - ADC_NCsub(conn) = ADC(conn) – k2·ADC(NC) – b2 (2)
  - ADC_NCCMsub(conn) = ADC_NCsub(conn) – k3 ·ADC_NCsub(CM) – b3 (3)

Common mode noise subtraction

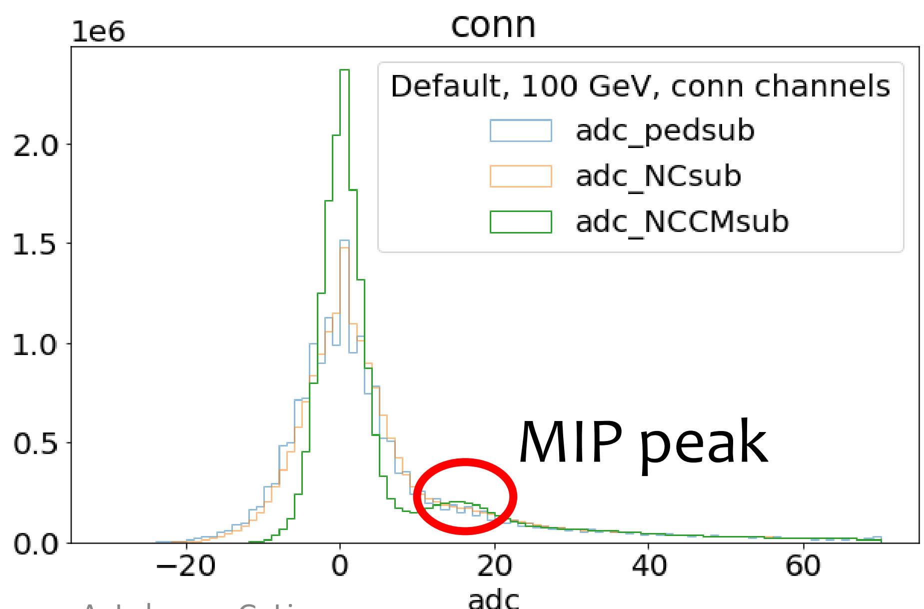
- Example of step 3



- Reduction of noise

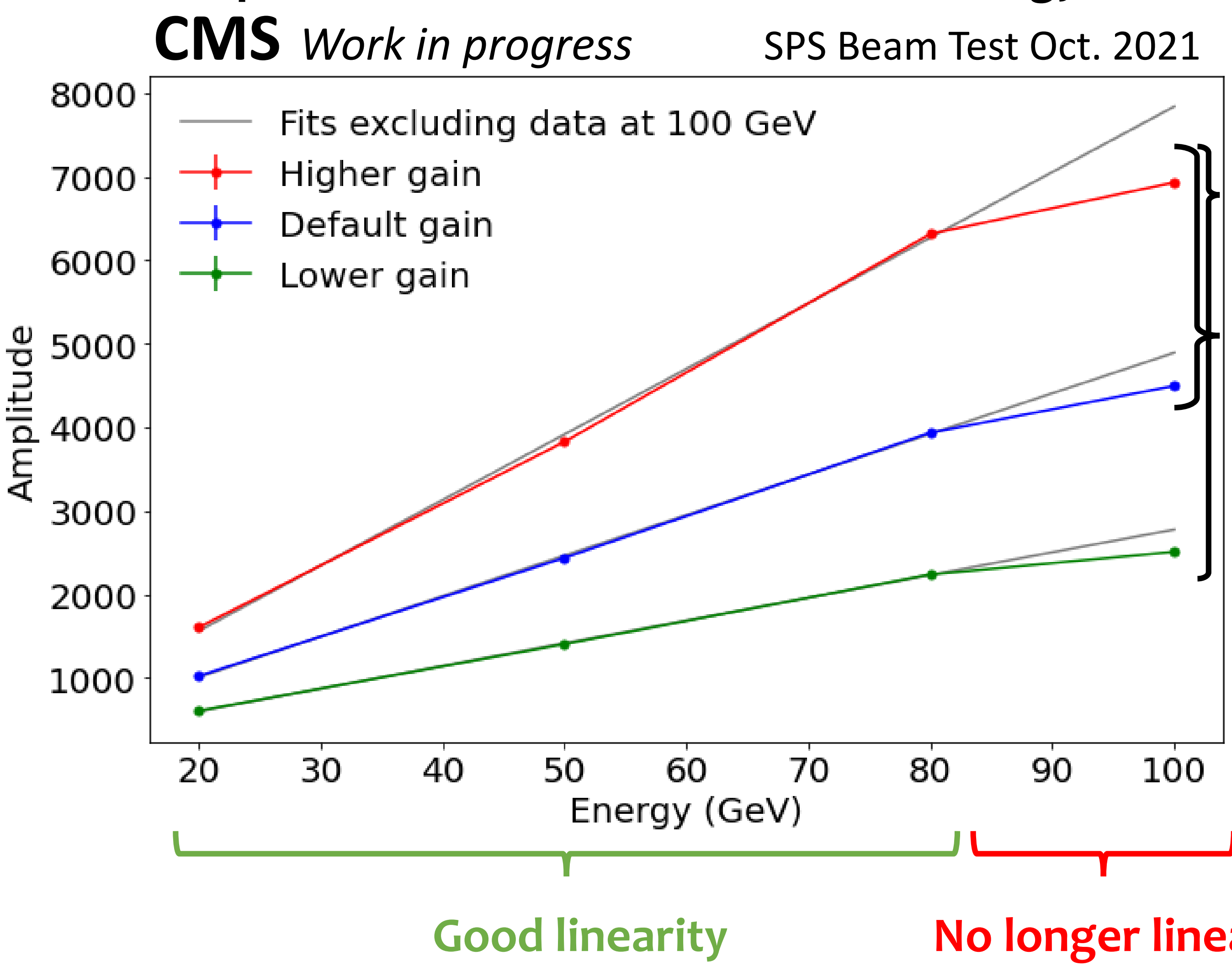
Stages	Noise
adc_pedsub	5.4
adc_NCsub	5.0
adc_NCCMsub	2.6

CM noise reduced a lot



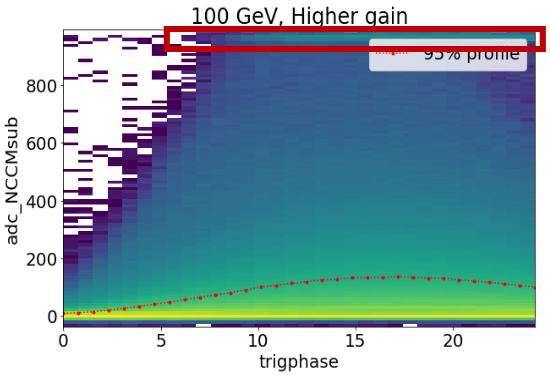
Linearity w.r.t. beam energy

- Summed ADC in connected channels v.s. trigger phase (pulse shape) -> fit the pulse shape -> get the amplitude (see backup for more details)
- **The amplitude as a function of the beam energy is shown.**



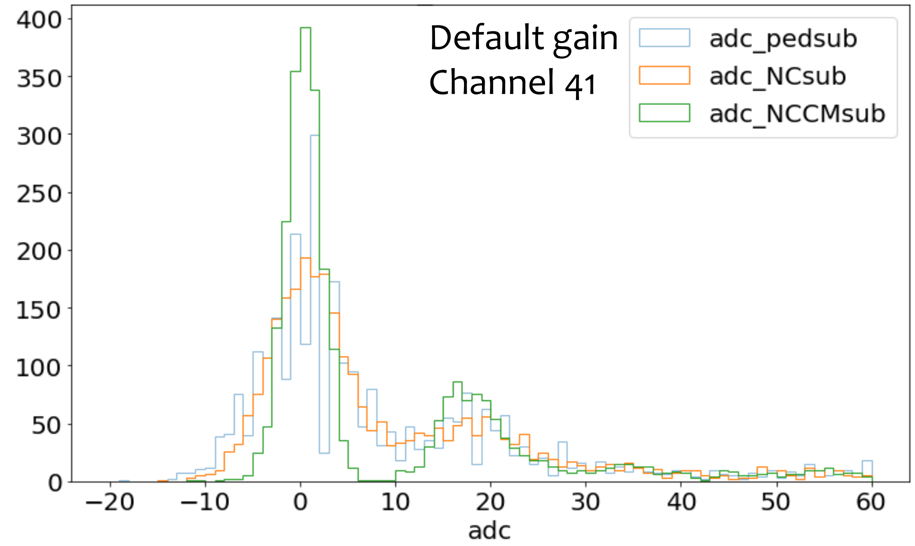
Reasons for the non-linearity

- The module is not at shower maximum for 100 GeV beam energy.
- ADC saturates at Higher and Default gain even not sampling at shower maximum: **need TOT for energy measure.**

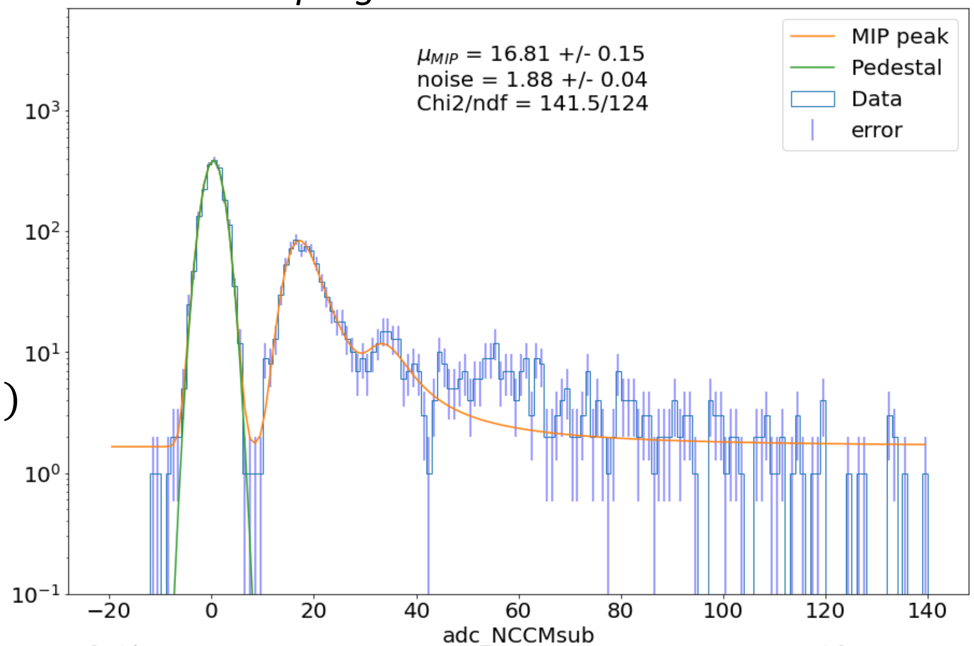


MIP peak reconstruction

- Datasets: 100 GeV electron beam datasets without the absorber
  - Provide MIP-like signature
  - Good beam quality: high rate, narrow
- Similar pedestal and CM noise subtraction methods are applied
- Best trigger phase is selected to have the highest signal amplitude
- MIP peaks seen in the adc distribution



CMS *Work in progress* SPS Beam Test Oct. 2021



➢ MIP peak fit

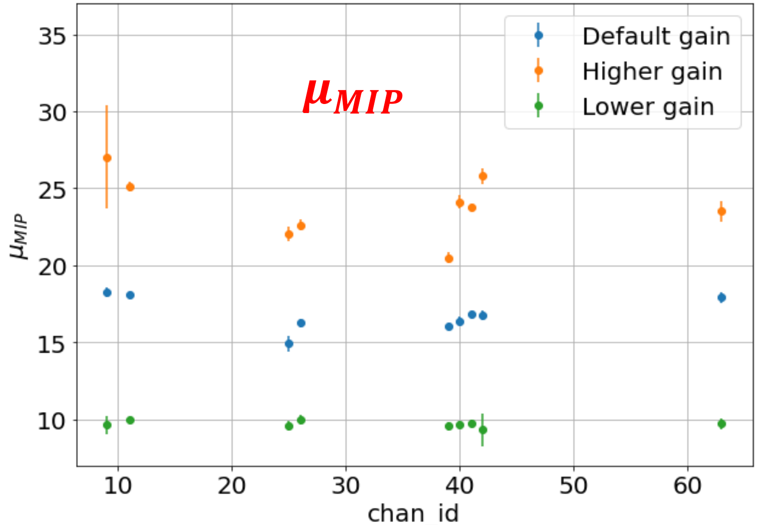
$$S(x \mid c, A_0, \mu_0, \sigma_0, A_1, A_2, \mu, \sigma) =$$
$$c + A_0 \cdot \mathrm{Gauss}(x, \mu_0, \sigma_0)$$
$$+ A_1 \cdot \mathrm{Landau}(x, \mu_0 + \mu_{MIP}, \sigma) \otimes \mathrm{Gauss}(x, 0, \sigma_0)$$
$$+ A_2 \cdot \mathrm{Landau}(x, \mu_0 + 2\mu_{MIP}, \sqrt{2}\sigma) \otimes \mathrm{Gauss}(x, 0, \sigma_0)$$

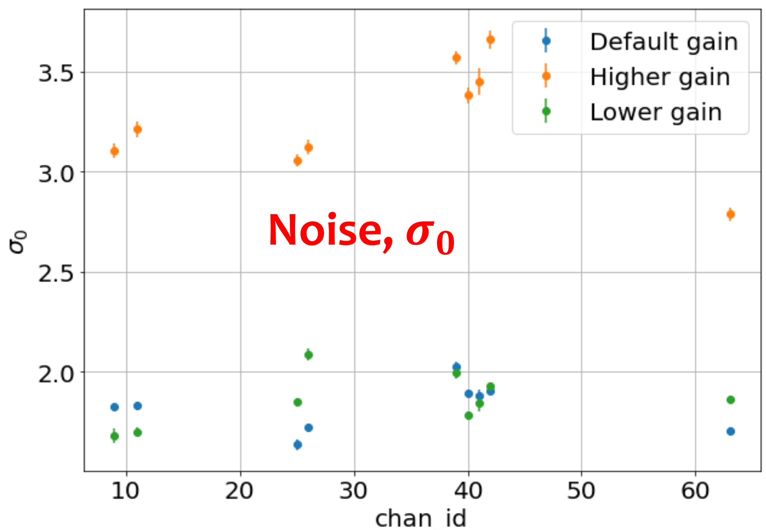
- Fit works well.

MIP peak reconstruction

Results in other channels

- Only channels exposed to the beams are shown (they are all full pads).





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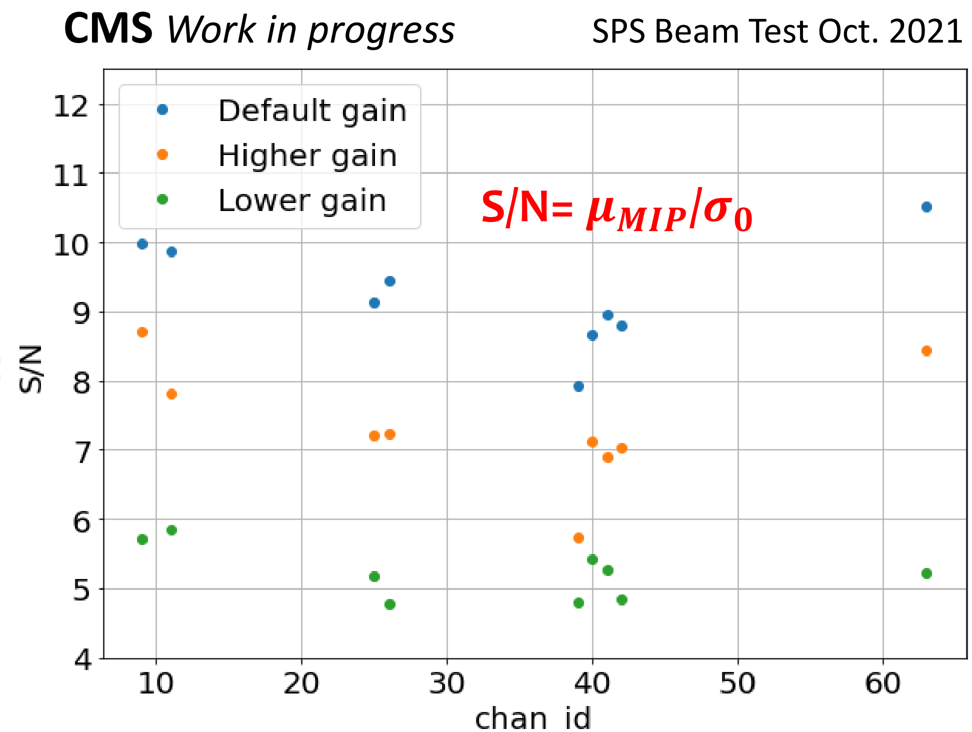
Signal-to-noise ratio

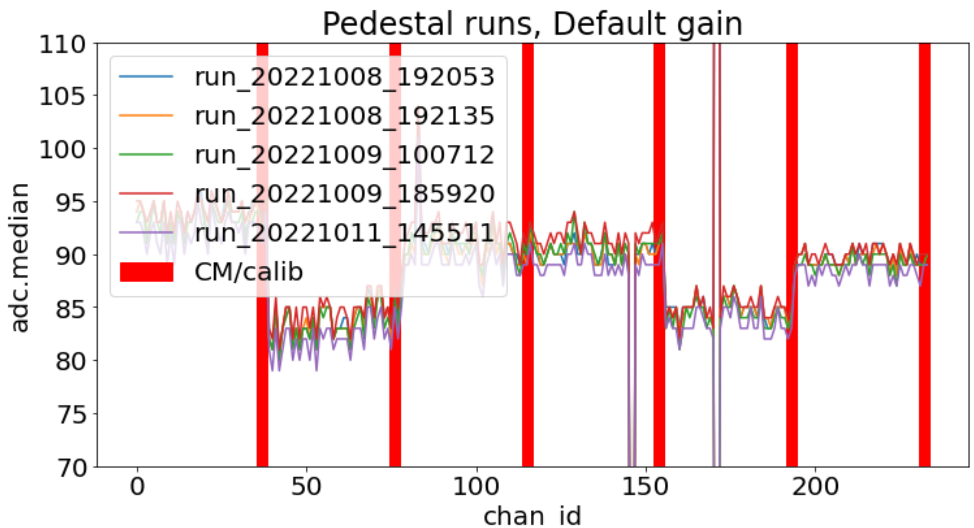


- 9 ~ 10 in the Default gain
- Only around 5 in the Lower gain

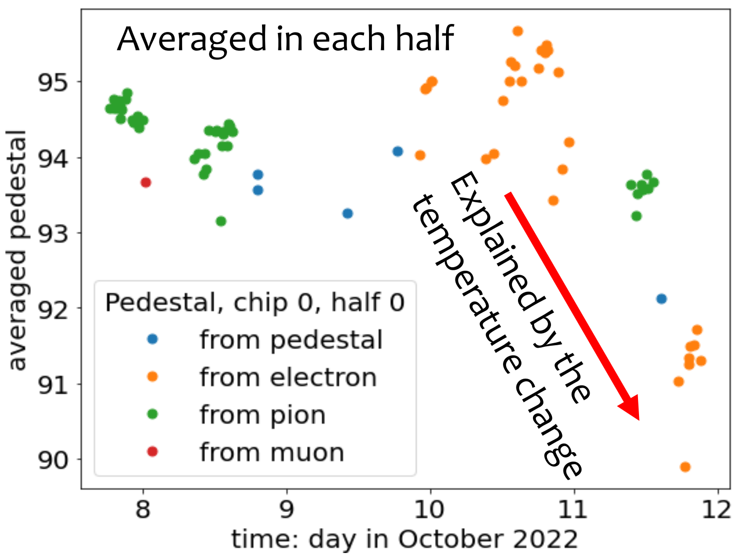
Results of the HGCAL silicon module beam test 2022

Pedestal subtraction

- Pedestal trimmed to be similar in each half



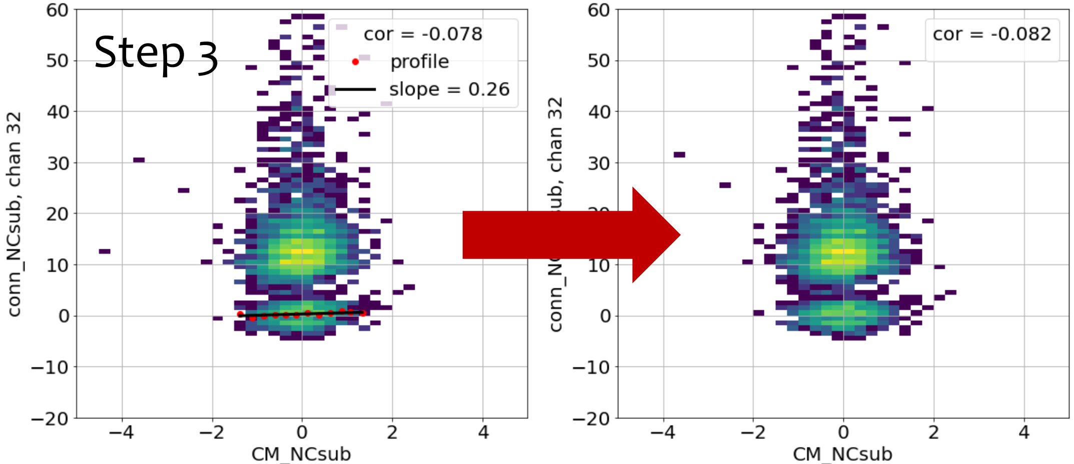
- Pedestals estimated from ADC in the pedestal runs and ADCm in the beam runs

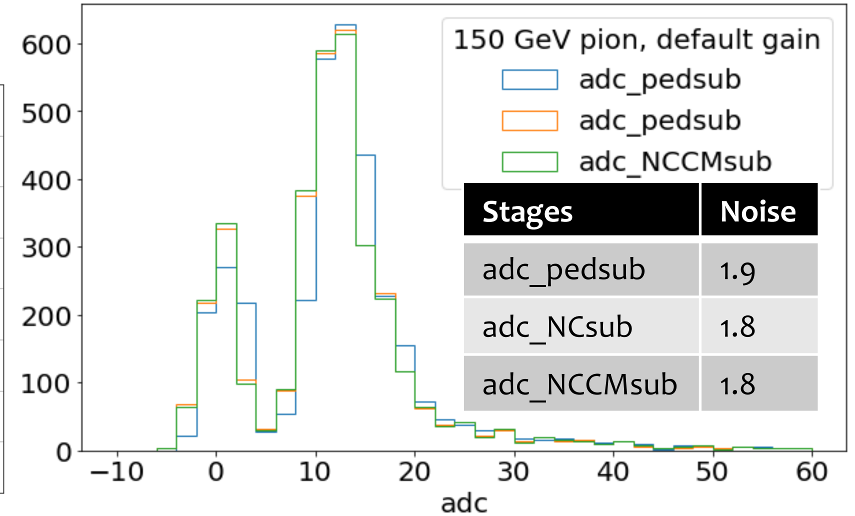


- Except the runs in the last day, pedestals are relatively stable regardless of the run types.
- **Pedestal runs can be used for pedestal subtraction in the beam runs.**

CM noise subtraction

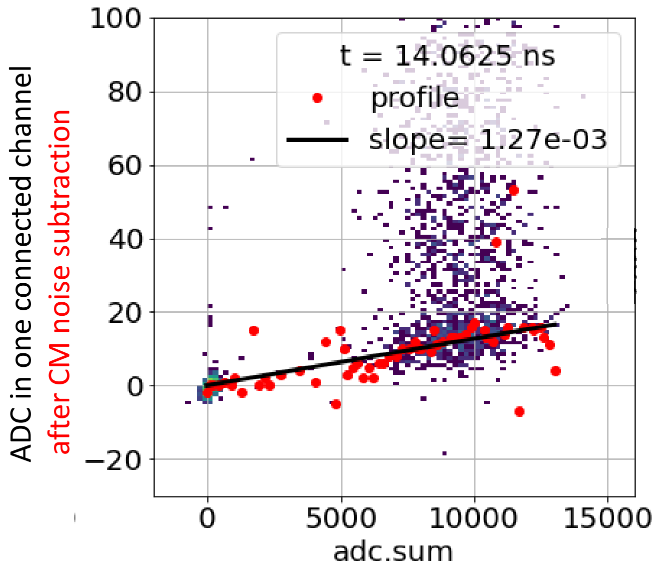
- Noise is lower by design, especially CM noise
- CM noise is negligible for pion data





Stages	Noise
adc_pedsub	1.9
adc_NCsub	1.8
adc_NCCMsub	1.8

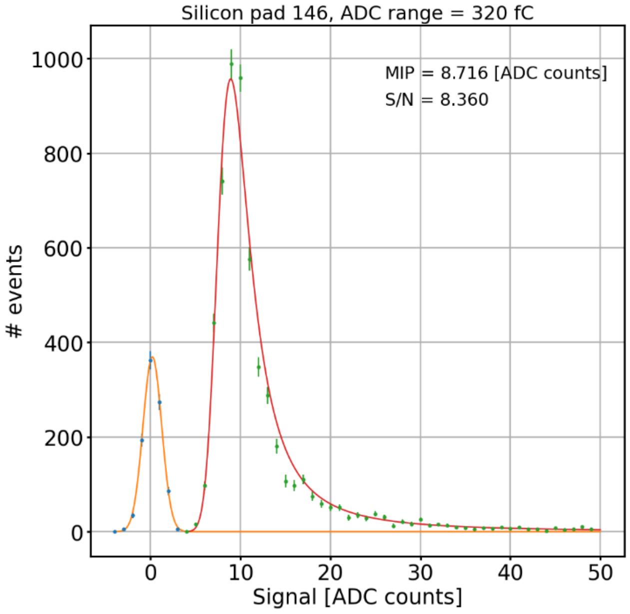
- For the electron beam data, the **shower effects** make things non-trivial.

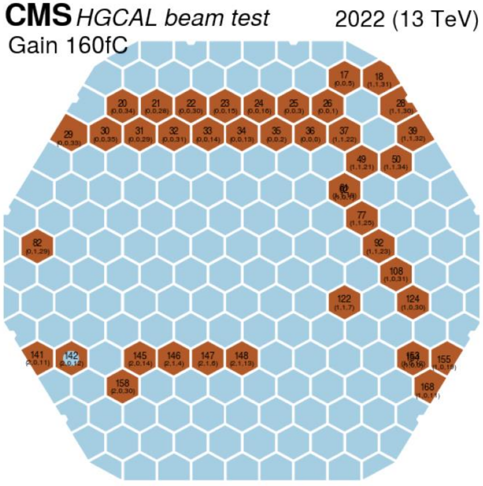


More studies are needed to accurately subtraction CM noise

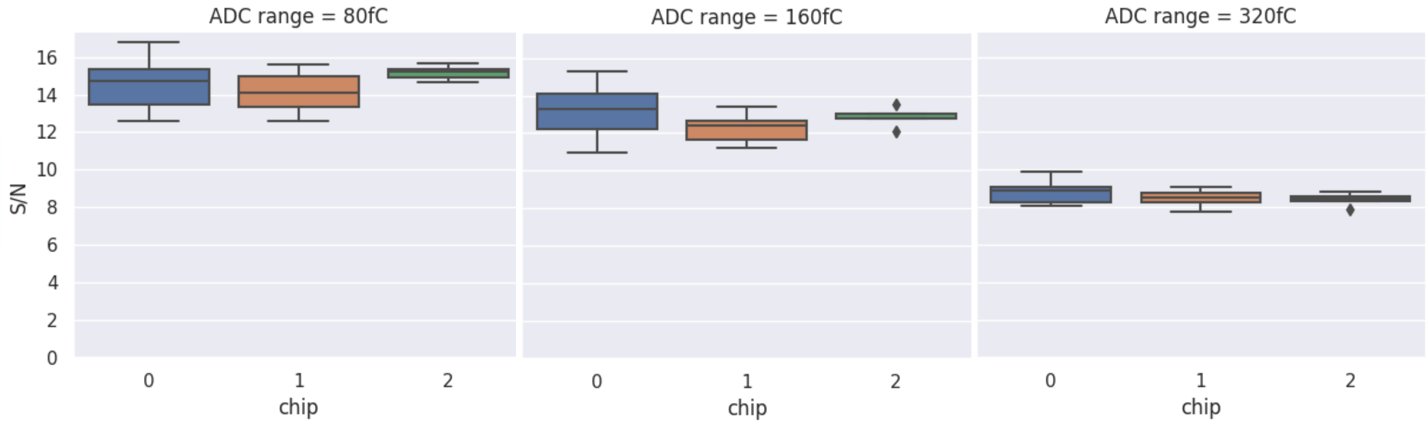
MIP peak reconstruction and S/N

- Datasets: 150 GeV pion beam datasets without the absorbers
- Similar pedestal and CM noise subtraction methods are applied
- One run for one channel; beam spot is scanned to have information in more channels
- Use only the best trigger phase to get highest S/N
- Fit function: Gauss + Landau ⊗ Gauss



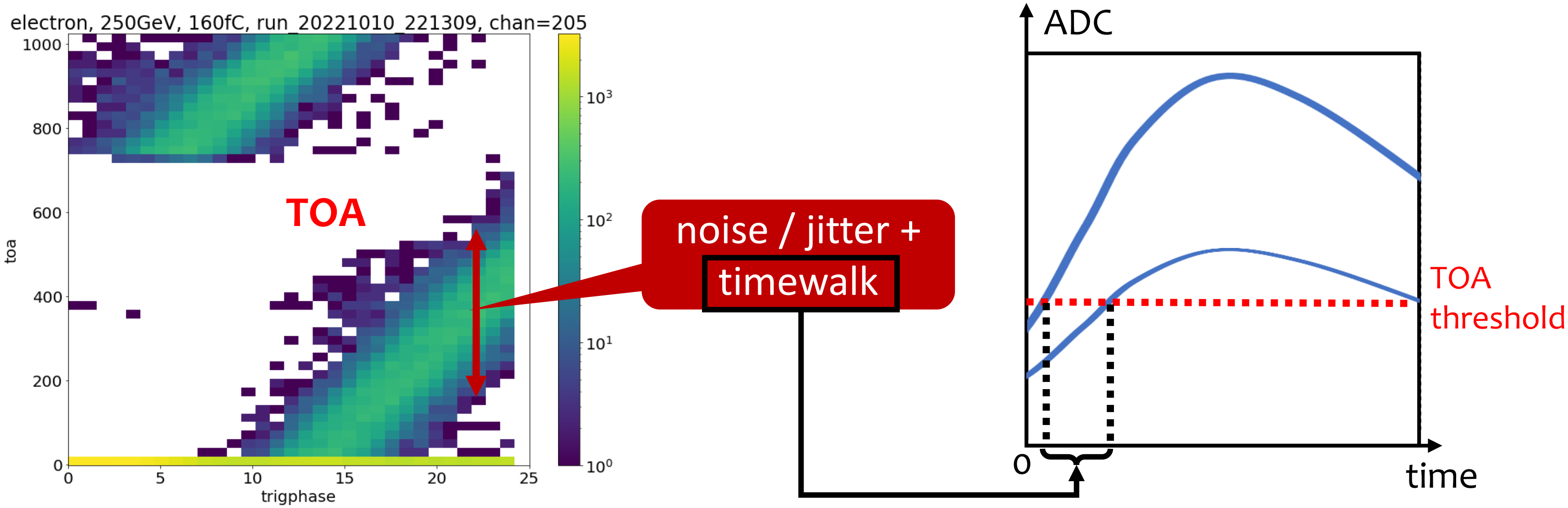


All channels with MIP information

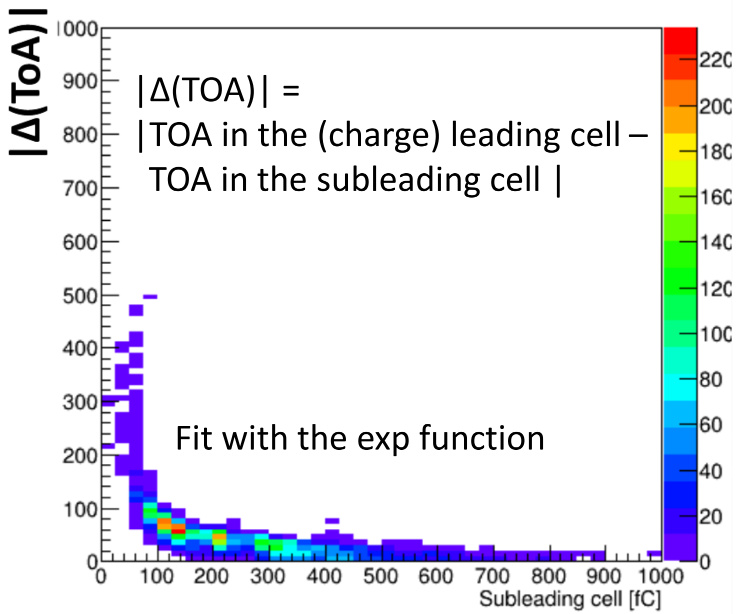


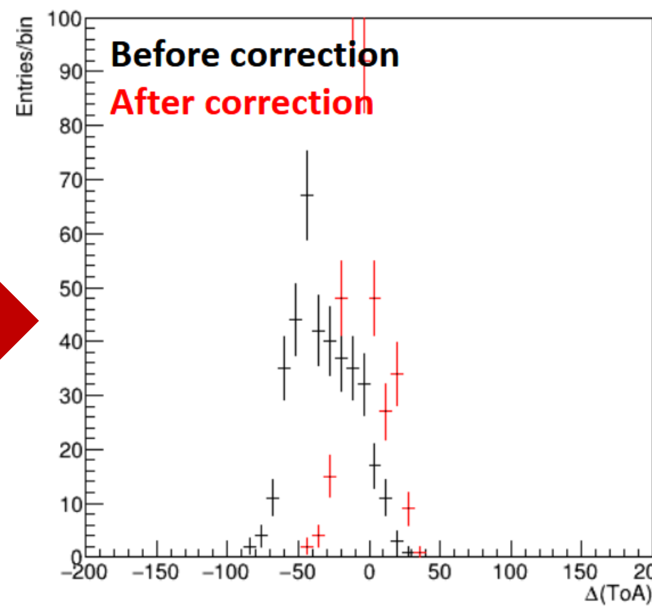
S/N much better than the 2021 beam test !!!

TOA studies

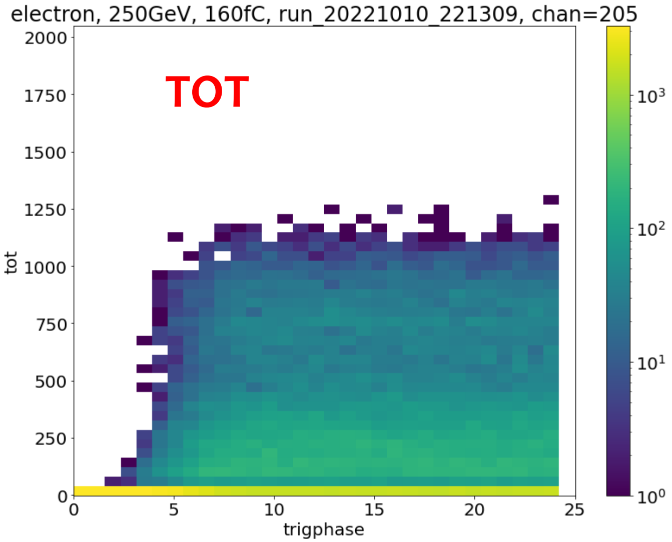


TOA calibration with the beam test data





TOT studies

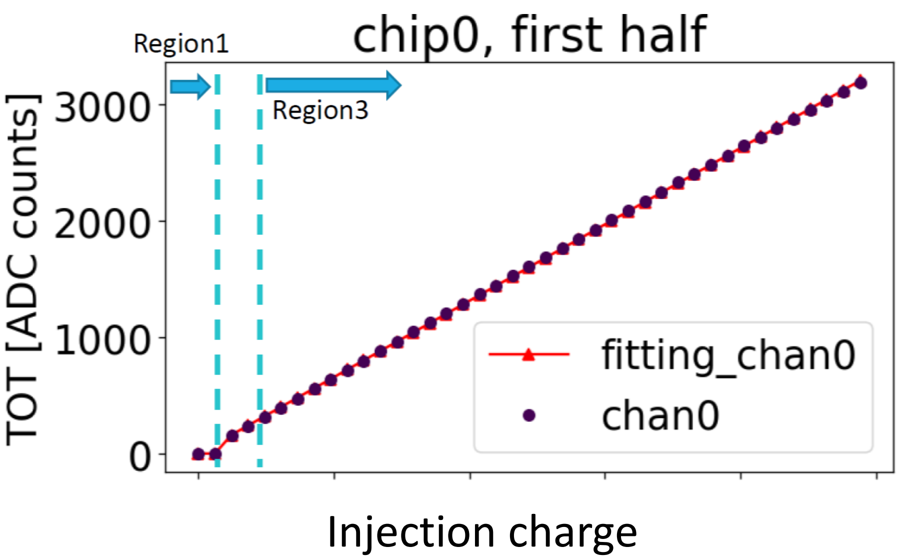


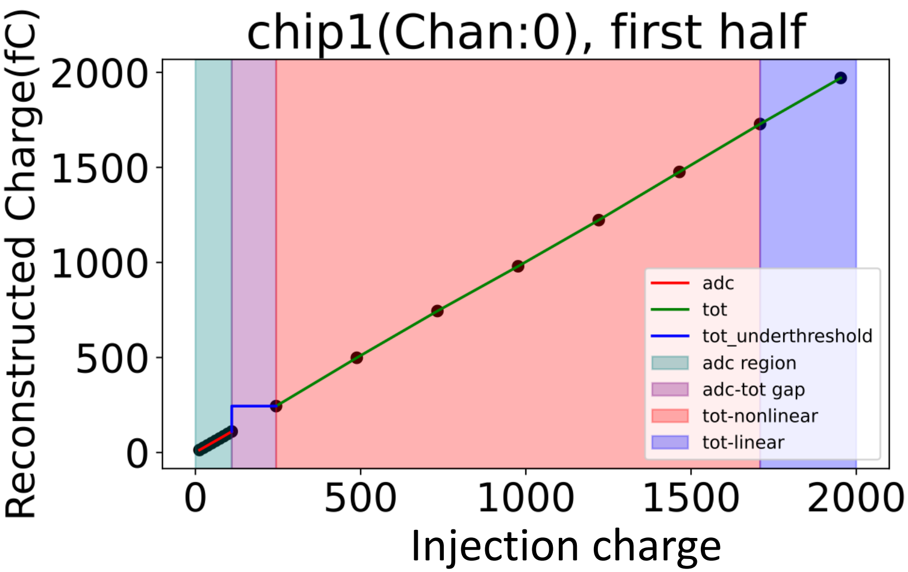
× TOTtoCharge converter

+ ADC × ADCtoCharge converter

=total deposited charge

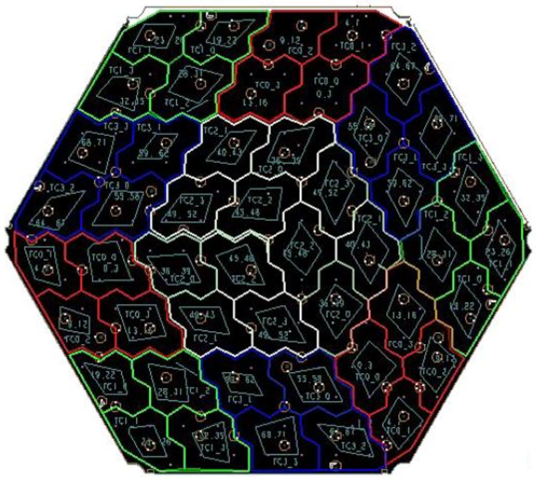
-------------------- TOT calibration with the injection data -------------------------

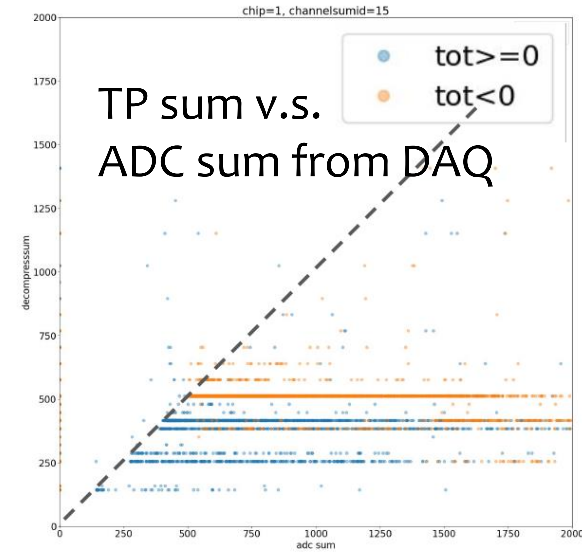




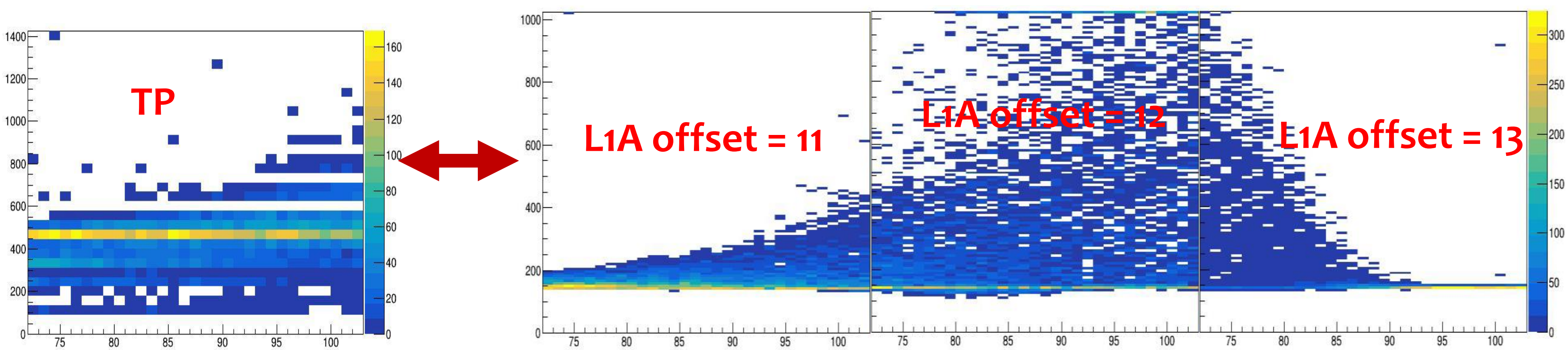
Trigger primitive studies

- Trigger primitive (TP): sum of the charges linearized across ADC / TOT range in the four adjacent cells
- ADC pedestal subtraction -> check ADC / TOT thresholds -> TOT2Charge conversion
- Unexpected distributions seen in the beam test data





➢ **Check different BXs using the datasets with different L1A offsets**



- **TP not synchronized with DAQ in most runs during the beam test !**
  - Set the ROC parameters to make TP work properly.
  - Monitor TPs in the future beam tests.

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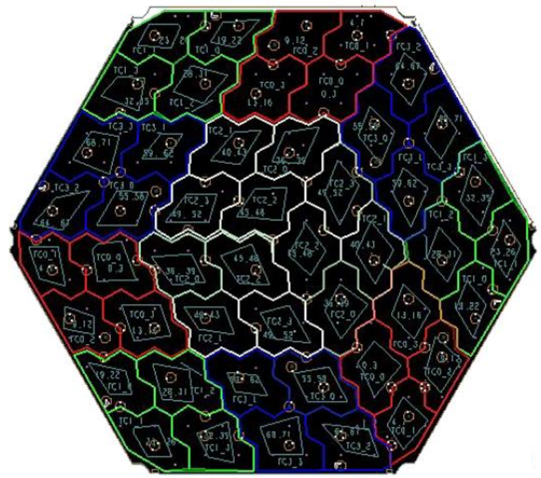

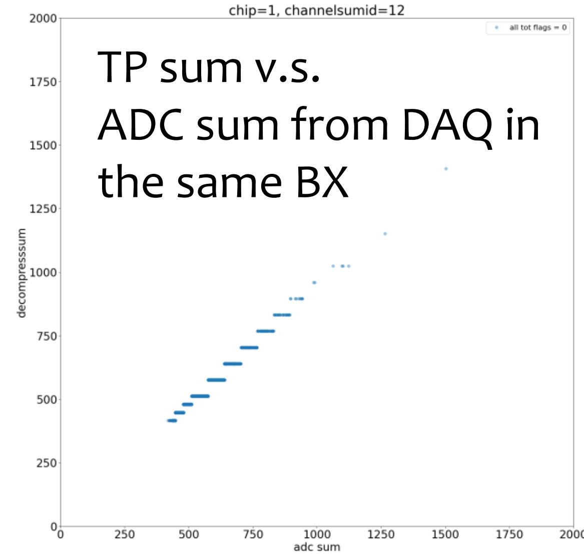

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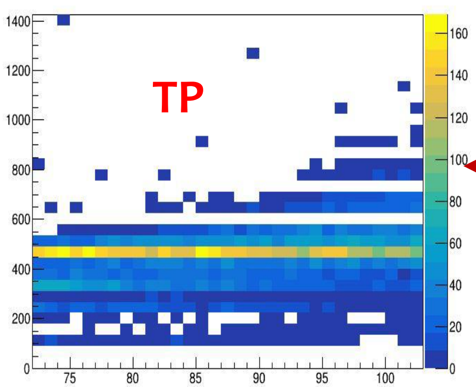
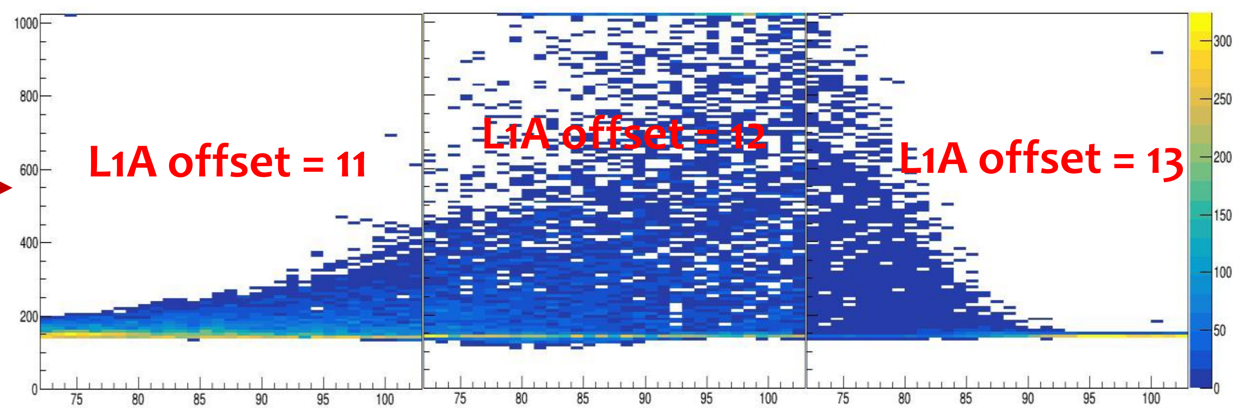




- **TP not synchronized with DAQ in most runs during the beam test !**
  - Should set the ROC parameters to make TP work properly.
  - Monitor TPs in the future beam tests.

Conclusion

- We managed to make the HGCROCs as well as the single silicon module work with good performances during the beam tests.
- Studies related to the ADC, TOA, TOT as well as trigger primitives have been done, and more improvements are being made.
- **Another two exciting beam tests are scheduled July and September 2023 !**
  - Upon all the measurements so far, settle and measure TPs accurately.
  - Even build multiple layers of silicon modules for testing.

Thanks for your attention !

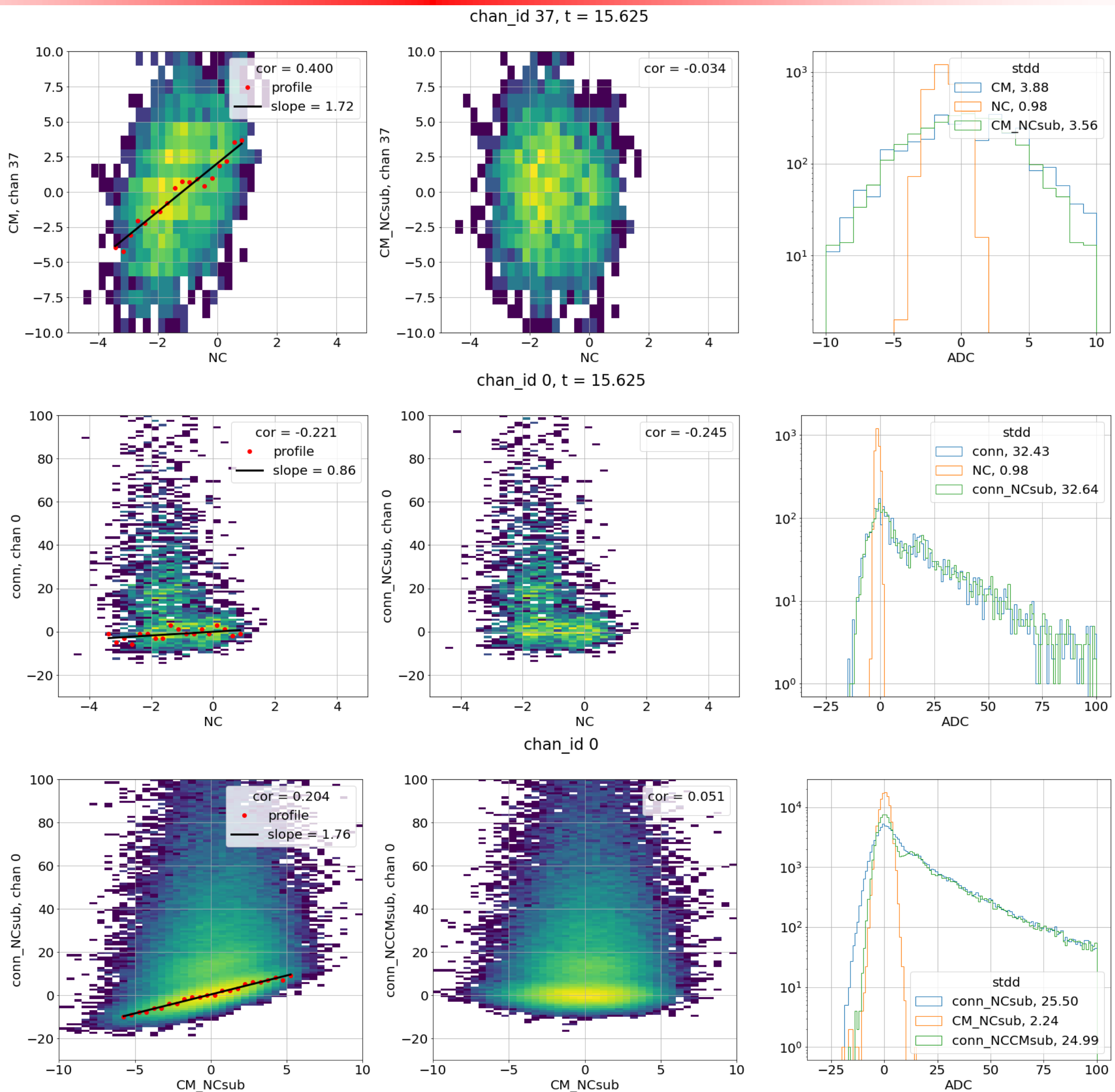
Backup

BT2021: CM noise subtraction (electron data)

Step 1

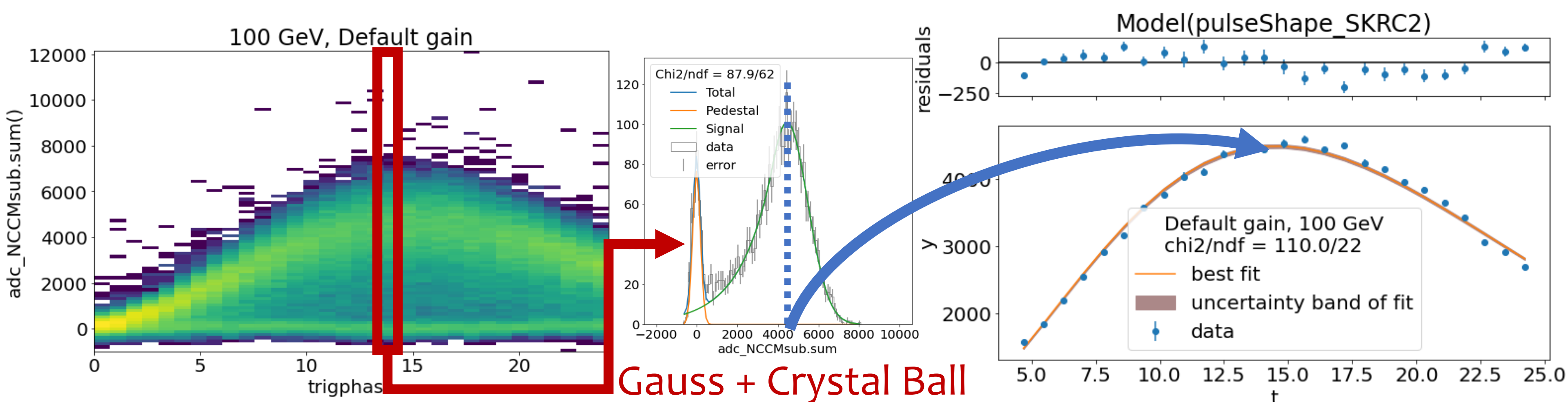
Step 2

Step 3



BT2021: pulse shape reconstruction

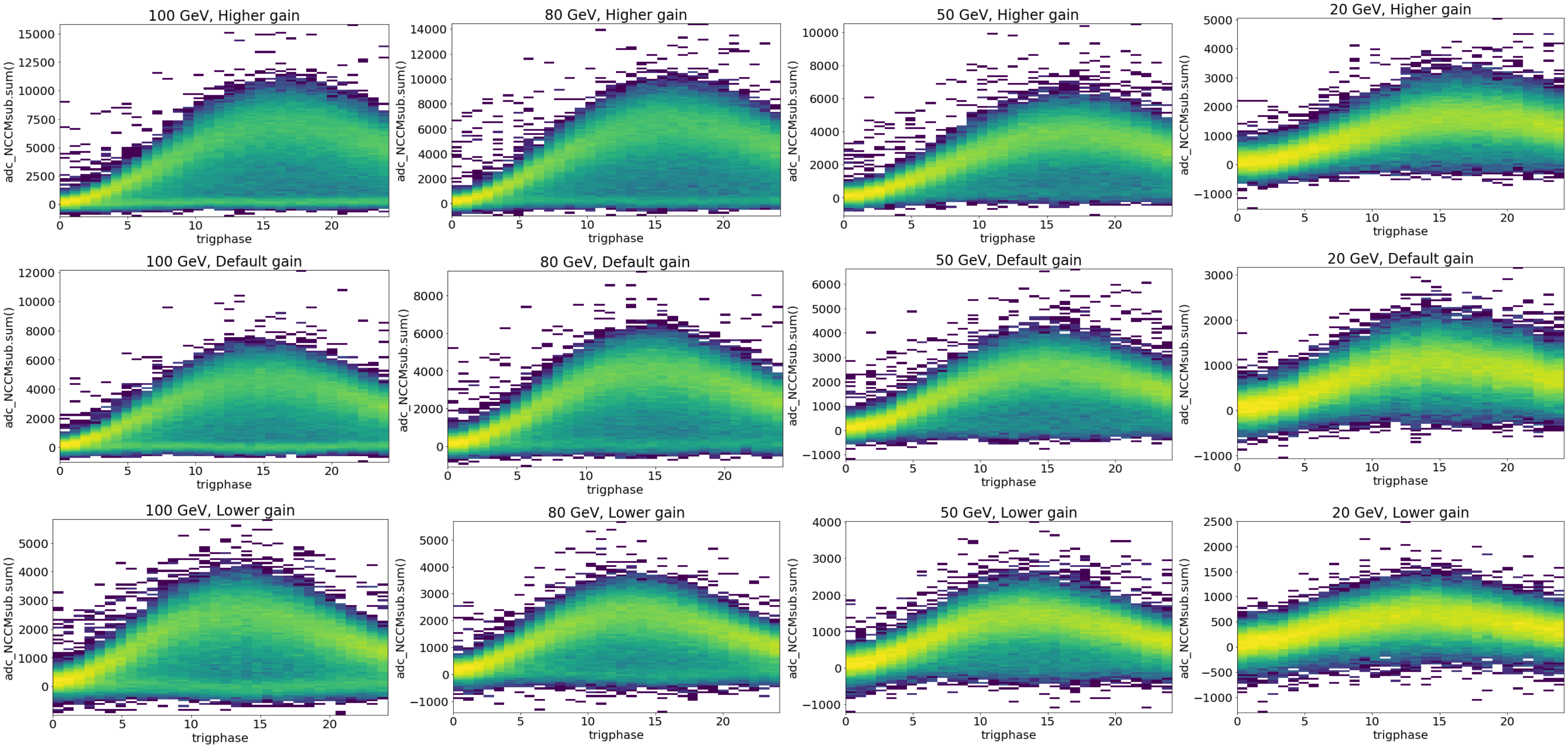
- **Adc.sum() over all connected channels v.s. trigphase**
  - Should be proportional to deposited energy



- **For Default and Lower gain:**
  - Based on the functional form of the Sallen Key – RC2 shaper
  - $S(t \mid A, \tau_{pa}, \tau_{sh}) = Ae^{-at}\left[e^{-ct}\left(\frac{t^3}{c} - \frac{3t^2}{c^2} + \frac{6t}{c^3} - \frac{6}{c^4}\right) + \frac{6}{c^4}\right], a = 1/\tau_{pa}, c = 1/\tau_{pa} - 1/\tau_{sh}.$
- **For Higher gain:**
  - Due to the undershoot, use the function from the [2018 BT]
  - $S(t \mid A, \tau, n, \alpha) = A\left[\left(\frac{t}{\tau}\right)^n - \frac{1}{n+1}\left(\frac{t}{\tau}\right)^{n+1}\right]e^{-\alpha \cdot \frac{t}{\tau}}.$

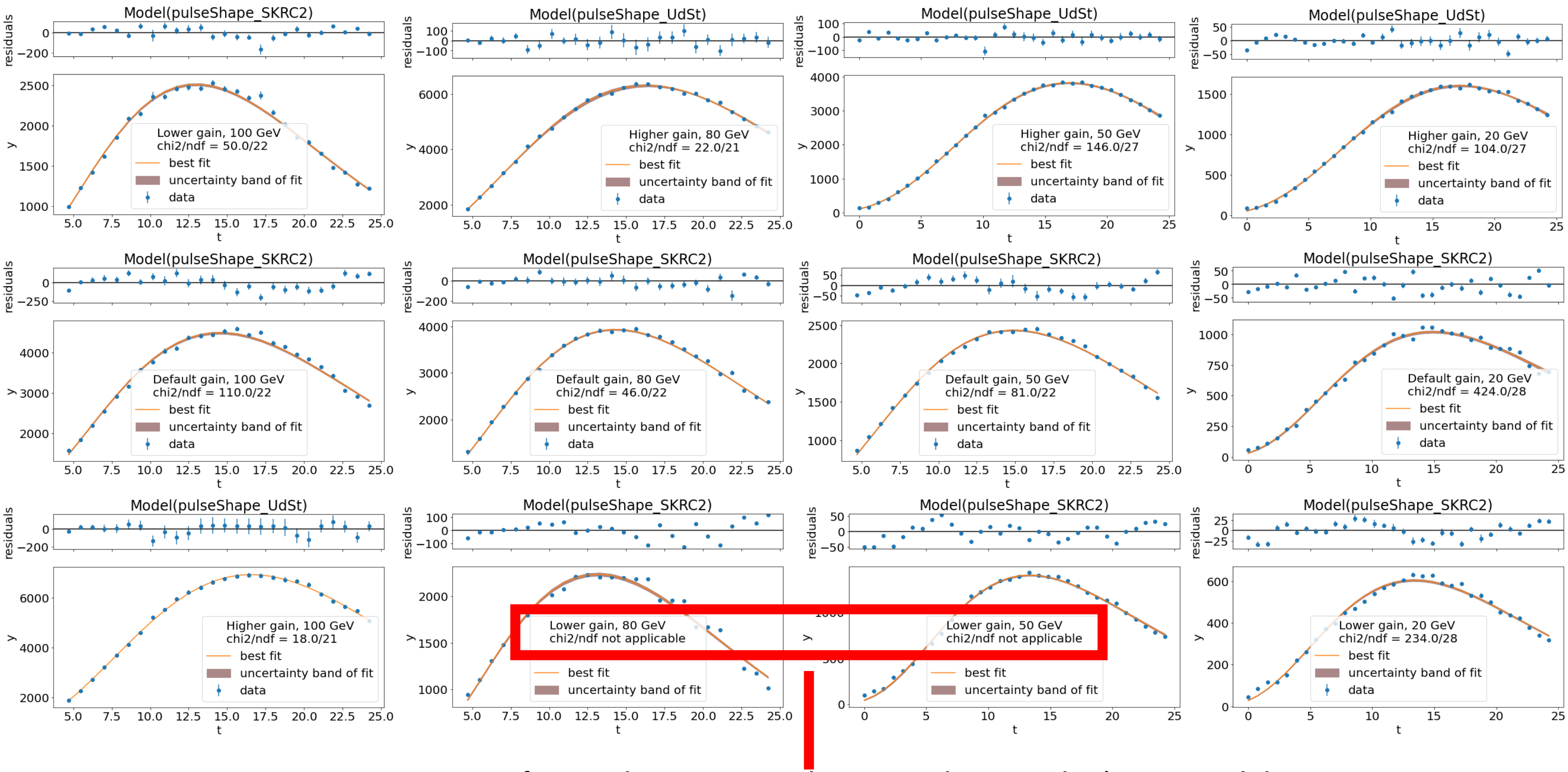
BT2021: pulse shape reconstruction

➢ **Adc.sum() over all connected channels v.s. trigphase in different datasets**



BT2021: pulse shape reconstruction

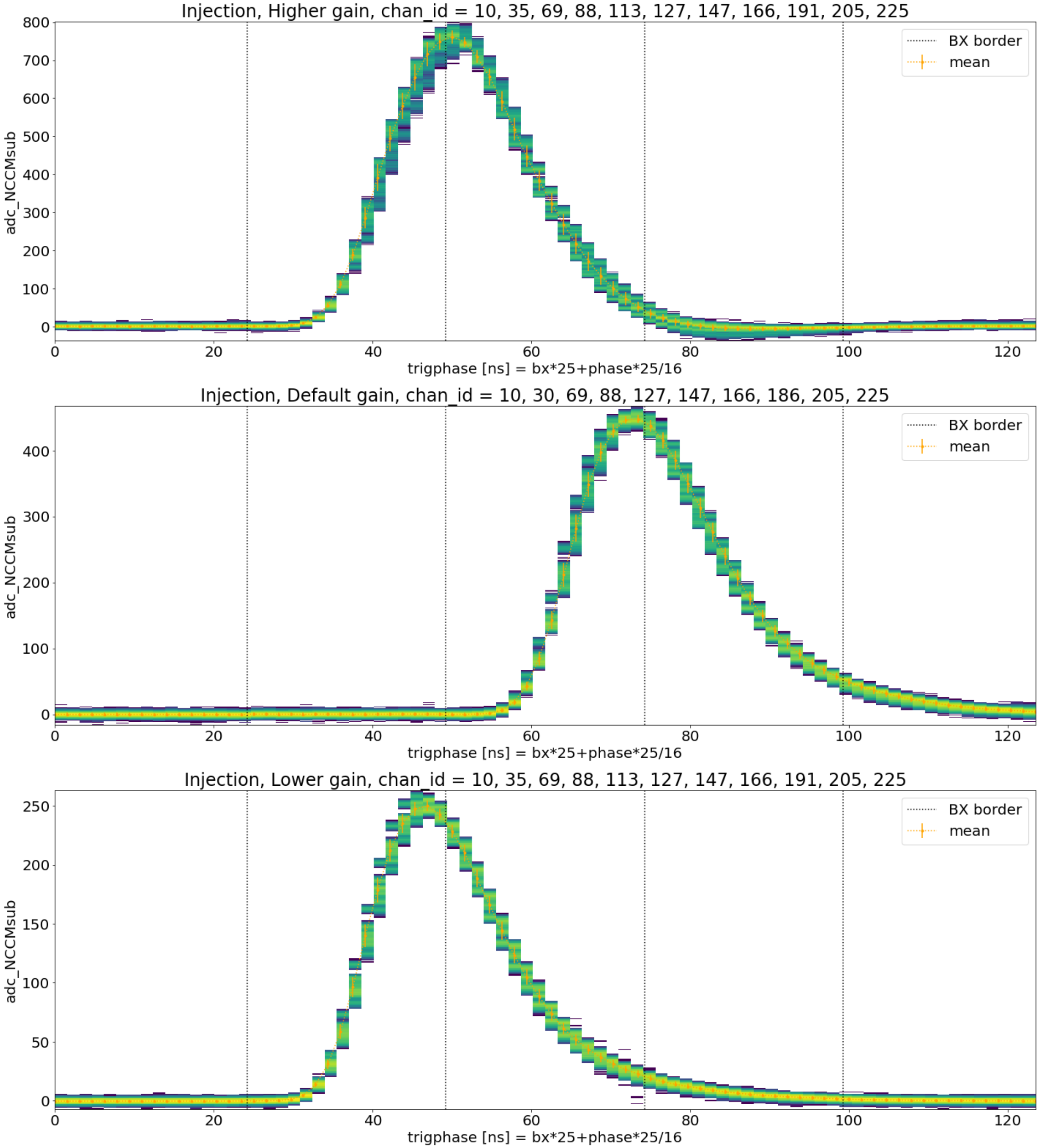
➢ **Pulse shape fits in different datasets**



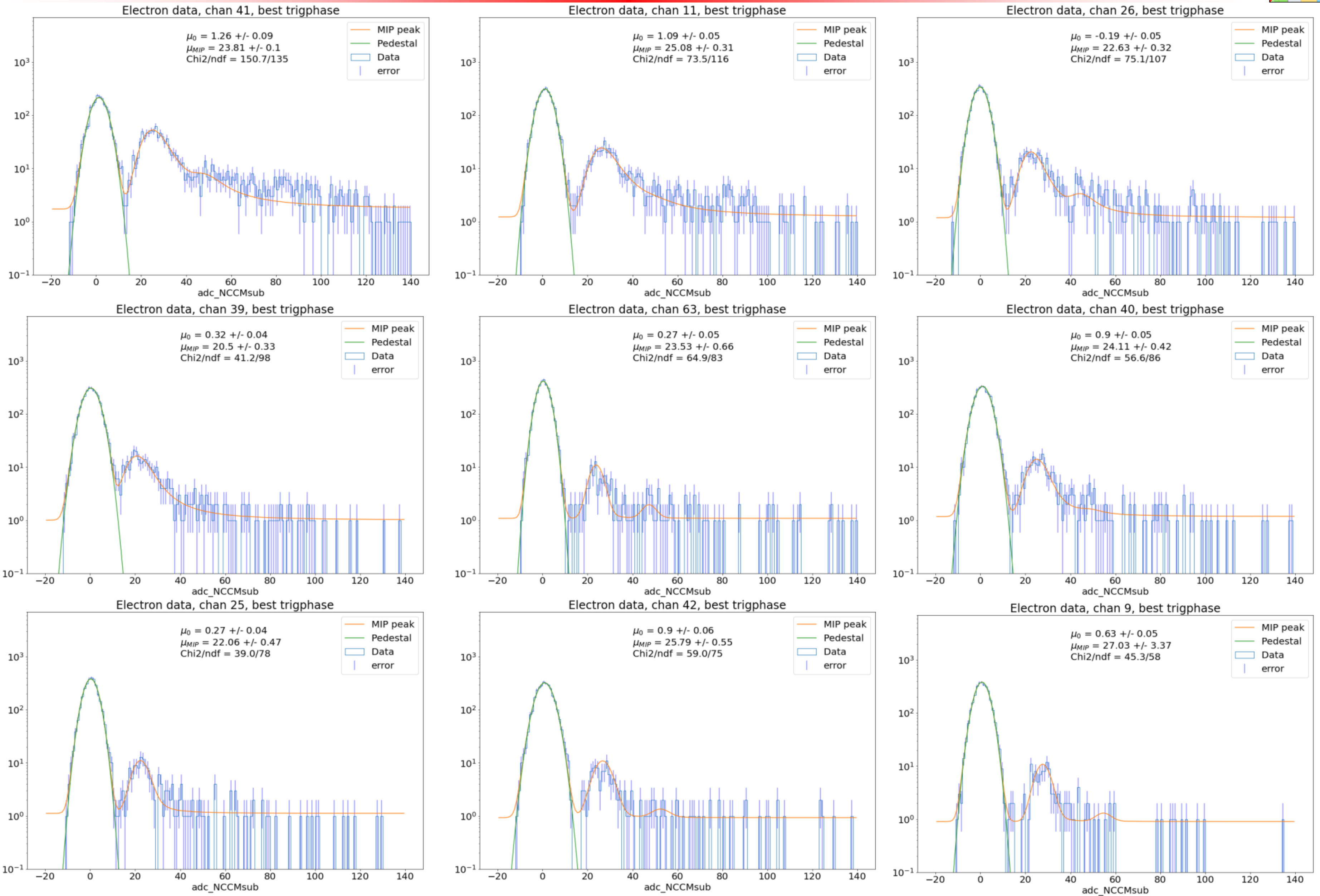
Fits of some data points in these two datasets don’t give a valid uncetainty.

BT2021: pulse shape reconstruction

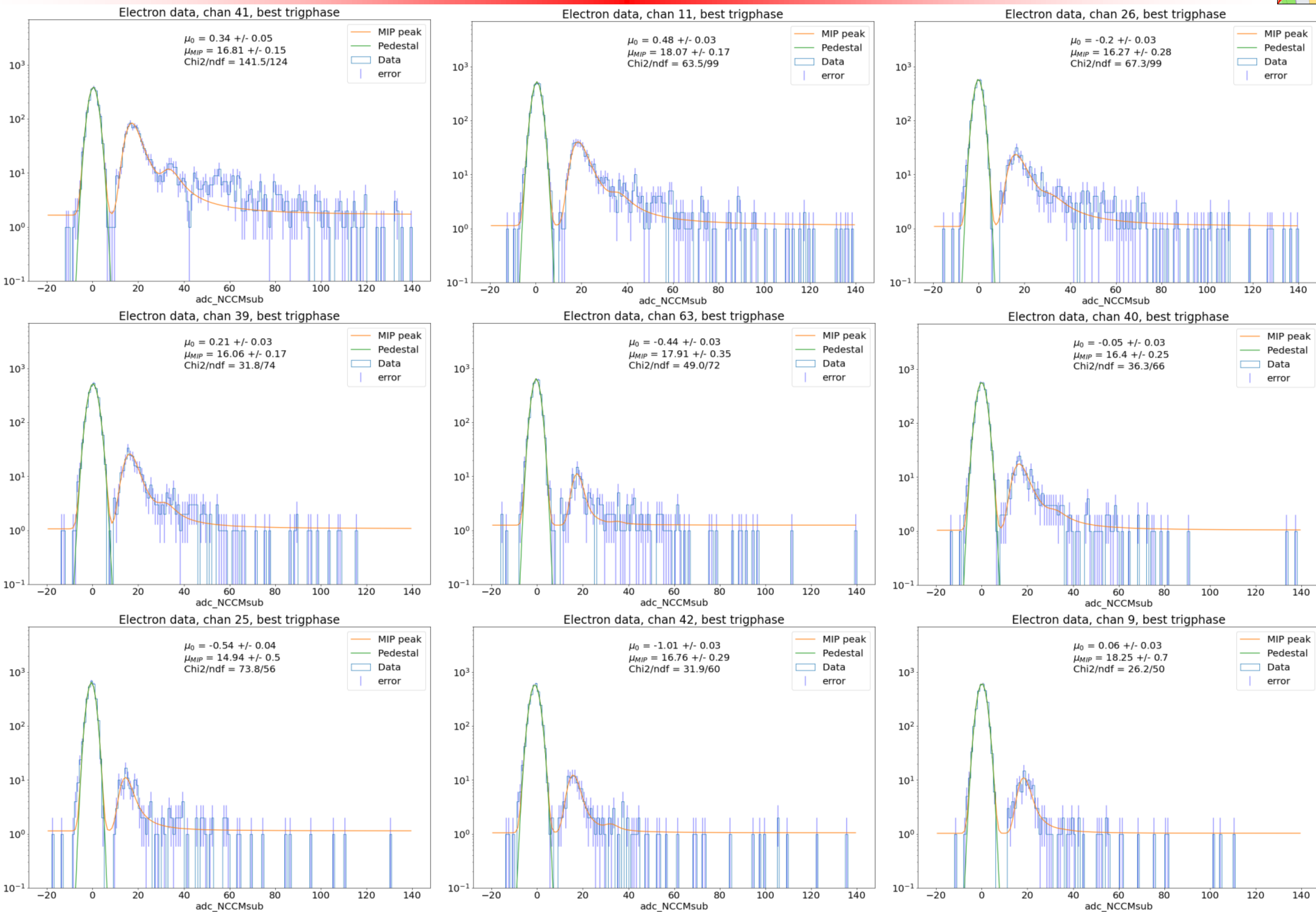
- ➢ **Pulse shapes from the injection data**



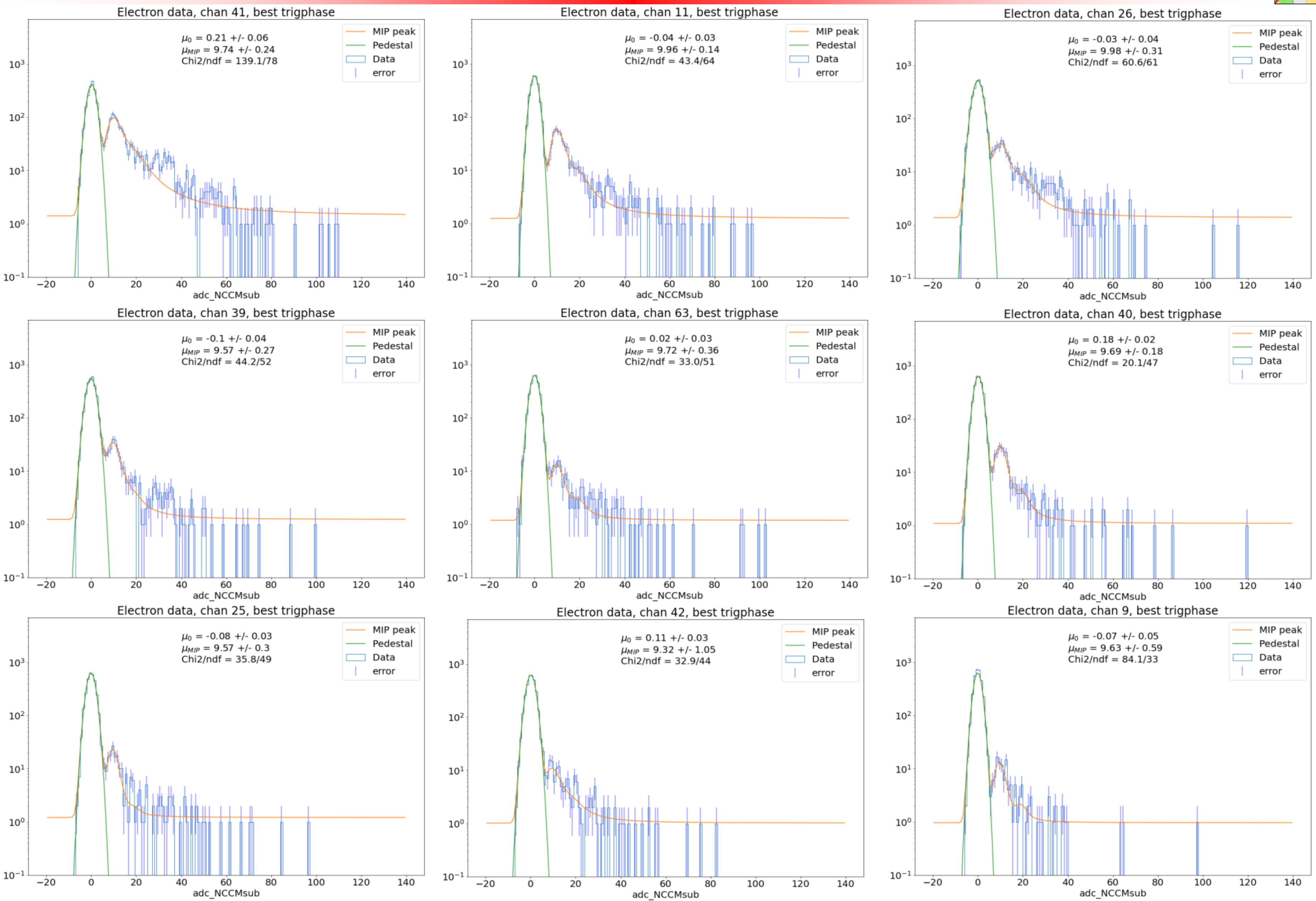
BT2021: MIP peak fits (Higher gain)



BT2021: MIP peak fits (Default gain)



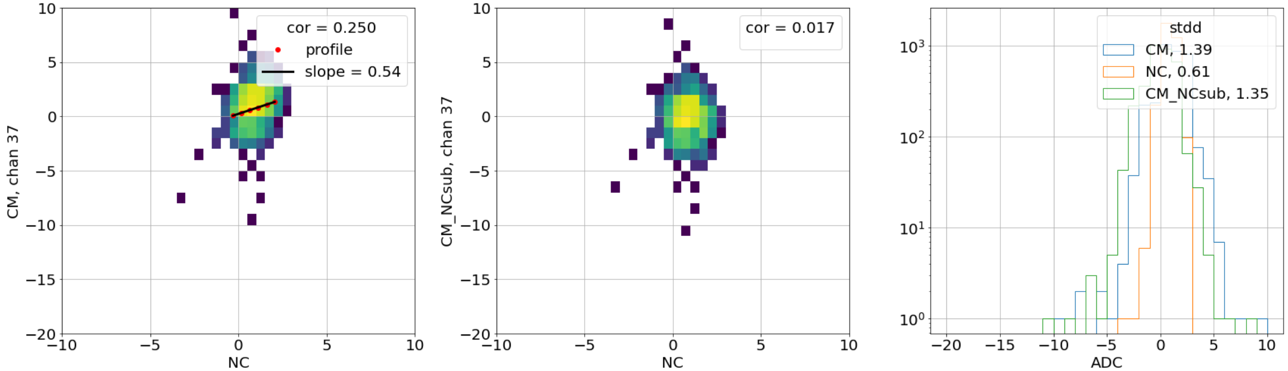
BT2021: MIP peak fits (Default gain)



BT2021: CM noise subtraction (pion data)

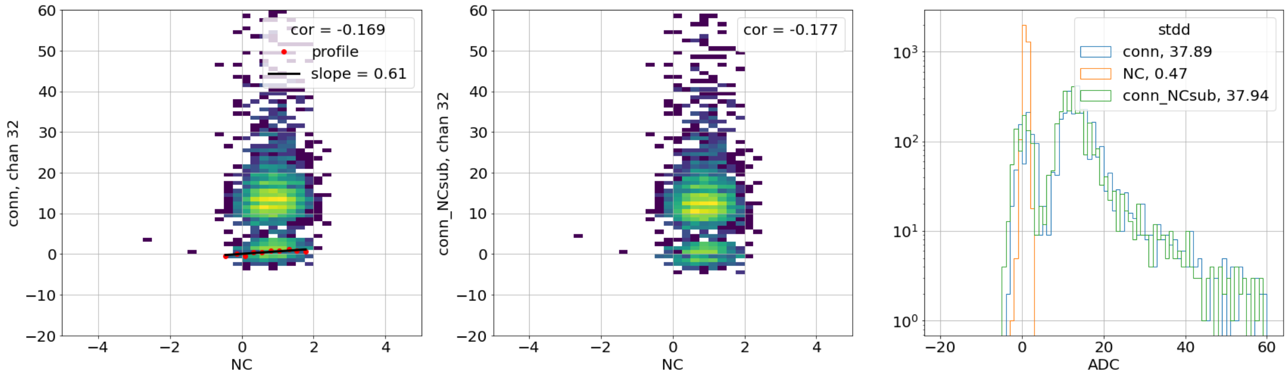
Step 1

chan_id 37, t = 15.625



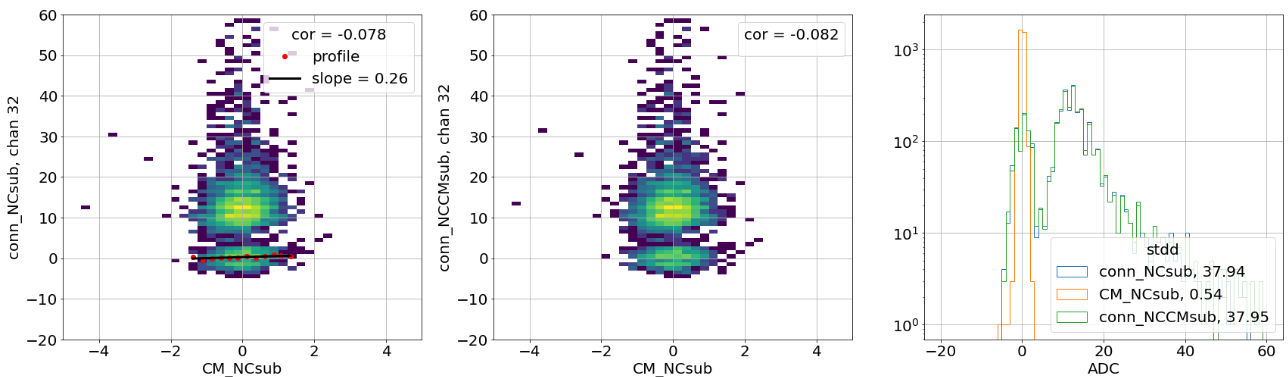
Step 2

chan_id 32, t = 14.0625

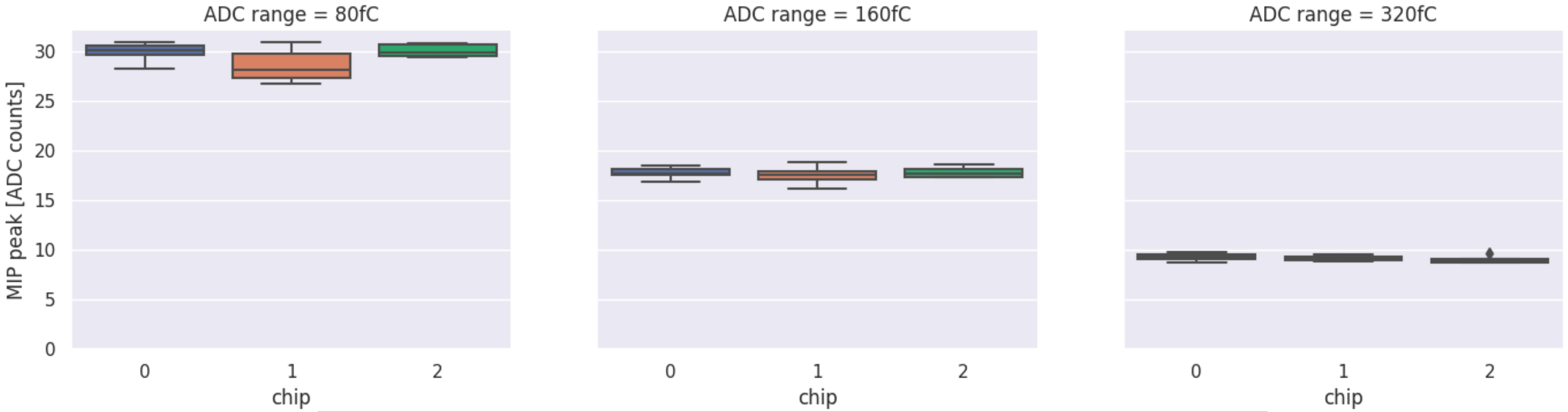


Step 3

chan_id 32, t = 14.0625



BT2022: MIP peak fits



gain	chip	MIP(mean)	MIP(std)	S/N(mean)	S/N(std)	nPad
80	0	30.01	0.76	14.61	1.18	15
80	1	28.47	1.59	14.12	1.07	8
80	2	30.05	0.63	15.15	0.38	5
160	0	17.8	0.4	13.18	1.29	16
160	1	17.49	0.81	12.28	0.75	8
160	2	17.8	0.58	12.86	0.53	5
320	0	9.31	0.32	8.8	0.54	16
320	1	9.17	0.28	8.51	0.43	8
320	2	9.0	0.39	8.43	0.34	5
80	all	29.58	1.23	14.57	1.08	28
160	all	17.71	0.56	12.88	1.11	29
320	all	9.22	0.33	8.66	0.5	29