# HGCROC chip test

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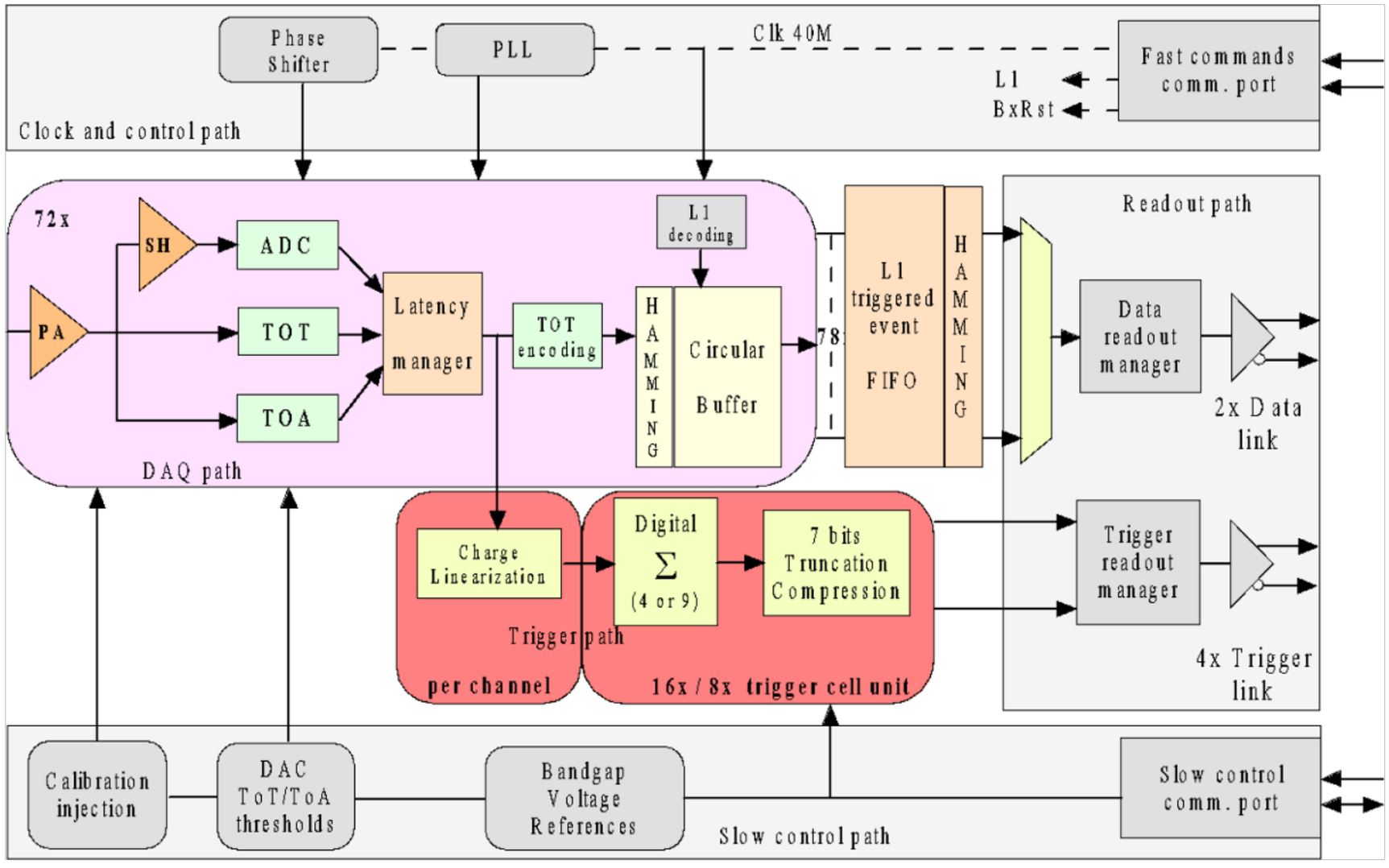
14/Mar/2023

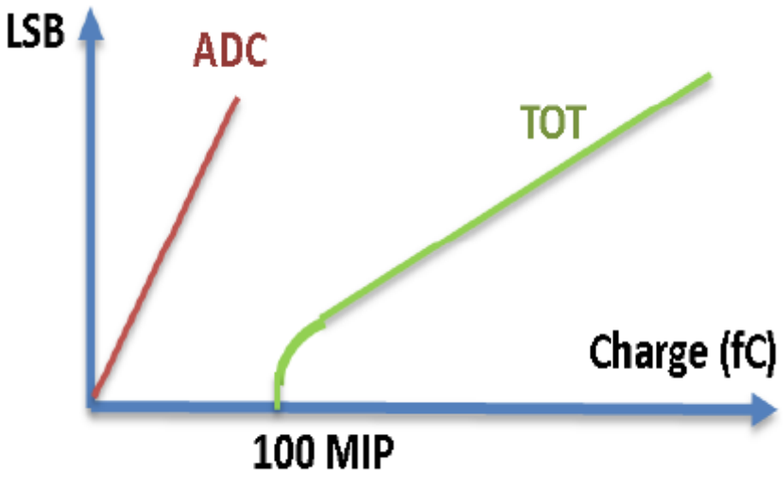
# Purpose of this study

- The HGCROC chip, which was developed for the CMS high-granularity calorimeter, is a good candidate for the ALICE FoCal-E readout.
- Characterization of charge measurement linearity and trigger latency for ALICE FoCal-E.
- For the ALICE FoCal-E, 1980 ( = 90 x 11 x 2 ) HGCROC chips are necessary. Design of a chip test system for the mass-production is necessary.
- For these purposes, we launched a test bench and started elementary tests.

# HGCROC overview

## HGCROC v2 diagram




- 72ch ADC (SAR, 10 bit, 40 Msps) up to 100 MIP typ.
- 72ch TOT (50ps, 12 bit) above 100 MIP
- 72ch TOA (25ps, 10 bit) arrival timing
- 2ch common-mode ADC

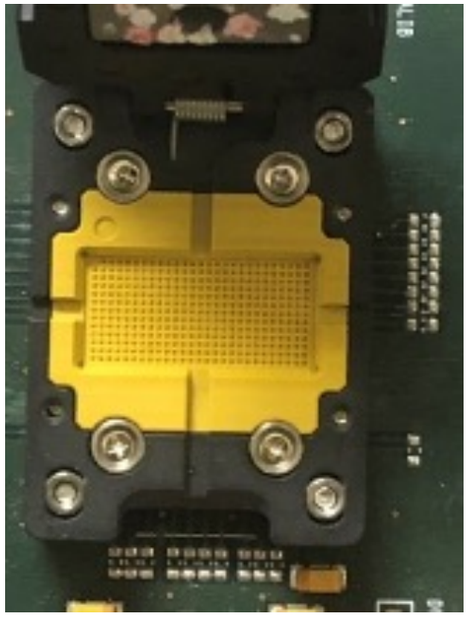
# HGCROC2 Test bench

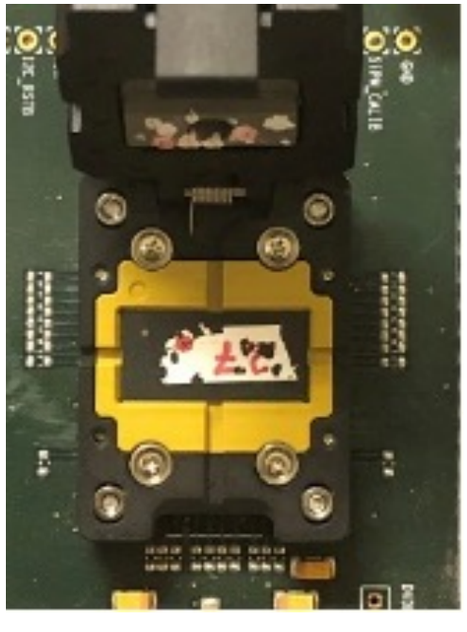
- We launched a characterization test bench at Saga Univ.
  with the help of Chujo-san and Abderrahmane-san (Aug/2022) from Tsukuba Univ.

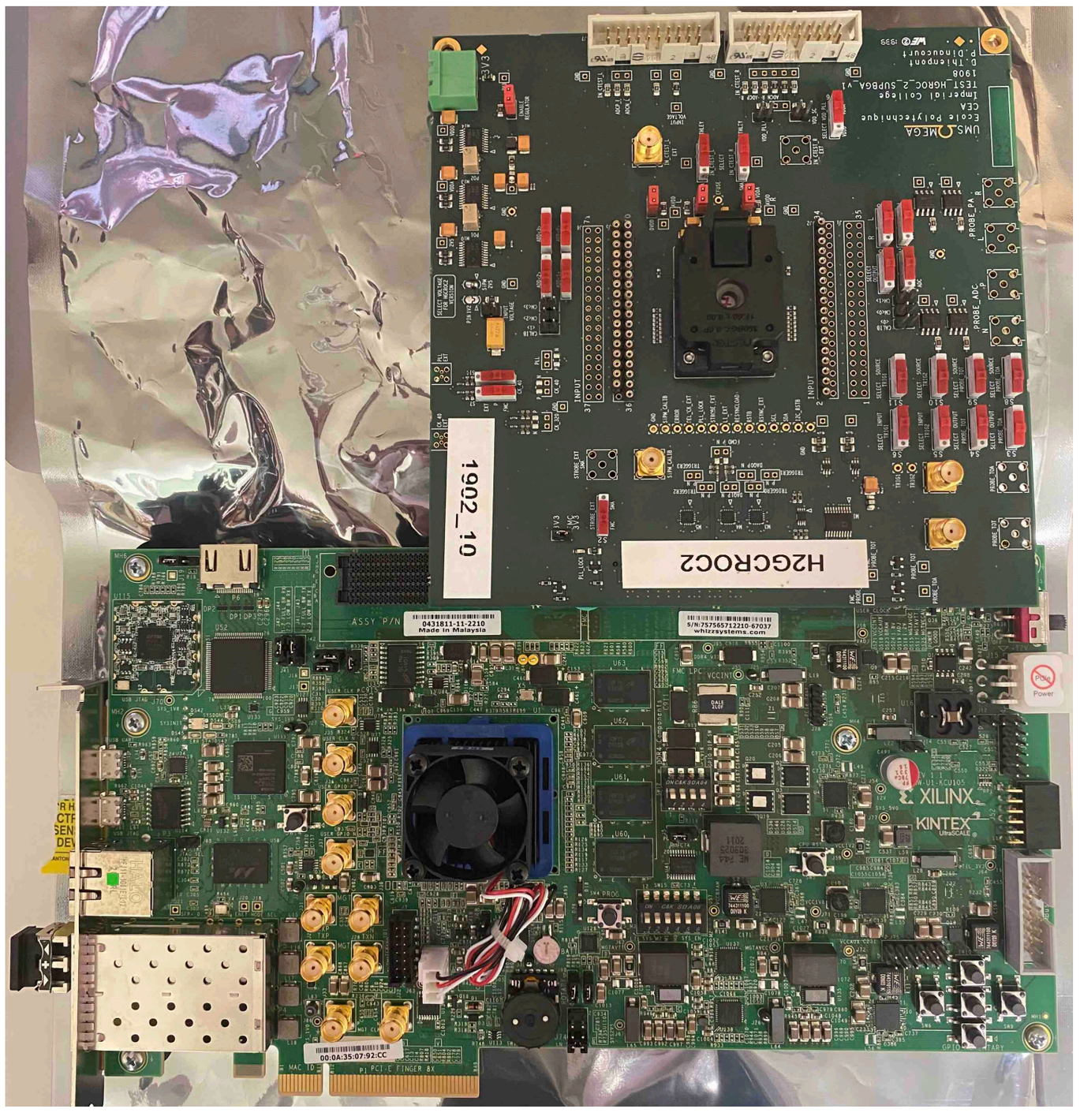
- HGCROC2 test board with a socket
  and control/DAQ software are
  provided by the Grenoble group.

- Control and DAQ are performed by
  a commercial Xilinx board KCU105.

- 23 BGA-packaged HGCROC2 chips
  at hand.

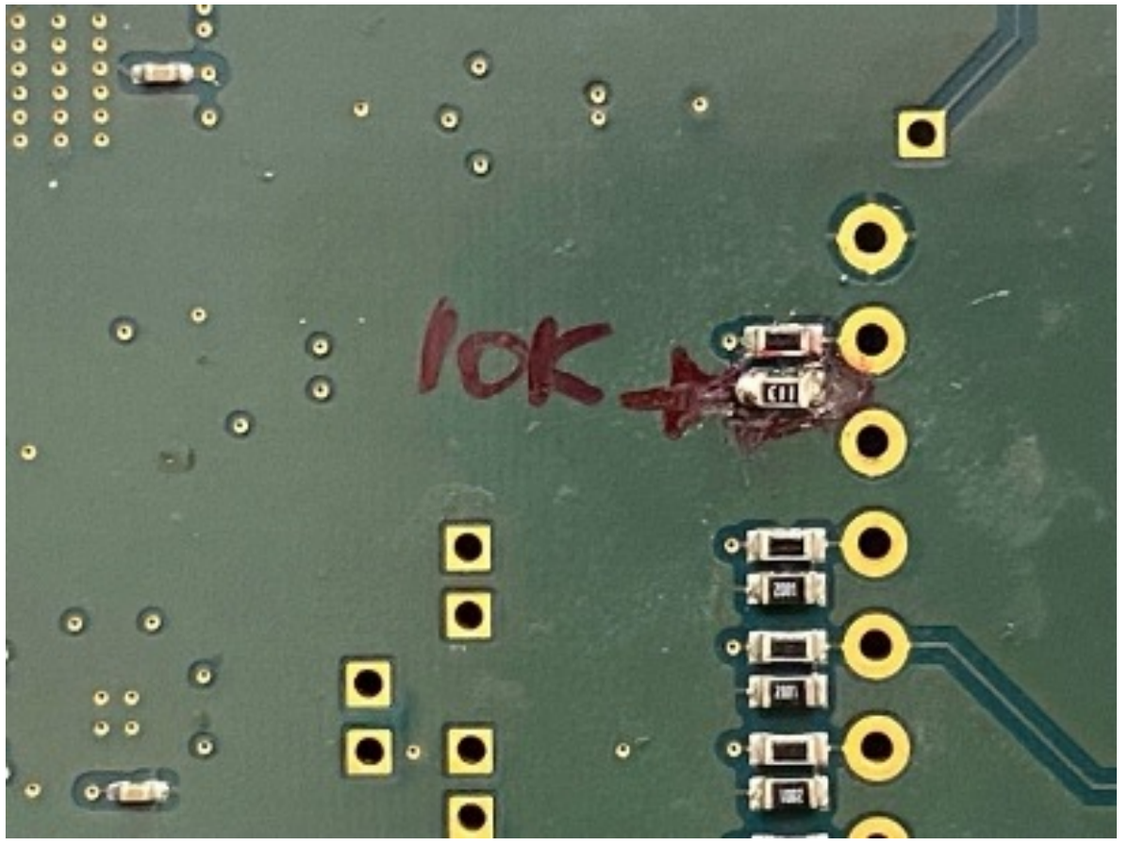


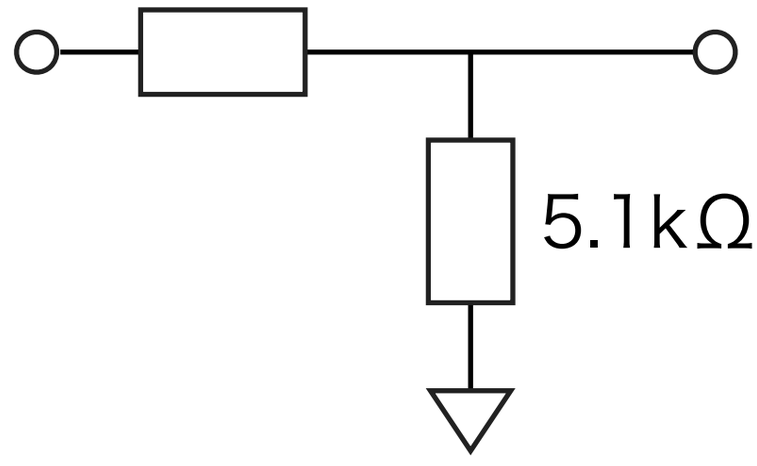




# Difficulties in I²C connection

Slow control btw. FPGA and HGCROC is communicated via the I²C protocol.
In our test, data taking is often interrupted by I²C errors.
The I²C clock line voltage is reduced by series resisters.
Original value 1.0 kΩ was found to be too low and replaced.
We tried various values and now 5.1kΩ is mounted.




Even after the treatment, our measurements were suffered from I²C errors.
At this moment, the problem is not yet solved.

# I²C pass/fail check of 23 chips

| TipNumber | PhaseNumber 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|
| 4 | × | △ | △ | △ | △ |
| 6 | × | × | △ | ○ | ○ |
| 7 | ○ | ○ | ○ | △ | × |
| 8 | △ | △ | △ | △ | △ |
| 10 | × | × | × | △ | △ |
| 12 | △ | △ | × | × | × |
| 13 | △ | △ | △ | △ | × |
| 14 | △ | △ | × | × | × |
| 15 | × | × | × | × | × |
| 16 | – | – | – | ○ | – |
| 19 | △ | △ | × | △ | ○※ |
| 20 | × | × | × | × | × |
| 21 | × | × | △ | △ | △ |
| 22 | × | × | × | × | × |
| 23 | × | × | × | × | × |
| 24 | × | × | ○ | △ | △ |
| 25 | △ | × | × | × | △ |
| 26 | – | – | – | ○ | – |
| 27 | × | △ | △ | ○ | ○ |
| 29 | △ | × | × | × | × |
| 30 | × | × | × | × | × |
| 31 | × | × | △ | △ | △ |
| 549 | ○ | △ | × | × | △ |

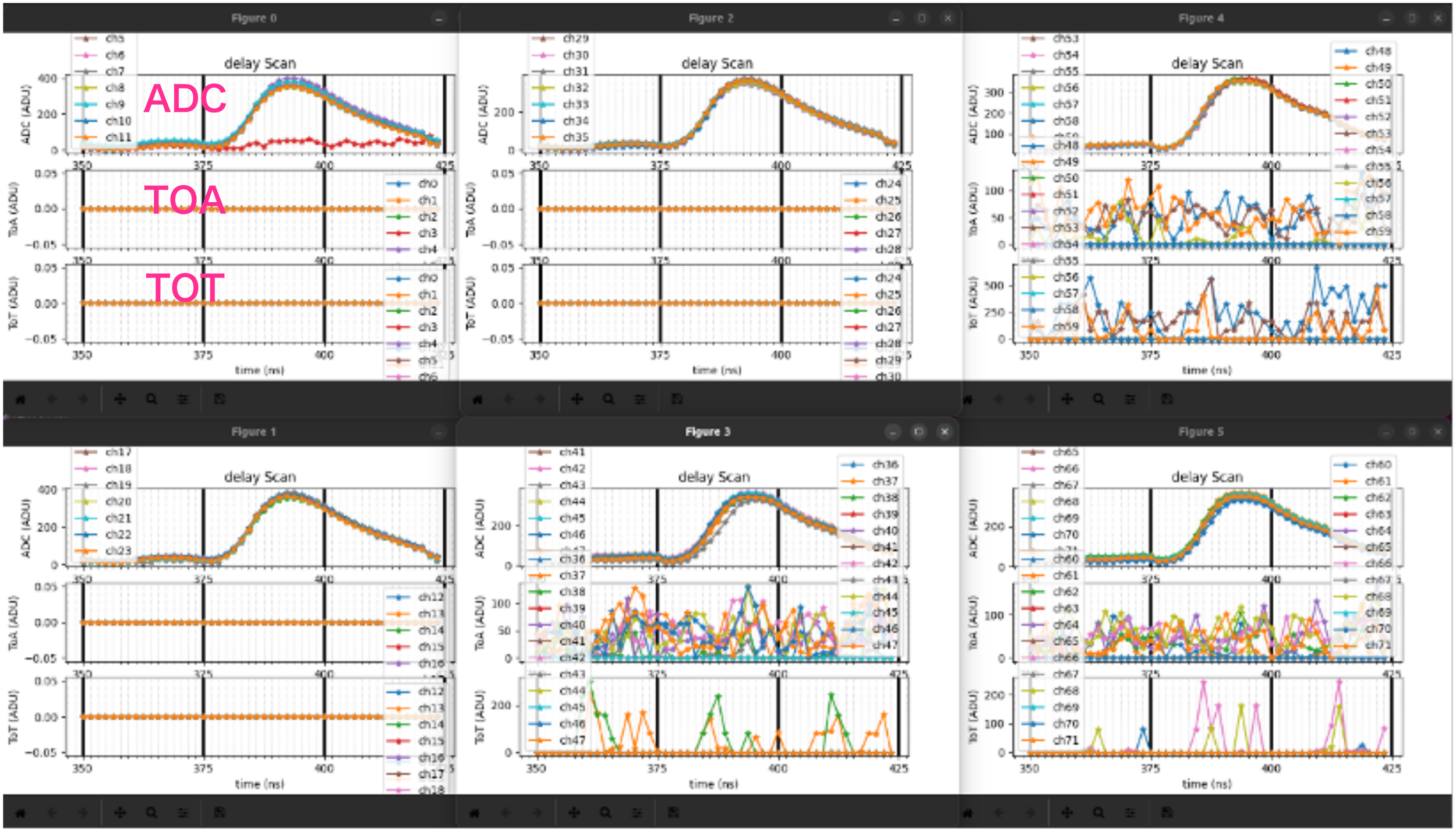
| | |
|---|---|
| ○ | DelayScan success |
| △ | I2C error in delayScan |
| × | Can't even open the application |
| ※ | Only one success |

Phase number
→ adjustment of I²C clock phase

Only 8 chips passed the delay scan test. If we think the chip yield shouldn't be such worse, then there might be a problem in the board or the test environment.
→ still in investigation.

# Delay scan test of ADC

While repeating the test pulse sampling, delay (ADC sampling timing) is increased every time by ~1.56ns, so that we can find the “peak” timing.




Results from all 72 channels

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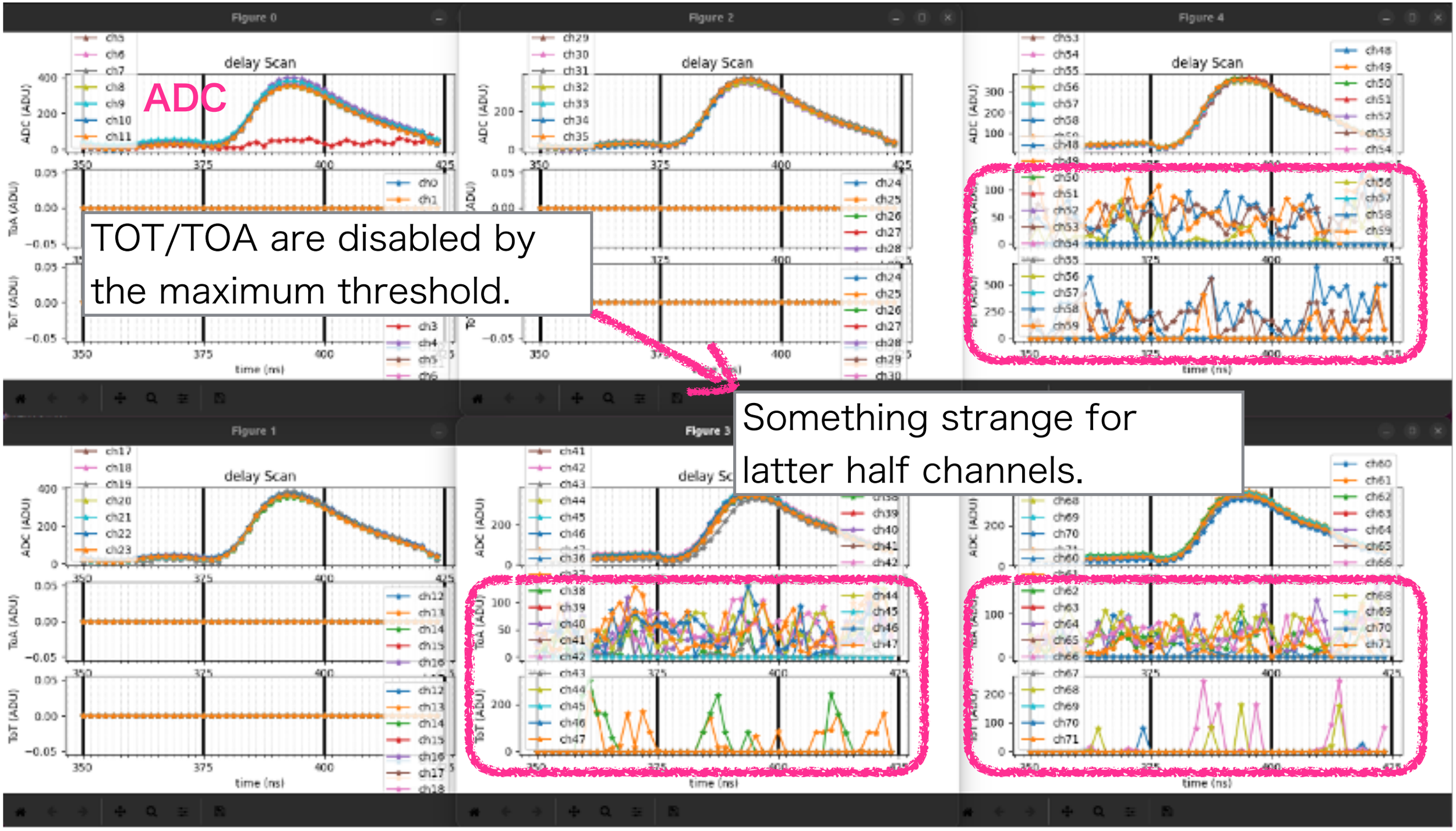
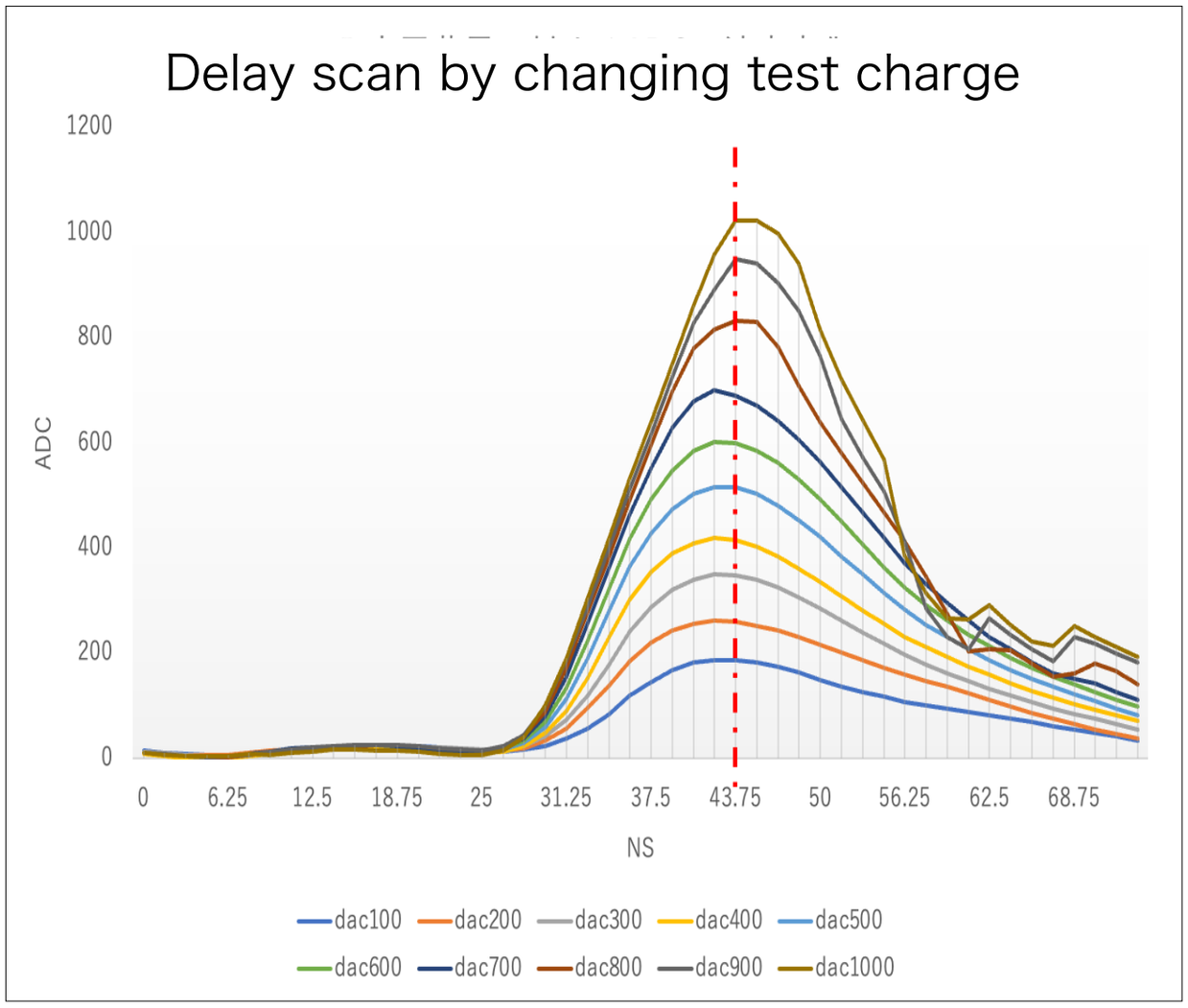
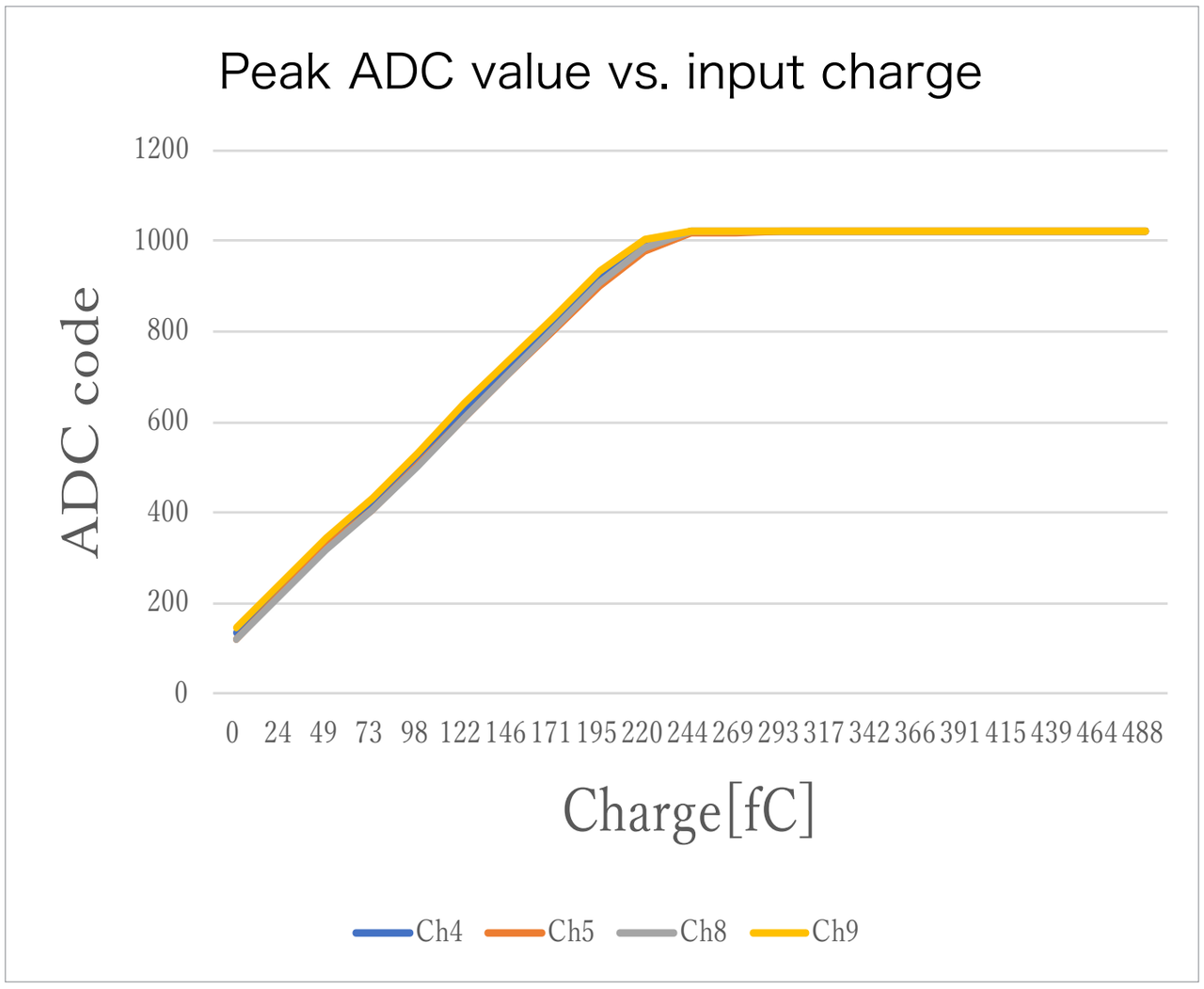


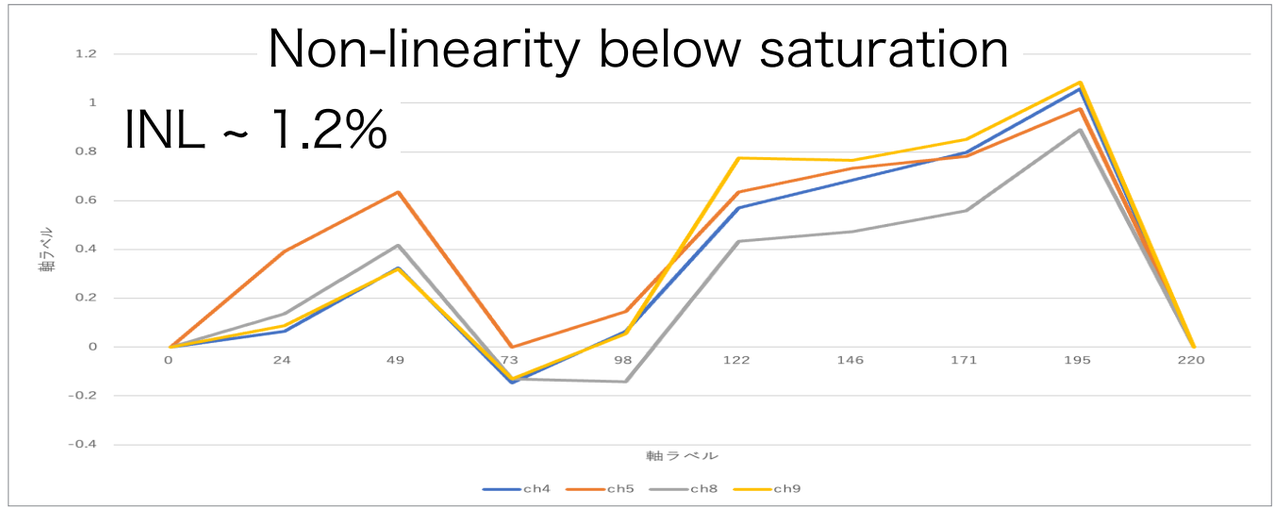

Results from all 72 channels

# ADC linearity measurement

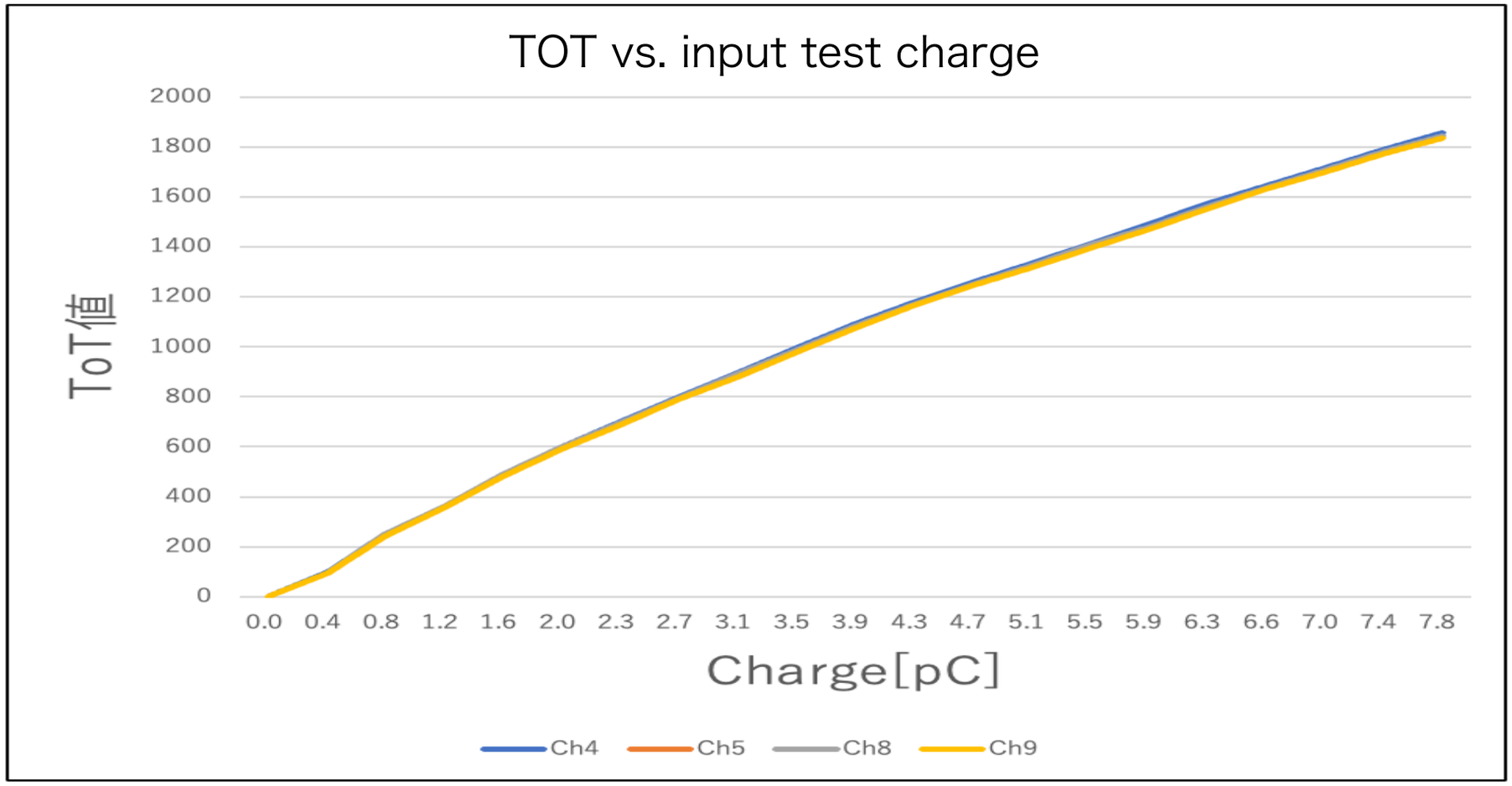


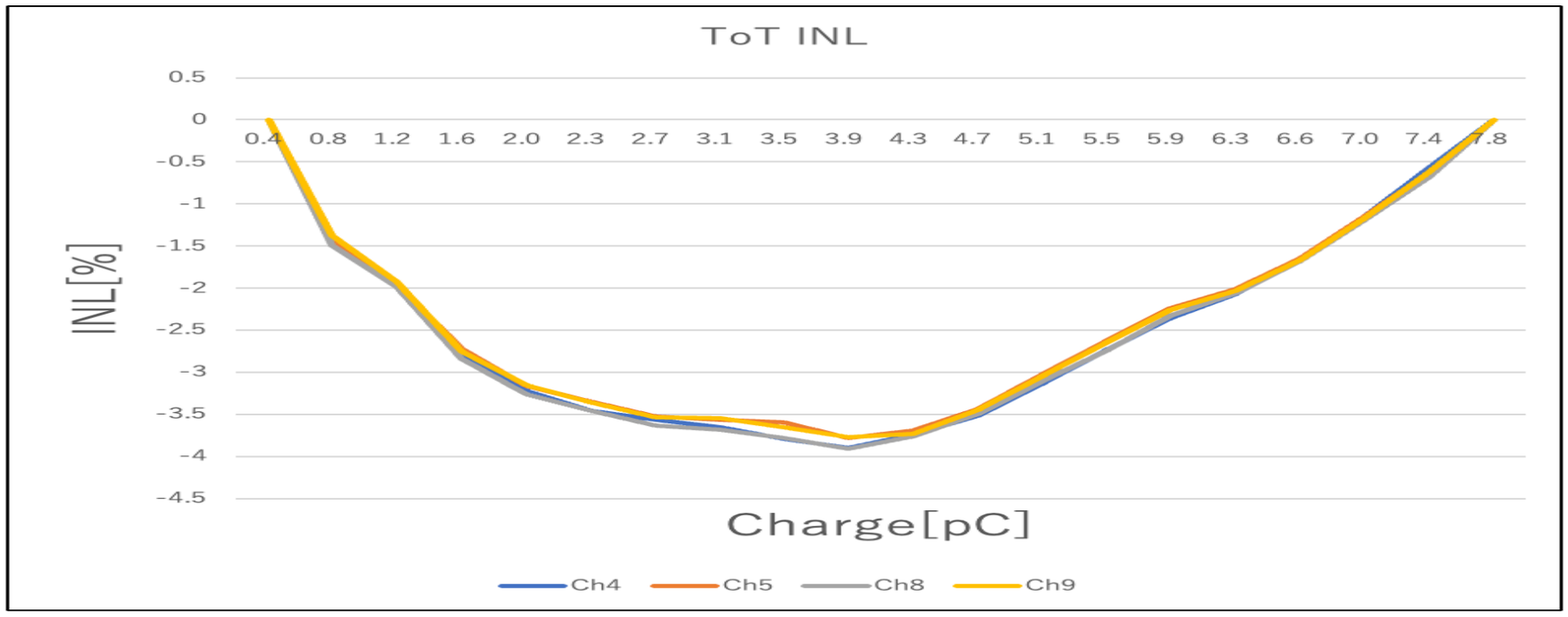




Good linearity is obtained below saturation.



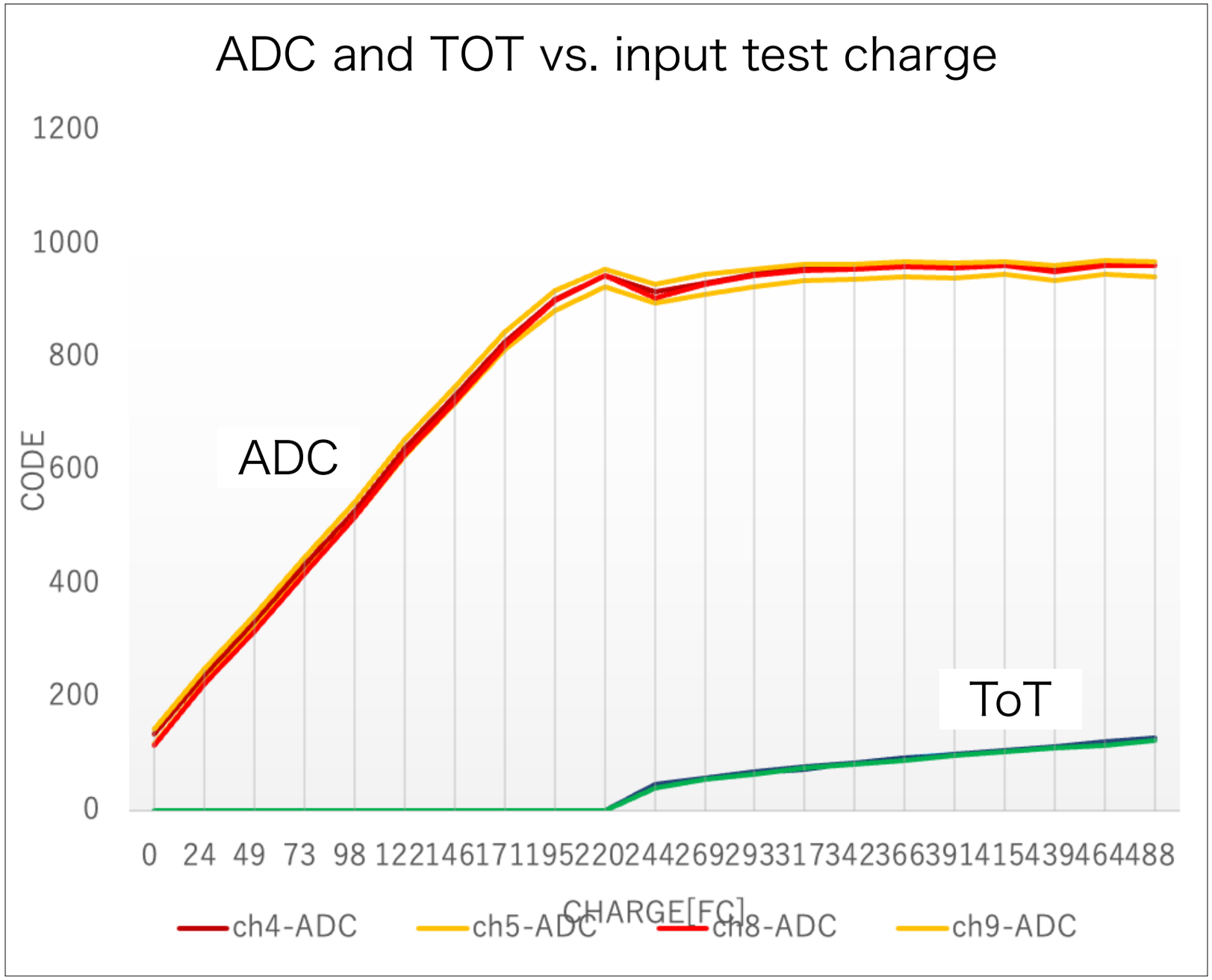
# TOT linearity




INL ~ 4%

# ADC / TOT connection




Except for small non-linear region, large dynamic range is covered.

# Summary and Plan

- We started the test study of HGCROC v2 for characterization and in preparation for mass production test in future.
- ADC / ToT linearities are obtained using internal test pulse.
- We need more understandings on the chip characteristics.
  ( $I^2C$ error, TOT behavior, ⋯)
- Test equipment will be designed using external test pulse so that I/O circuit failure should be detected.