Machine Interlocks in the Injectors

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IEFC workshop

22nd March 2011



Menu

Starter

Reminder on Machine Interlocks

Main course

Warm magnets Interlock system

Beam Interlock system

its Linac4 deployment

Desserts

Wrap-up

What are the "Machine Interlocks"?



Machine Interlocks hierarchy (LHC case)



(TE/MPE systems are in red)

Bruno PUCCIO (TE/MPE)

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Warm Magnets Interlock (WIC system)

Pierre Dahlen (TE/MPE)

WIC system Overview



WIC systems currently in Operation



WIC system: the main features

- □ Based of Safety PLC (Siemens S7-300 F series)
- □ (on purpose) Very simple process for PLC software
- Sensors/Magnets/Converters partition described in Configuration DB
- Reliable solution
- Remote test facility
- Generic solution to be deployed on any type/size of machine
- Dedicated PVSS application to allow supervision of:
 - ❑ Magnets & Power Converters Status
 - Interlock process (history buffer)
 - **Communication state (Ethernet & Profibus)**





PVSS application: few screen-shots...

SPS Transfer Lines



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PVSS application: monitoring views...

Magnets status



PVSS application: History Buffer

🏘 History Buffer						? 🗙
Mode History Snapshot Online Lines	_PS] isable the G displayed	Query optimisat	Time Filter From : 2011 🚖 To : 2011 🚔	/3 ♥/13 ♥ 10 ♥:50 /3 ♥/15 ♥ 14 ♥:19	139 Now Time zone = LOCAL TIME 139 Now * 140 Now * 140 Now * Events •	2014
	Ty	уре	Entity	Quantity	Status Invalid	
	*	-	*	*	v x x	
Local Time	Туре	Location	Entity	Quantity	Description	Status Invalid 🔺 🖛
2011.03.15 14:19:40.122						BAD 🗶
2011.03.15 14:19:40.122						BAD
2011.03.15 14:19:40.122						BAD
2011.03.15 14:19:40.122						BAD
2011.03.1514:19:40.122	CIWRA	LINAC3	CIWRA.351.LINAC3	ST_SUPPLY_24V_2	Status of the power supply 24V_2	ок
2011.03.1514:19:40.122	CIWRA	LINAC3	CIWRA.351.LINAC3	ST_SUPPLY_24V_1	Status of the power supply 24V_1	ок 📃
2011.03.1514:19:40.122	CIVRA	LINAC3	IA1.QDN02	ST_WATER_PRESS	Water pressure default	ок
2011.03.15 14:19:40.122		LINAC3	IA1.QDN02			ок
2011.03.1514:19:40.122	CIWRA	LINAC3	IA1.QDN04	ST_WATER_PRESS	vVater pressure default	ок
2011.03.15 14:19:40.122						ок
2011.03.15 14:19:40.122	CIWRA	LINAC3	IA1.QDN06S	ST_WATER_PRESS	vVater pressure default	ок
2011.03.15 14:19:40.122	CM/RA	LINAC3	IA1.QDN06S	ST_OVERTEMP	Signal received by the WIC from the thermo-switches mounted on the magnet	ок
2011.03.15 14:19:40.122	CIVRA	LINAC3	IA1.QDN08	ST_WATER_PRESS	Water pressure default	ок
2011.03.15 14:19:40.122						ок
2011.03.15 14:19:40.122	CINRA	LINAC3	IA1.QFN01	ST_WATER_PRESS	Water pressure default	ок
2011.03.15 14:19:40.122						ОК
2011.03.15 14:19:40.122	CIVRA	LINAC3	IA1.QFN03S	ST_WATER_PRESS	Water pressure default	ок
2011.03.15 14:19:40.122						
						Courtesy of F. Bernard (EN/ICE)

WIC system: future deployments

		Number of			
Machine	Protected Magnets	PLC crate	Remote I/O crates	Installation date	
HiRadMat	25	2	2	Q1/2011 🔶	ready for 1 st dry run (April 2011)
Booster	172	4	53	during 2011 + Xmas 2011/12	
Linac4 & Transfer line	98	2	6	2013	

Isolde	50	1	1	2013	should match
					corresponding
Elena ring	48	1	1	201x	schedules
0					

LHC chain status after planned deployments



+auxiliaries

	Protected Magnets	PLC crate	Remote I/O crates		
Machine					
PS main	~100	1	11		Not decided on
PS Auxiliary	~50	2	1		(first study only)
					(Due to lack of
SPS ring	~900	9	15	\mathbb{N}^{\perp}	resources) Not

possible to tackle so

large installation....



Benjamin Todd + Christophe Martin (TE/MPE)

Beam Interlock System Function



 Σ (User Permit = "TRUE") => Beam Operation is allowed

IF one User Permit = "FALSE" => Beam Operation is stopped

BIS: simplified layout

- Remote User Interfaces safely transmit Permit signals from connected systems to Controller
- **Controller** acts as a concentrator
- collecting User Systems Permits
- generating local Beam Permit
- **Controllers could be daisy chained** (Tree architecture) or could share Beam Permit Loops (Ring architecture)



Configuration

DB

JAVA

Application

Software Interlock System (SIS)

- Currently used for interlocking: SPS extractions, LHC Injection regions and circulating LHC beams (=> dump)
- Subscriptions to <u>thousands</u> control system devices / parameters.
- Export (among other tasks) signals to the different BIS (update period 2 s)
- □ Interlock types:
 - Initially: used simple test logic comparison of acquired value to reference value (number or Boolean) – hardcoded into configuration.
 - Now: more and more complicated interlocks (JAVA) that pull together multiple signals and DB references. Very flexible, but complex interlocks that are less easy to test.
- □ Very high reliability given the number of signals.
 - The SIS processes of SPS and LHC have never failed during operation in the last 2 years.
 - In case of failure, the timeouts (20 sec.) on the SIS inputs to the BICs lead to beam dump/injection or extraction inhibit.

BIS (&SIS) currently in Operation



BIS: main features

- Fast (~20µS reaction time from User Permit change detection to corresponding Local Beam Permit change)
- Reliable
 - Fully redundant HW process
 - Fail-Safe concept
- Available (Redundant Power Supplies)
- Maintainable
 - 100% Online Test Coverage
 - History buffer for recording I/O changes
- "Flexible"
 - half of User Permit signals could be remotely masked
 Masking conditioned by external signal (Safe_Beam Flag)
- Modular and Scalable
 - Ring architecture or Tree architecture
 - Daisy chain possible (BIC output connected to input of another BIC)
- Generic solution to any fast and reliable interlock requirement
 - Protect as much as small installation as large machine (27 km ring)
 - Based on BE/CO standard solutions (HW & SW)
- In operation in the SPS since 2005 with an extremely high availability



Manager board





BIS Application for CCC



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LHC

CNGS

LHC

TI8D

TI2D

BIS Application: History Buffer

🕌 New Histor	ry Buffer: CIB.BA4.TT40A				
History Buff	fer Memory Map				
-		F			
FILTER:	OPERATOR		Logging USE SNAPSHOT		
PERMIT	TIMESTAMP	DEVICE	DESCRIPTION		
	2011-03-21 11:13:39.73600	1 CIB.BA4.TT40A	MARKER: 1 us		
	2011-03-21 11:13:38.28238	CIB.BA4.TT40A	USER PERMIT: Ch 11(FMCM_MSE4183M): B T -> F		
	2011-03-21 11:13:38.2823/	8 CIB.BA4.114UA	USER PERMIT: Ch 11(FMCM_M5E4183M); A 1 -> F		
	2011-03-21 11:13:38:23333	6 CIB BA4 TT40A	USER PERMIT: CH 12(FMCM_RBH,400107): B T -> F		
	2011-03-21 11:13:38.25175	6 CIB.BA4.TT40A	USER PERMIT: Ch 13(EMCM_RBIH.400309); B T -> E		
	2011-03-21 11:13:38.25175	5 CIB.BA4.TT40A	USER PERMIT: Ch 13(FMCM RBIH.400309): A T -> F		
	2011-03-21 11:13:38.20734	3 CIB.BA4.TT40A	USER PERMIT: Ch 10(Bumpers currents): A T -> F		
	2011-03-21 11:13:38.20734	3 CIB.BA4.TT40A	USER PERMIT: Ch 10(Bumpers currents): B T -> F		
	2011-03-21 11:13:38.20723	6 CIB.BA4.TT40A	USER PERMIT: Ch 9(MSE septum current): B T -> F		
	2011-03-21 11:13:38.20723	6 CIB.BA4.TT40A	USER PERMIT: Ch 9(MSE septum current): A T -> F		
	2011-03-21 11:13:38.20679	CIB.BA4.TT40A	LOCAL PERMIT: B T -> F		
X m	2011-03-21 11:10:36:20079		LICED DEDMIT: Ch OTTAR convertore durrente): B.T>.E.		
	2011-03-21 11:13:38:20076	8 CIB BA4 TT40A	LISER PERMIT: Ch 8(TT4U sonverters currents): A T -> F		
	2011-03-21 11:13:38.20600	2 CIB.BA4.TT40A	MARKER; 2 us		
	2011-03-21 11:13:38.20274	1 CIB.BA4.TT40A	LOCAL PERMIT: A F -> T		
	2011-03-21 11:13:38.20274	CIB.BA4.TT40A	LOCAL PERMIT: B F -> T		
	2011-03-21 11:13:38.20274	CIB.BA4.TT40A	USER PERMIT: Ch 10(Bumpers currents): B F -> T		
	2011-03-21 11:13:38.20274	CIB.BA4.TT40A	USER PERMIT: Ch 10(Bumpers currents): A F -> T		
	2011-03-21 11:13:38.20266	4 CIB.BA4.TT40A	USER PERMIT : Ob 9(MSE septum current): B F -> T		
	2011-03-21 11:13:38.20266	4 CIB.BA4.114UA	USER PERMIT: Ch 9(Inve septum current): A F -> 1		
	2011-03-21 11:13:38:20222	5 CIB BA4 TT40A	LISER PERMIT: Ch 8(TT40 converters currents): A E -> T		
	2011-03-21 11:13:38.19524	3 CIB.BA4.TT40A	USER PERMIT: Ch 10(Bumpers currents): A T -> F		
	2011-03-21 11:13:38.19524	3 CIB.BA4.TT40A	USER PERMIT: Ch 10(Bumpers currents): B >> F		
	2011-03-21 11:13:38.19513	6 CIB.BA4.TT40A	USER PERMIT: Ch 9(MSE septum current): B T -> P		
	2011-03-2 11:13:38.19513	6 CIB.BA4.TT40A	USER PERMIT: Ch 9(MSE septum current): A T -> F		
	2011-03-21 1:13:38.19479	CIB.BA4.TT40A	LOCAL PERMIT: B T -> F		
	2011-03-21 11:13:38.194/9	CIB.BA4.114UA	LOCAL PERMIT: A 1 -> F		
	2011-03-21 11:13:38.19478	8 CIB.BA4.114UA	USER PERMIT: Ch 8(1140 converters currents): B 1 -> F		
	2011 03-21 11:13:38 19070	8 CIB.BA4.TT40A	LOCAL PERMIT: B E -> T		
	2011-03-21 11:13:30.19070	8 CIB.BA4.TT40A	LOCAL PERMIT: A F -> T		
	2011-03-21 11:13:38,19070	8 CIB.BA4.TT40A	USER PERMIT: Ch 10(Bumpers currents): B F -> T		
	2011-03-21 11:13:38.10070	8 CIB.BA4.TT40A	USER PERMIT: Ch 10(Bumpers currents): A F -> T		
	2011-03-21 11:13:38.19062	4 CIB.BA4.TT40A	USER PERMIT: Ch 9(MSE septum current): B F -> T		
	2011-03-21 11:13:38.19062	4 CIB.BA4.TT40A	USER PERMIT: Ch 9(MSE septum current): A F -> T		
	2011-03-21 1:13:38.19025	CIB.BA4.114UA	USER PERMIT: Ch 8(1140 converters currents): B F -> 1		
	2011-03-21 11 13:38 15724	4 10.0A4.1140A			
	2011-03-21 11:13:38.15724	4 C m m	2011-02-21 11:12:20 10/70		LICER REPAIT: Ch 9/TT/0 convertore currente): P.T> E
pi pi	2011-03-21 11:13.88.15723	6 CI P-3 P-3	2011-03-21 11,13,30,19476	0 CID.0A4.1140A	OBER FERMIT, CHO(THO CONVENERS CUITERIS), BIT -> P
p p p	2011-03-21 11:13:30.15723	6 CL 🛄 🛄	2011-03-21 11:13:38.19478	8 CIB.BA4.TT40A	USER PERMIT: Ch 8(TT40 converters currents): A T -> F
	2011-03-21 11:13:38 15689				
			2011-03-21 11:13:38.190/0	J8 CIB.BA4.114UA	LOCAL PERIMIT: B F -> 1
	\ \		E 2011-03-21 11/13/38 10076		LOCAL PERMIT: & E -> T
	\				
	, in the second s		➡ 2011-03-21 11:13:38.19070	18 CIB.BA4.TT40A	USER PERMIT: Ch 10(Bumpers currents): B F -> T
			2011 02 21 11 12 20 10070		LICED DEDMIT, Ch 10/Dumporo curronto), A.F. > T
			2011-02-51 11:12:38:180\(10 CIB, BA4, 1 14UA	ODER FERMIT : UN 10(BUMPERS LUMENS) : A F *> 1

BIS Application: Extraction cycles view

SPS BIS Monitor V6.0.9/Mar 11		
File BIC Details MKE & BETS LTIM & Prepulse Inits & Resets Help	Timing	
LHCB1 RBA: jwenning	LHC2 >> SPS_DUMP # 57638	
Extraction Overview MKE6 Status BIC Overview Active Intlks Masks		
BIC Permit Status LHCB1		
Time User EXT1 TT60A TT60B TI2U TI2D	INJ1.1 INJ1.2	
15:27:00 LHC3		
15:26:52 LHCFAS11		
15:26:28 EHC2 8	BIC Details	
15.28.03 LHCFAST1		
15:25:39 LHC2 8	Extraction	
15:25:21 LHC3	Extraction times [ms] : 5345	
15:25:14 LHCFAST1	Channel Mapping	
15:24:50 LHC2 8	1: Vacuum TT60 2: WIC TT60 3: OP Switch 4: MKE6 Status	
15:24:32 LHC3	5: MSE/MST Girder & Magnet 6: 7: 8: PC FEI TT60	
15:24:25 LHCFAST1	9: PC FEI NSE/NST/LSS6 Bumpers 10: PC FEI NBB TT60 11: 12: 13: FM/W NSE618M 14: FM/W NST617M	
15:24:01 LHC2 8		
15:23:43 LHC3	All Channels Overview Mask Control	
15:23:36 LHCFAST1	Summary CIB.BA6.TT60A	
15:23:12 LHC2 8	Time User In1 In2 In3 In4 In5 In6 In7 In8 In9 In10 In11 In12 In13 In14 Sw SBF Out	
	15:28:52 LHCFAST1	
	15:26:28 LHC2 20 20 20 20 20 20 20 20 20 20 20 20 20	
Courtesy of		
0.vvenninger		
	15:24:25 LHCFAST1	
	15:23:12 LHC2 LHC2 LHC2 LHC2 LHC2 LHC2 LHC2 LHC	
	15:22:54 LHC3 20 20 20 20 20 20 20 20 20 20 20 20 20	

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BIS Application: Timing Diagram



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BIS: Future deployments



	Num	ber of		
Machine	User Interface	Controller	Installation date	
HiRadMat	10	1	Q1/2011	ready for 1 st dry run (April 2011)
3 MeV Test Stand	7	1	Mid 2011	
Linac4 & Transfer line	23	3	2013	
Booster ring & ejection	24	2	2013	

LHC chain status after planned deployments





BIS Engineering Specifications



Linac4, Transfer Lines and Booster

3Mev Test Stand

BIS for LINAC4 & PSB: Design Principle (1)

- Main constraints:
 - Multiple 'interlock zones' due to several destinations
 - for Linac4: L4DUMP, LBE, LBS, PSB
 - for Booster: BDUMP, ISOGPS, ISOHRS, PS
 - PSB is (timing) master of Linac4
 - Maximize proton delivery to the experiments via 'External Conditions'; the user (+beam destination) is calculated for the current cycle depending on some necessary conditions;
 - This analysis takes up to 3 basic periods and yields the decision if the 'normal' or 'spare' (or none) cycle should be executed
 - Beam stoppers and bending magnet rise-time too slow
- Must consider PSB and Linac4 interlock systems in parallel (also due to new PSB injection with Linac4)

Courtesy of B.Mikulec

BIS for LINAC4 & PSB: Design Principle (2)

- Three actors:
 - 1. Hardware interlock system (BIS): reliable, fast
 - For fast reaction times
 - If considered useful to avoid machine activation
 - 2. Software interlock system (SIS): flexible
 - For slow-changing parameters
 - If some more complex logic needs to be adopted
 - 3. External conditions (EC): for proton optimization
 - Consider user requests
 - Method also useful for ring-specific interlocks

Courtesy of B.Mikulec

Interlock Zones

• Linac4 interlock zones





BIS Linac4 & PSB layout



Truth table example: "Choppers" BIC



Wrap-up (wic)

- WIC = improved system
- Generic solution to protect resistive magnets
- Rely on partnership with EN-ICE group
- After the long shutdown:

- WIC system will be present in two ends of the LHC injectors chain
- => Not deployed in PS & <u>SPS</u>
- Resources issue
 - Minimal level of staffing for coming deployments (and subsequently the Maintenance)
 - Not possible to tackle large installations in the near future

Wrap-up (BIS)

Fast & reliable

- Modular & scalable
- □ BIS (&SIS) = CERN Generic solution
- For Linac4 & PSB: Timing provides more flexibility
- Maximize efficiency for Beam Operation
- After the long shutdown:
 - BIS installed in two ends of the LHC protons chain
 - No decision has been made for deployment to PS
- □ (f.t.b.) There are no plans to deploy BIS elsewhere...

Fin

Thank you for your attention