The TOF detector of the ALICE experiment

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for the ALICE-TOF Group,

Seoul, October 9, 2004

- The role of the TOF in ALICE;
- Detector choice and performance;
- The front end electronics;
- Read out electronics;
- Irradiation results;
- Module “0” construction;
- Starting MRPC massive production

ALICE TOF is a Italian-Russian-Korean collaboration led by A. Zichichi

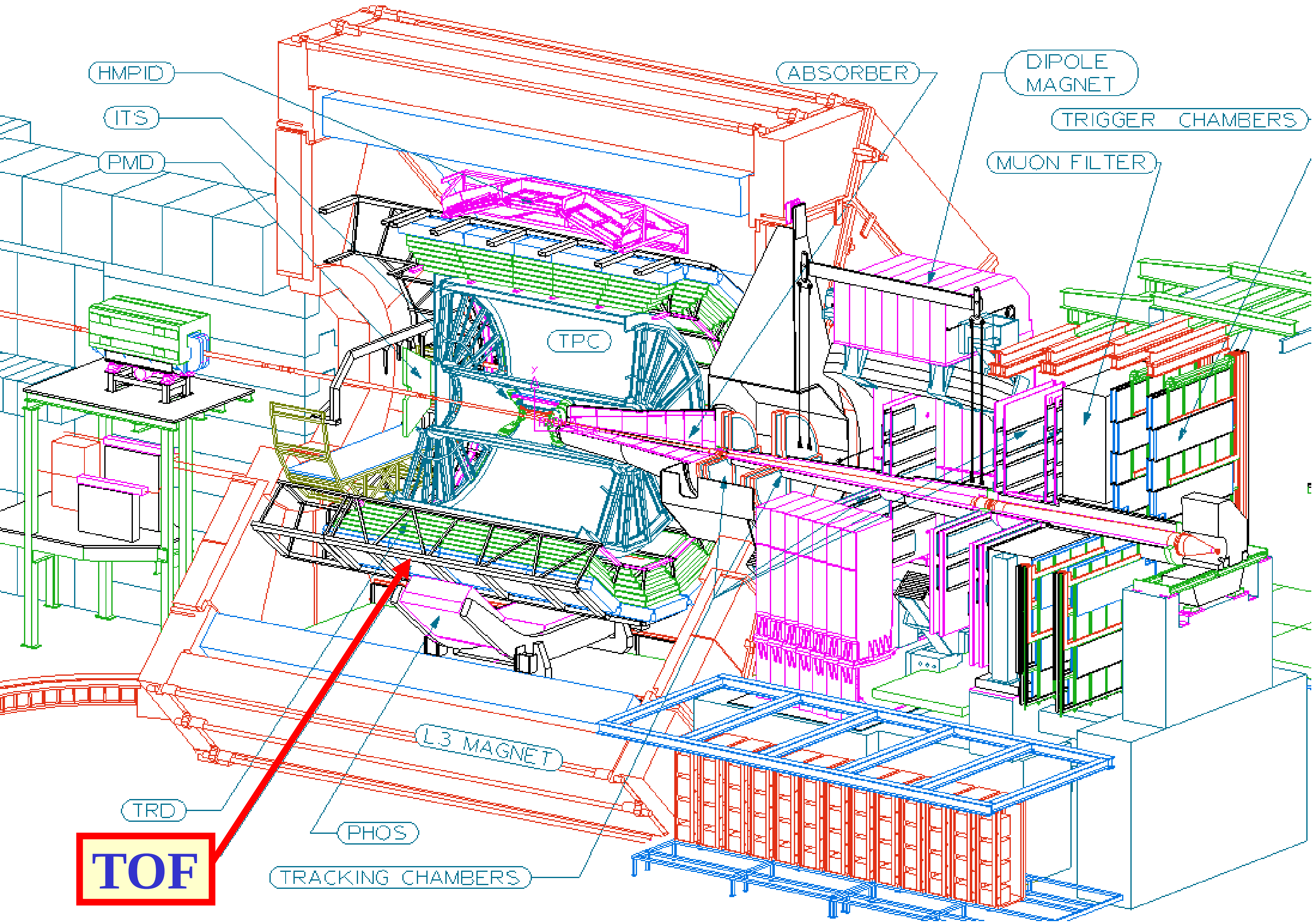
- University and INFN of Bologna (Italy);

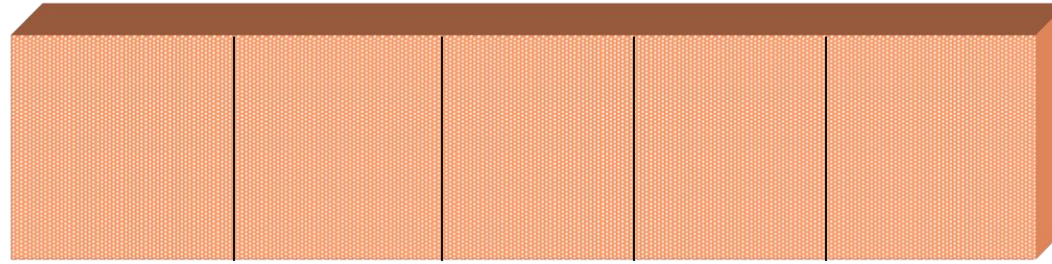
- University and INFN of Salerno (Italy);

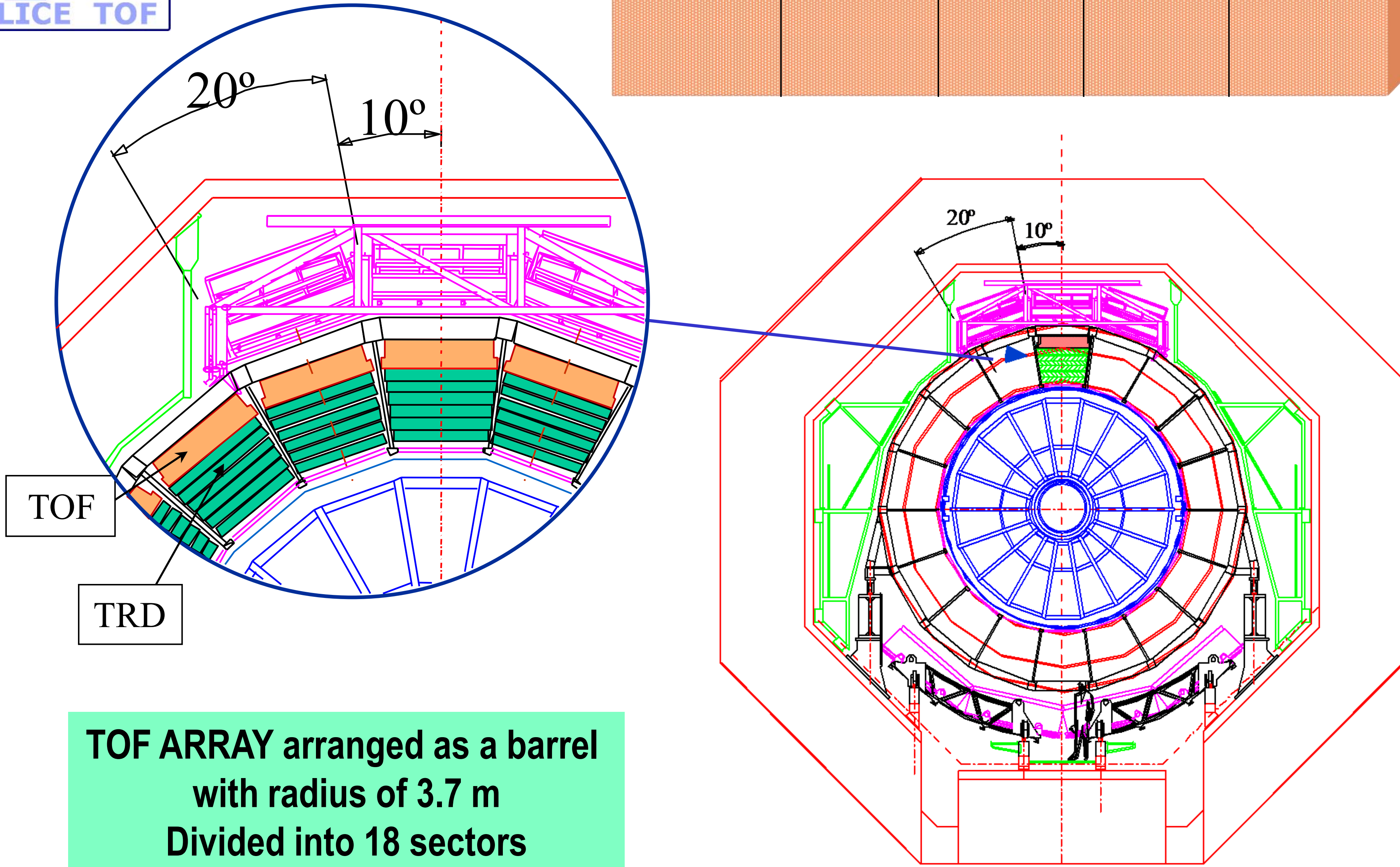
- ITEP Moscow (Russia);

- University of Kangnung (South Korea);

About 50 physicists.


HMPID
ITS
PMD
ABSORBER
DIPOLE MAGNET
TRIGGER CHAMBERS
MUON FILTER
TPC
L3 MAGNET
TRD
PHOS
TRACKING CHAMBERS
TOF



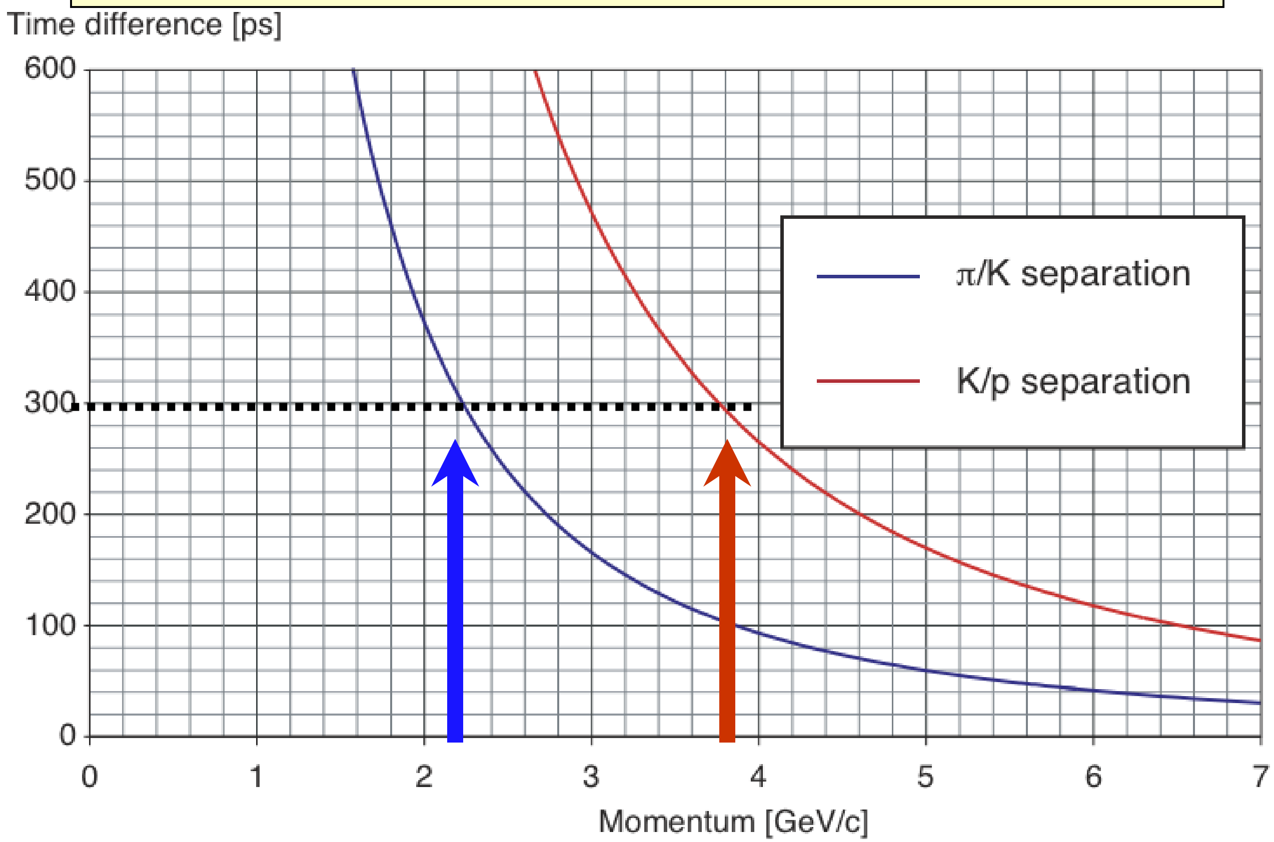


TOF ARRAY arranged as a barrel with radius of 3.7 m Divided into 18 sectors

Time difference = f(L,p,m_1,m_2)

$$\Delta t_{1\text{-}2} = \frac{L}{c}\left(\frac{1}{\beta_1} - \frac{1}{\beta_2}\right) = \frac{L}{c}\left(\sqrt{1 + m_1^2c^2/p^2} - \sqrt{1 + m_2^2c^2/p^2}\right) \approx \frac{Lc}{2p^2}\left(m_1^2 - m_2^2\right)$$

Time difference at 3.7 m



For example if time resolution of TOF is 100 ps
3σ separation equivalent to 300 ps difference

π/K up to 2.2 GeV/c

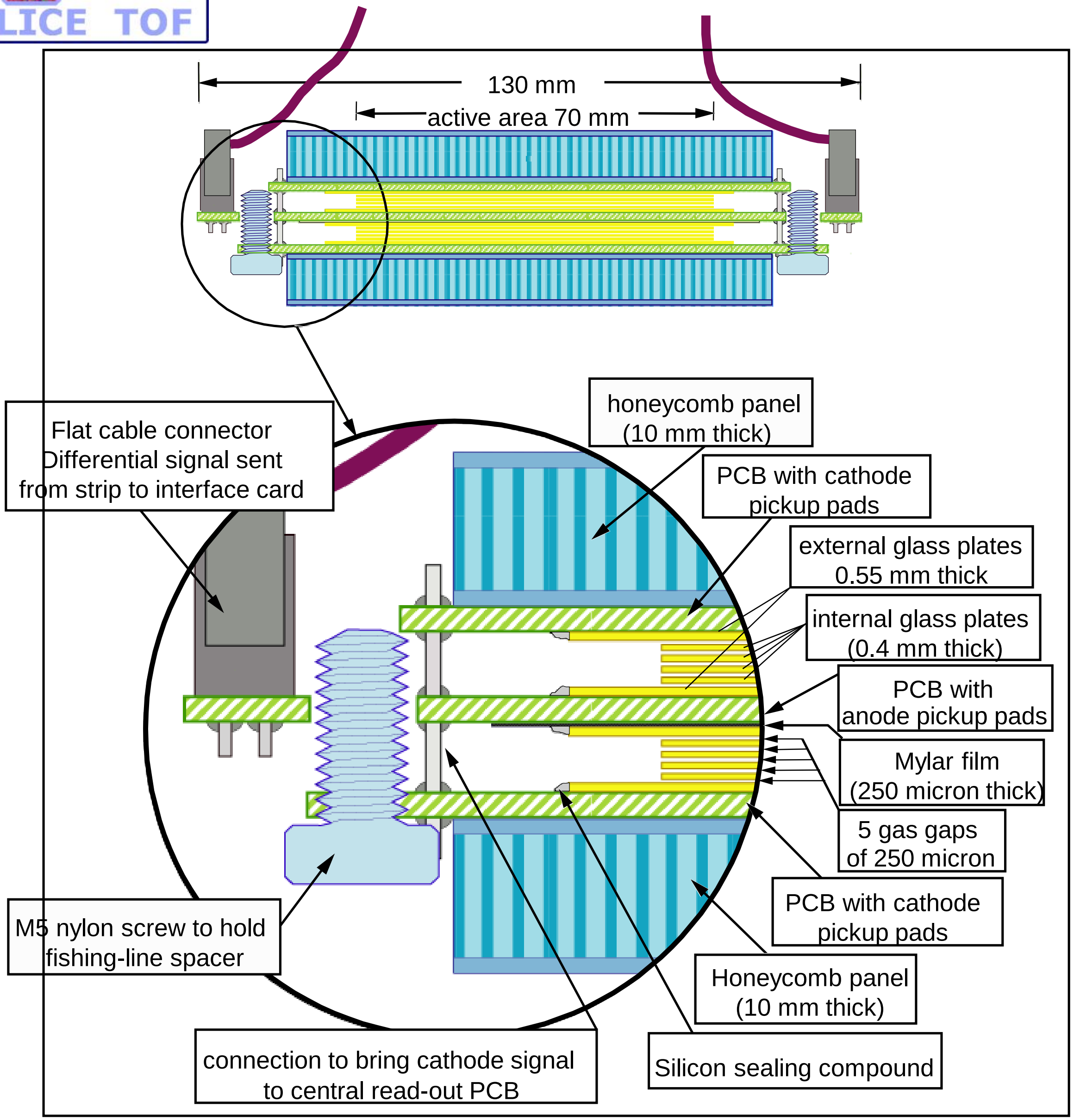
K/p up to 3.8 GeV/c

What is needed?

- 100 ps time resolution;
- Large array to cover whole ALICE barrel ~ 160 m^2 ;
- Highly segmented - 160,000 channels of size (2.5 x 3.5) cm^2.

GASEOUS DETECTOR IS THE ONLY CHOICE

Cross section of double-stack MRPC



Specifications

Double stack
- each stack has 5 gaps
(i.e. 10 gaps in total)

250 micron gaps with spacers made from nylon fishing line

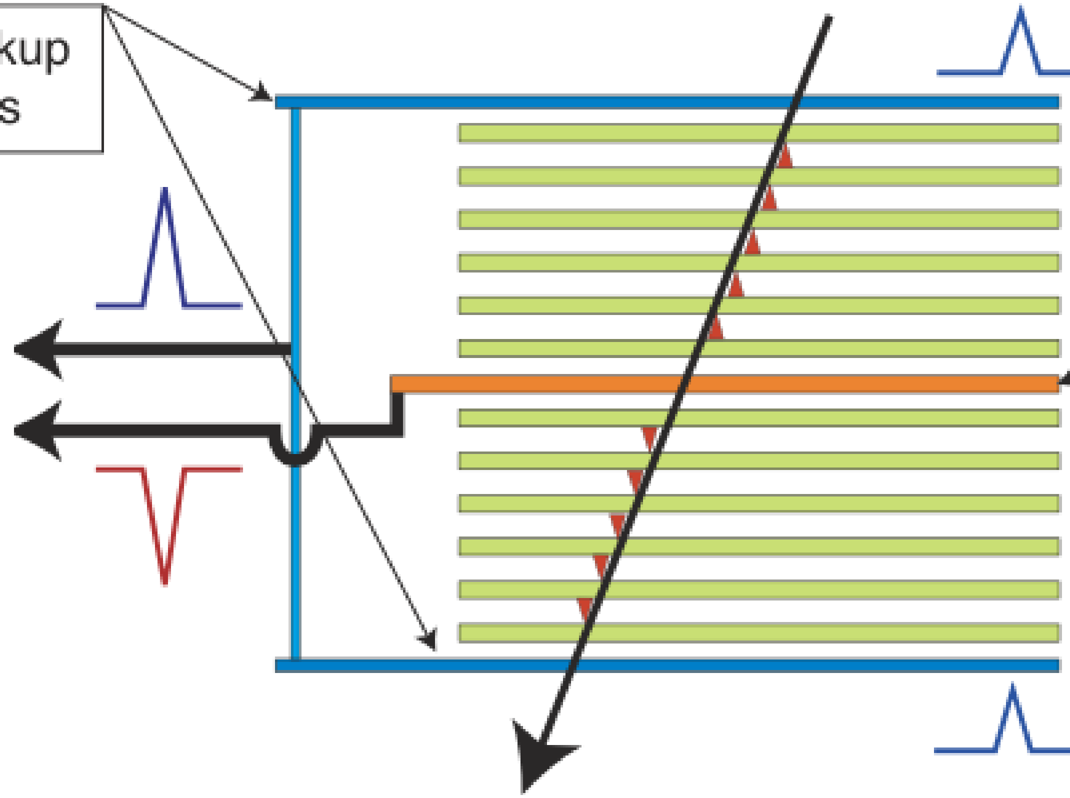
Resistive plates 'off-the-shelf' soda lime glass

400 micron internal glass
550 micron external glass

Resistive coating 5 MΩ/square

ALICE-TOF MRPC has 10 gas gaps, each of 250 micron width. Built in the form of strips, each with an active area of 120 x 7 cm^2 read by 96 pads (each 2.5 x 3.5 cm^2)

Gas mixture: $C_2F_4H_2(90\%)$- $C_4H_{10}(5\%)$ + $SF_6(5\%)$

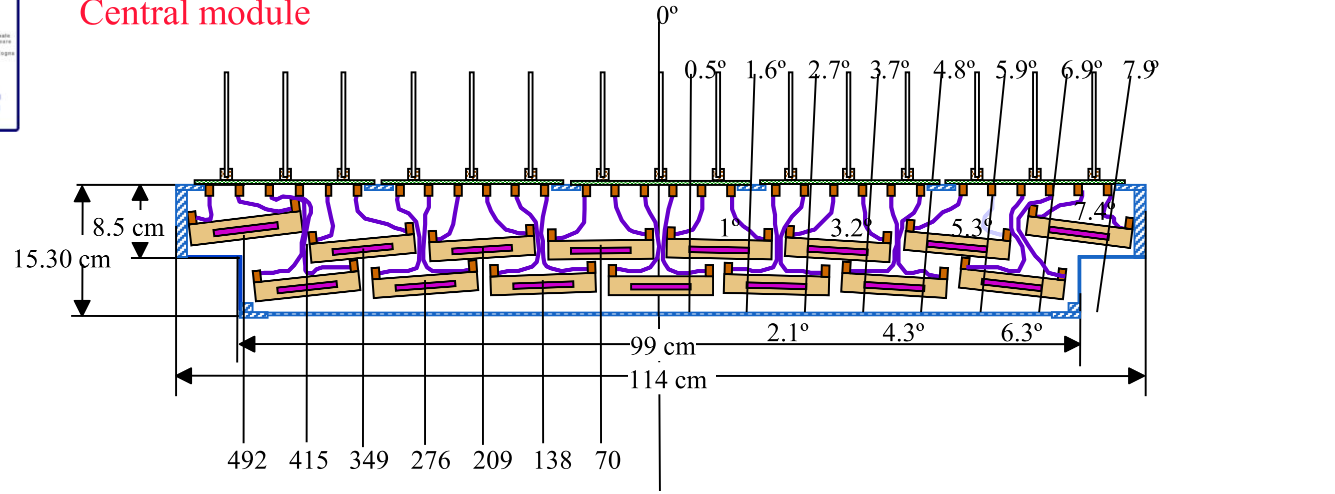


Stack of equally-spaced resistive plates with voltage applied to external surfaces (all internal plates electrically floating)

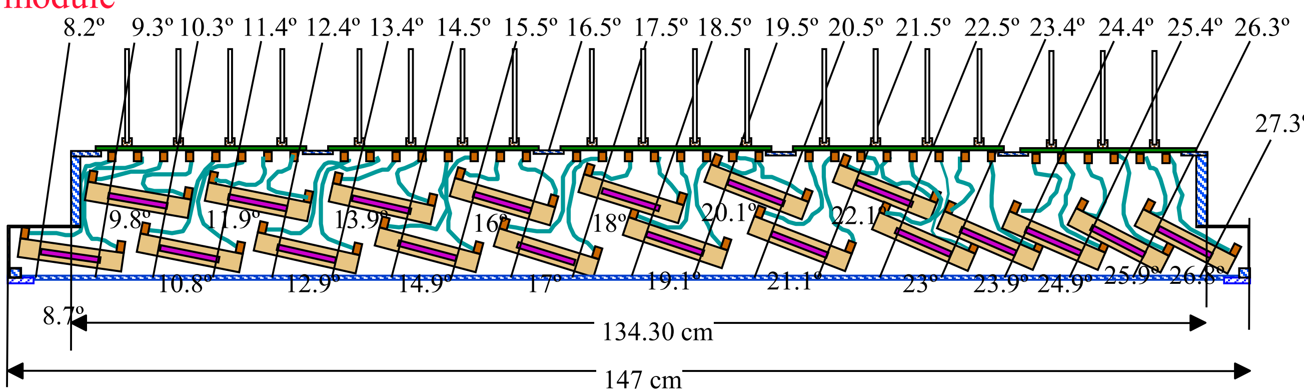
Pickup electrodes on external surfaces (resistive plates transparent to fast signal)

Timing depends on individual gap; Efficiency depends on total gas gap (10x250 μm)

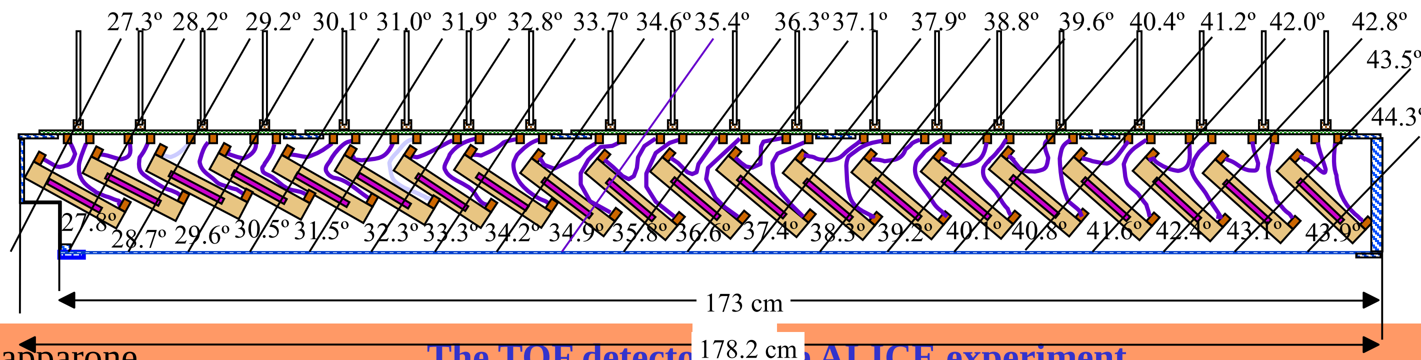
Central module

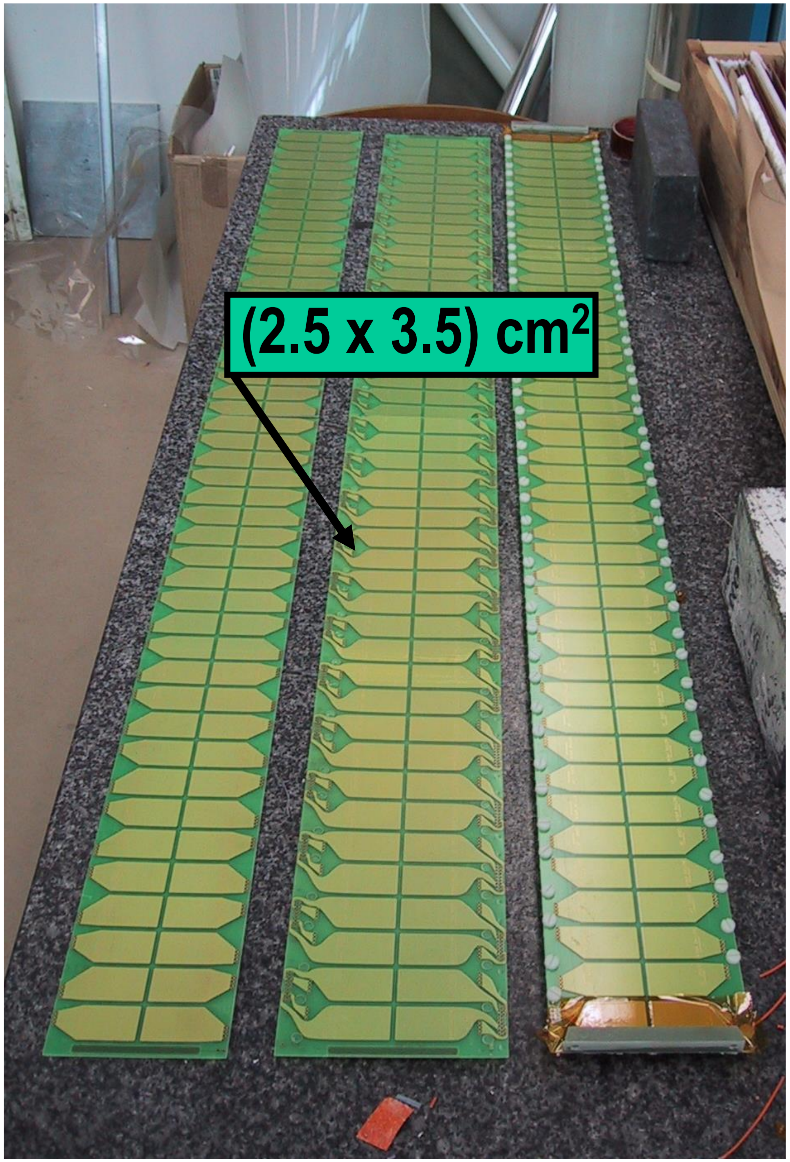


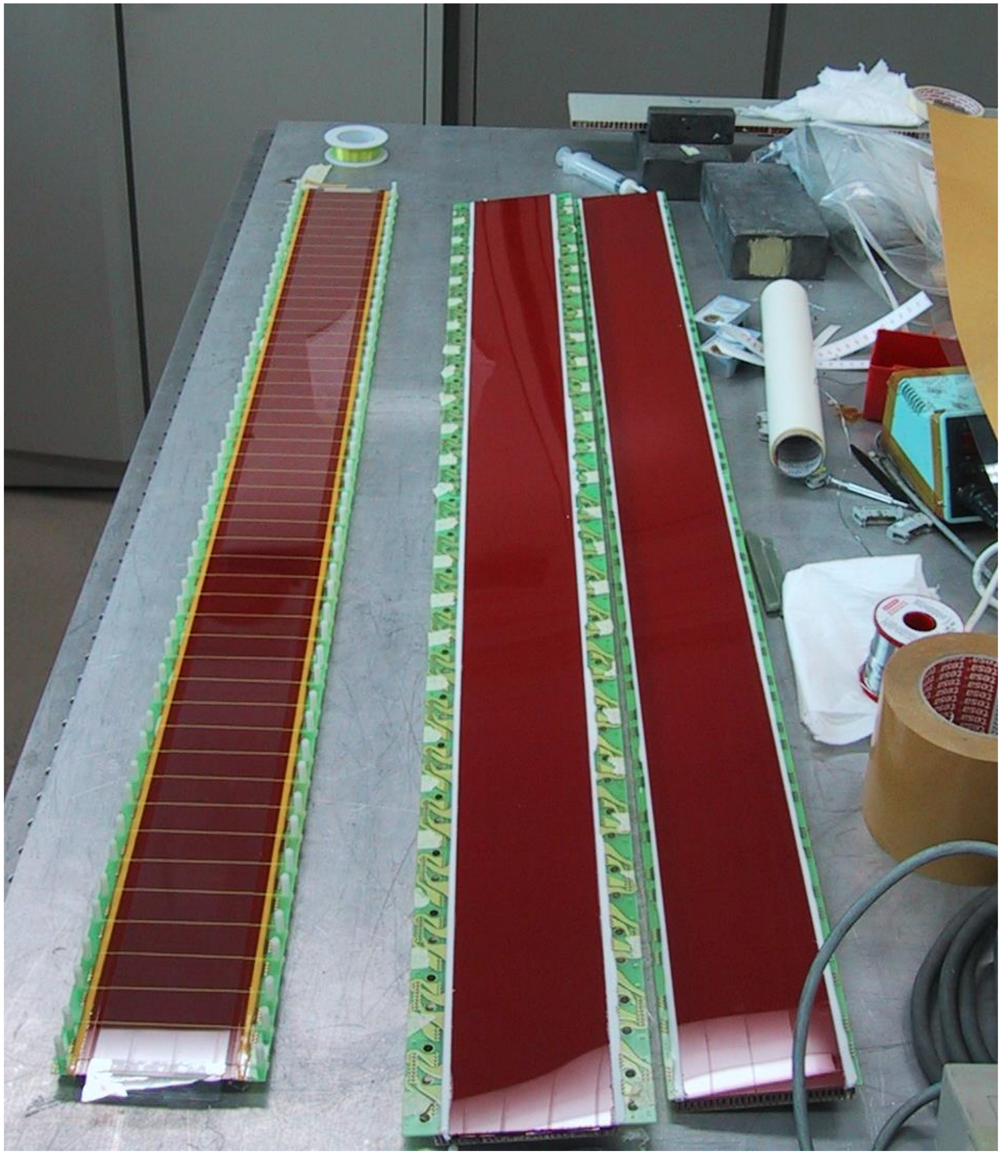
Intermediate module

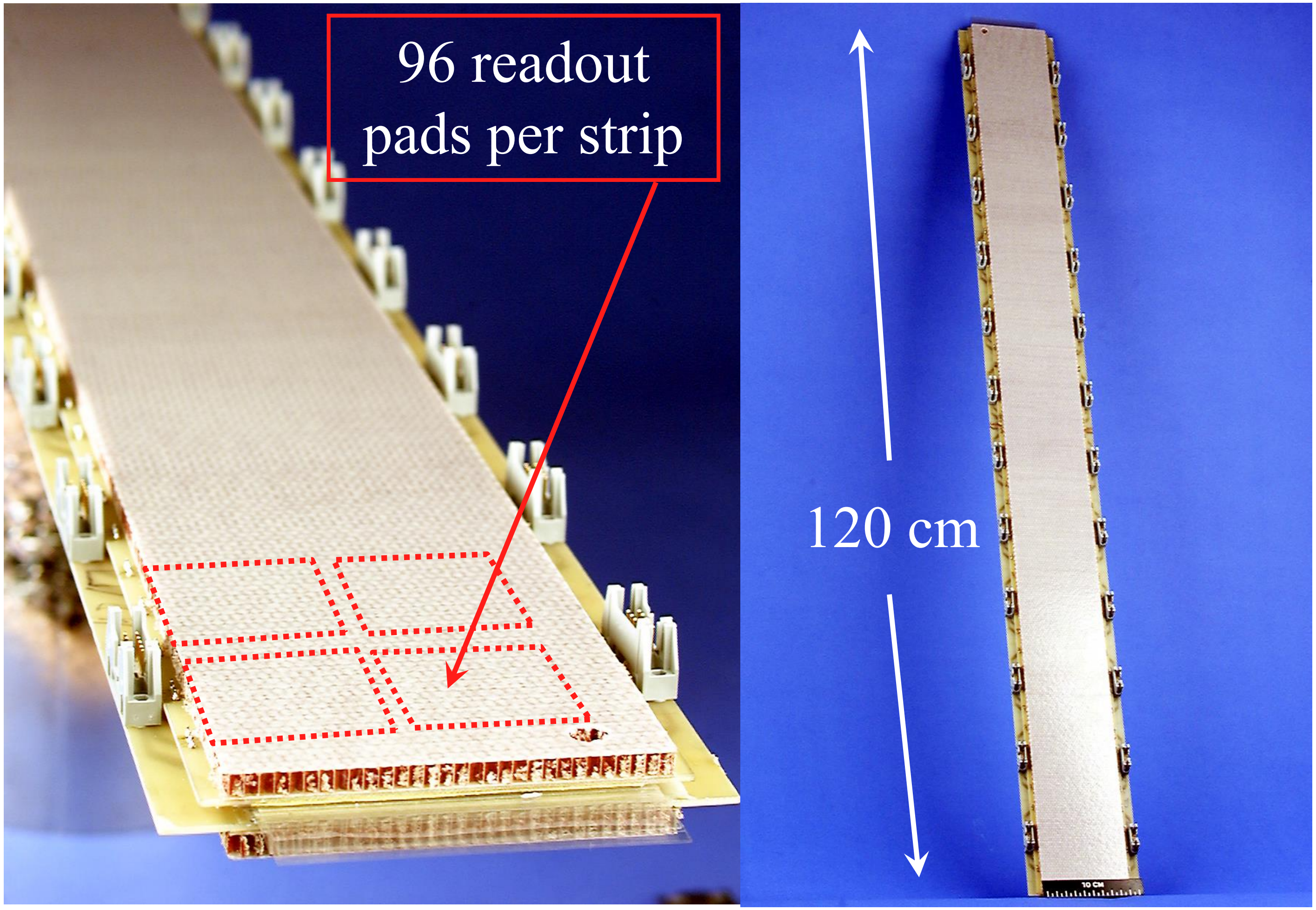


Outer module




(2.5 x 3.5) cm^2




96 readout
pads per strip
120 cm

Front end Electronics

Good results obtained with a FEC made of discrete components (Ampli Maxim 3760, Comparator Maxim 9691) :

Test beam October 2002, 152 pads analyzed:

$<\varepsilon> = (99.60 \pm 0.05)$ **$<\sigma_t> = (63 \pm 1)$ ps**

Maxim based FEC lacks:

- Dissipated power: 400 mW/ch;
- Mounting on the FECs of an high number of components;
- Non ideal choice: (non differential input signal, input capacitance not fully matched, etc.)

ASIC Front End Card

New Front End Card ASIC based (0.25 μm CMOS)

Main advantages

- Input stage (and following) fully differential;

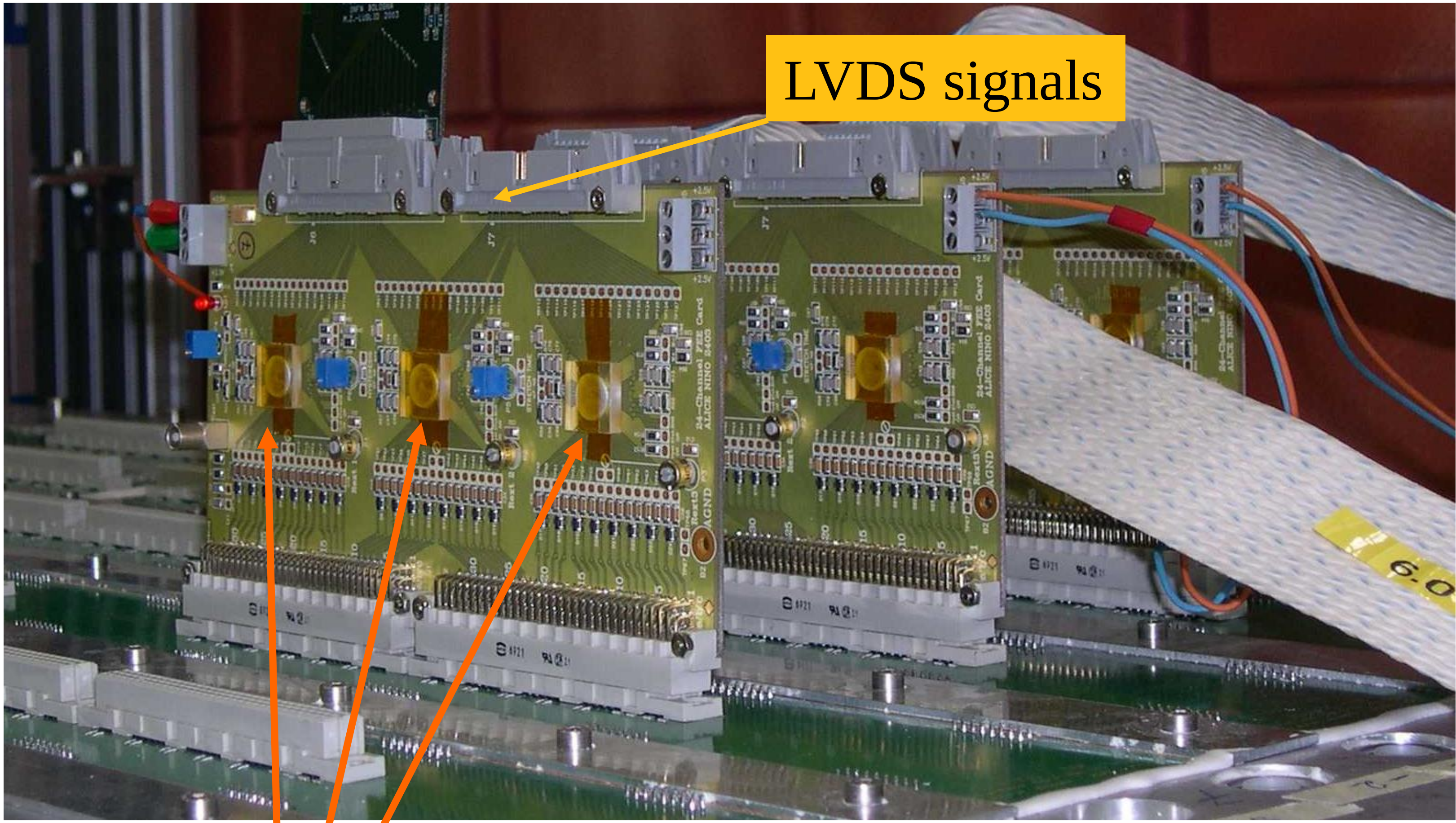
- Adjustable input resistance (30 Ω – 100 Ω);

- Power: 40 mW/channels (to be compared with 400 mW/channels of the Maxim based FEC);

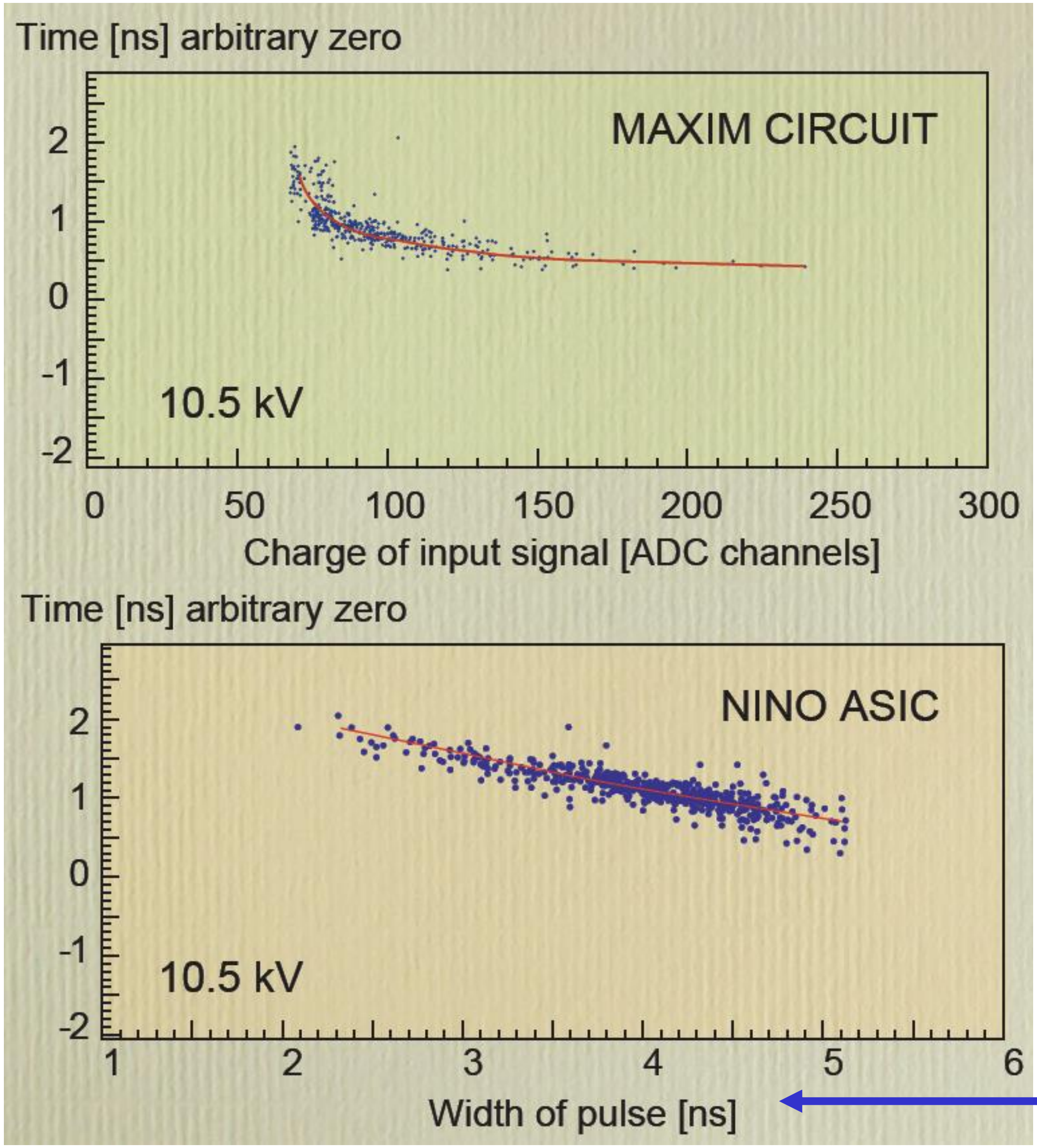
- Nice matching with detector capacitance (30 pF);

-LVDS Output signal, compatible with HPTDC input (no ECL-LVDS conversion required).

Test beam October 2003



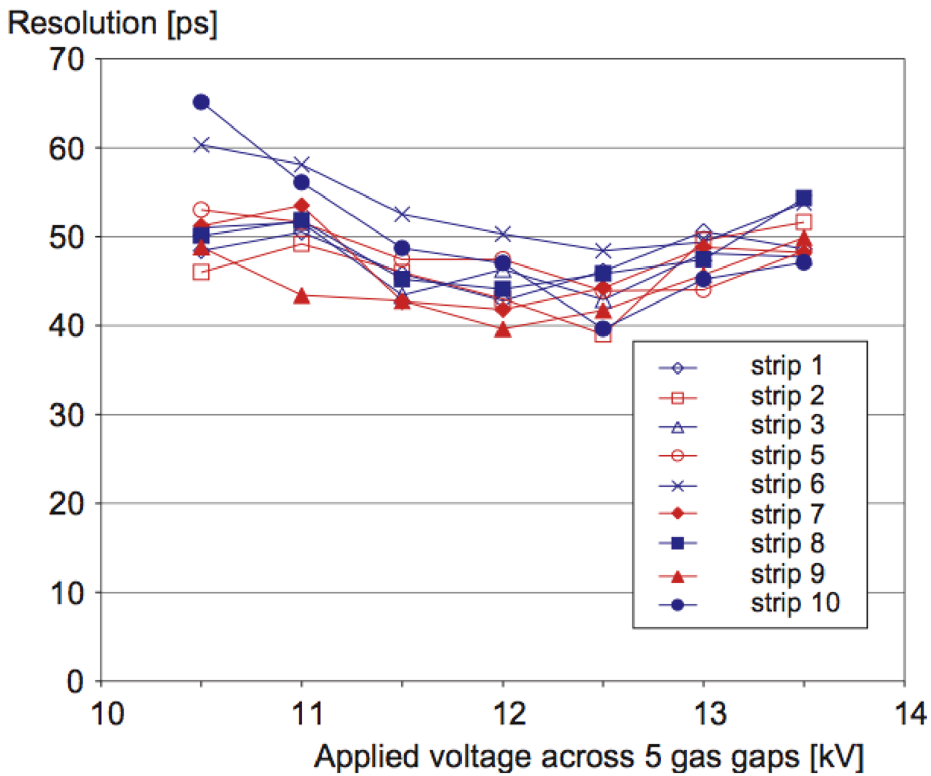
ASIC chips (8 channels/chip)

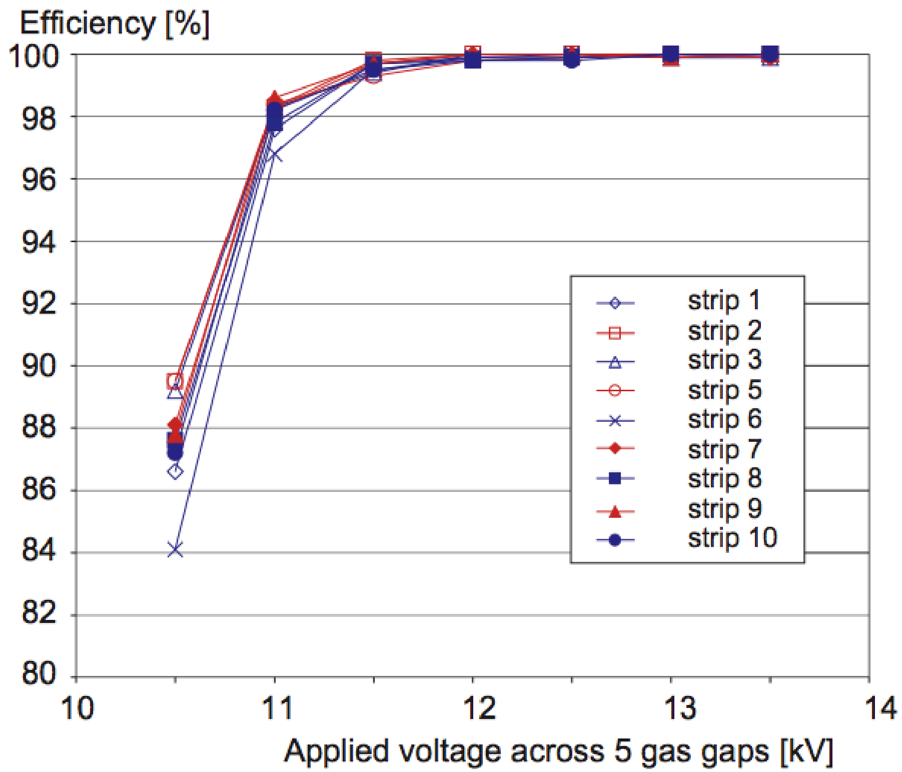


ASIC: Timing improved in the low pulse region (short duration); time-slewing correction easier

Pulse width appropriate for T-S correction

October 2003 test beam with NINO ASIC



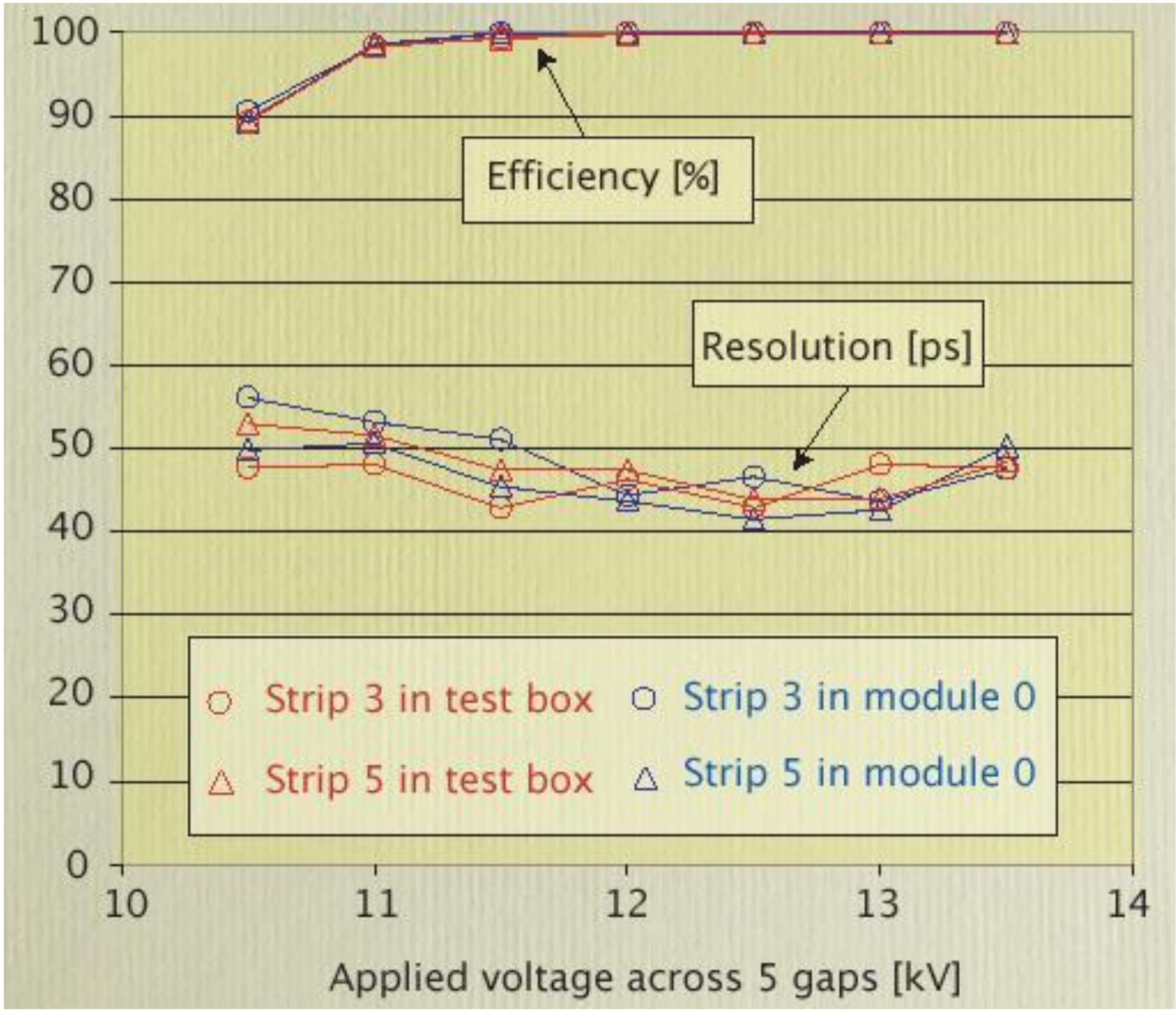


Time resolution: **40 - 50 ps** between **11.5 and 13 kV**

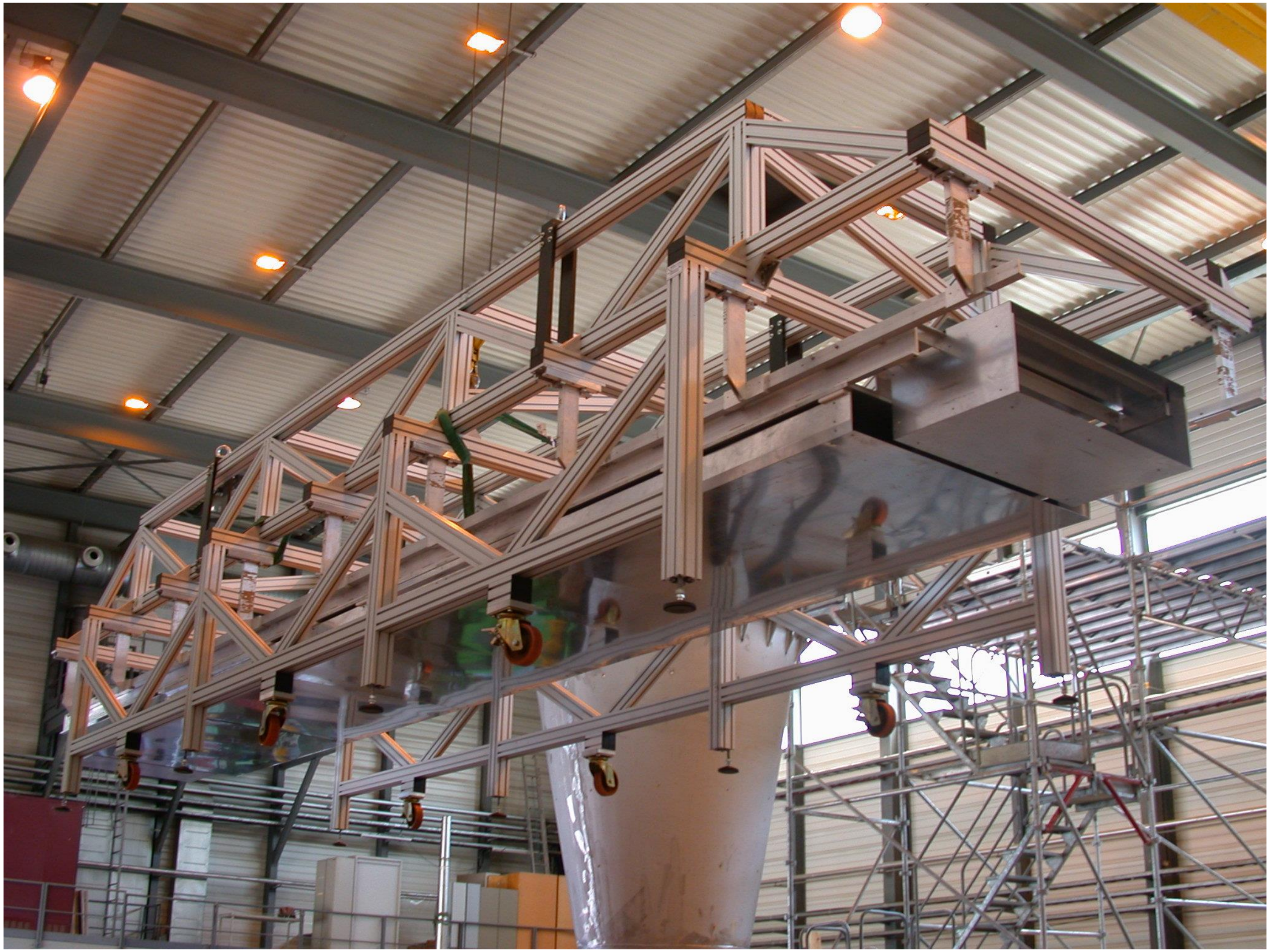
MODULE “0” CONSTRUCTION..

Test beam, (October 2003)

No difference in performance observed when strips inserted in module 0



MECHANICS: MODULES MOUNTING



TOF CRATES

19 TRM

(TDC readout module)

2 DRM

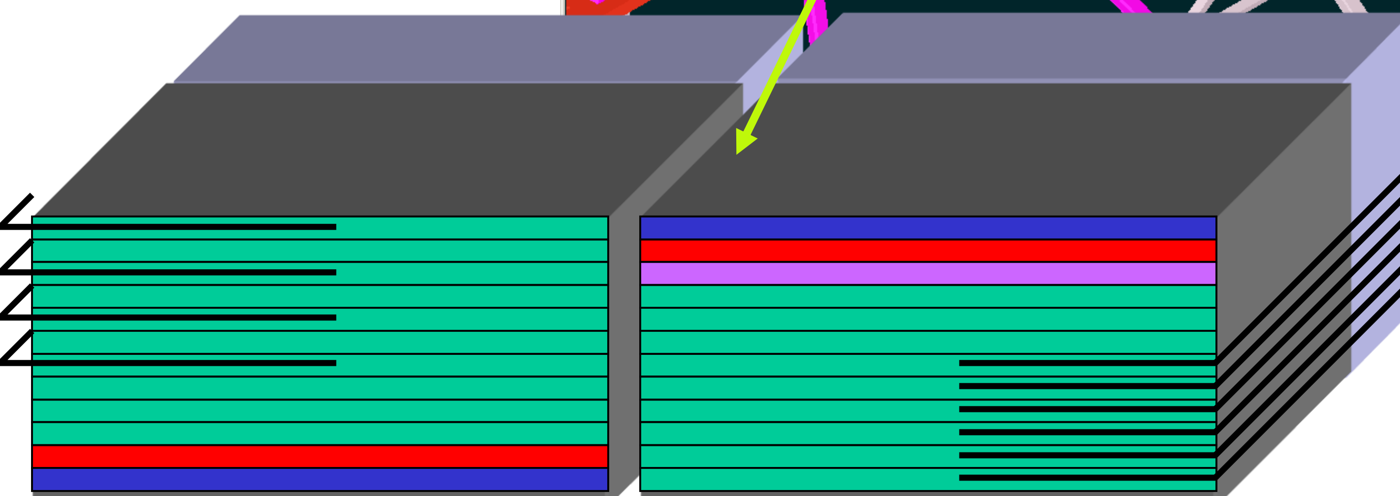
(Data Readout Manager)

2 LTM

(Local Trigger and Module)

1 CPM Clock and

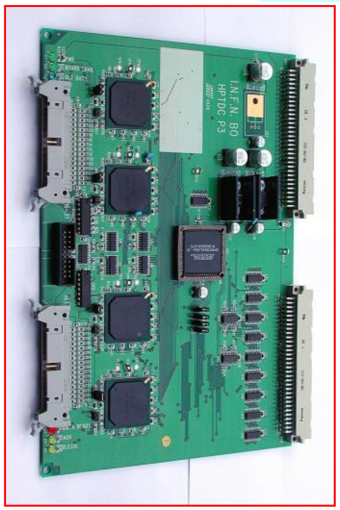
Pulser Module

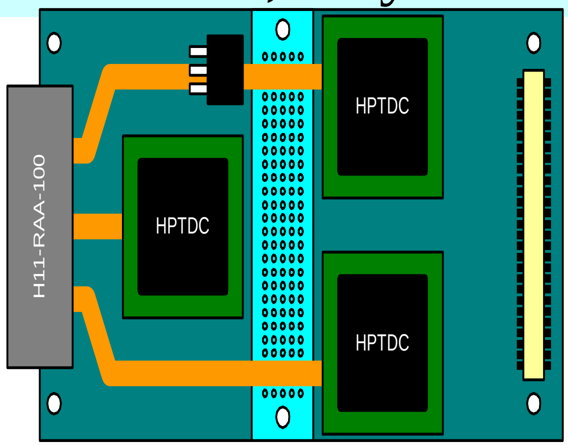


Final TRM layout

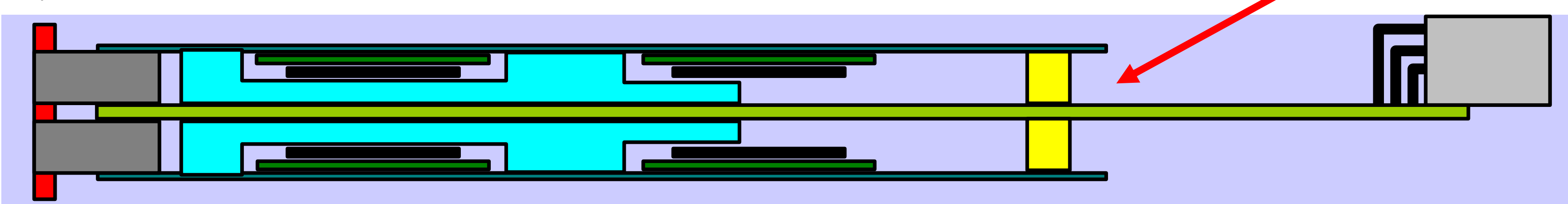
-19 TRM cards housed in two crates at the side of the sector;

- Each TRM made of 1 central PCB for the FPGAs, SRAM and FIFO (master).
- 5 “piggyback” cards(slaves) per side, each with 3 HPTDC chips (match with FEA, easy mounting) .





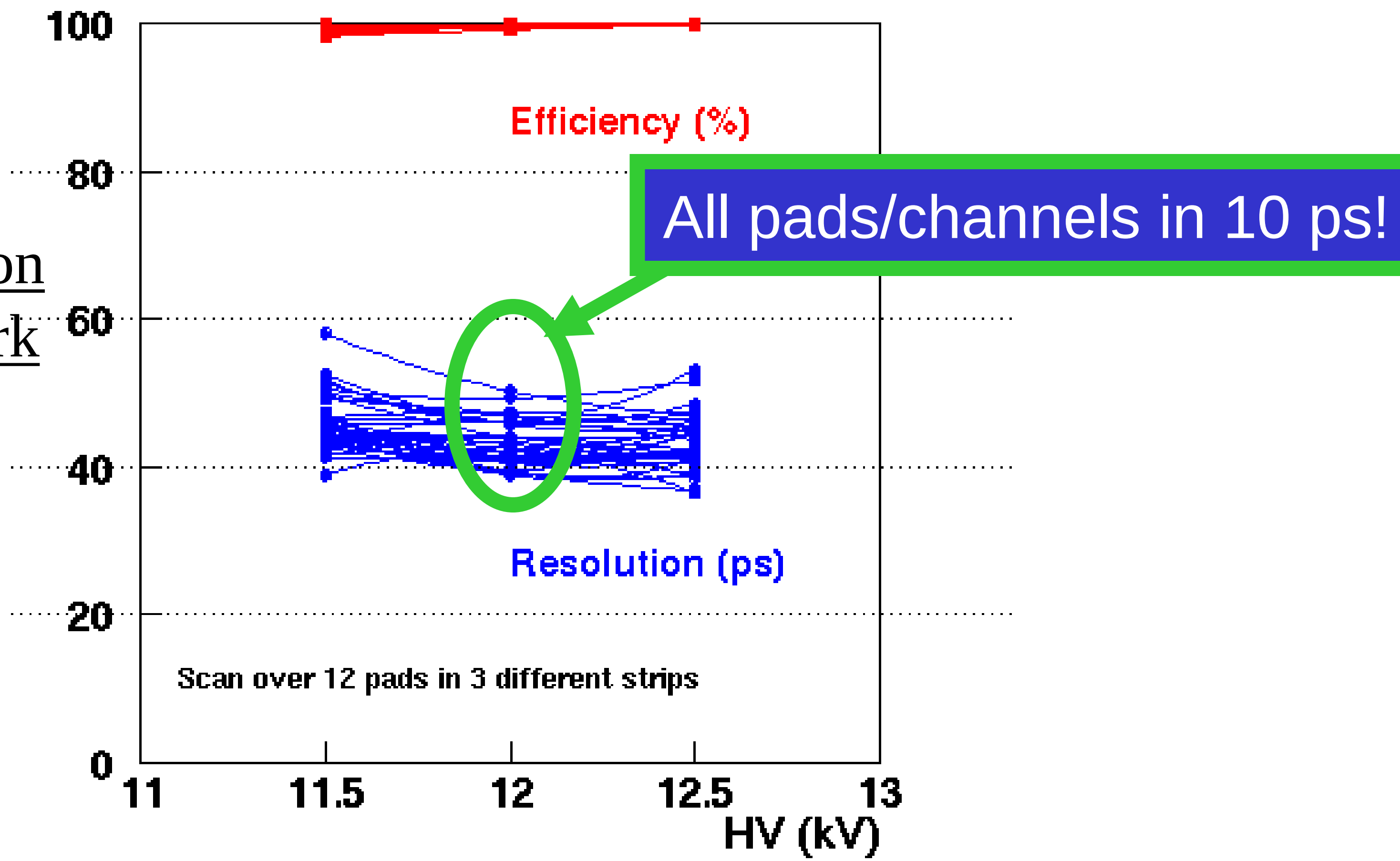
10 cards



central aluminium bar for heat dissipation

Full chain MRPC+FEA+HPTDC test

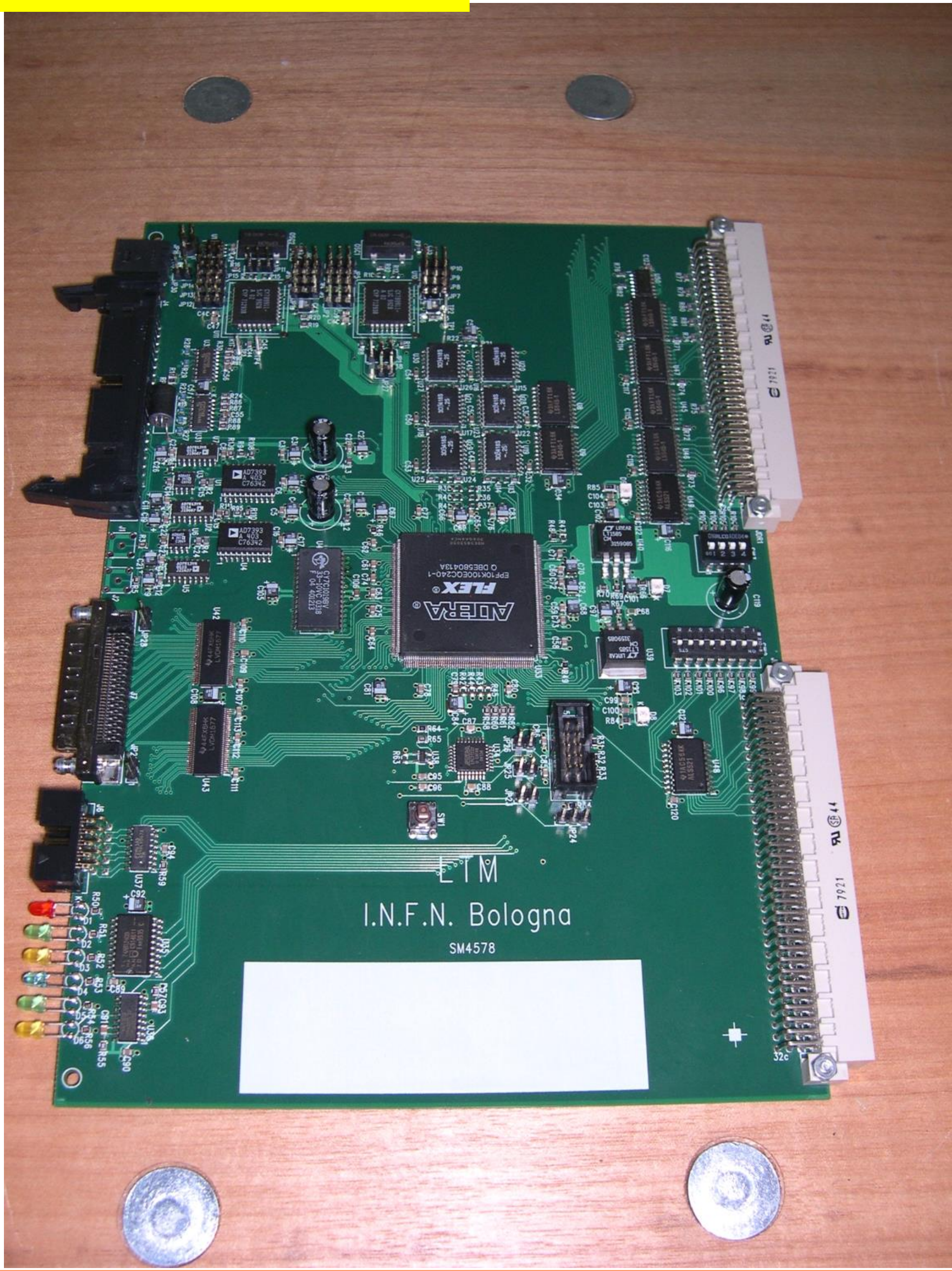
36,000 calibration constants @ work



36 pads/ASIC channels/HPTDC channels tested

LOCAL TRIGGER MODULE

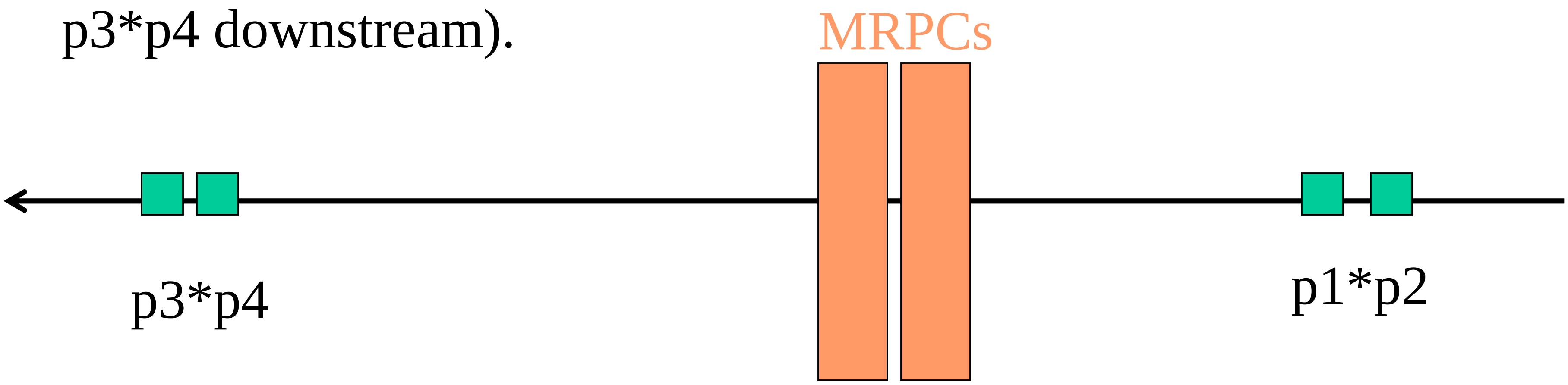
First LTM prototype,
6 channels version, tested
at T10 on July 2004.



- Preparation of the trigger signal (latch of FEA Or signals) .
- Slow controls:
- FEA Low Voltage Monitor;
- Temperature on the Module;
- Thresholds to the FEA.

LTM TRIGGER TEST

ORs signals are made ORing 24 pads = 210 cm^2 area.
At PS-T10, scintillators p1*p2*p3*p4 select a 1 cm^2 area, fully contained within the 210 cm^2 area (p1*p2 upstream , p3*p4 downstream).



We expect at any p1,p2,p3,p4 coincidence trigger, a LTM trigger too.

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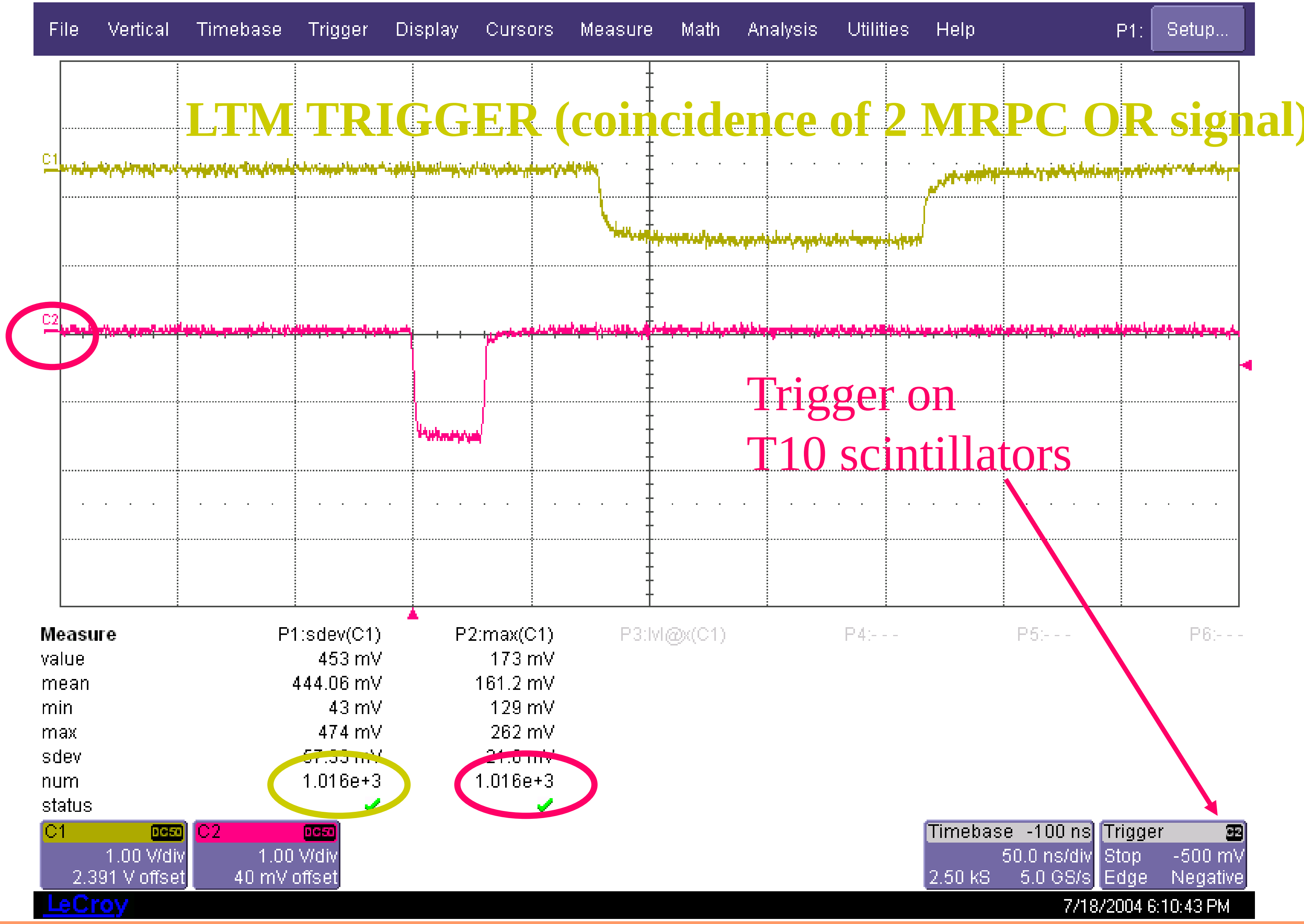
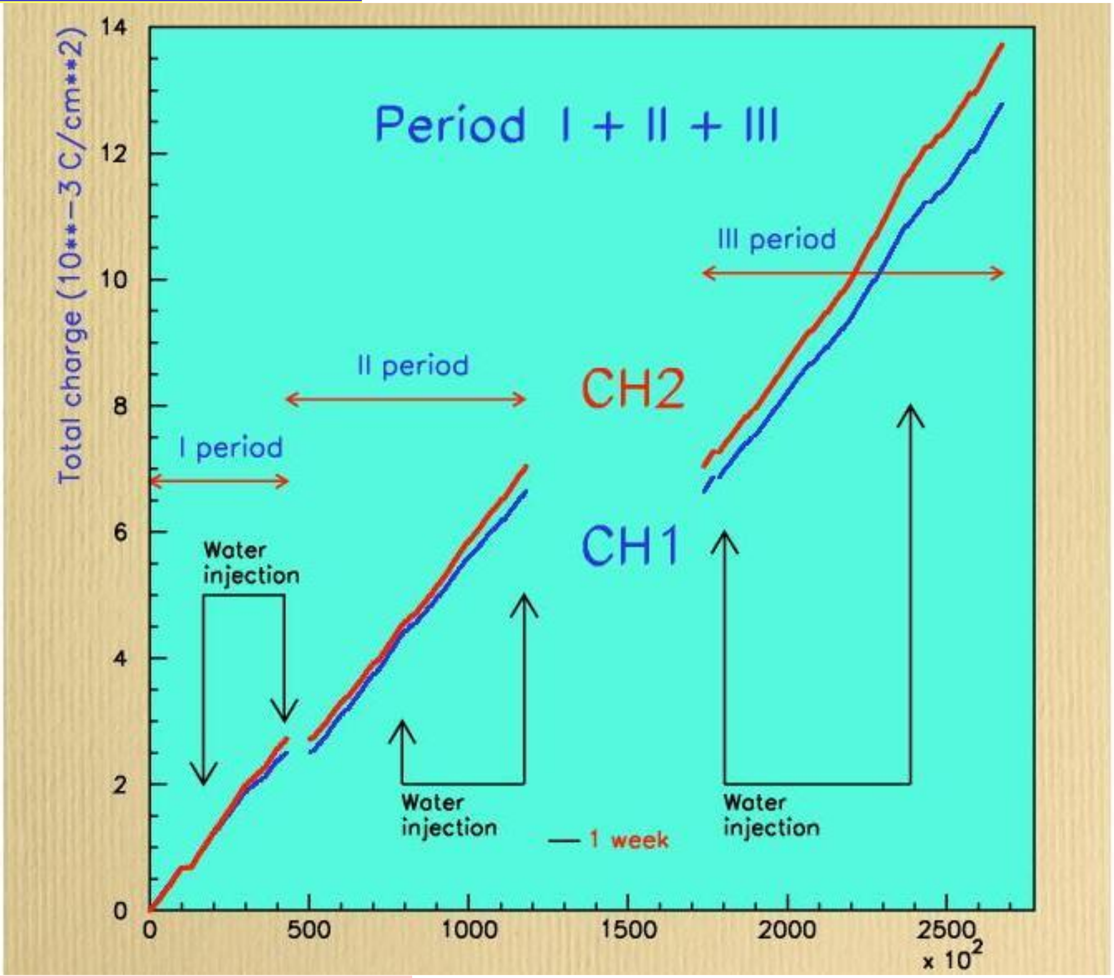
July 04 test beam: 100 % LTM trigger efficiency compared to T10 scintillator coincidence



GIF results: two MRPC strips irradiated



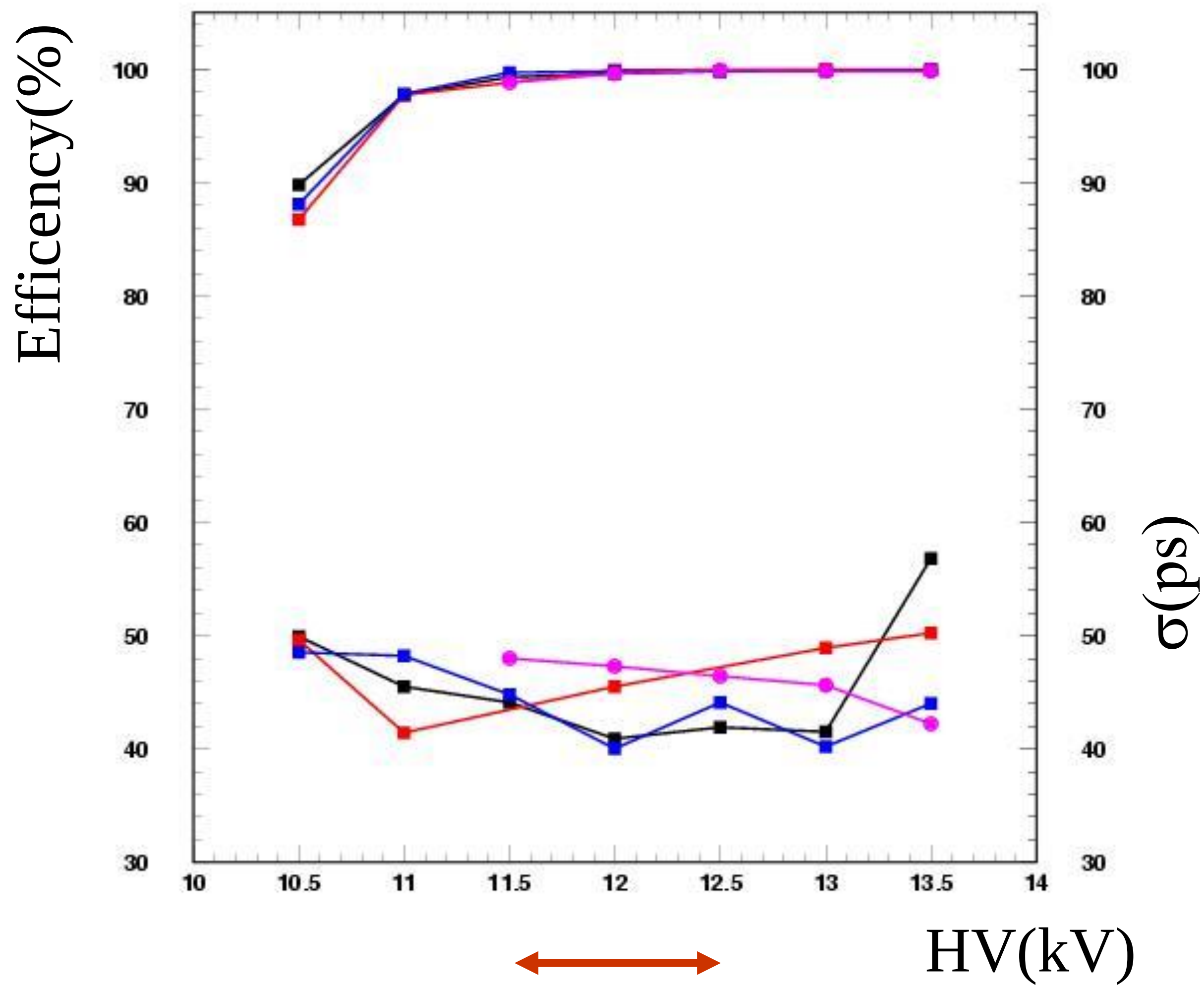
Time(min)

Total charge = 14 mC/cm^2

Charge/event = 2 pC

7 *10^9 events /cm^2 @ 50 Hz/cm^2
T=1.4 10^8 sec = 1620 days

Strips previously exposed at GIF were analyzed at PS-T10 in October.



Time resolution 40-50 ps, Efficiency >99.5 %

Chemical analysis (Chromatography) of the outgoing gas from both MRPCs (CH1, CH2) by CERN EST/SM-CP :

measured concentration of Fluorine under the limit of detection (0.02 **ppm**), I.e. no trace of HF in the samples

- Active detector volume is 2% of the total volume of the gas box;
- Diffusion for the gas exchange between strip and the surrounding gas.

- No sign of degradation;
- No increase of dark current;
- No degradation in efficiency;
- No degradation in time resolution;

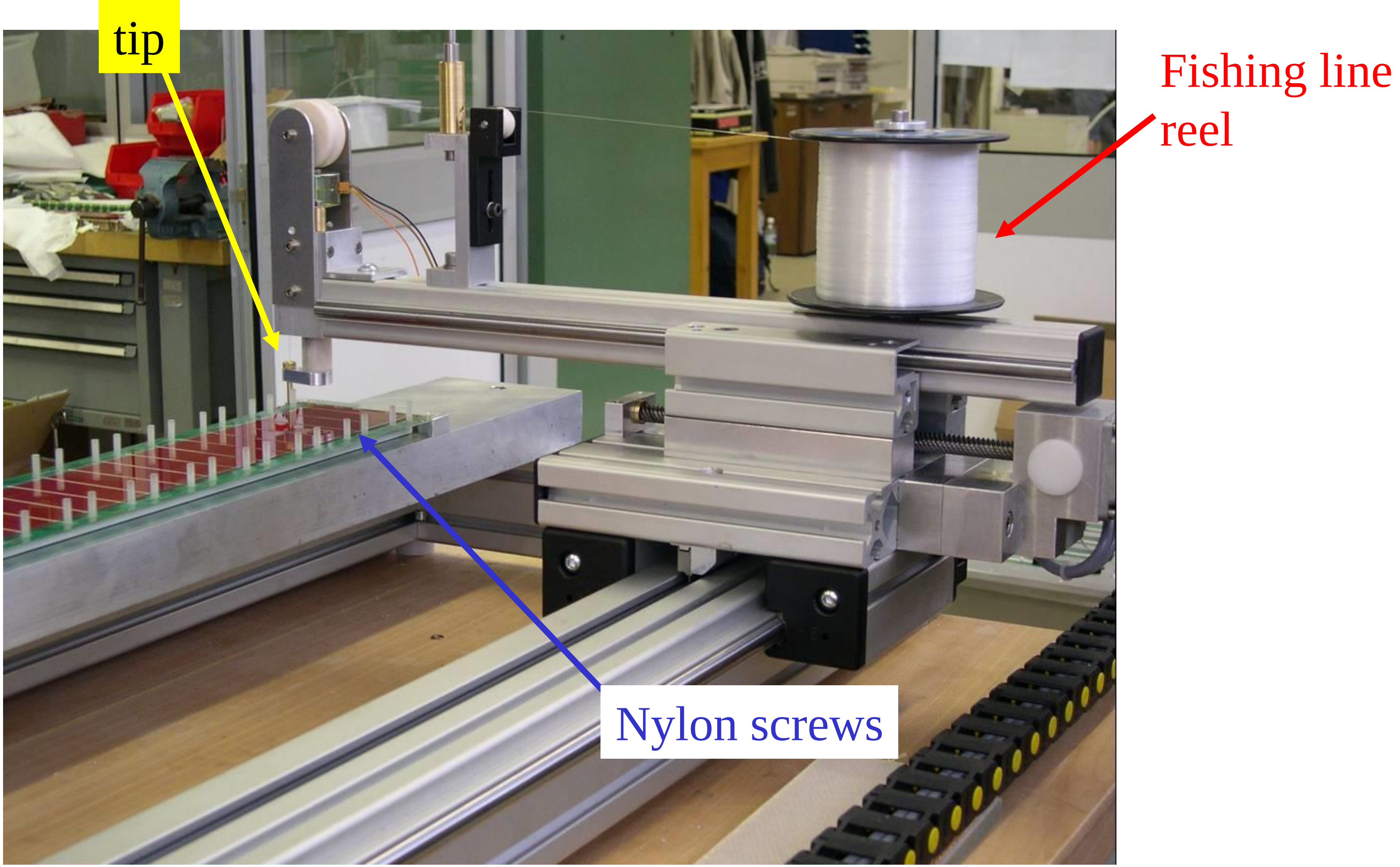
Detector construction optimization

- Massive production: **~ 2000 strips**.

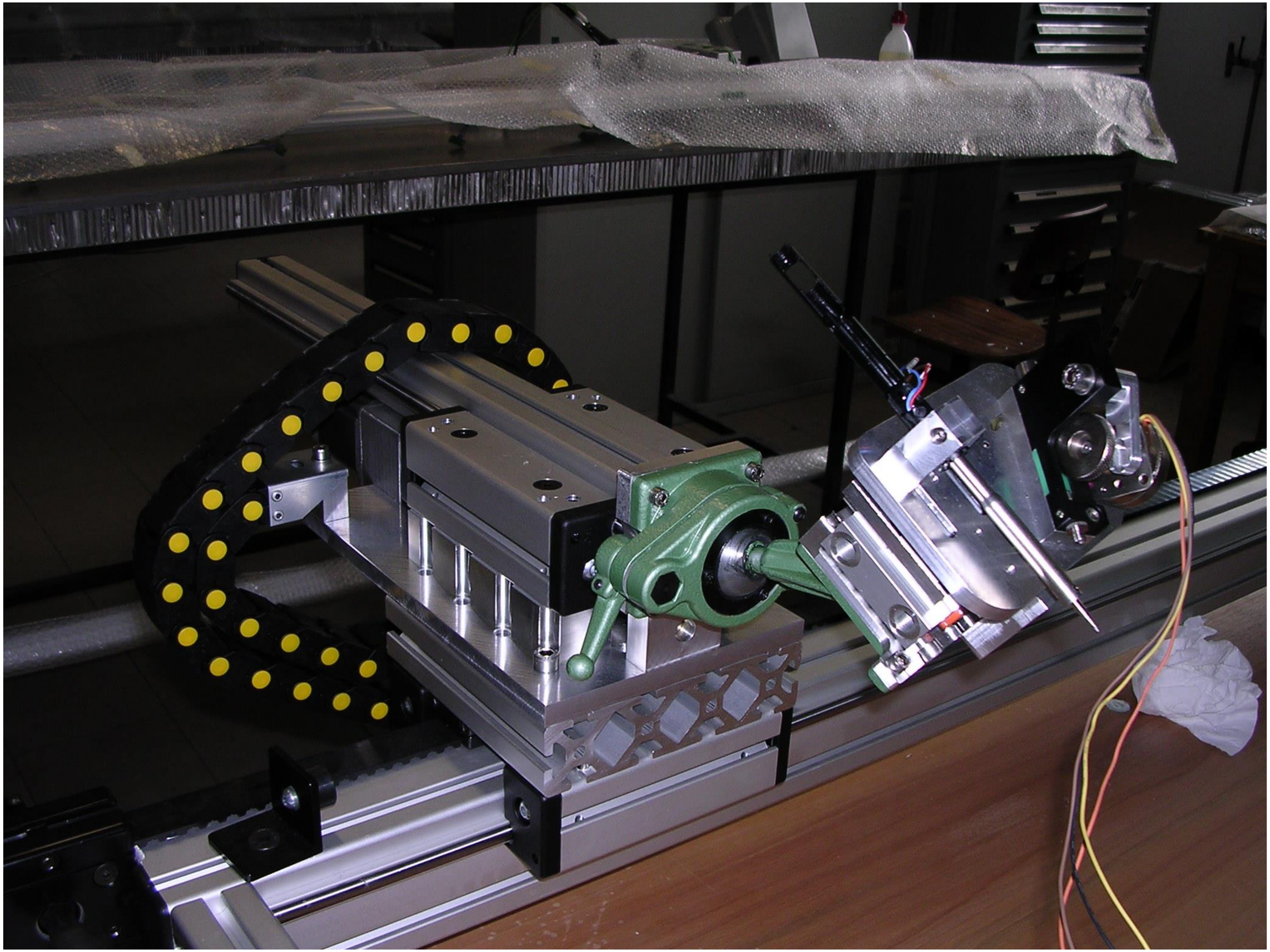
Development of methods to automate as much as possible the strip production (construction speed, human error reduction, quality controls);

Quality tests:
- Glass resistivity checks;
- Gaps uniformity with microscope + CCD;
- HV test in air;
- Pulser test;
- HV test in gas;
- Cosmic ray tests;

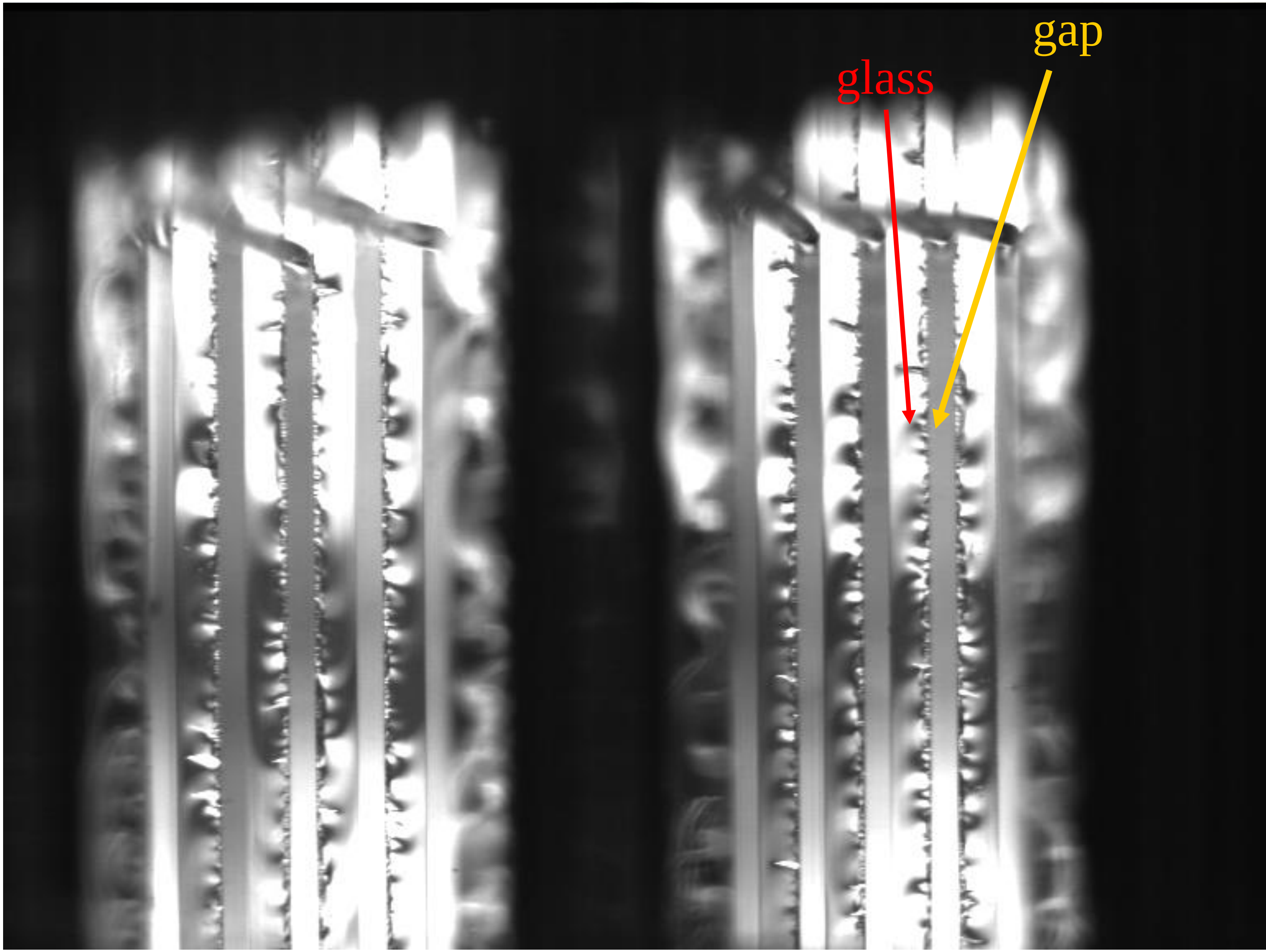
About 30 m fishing line/strip.
Wiring machine, PC controlled.



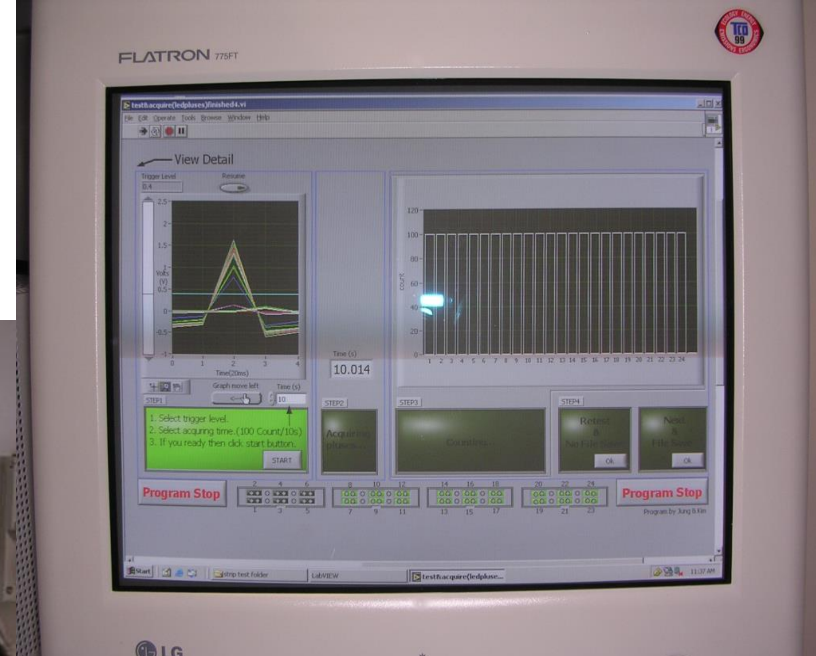
About 1600 soldering/strip



c) Microscope + CCD to check gap width uniformity



PULSER TEST


FLATRON 775FT
View Detail
10.014
1. Select trigger level.
2. Select acquiring time.(100 Count/10s)
3. If you ready then click start button.
START
Program Stop
Program Stop
LG

CONCLUSIONS

- After many years of R&D, the MRPC reached a time resolution better than 50 ps, efficiency > 99.9%;

- Asic Front End Card improved the time resolution and decreased the power consumption;

- Read out electronics in well advanced state;

- No sign of degradation after irradiation;

- Module "0" successfully constructed and tested;

- MRPC massive production just started.