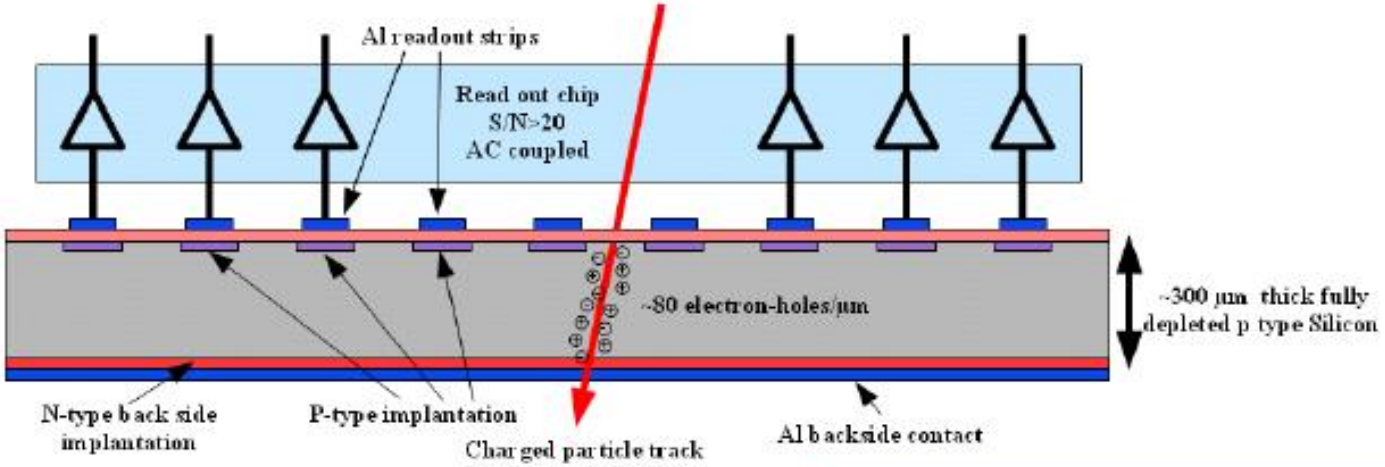
Prospect for Si sensors in Korea

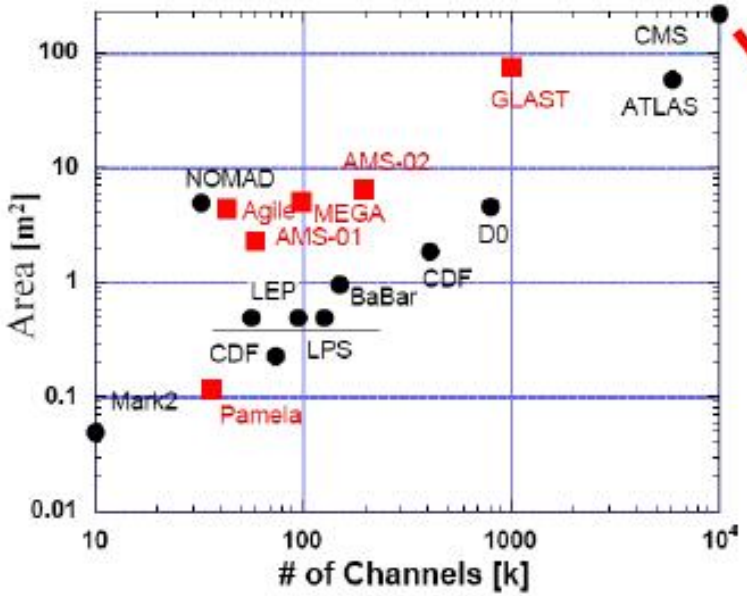
Y. Kwon
(Yonsei Univ.)

Si sensor in general

- Mature technology
- Reliable performance
- Fine granule
- Higher energy and time resolution (than gaseous ionization detectors)
- Key burden is cost.

Microstrip silicon sensors in particle physics: a success story!





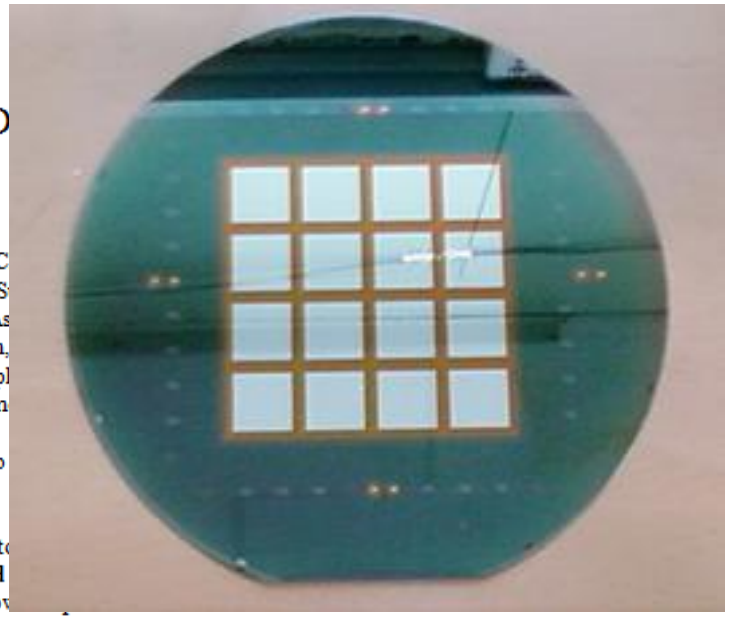
CMS Silicon Inner Tracker:
223 square meters of silicon!!!

Korean Strength

- Productivity!
  - **Large amount of Si sensors** produced with the **standard CMOS process**

R&D environment

6 inch fabrication line



300 cm^2 ~ $ 500

8 inch fabrication line

MEMORAND

(1) Youngil Kwon, Mann-Ho C
(2) Edward Kistenev, Andrey S
(3) John Lajoie, Physics and As
(4) Yongsun Yoon, BT division,
(5) Kwun-bum Chung, Elecropl
(6) Zheng Li, SDDPL, Instrum

(7) Jinsoo Kim, National Nano

I. Purpose & Scope

The purpose of this MOU is t
the '**Radiation damage and**
planning to contribute their ov
studies. This MOU clarifies the areas of pa rties will
collaborate by sharing their expertise and se ticipating
parties for the stated academic goal.

II. Responsibilities Under this MOU

A. Dr. E. Kistenev, and Prof. J. Lajoie, and Prof. Y. Kwon will propose silicon semiconductor detectors/devices to achieve academic goals in their field of interest in the experimental nuclear and high energy physics.

B. Dr. Z. Li will design the proposed silicon semiconductor detectors/devices using standards approved by industry for large area radiation hard Si devices and will advice on the radiation induced defects in Si devices.

C. Dr. A. Sukhanov will advice on the electronic design and implementation of the readout electronics for silicon semiconductor device testing.

D. Dr. Yoon will inspect designs of the proposed detectors/devices and advise on matching design ideas to fabrication technologies. He will also perform his own radiation hardness testing of the devices he develops.

E. Prof. M.-H. Cho, Prof. G. T. Park, and Prof. K. B. Chung will advise on possible defects in silicon sensors/devices and will study radiation defects in the produced sensors/devices exposed to different kinds of radiation.

F. Mr. Kim, leader of nano patterning process team in National Nanofab Center, will assist in fabrication of the silicon sensors/devices with university discount program and consult on details of silicon detector/device fabrication process.

SK hynix

SK하이닉스 M8라인, 시스템반도체 전환 완료

애플을 최대 고객사로 확보

서울시민신문

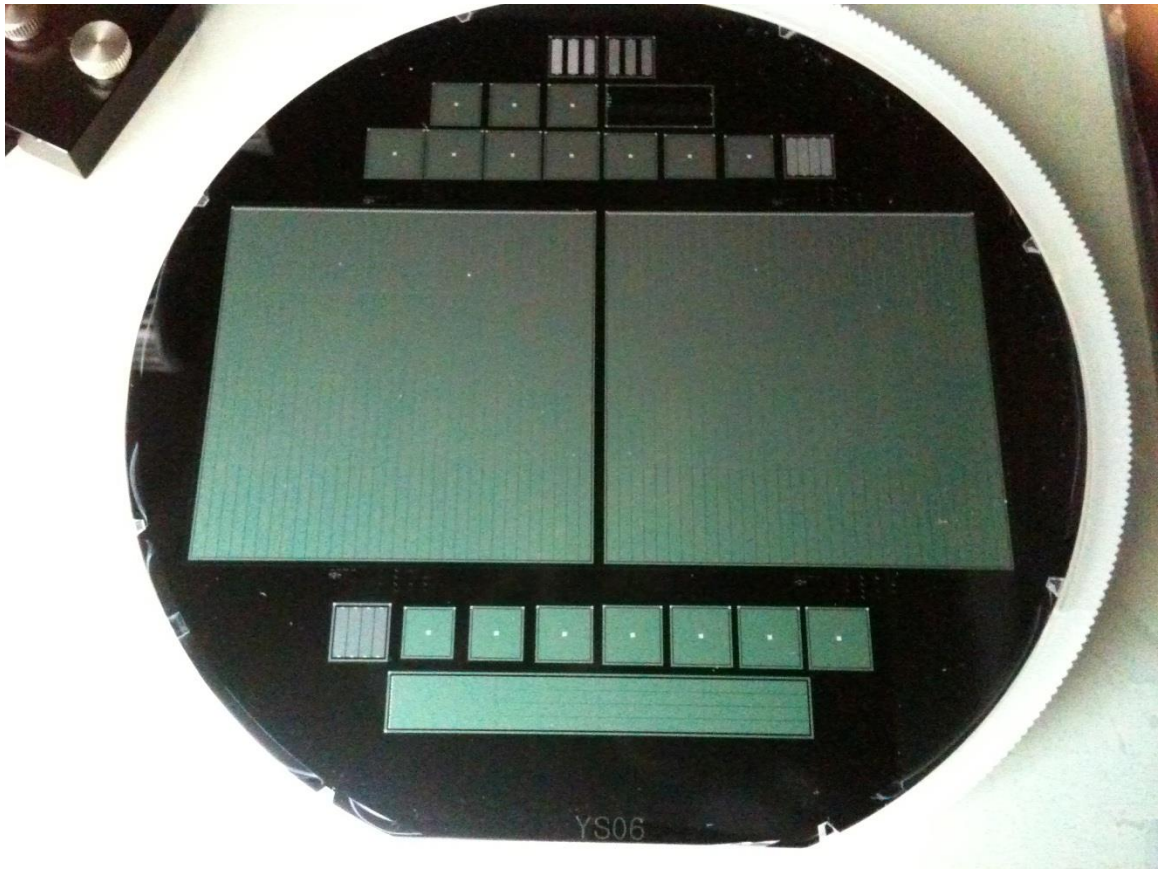
▲ SK하이닉스 M8라인. © 서울시민신문

SK하이닉스가 청주 M8 라인을 거점으로 시스템반도체 생산을 본격화했다.

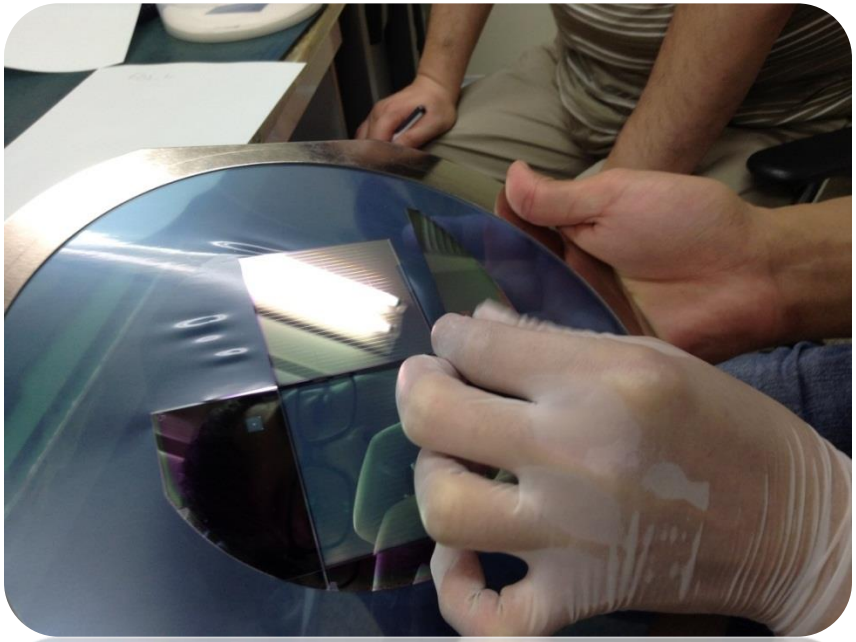
10월 25일 유경동 SK하이닉스 상무는 `국제반도체컨퍼런스 2012`에서 청주 소재의 자사 M8 공장을 메모리에서 시스템반도체로의 전환 작업을 성공적으로 끝냈다고 밝혔다.

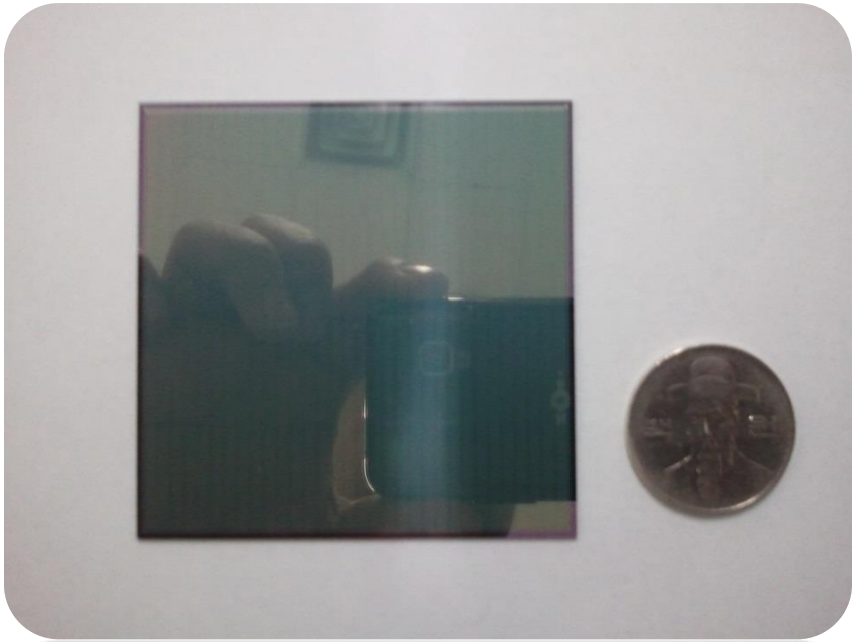
M8 공장은 CMOS 이미지 센서(CIS)와 DDI, 전력반도체(PMIC), 고주파(RF), 메모리 반도체를 생산한다. CIS의 경우 90나노미터(㎚) 공정 기반으로 터치스크린과 드라이버칩

What is Si sensor? (Sensor on Si wafer)



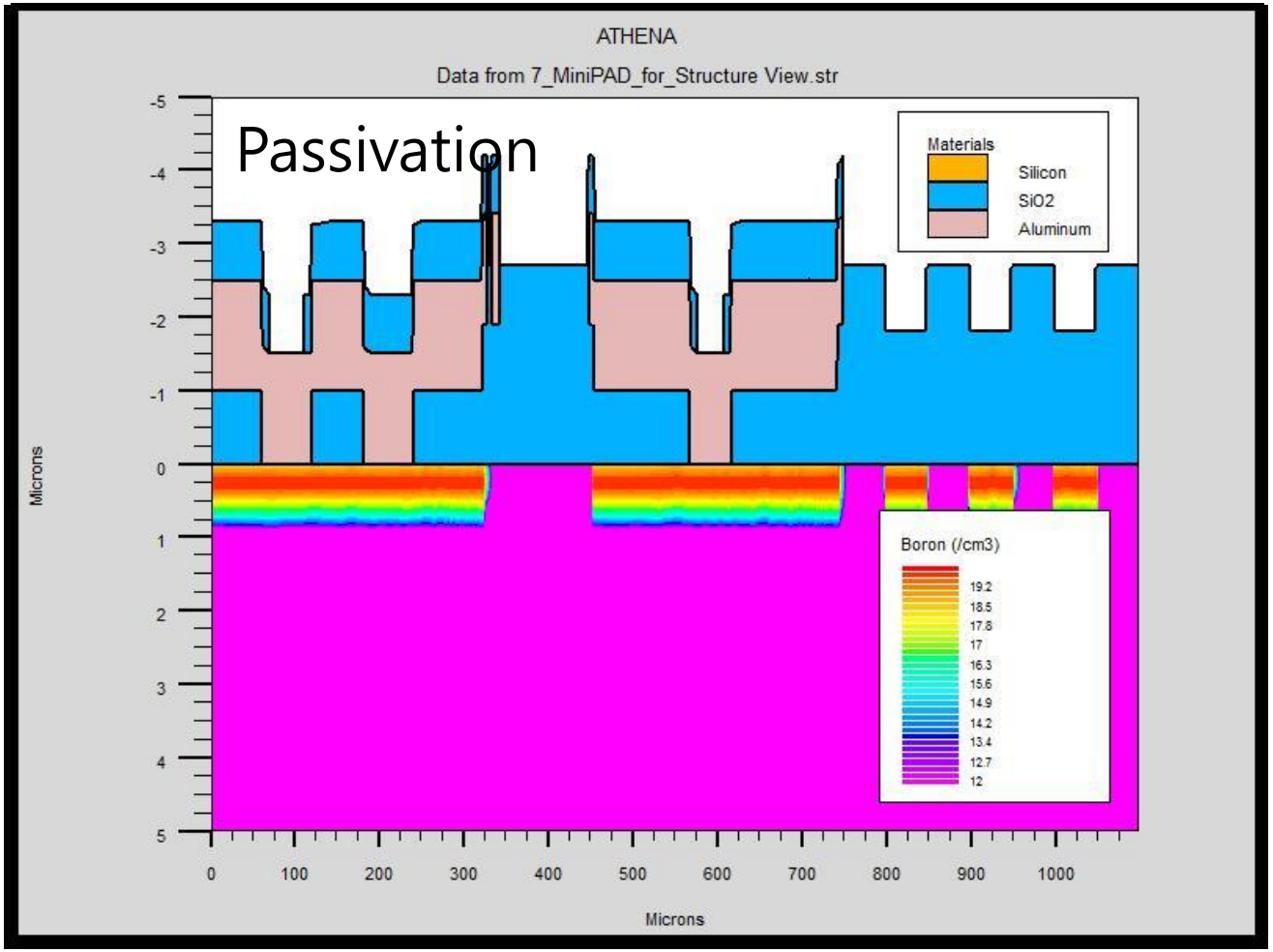
Diced sensor



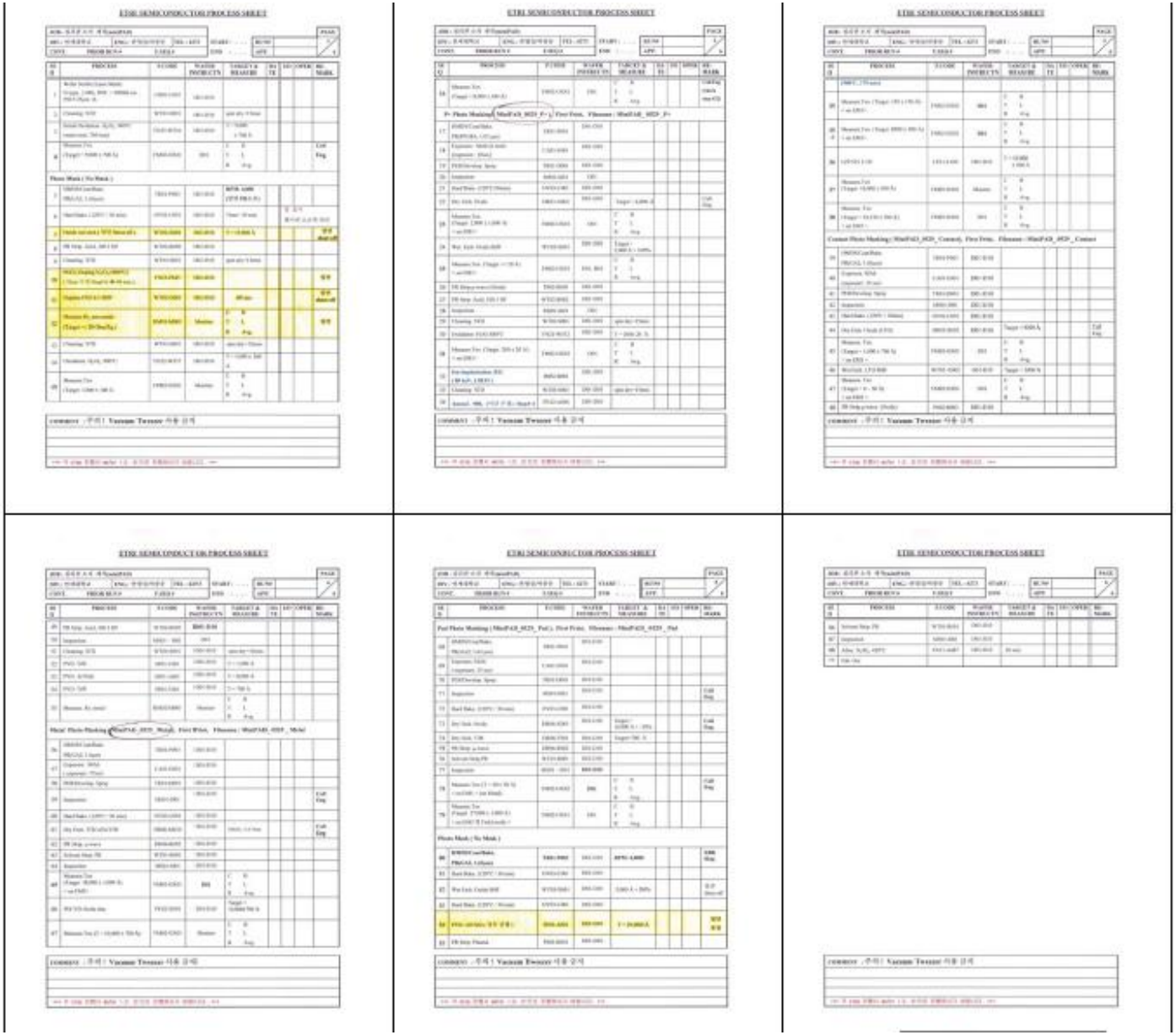


Introduction for student

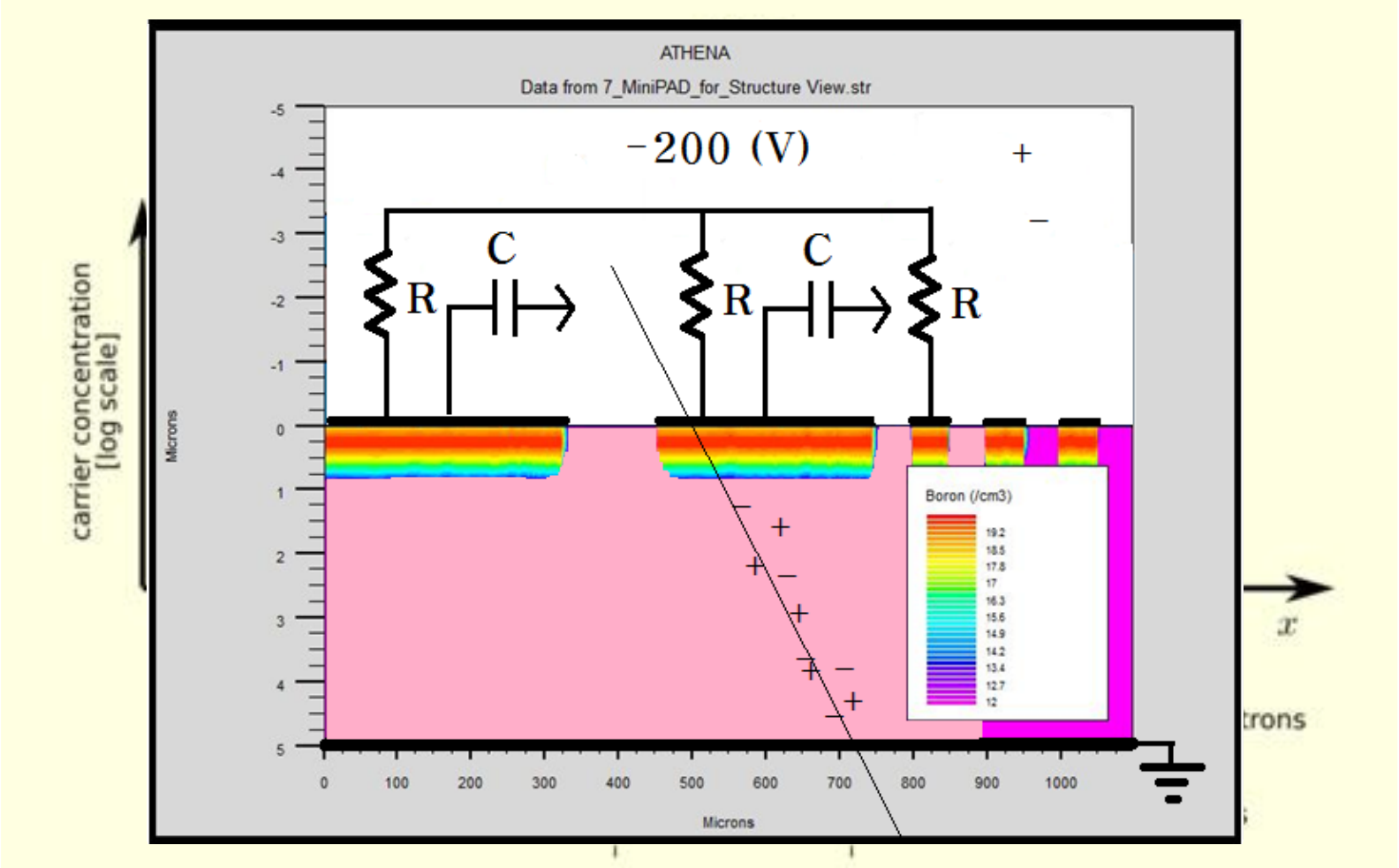
How do we make it? (CMOS process)



Actual process sheet

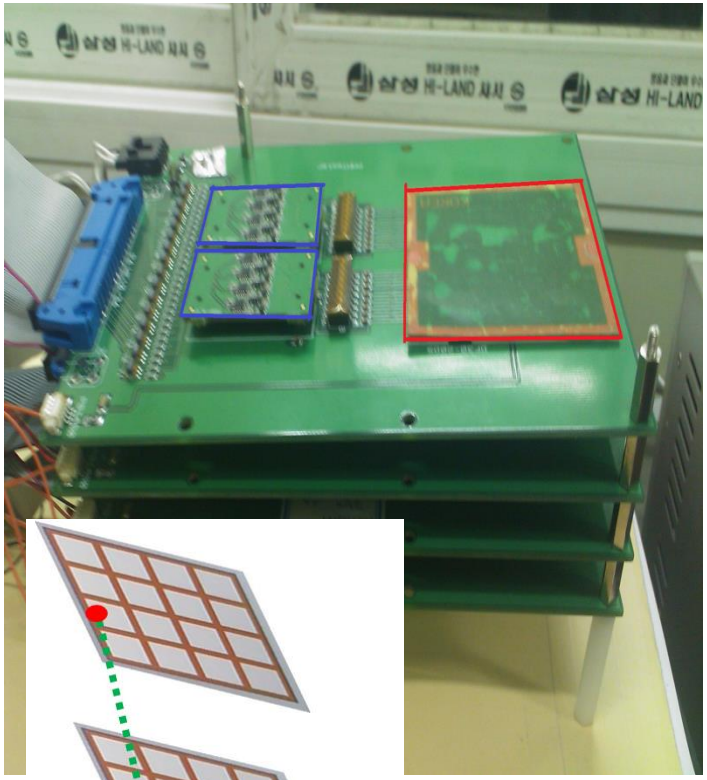


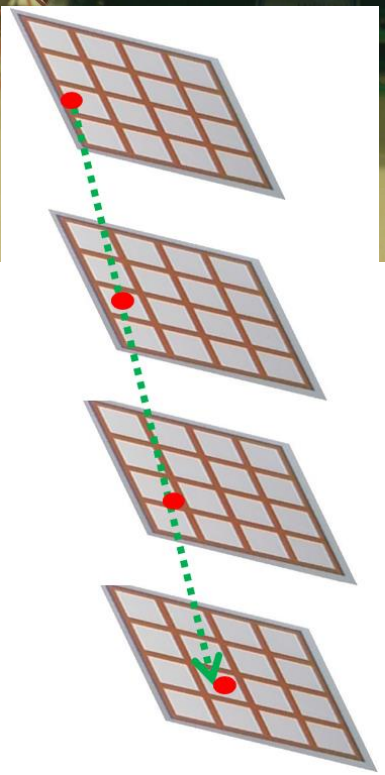
How does it operate?

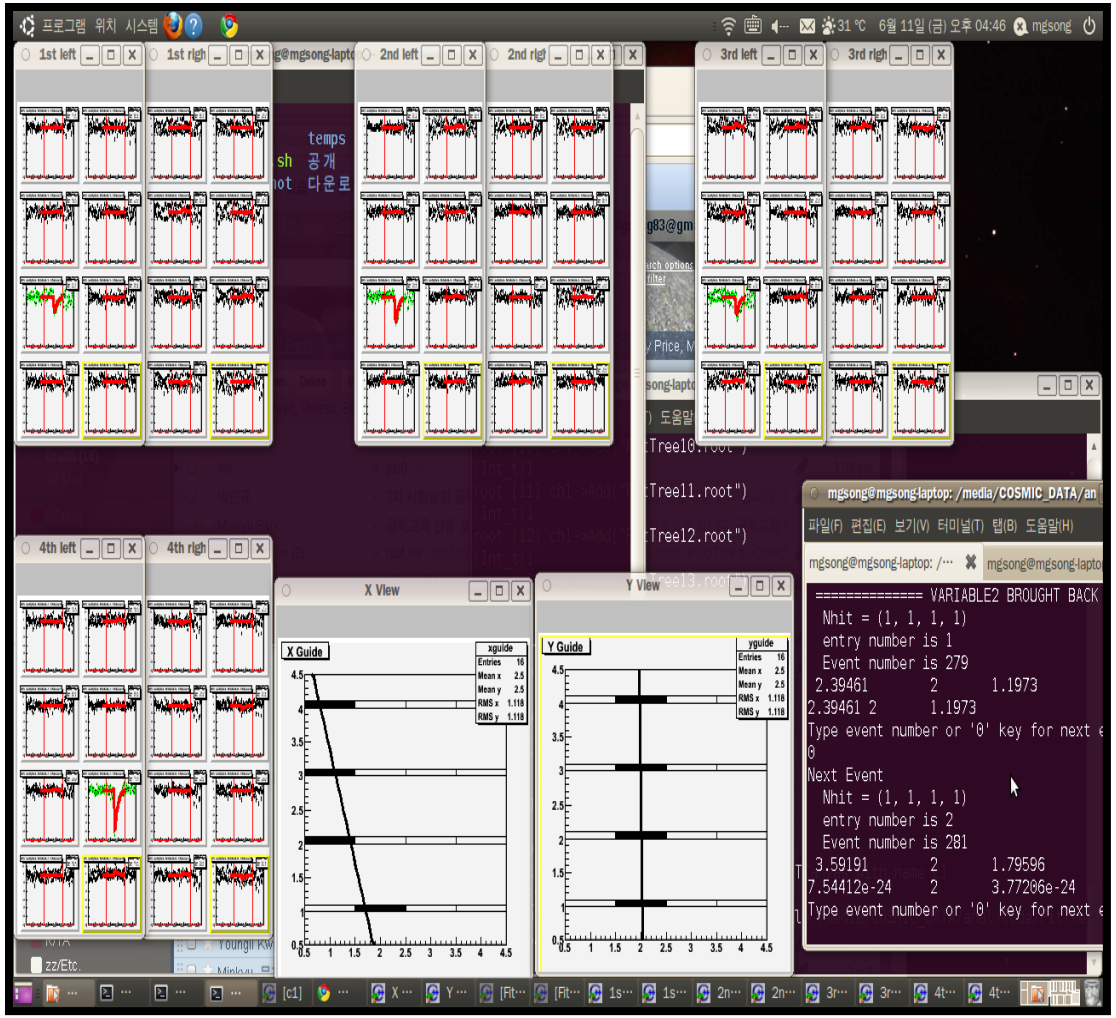


$$W = \sqrt{2\rho\mu\varepsilon\left(V + V_{bi}\right)}$$

Cosmic muon test





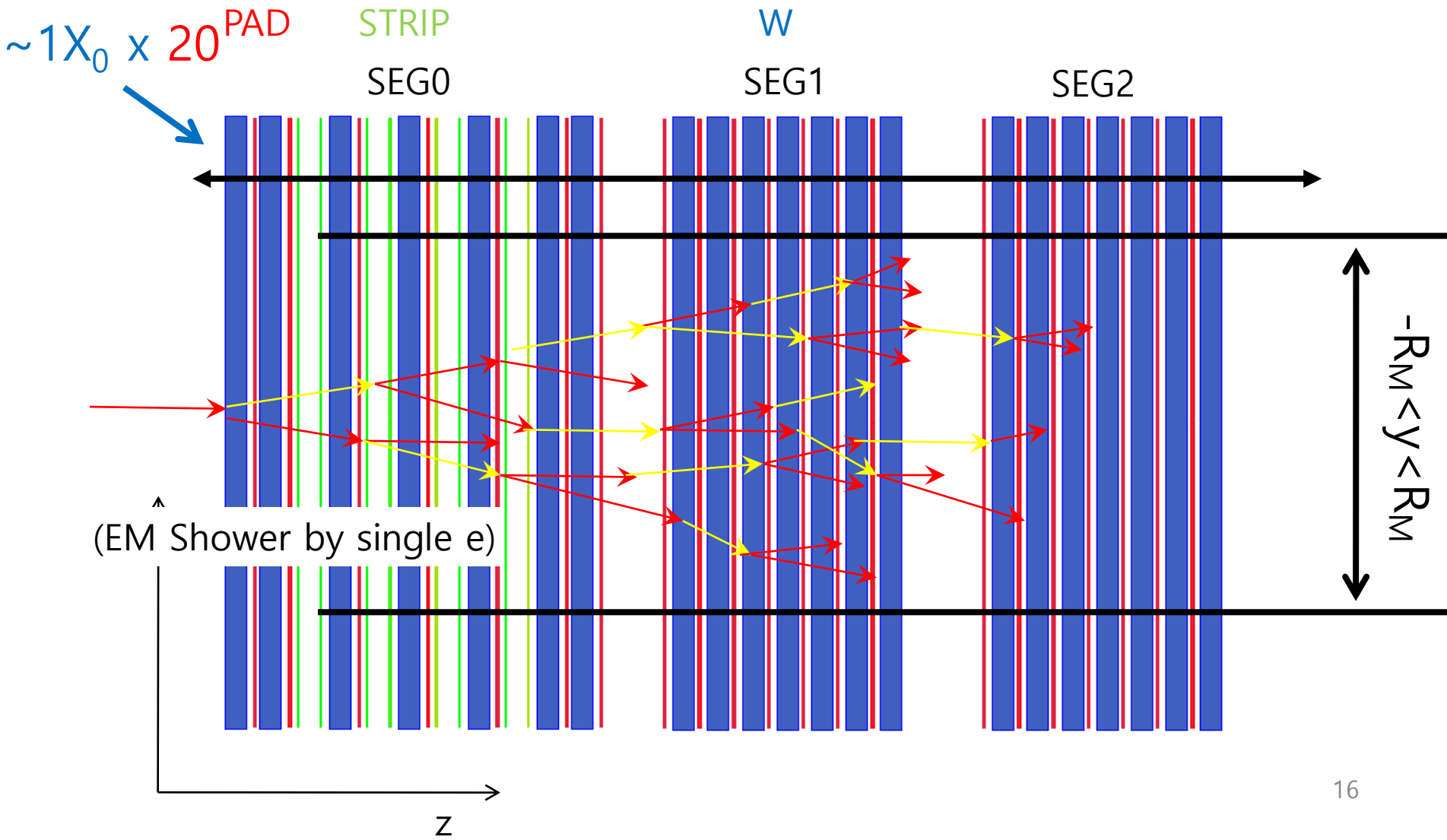


Applications

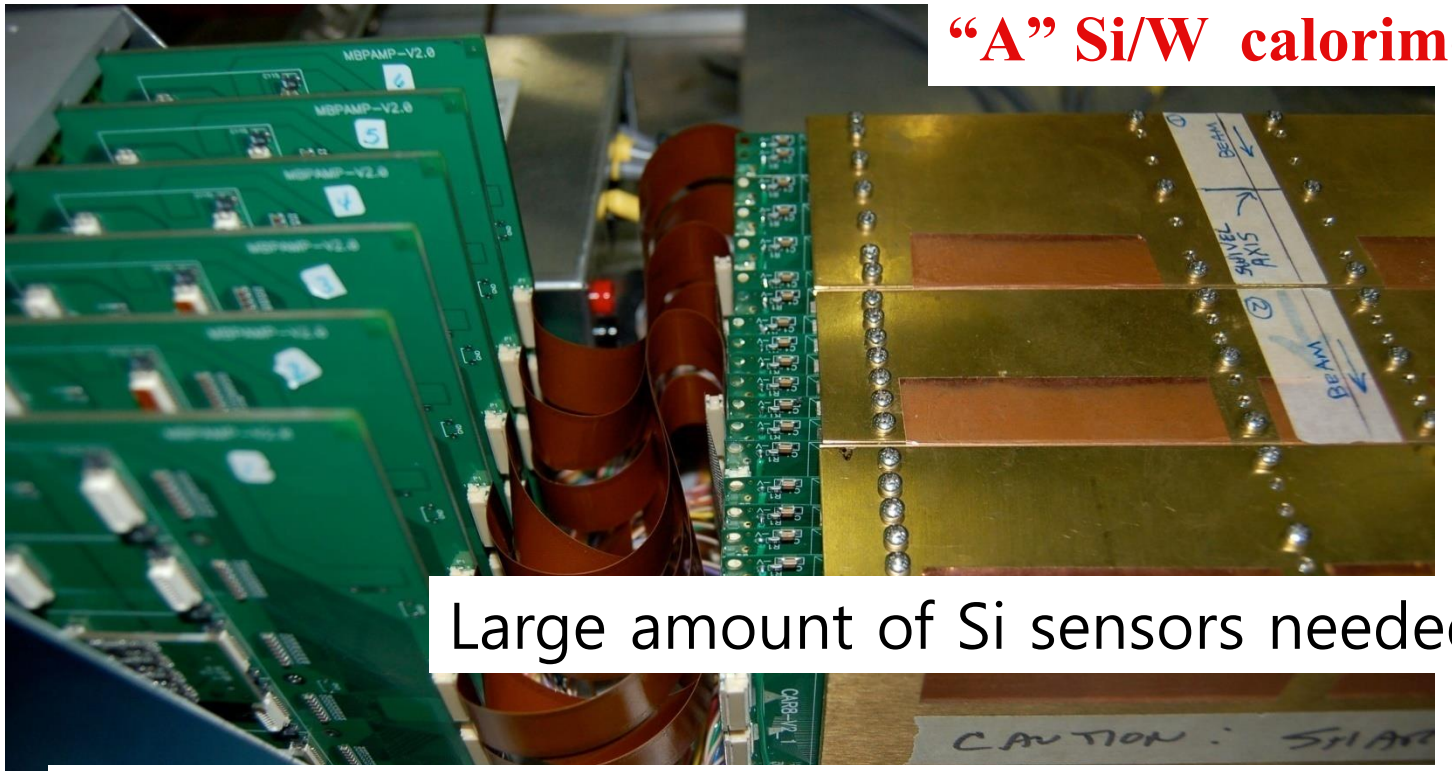
- Calorimeter :
  - Active layer (Old)
  - PHENIX MPC-EX
- Tracker :
  - ALICE ITS Upgrade

PAST

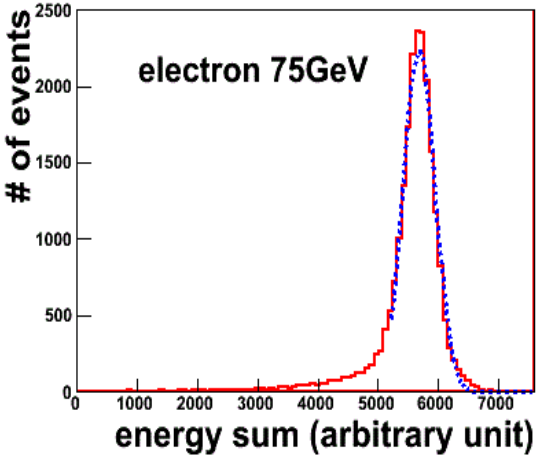
FOCAL - schematic view (y-z view)



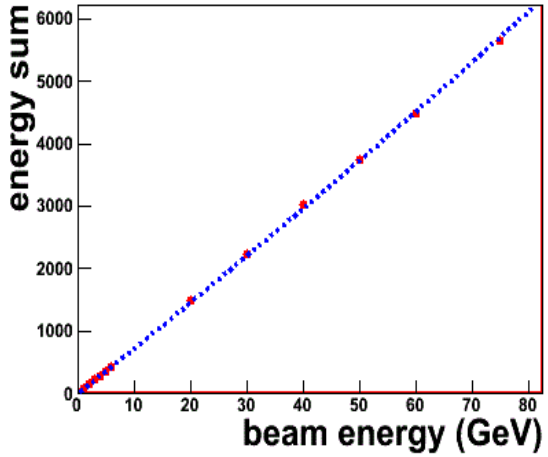
“A” Si/W calorimeter prototype



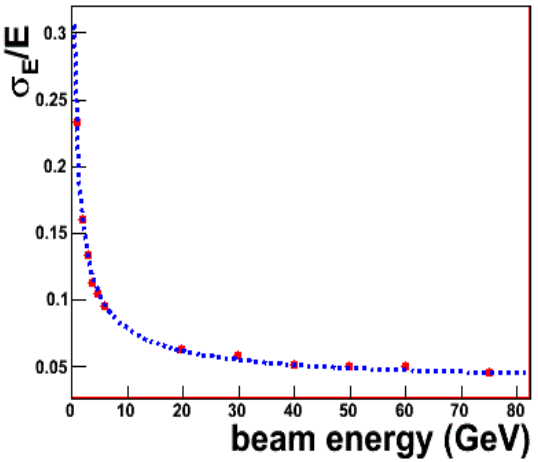
Large amount of Si sensors needed!



(a)

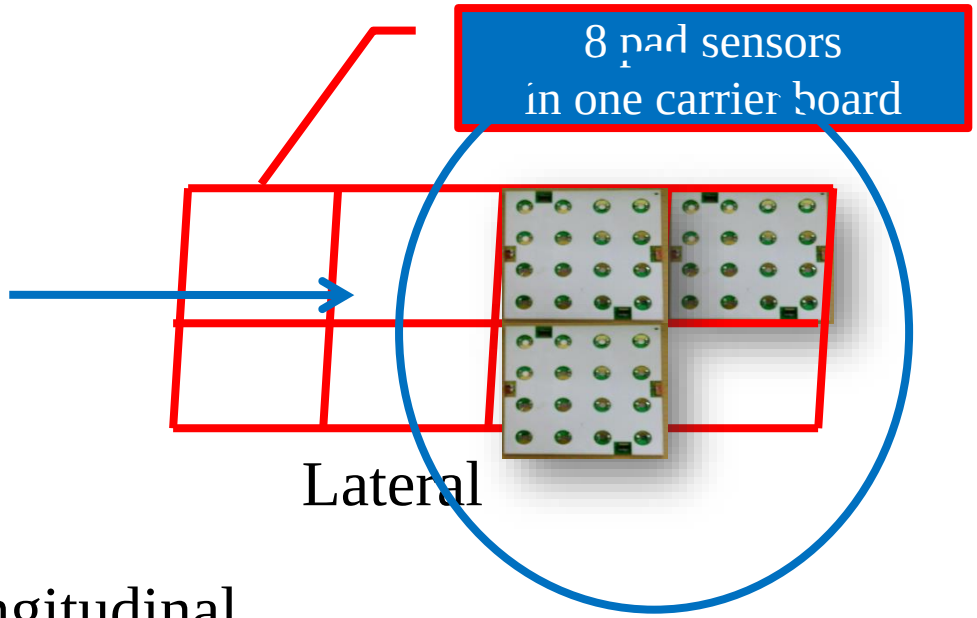


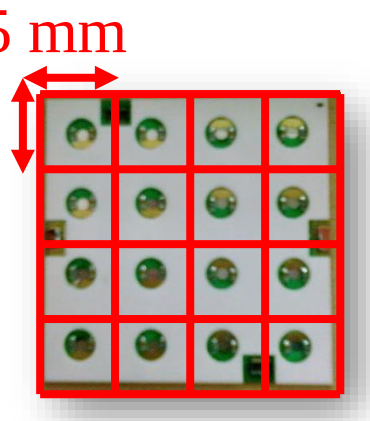
(b)



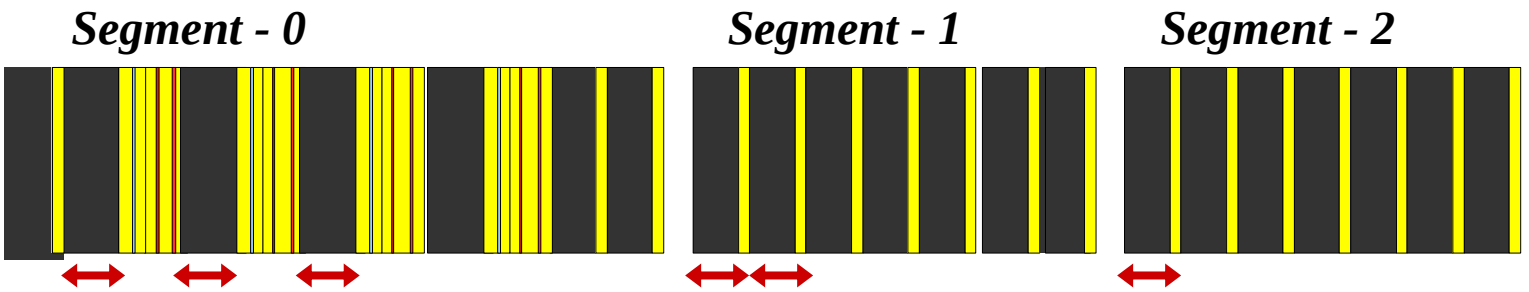
(c)

Schematics





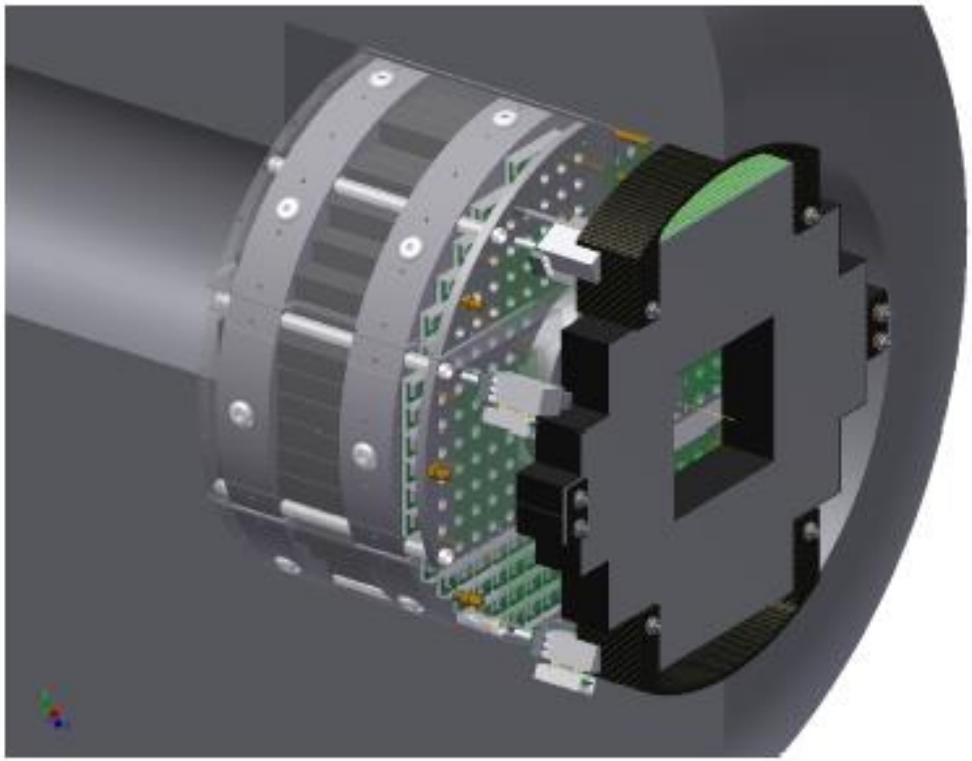
Longitudinal



PHENIX MPC-EX

MPC-EX for PHENIX

- Application as a pre-shower for EMCal (Electromagnetic calorimeter)



Korean MPC-Ex group

J.S. Chai[5], K.I. Hahn[2], S.Y. Han[2], H.S. Hong[4], K.S. Joo[4], D.S. Kim[4], E.J. Kim[1], Y.K. Kim[3], Y. Kwon[6], J.H. Lee [1], K.S. Lim[4], H.J. Moon[4], H.M. Park[4], J.M. Park [1], S.Y. Park, D.G. Sue[6]

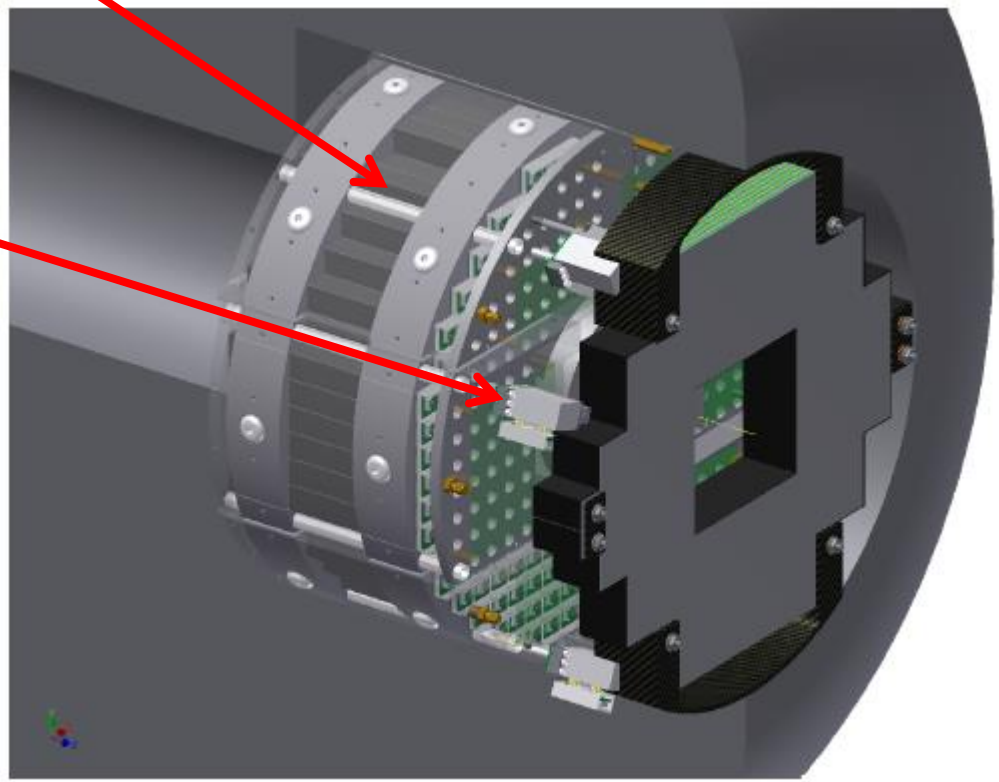
Chonbuk National University. [1] ETRI. [2]Ewha Womans University. [3]Hanyang University, RISP. [4]Myongji University. [5]Sungkyunkwan University. [6]Yonsei University.

PHENIX MPC-Ex detector

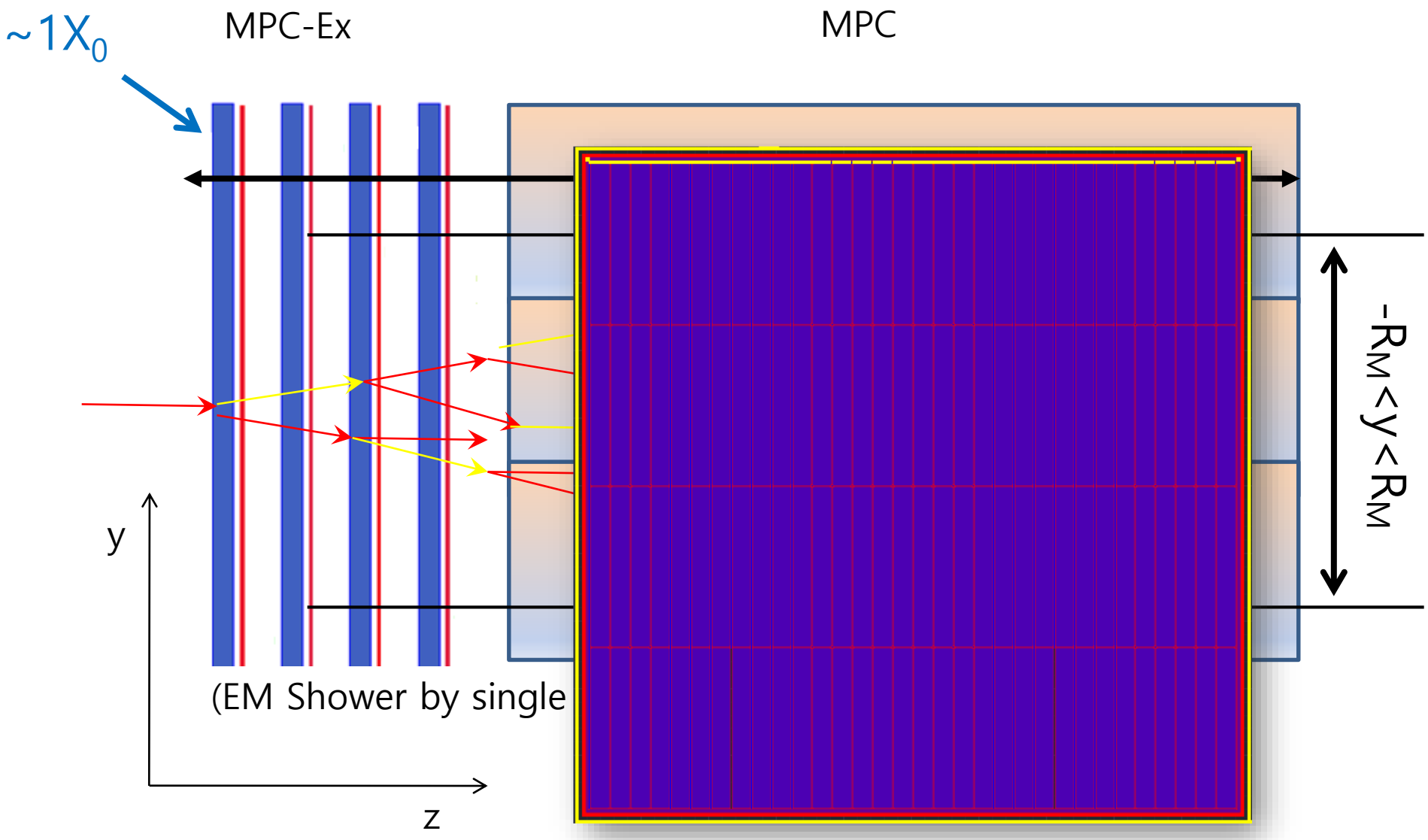
MPC
(Muon Piston Calorimeter, An EMCal)

MPC-Ex
(MPC Extension)

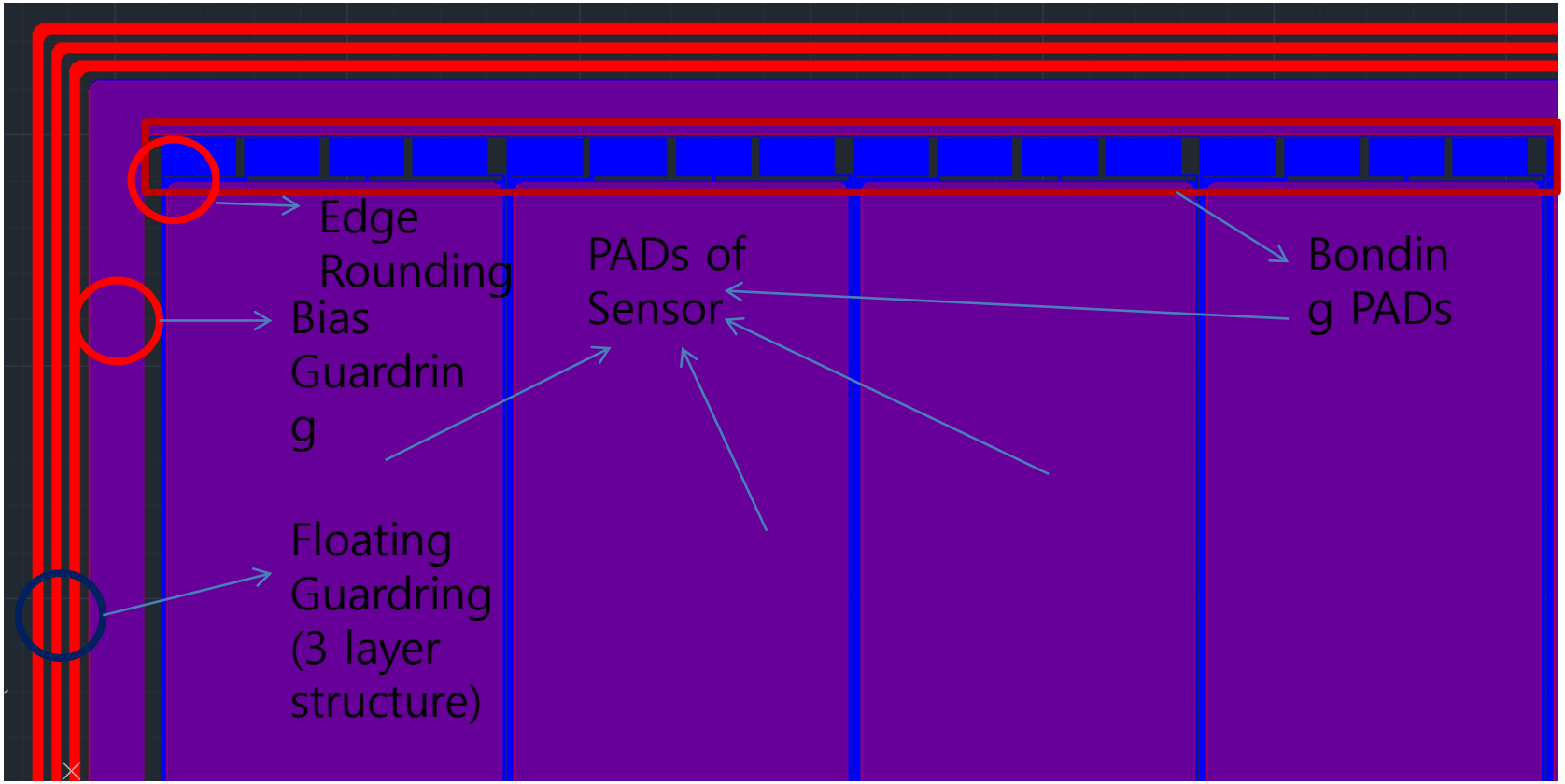
π^0 & γ
$3 < |y| < 4$
separation up to E>100 GeV



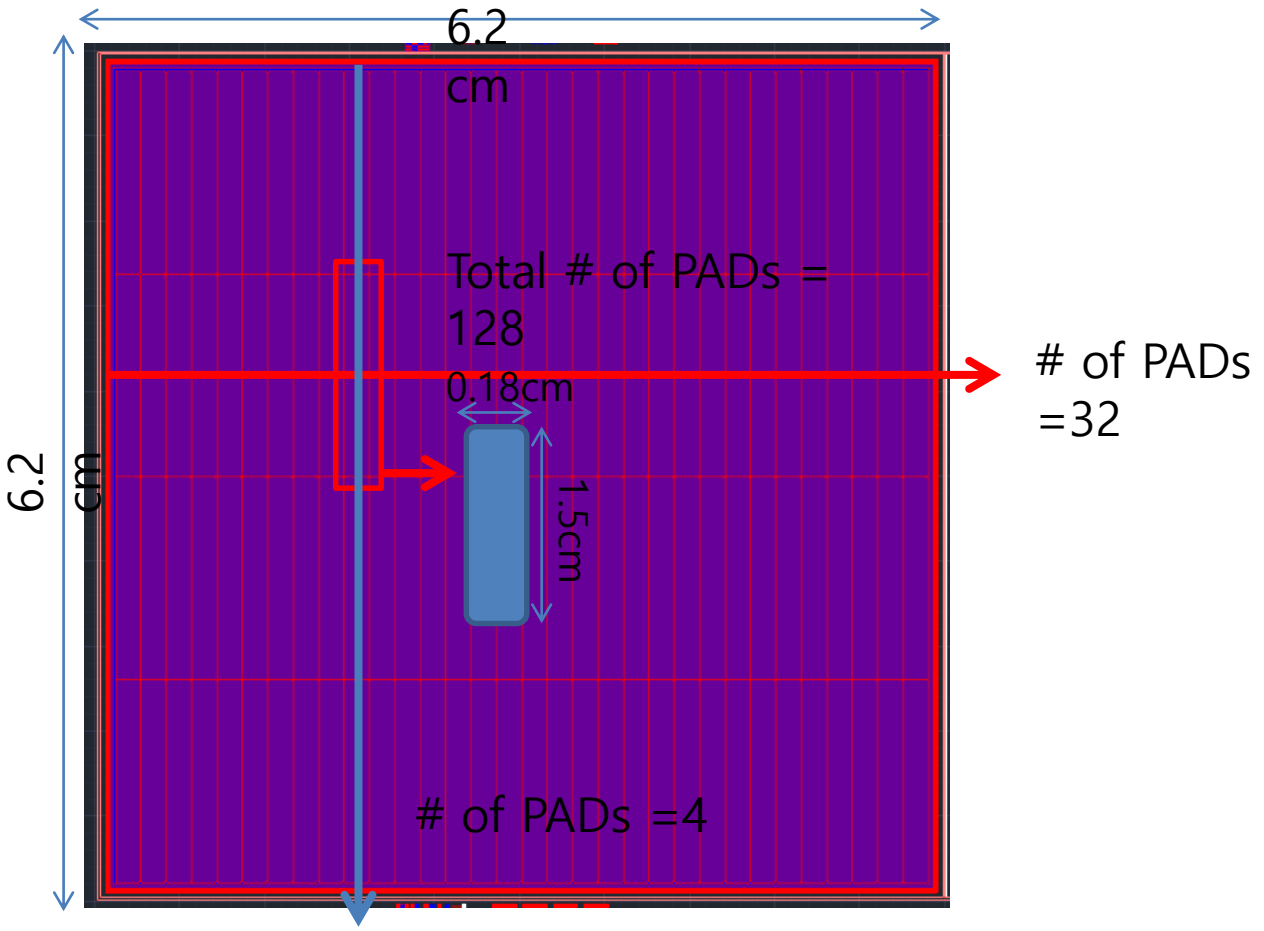
Si-W sandwich preshower detector



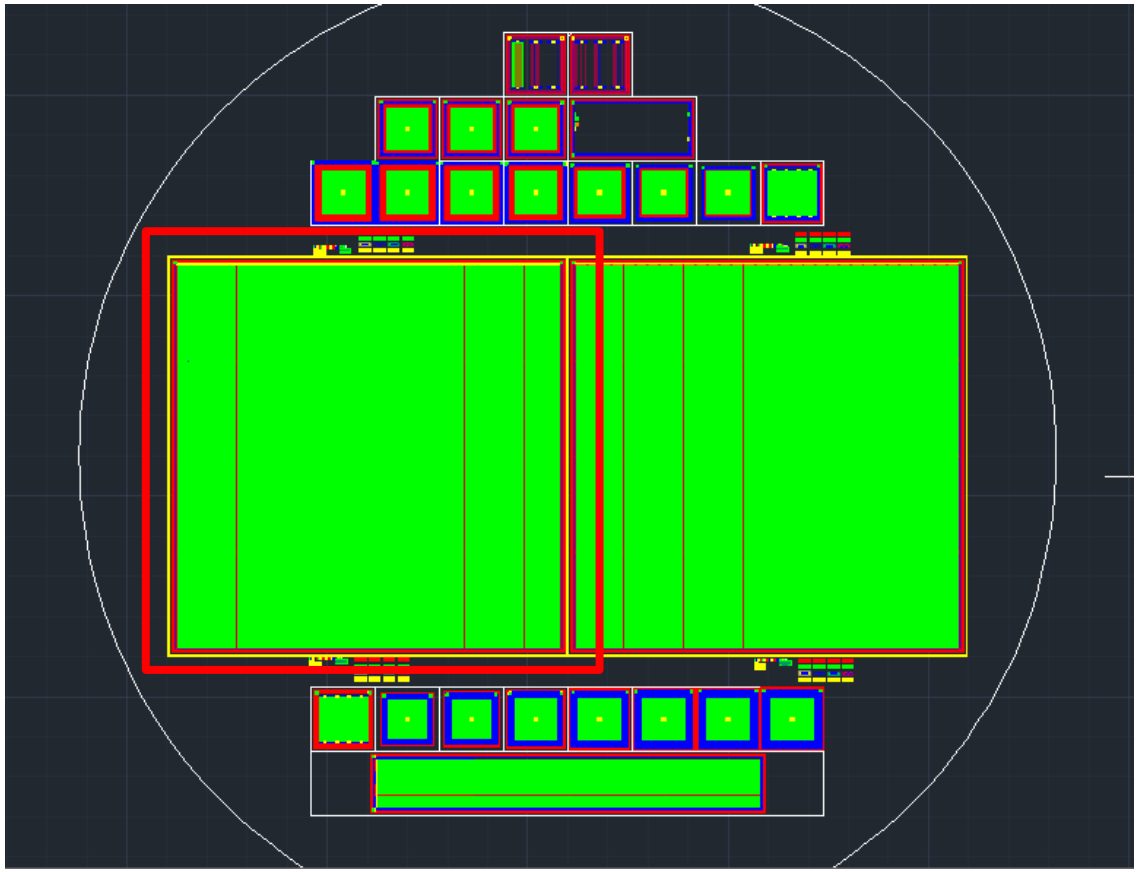
Fine structure



Segmentation as a pre-shower



Sensor Design



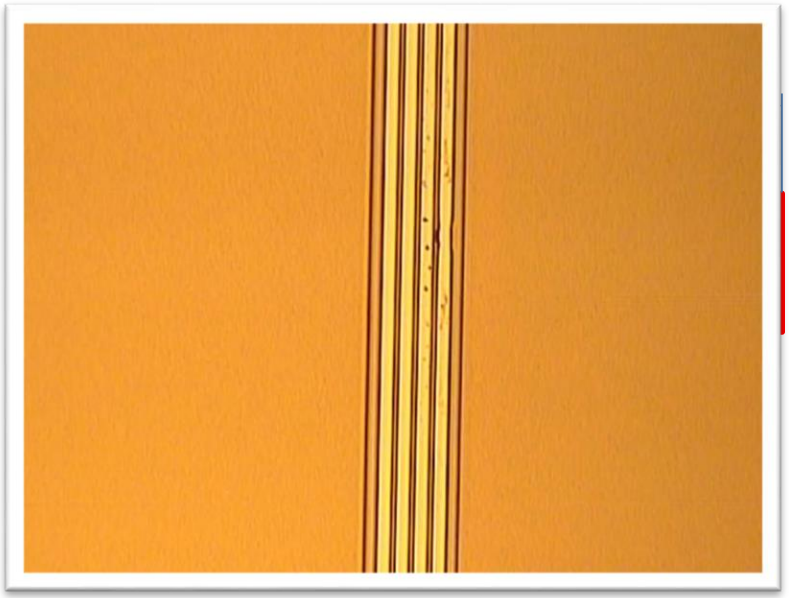
2013 IEEE NSS/MIC/RTSD, COEX, Seoul, Korea, October 27-November 2, 2013

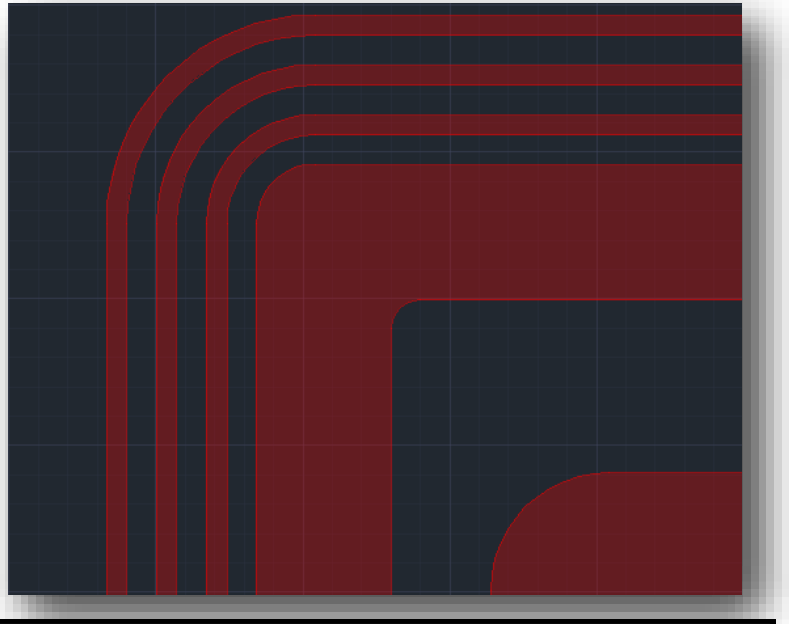
Novel guard ring system design and implementation for punch-through protection toward the detector dicing edge with improved radiation tolerance and reduced dead area

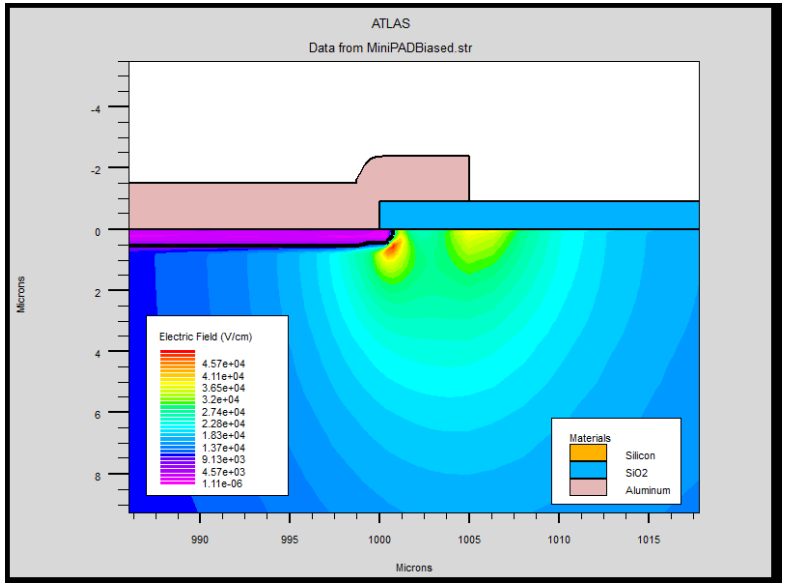
Zheng Li, Wei Chen, Edward Kistenev, and Andrei Sukhanov
Brookhaven National Laboratory, Bldg. 535B, Upton, NY 11973-5000, USA
Youngil Kwon, Dong gon Sue
Department of Physics, Yonsei Univ., 50 Yonsei-ro, Seoul, 120-749, Korea
Kunsik Park, Jongmoon Park
Electronics and Telecommunications Research Institute, 218 Gajeong-ro, Daejeon, 305-700, Korea
John Lajoie
Iowa State University, 2229 Lincoln Way Ames, IA 50011, USA

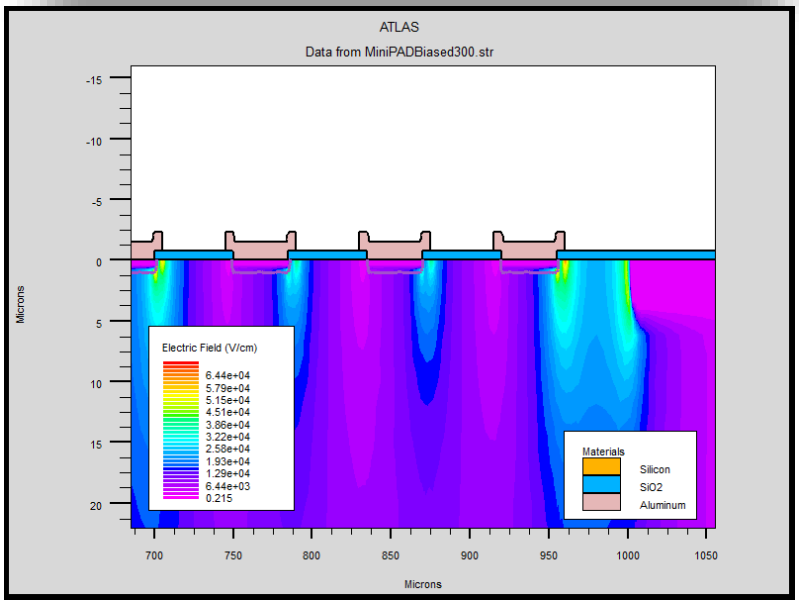
This research was supported by the U.S. Department of Energy: Contract No. DE-AC02 -98CH10886

Improvements (Details by K.S. Lim)









Submission for main production

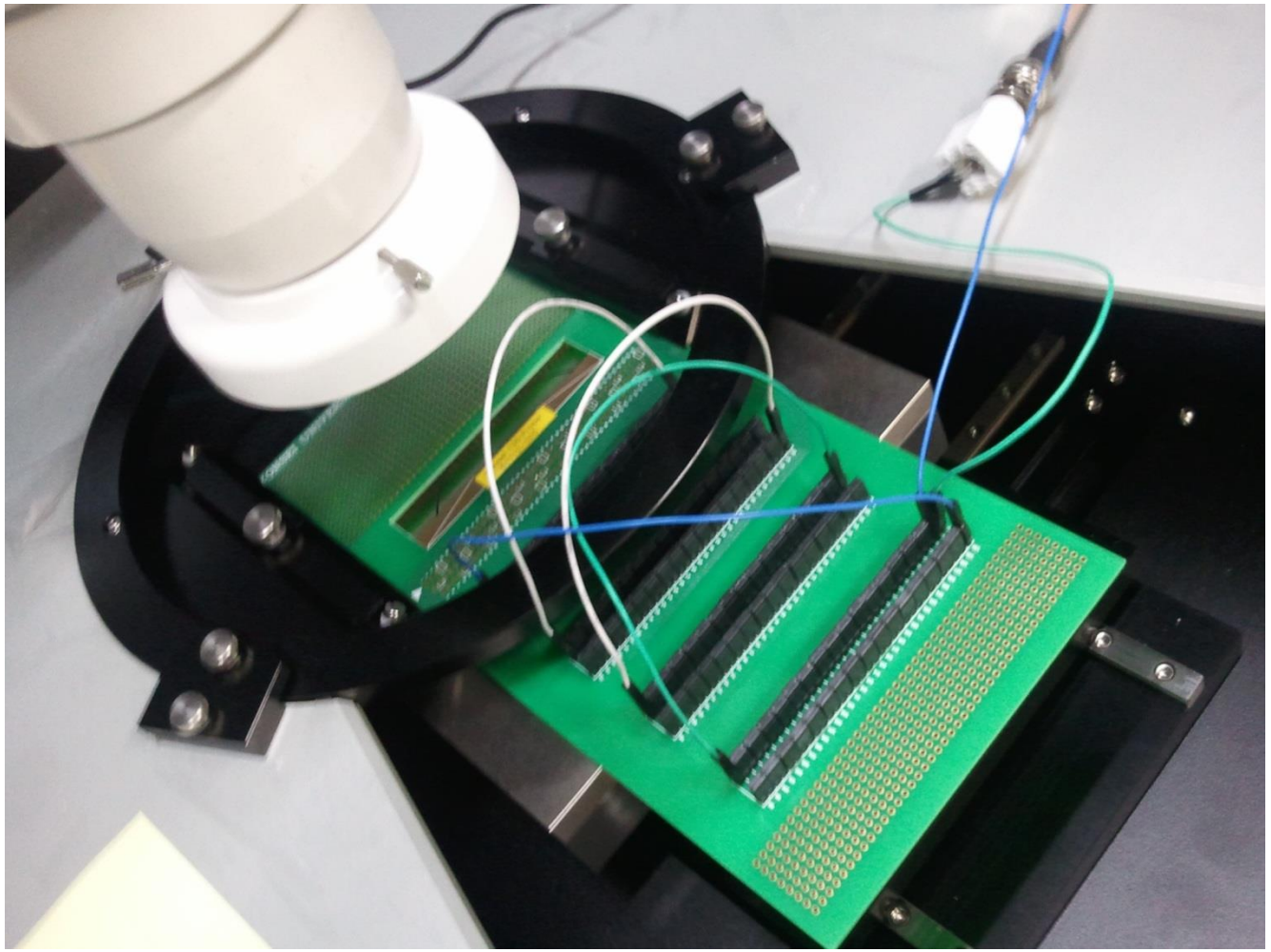
- Main production started and new submission will be made in every 3 weeks.
  - 1st submission(executed), the last week of Sep.
  - 2nd submission(executed), the 3rd week of Oct.
  - 3rd submission(planned), the 2nd week of Nov.

Sensor Certification log (Details by S. Y. Hahn)

- CV test

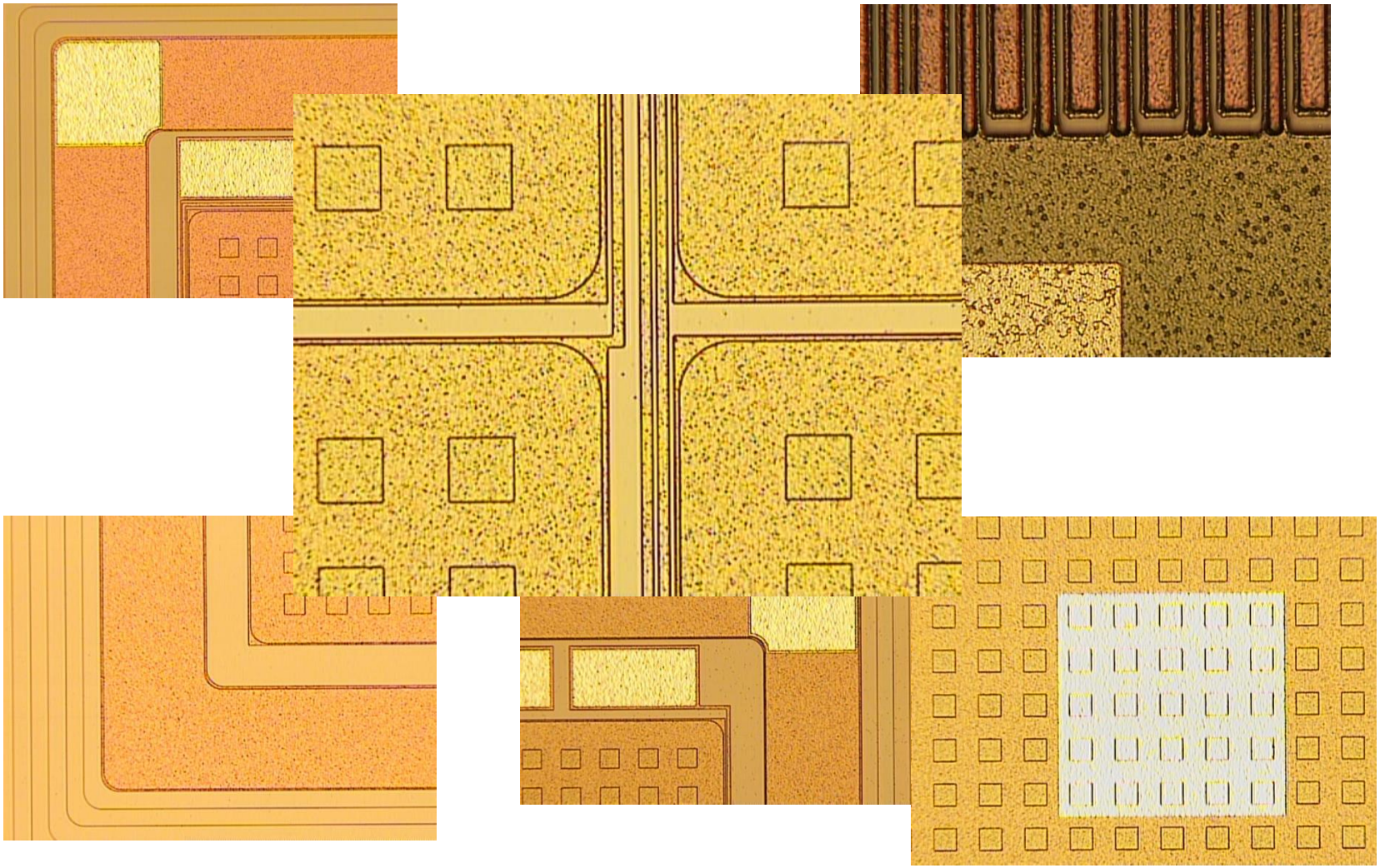
- Before dicing
  - Short test
  - Guard ring & pattern leakage current test
- After dicing
  - Guard ring & pattern leakage current test
  - Stability : x3 of full depletion voltage (90V) & 2 hours

Test system



Test electronics

Process monitoring

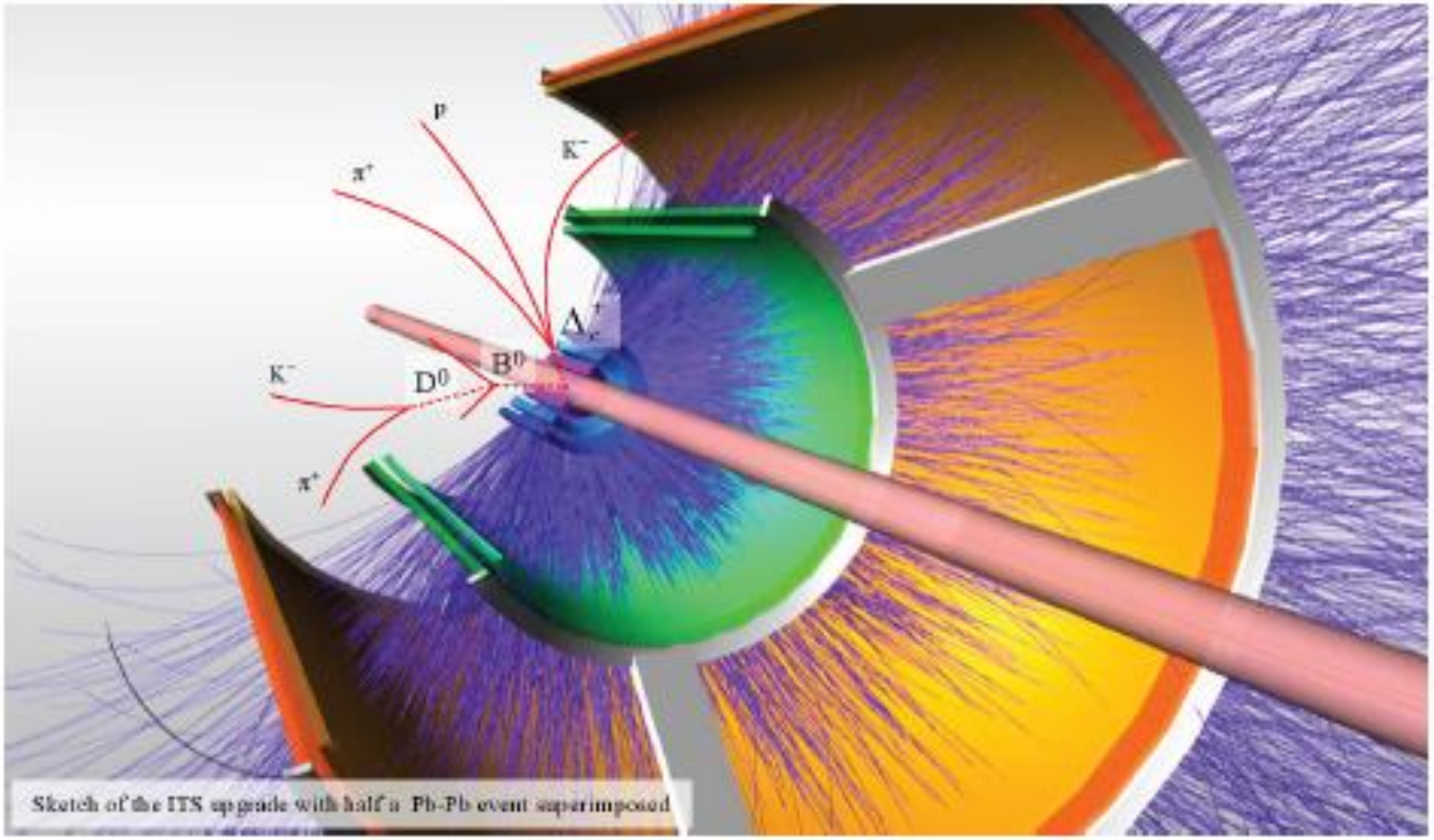


Summary

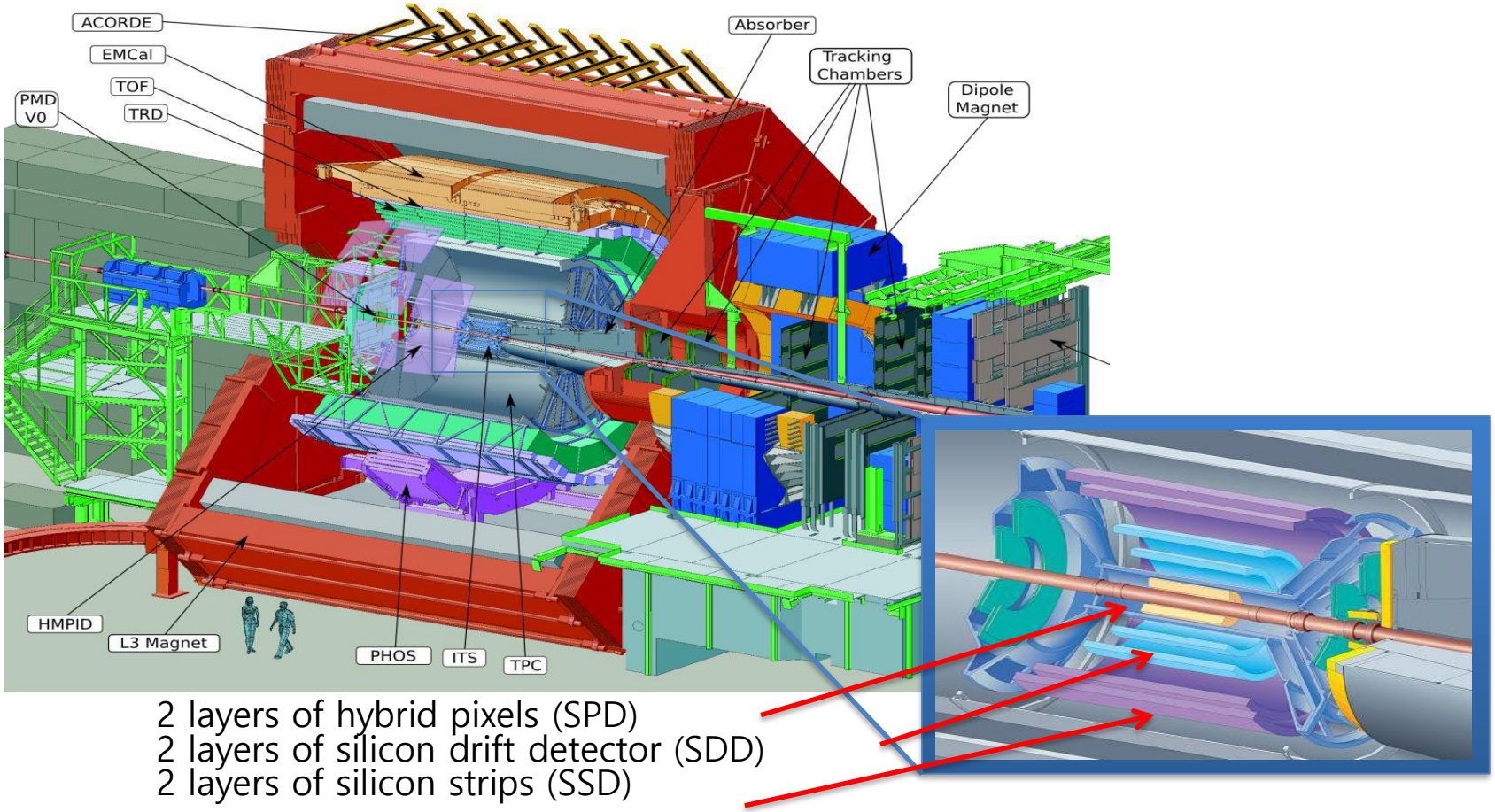
- Korea has a good potential in silicon sensor.
- A sequence of R&D for the silicon minipad sensor has been performed.
- Main production has started.
- Sensor log has been defined.

ALICE ITS UPGRADE

ALICE ITS Upgrade



ALICE Inner Tracking System at present

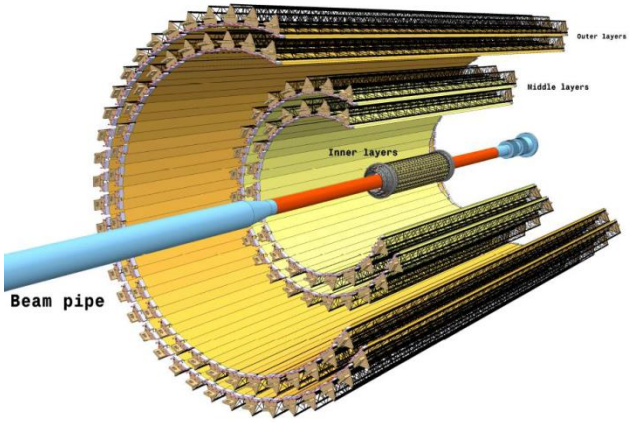


2 layers of hybrid pixels (SPD)
2 layers of silicon drift detector (SDD)
2 layers of silicon strips (SSD)

ITS upgrade

Design Objectives

- record collisions:
  - Pb-Pb at 50 kHz
  - pp at 1MHz
- improve impact parameter resolution by a factor 3
- improve standalone tracking efficiency and p_T resolution
- fast insertion/removal for yearly maintenance
- installation 2017-2018

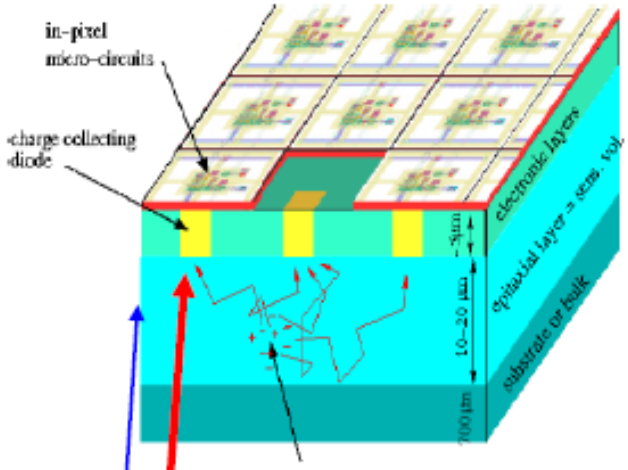


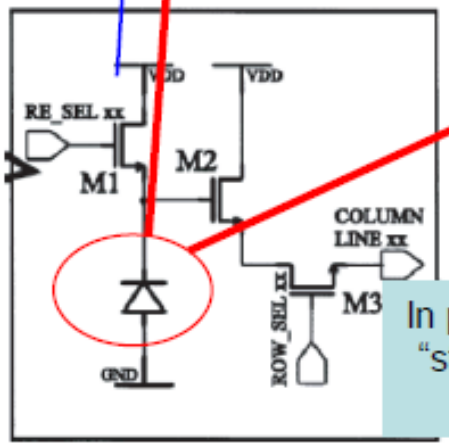
New layout

- 7 layers (3 inner, 4 middle+outer)
- reduce:
  - X/X0 per layer from 1.14 to 0.3 %
  - pixel size from 400x50 to O(30x30) μm^2
  - first layer radius from 39 to 22 mm
- beam pipe outer radius: 19.8 mm

The MIMOSA (Minimum Ionizing MOnolithic Active pixel Sensors) idea Working principle: Use of the epitaxial layer of STANDARD CMOS microelectronic processes as detecting sensitive volume.

R.Turchetta, et al. , "A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology", NIM A 458 (2001) 677-689





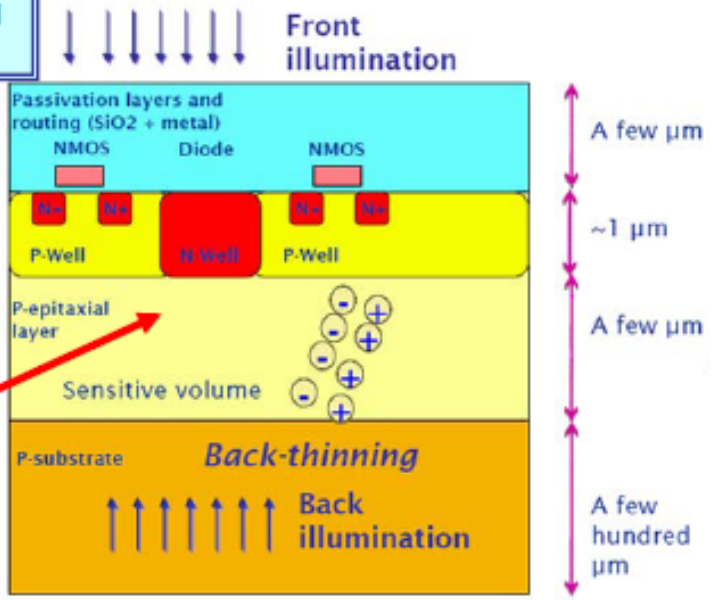
In pixel 3 transistor "standard" MAPS configuration

Recombination time:

~1 *μs*

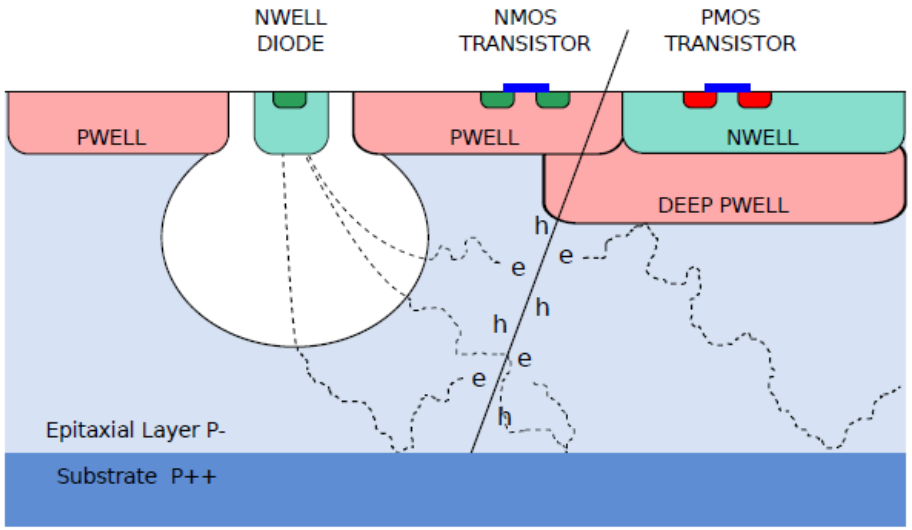
~10 *μs*

~10 *ns*



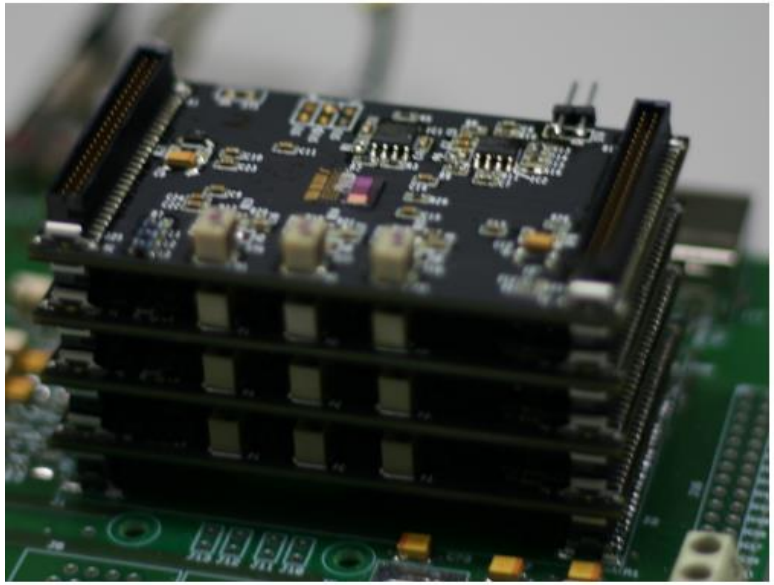
- small signal ~80 e-h/ μm, epi 2-14 μm
- Undepledet detecting volume, charge collected by diffusion and not by drift , cluster size ~ 50-100 μm, collection time ~ 150 ns
- 3T basic readout allows noise: ~ 15-20 electrons
- only N-MOS transistors allowed in pixel area
- easy access to technology through multiproject runs: ~5-50 Keuro

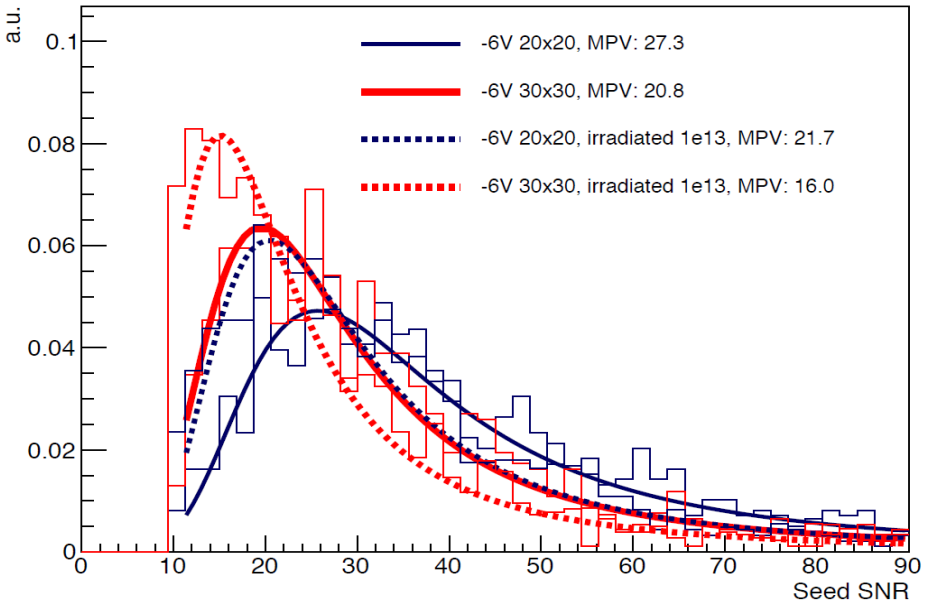
Technology : MAPS



- Gate oxide < 4 nm
  → better radiation tolerance
- 6 metal layers
- Epitaxial layer between 1 and 5 kΩcm, 15-18 µm
- Deep Pwell shields Nwell with PMOS transistors from the epitaxial layer and allows full CMOS within the pixel without efficiency loss
- Difficult to deplete epitaxial layer under Pwell far from Nwell collection electrode, but radiation tolerance sufficient
- Stitching possible up to 200mm wafer scale

Explorer-0 : Test beam

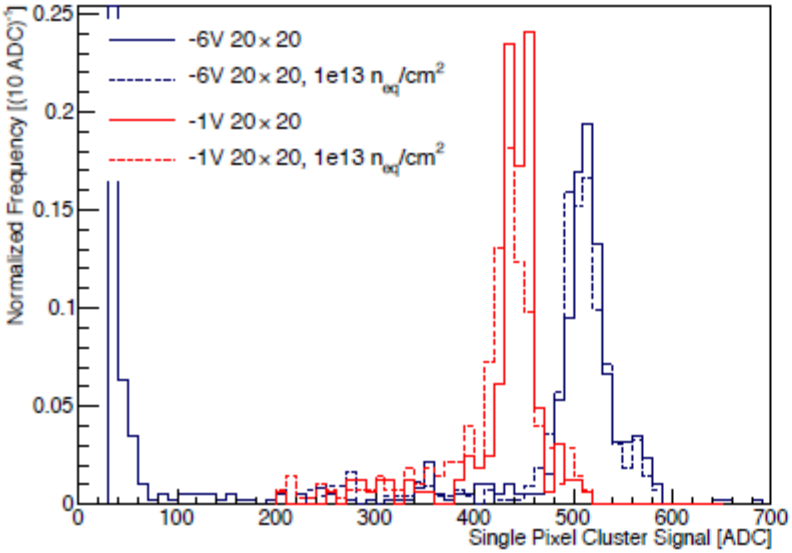




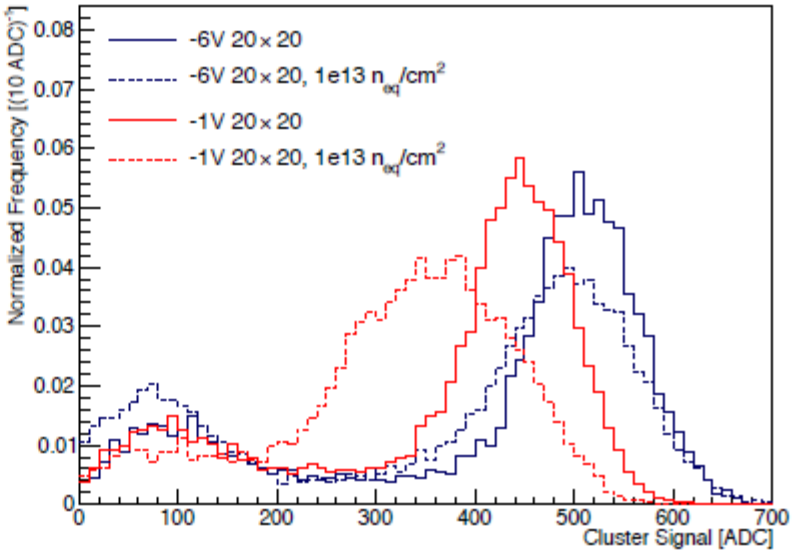
- 4 layers of explorer-0
- 6 GeV/c pions
- Reverse substrate bias gives extra margin
- Penalized by too large input capacitance, corrected for Explorer-1.

Charge collection efficiency, Explorer-1(April 2013 submission)

Response to ^{55}Fe X-rays



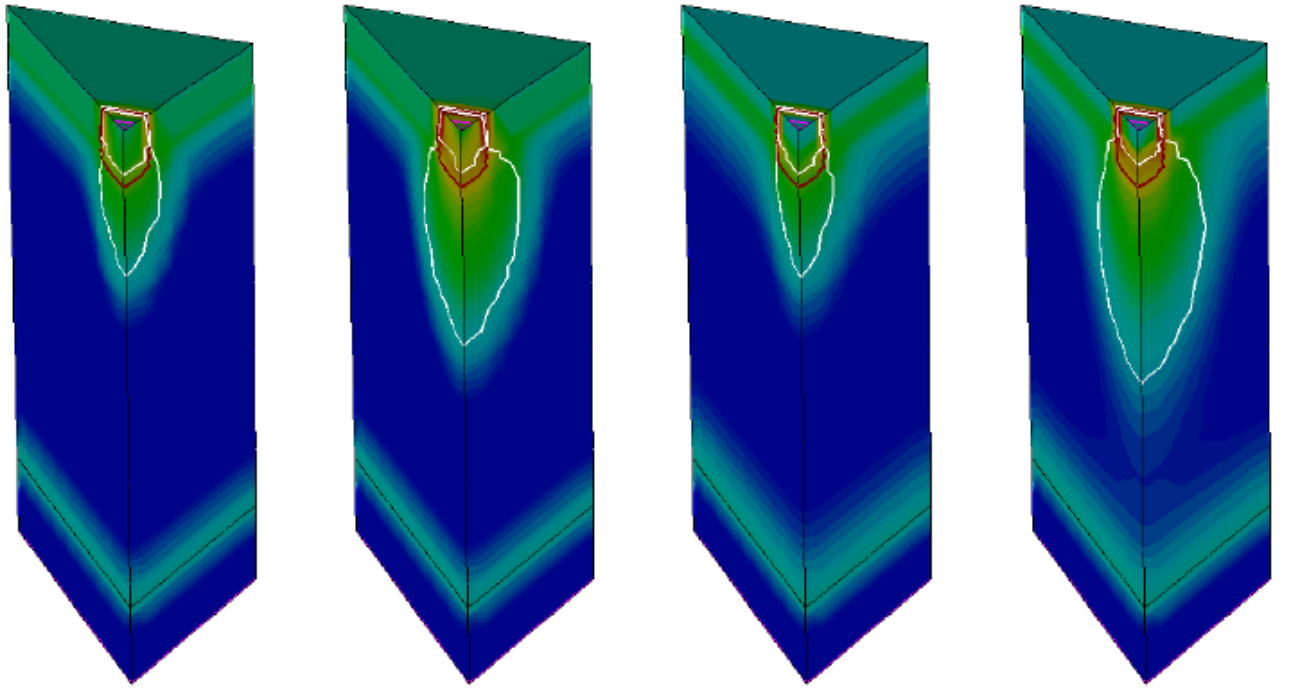
(a) Single-pixel cluster signal



(b) Cluster signal (sum of 5×5 matrix around seed pixel)

- With/without irradiation, with the larger or the smaller back bias voltage, for a chosen n-well electrode

TCAD field simulation



(a) $-1\,\mathrm{V}$, $10^{13}\,\mathrm{cm}^{-3}$ (b) $-6\,\mathrm{V}$, $10^{13}\,\mathrm{cm}^{-3}$ (c) $-1\,\mathrm{V}$, $10^{12}\,\mathrm{cm}^{-3}$ (d) $-6\,\mathrm{V}$, $10^{12}\,\mathrm{cm}^{-3}$

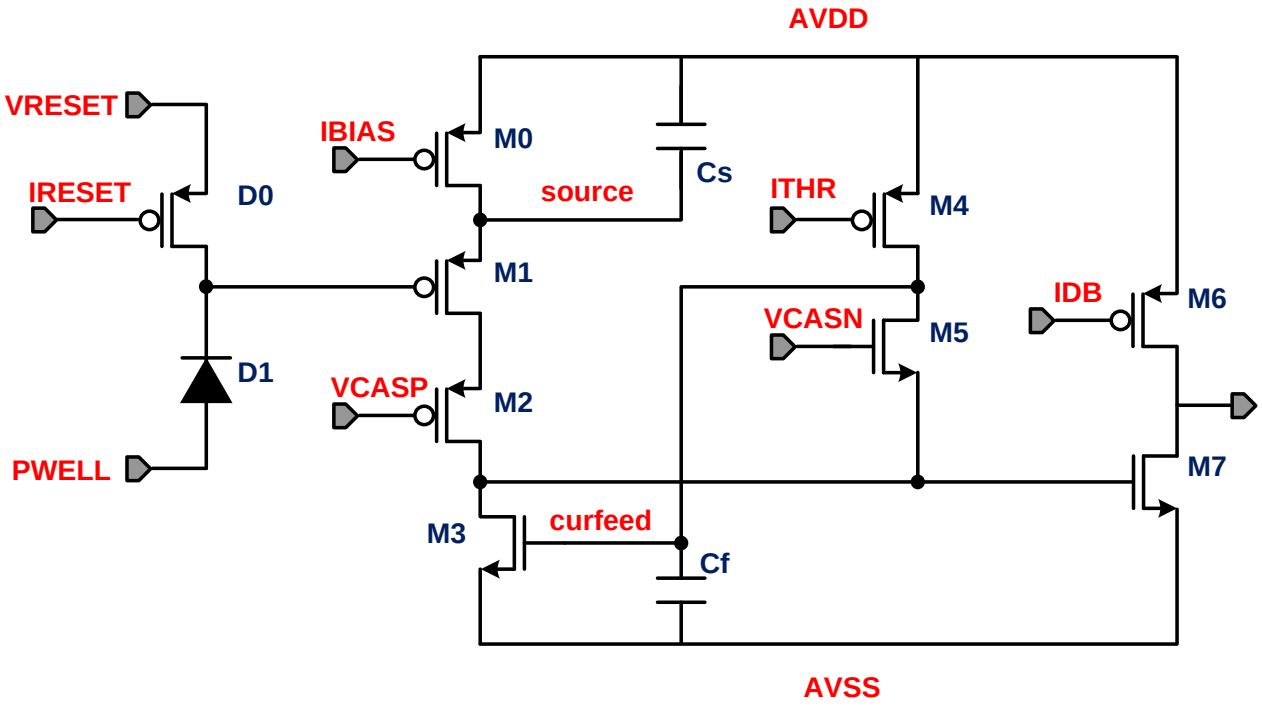
TCAD simulations, the different settings of total diode reverse bias and epitaxial layer doping.

More detail on the collection electrodes

Sector	Type	Diameter [µm]	Spacing [µm]	
1		2	0	smallest diode, lower collection eff.
2		3	0	intermediate performance, S/N lower
3		4	0	larger diode, no spacing, more noise
4		3	0	performance similar to sector 2
5		3	0.6	small spacing, lower efficiency
6		3	1.04	better S/N increasing spacing
7		2	1.54	better collection eff., better S/N, TW
8		3	0	triple well
9		3	1.04	triple well

IV. Full analog – Our study for ITS upgrade

- Specification - Front End Schematic



Requires two types of bias – current & voltage
→ Current & Voltage DACs should be designed

Summary

1. Scientific scope for the ALICE ITS upgrade and the needed specification was laid out.

2. Chosen technology is the **M**onolithic **A**ctive **P**ixel **S**ensors.

3. A sequence of R&D is in progress on a pixel chip named explorer for the ALICE ITS upgrade.

4. The R&D up to now showed, for a given pixel, how to improve the collection electrode and optimize the operation condition.

5. Korean groups, PNU, Inha Univ., and Yonsei Univ., are preparing the test system of the chips under development.

6. We joined the design R&D recently and will take part in the design improvement.