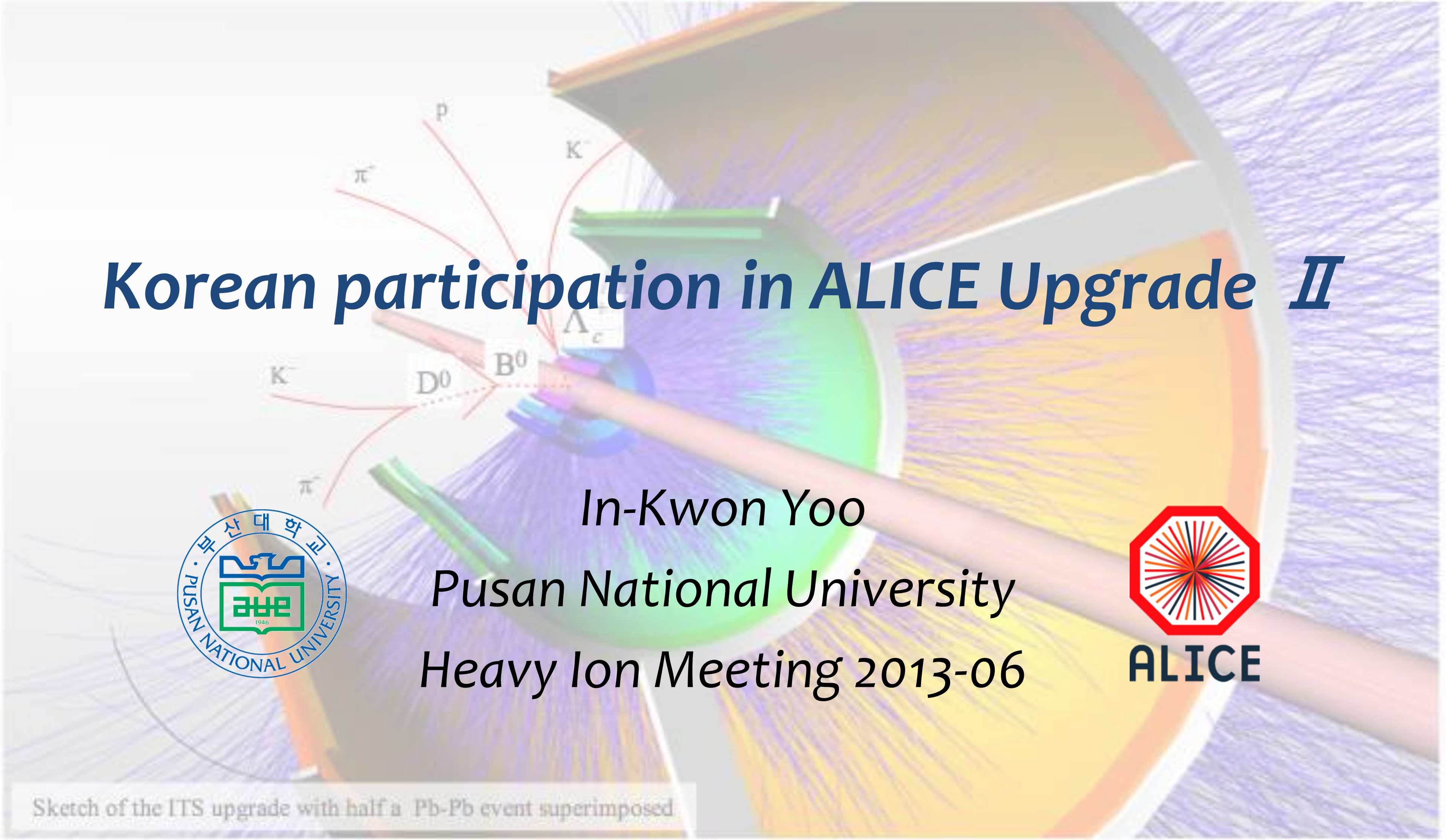
Korean participation in ALICE Upgrade Ⅱ

In-Kwon Yoo

Pusan National University

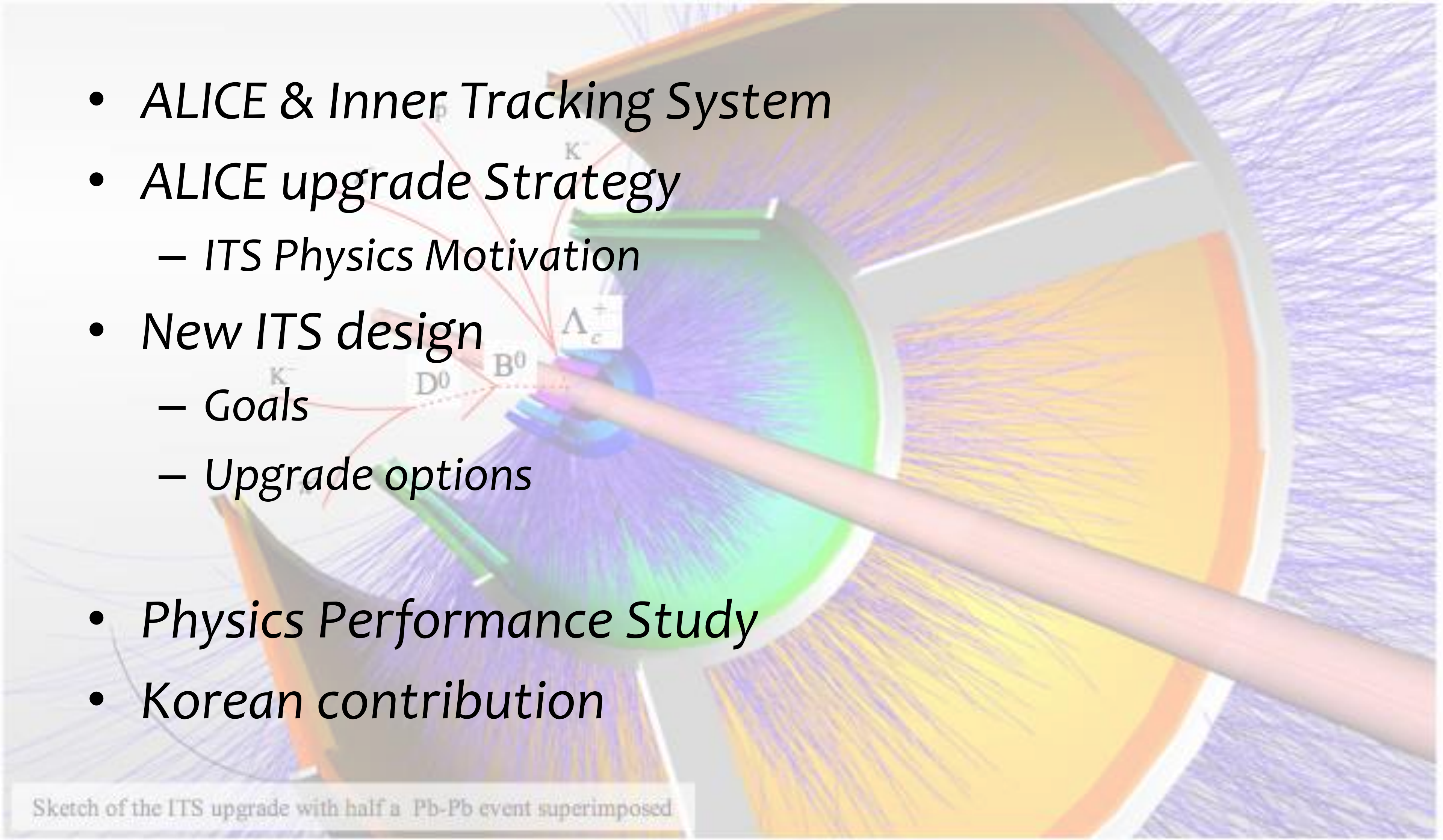
Heavy Ion Meeting 2013-06



Sketch of the ITS upgrade with half a Pb-Pb event superimposed

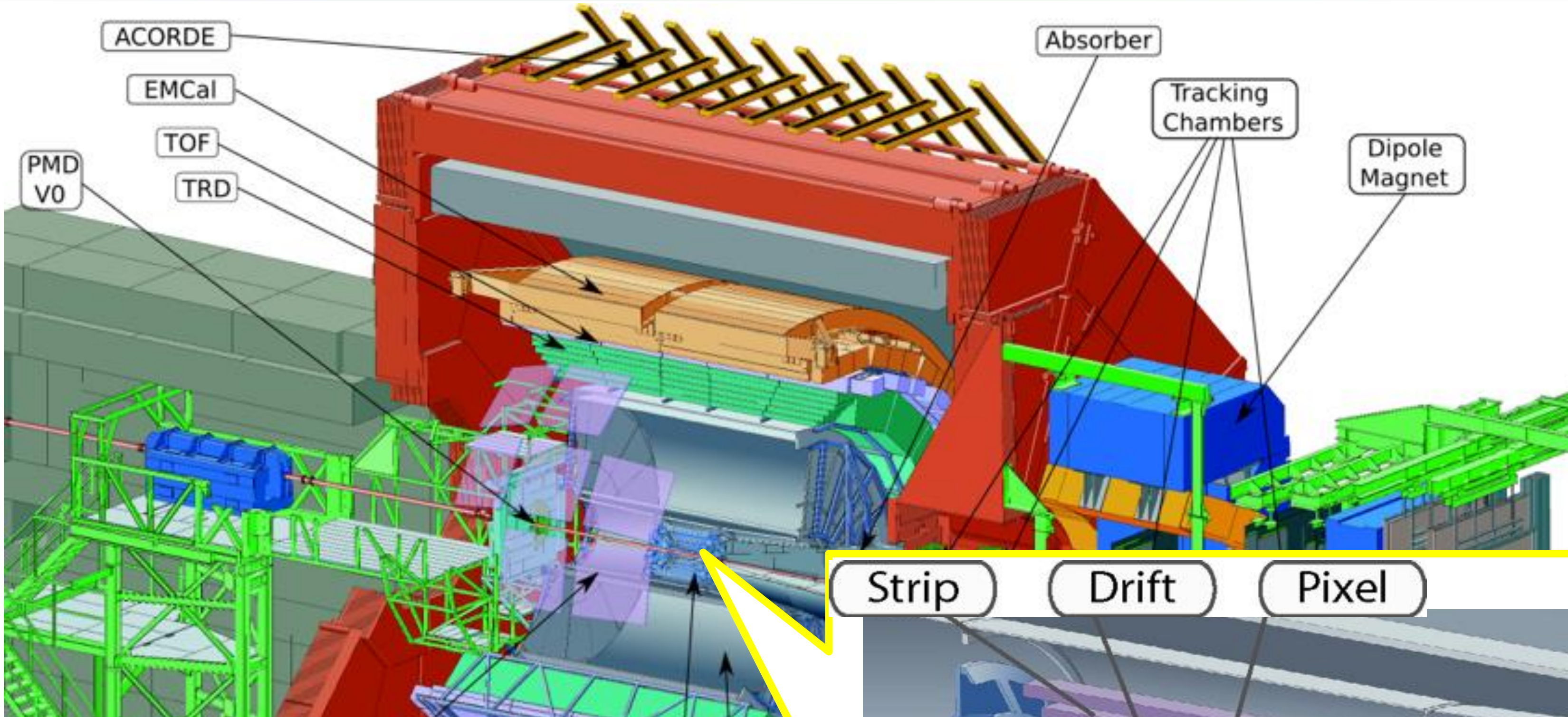
Outline

- *ALICE & Inner Tracking System*
- *ALICE upgrade Strategy*
  - *ITS Physics Motivation*
- *New ITS design*
  - *Goals*
  - *Upgrade options*
- *Physics Performance Study*
- *Korean contribution*



Sketch of the ITS upgrade with half a Pb-Pb event superimposed

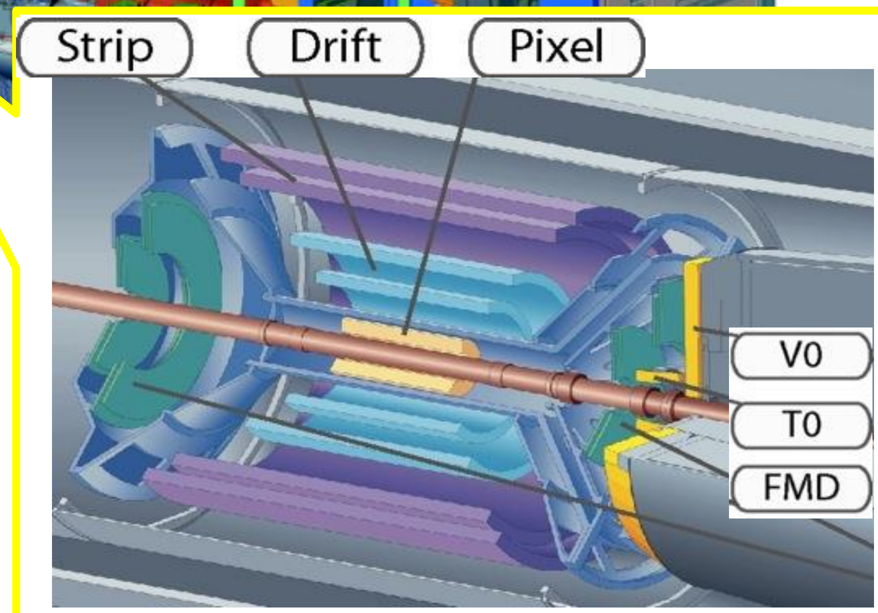
ALICE Detector



Current ITS

6 concentric barrels, 3 different technologies

- *2 layers of silicon pixel (SPD)*
- *2 layers of silicon drift (SDD)*
- *2 layers of silicon strips (SSD)*



ALICE Upgrade Strategy

☐ *High precision measurements of rare probes at low p_T, which can not be selected with a trigger, require a large sample of events.*

Target

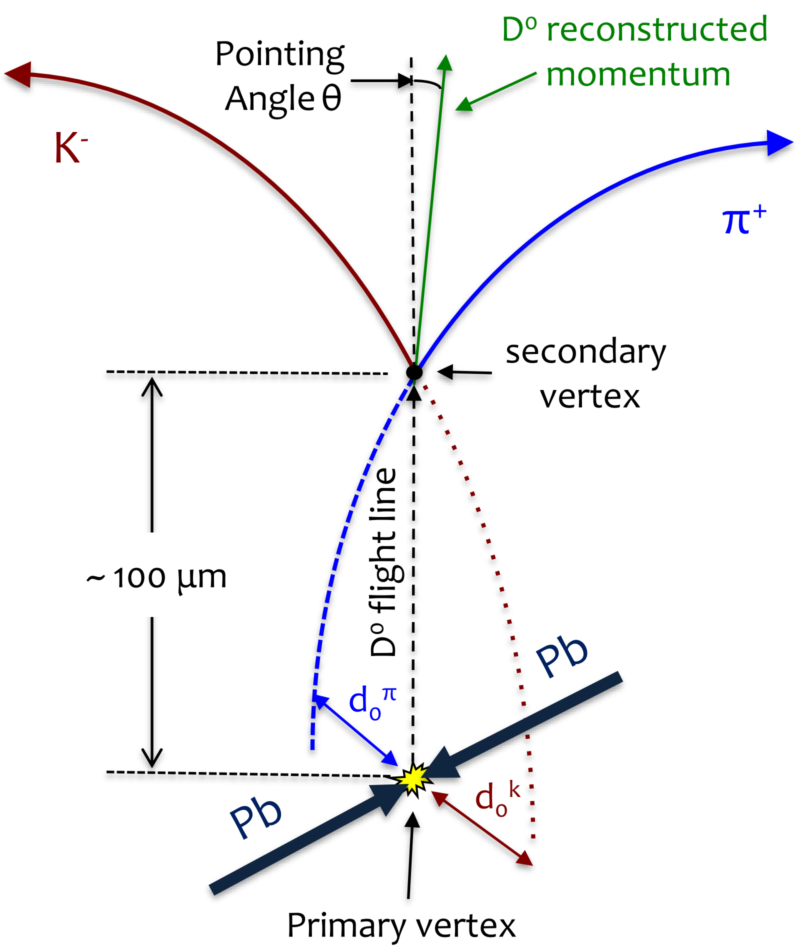
- *Gain a factor **100** in statistics over approved program.*
  - *Pb-Pb recorded luminosity ≥ 10 nb^{-1} ➔ 8 x 10^{10} events*
  - *pp (@5.5 TeV) recorded luminosity ≥ 6 pb^{-1} ➔ 1.4 x 10^{11} events*
- *Significant improvement of vertexing & tracking capabilities.*

Goals

- *Upgrade the ALICE readout system & online system*
- *Improve vertexing & tracking at low pT* ➔ *New ITS*

ITS performance - Tracking and vertex determination

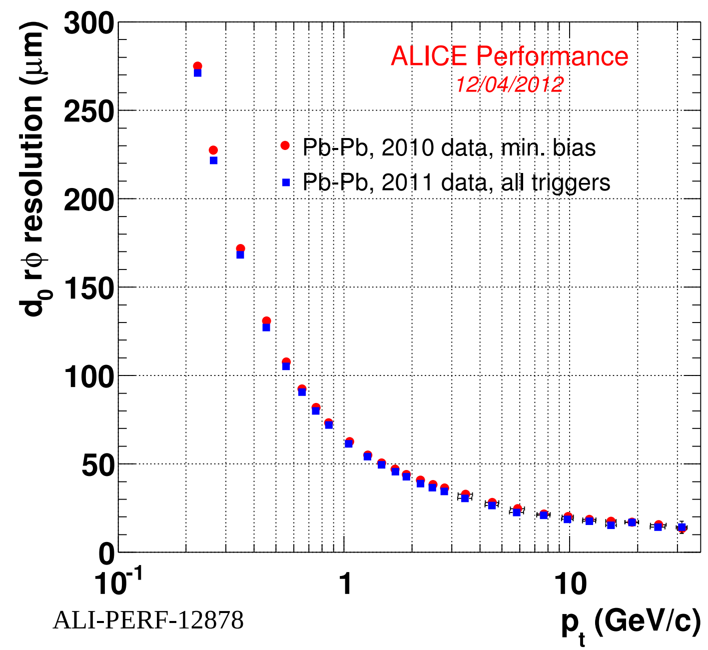
Example: D^0 meson



Analysis based on decay topology and invariant mass technique

Open charm

Particle	Decay Channel	cτ (μm)
D^0	$K^- \pi^+$ (3.8%)	123
D^+	$K^- \pi^+ \pi^+$ (9.5%)	312
D_s^+	$K^+ K^- \pi^+$ (5.2%)	150
Λ_c^+	$p K^- \pi^+$ (5.0%)	60



What determines the impact parameter resolution

Vertex projection from two points: a simplified approach (telescope equation)

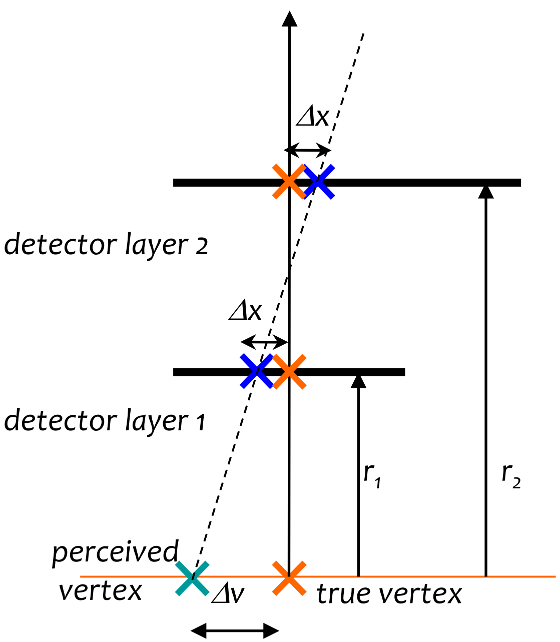
current ITS ➡ pointing resolution = $(13 \oplus 22 GeV/p \cdot c)\ \mu m$

from detector position error

from coulomb scattering

first pixel layer

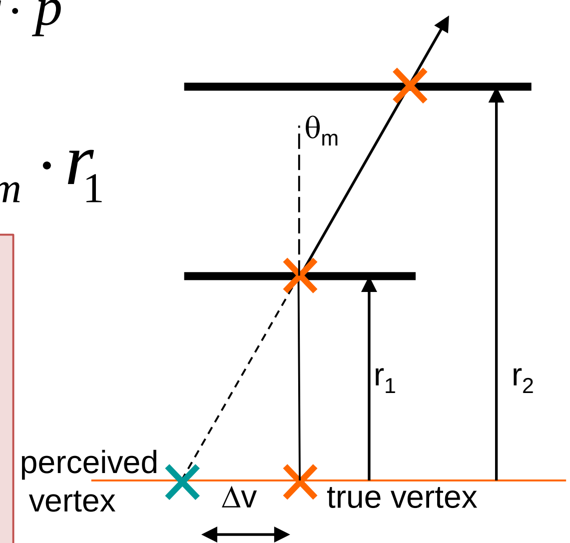
$$X_0 = 0.3\%$$



$$\Delta v = \Delta x \bullet \sqrt{\frac{r_2^2 + r_1^2}{(r_2 - r_1)^2}}$$

$$\theta_m = \frac{13.6 Mev}{\beta \cdot c \cdot p} \cdot \sqrt{X_0}$$

$$\Delta v = \theta_m \cdot r_1$$



For higher Pointing resolution,

- Smaller pixel size
- less material budget
- Add layers
- Reduce distance between layers

New ITS Design goals

1. Improve impact parameter resolution by a factor of ~3

- Get closer to IP (position of first layer)

: 39mm ➡ 22mm

- Reduce material budget (X/X_0 /layer)

: ~1.14% ➡ ~ 0.3% (for inner layers)

- Reduce pixel size

: currently 50mm x 425mm

monolithic pixels ➡ 20 mm x 20 mm

hybrid pixels ➡ state-of-the-art , 50 mm x 50 mm

2. Improve tracking efficiency and p_T resolution at low p_T

- Increase granularity: 6 layers ➡ 7 layers , reduce pixel size
- Increase radial extension: 39-430 mm ➡ 22– 430 (500) mm

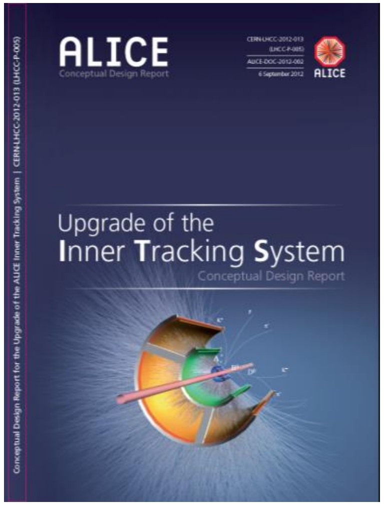
3. Fast readout

readout of Pb-Pb interactions at > 50 kHz and pp interactions at ~ several MHz

4. Fast insertion/removal for yearly maintenance

possibility to replace non functioning detector modules during yearly shutdown

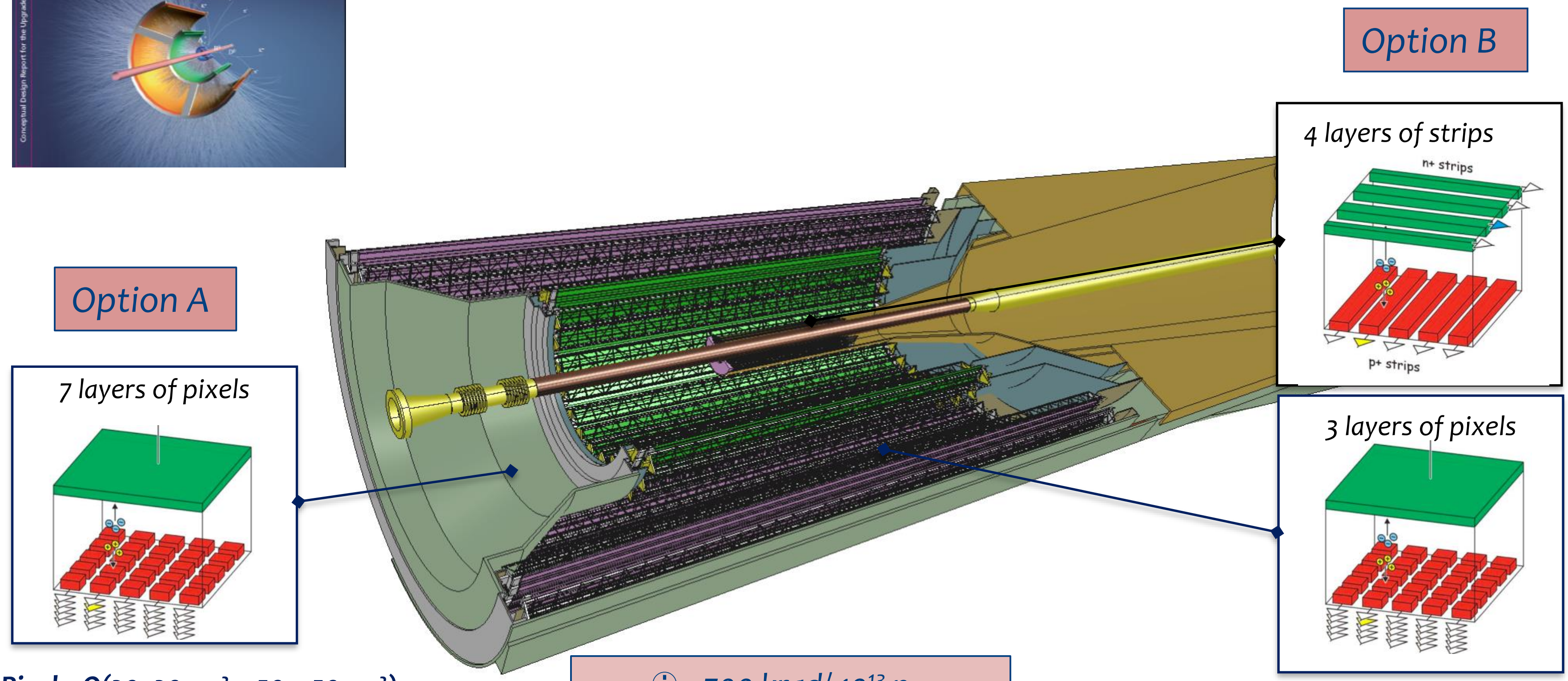
Upgrade options



Two design options have being studied

A. *7 layers of pixel detectors (baseline)*

B. *3 inner layers of pixel detectors and 4 outer layers of strip detectors*



Pixels: O(20x20μm² – 50 x 50μm²)

700 krad/ 10^{13} n_{eq}

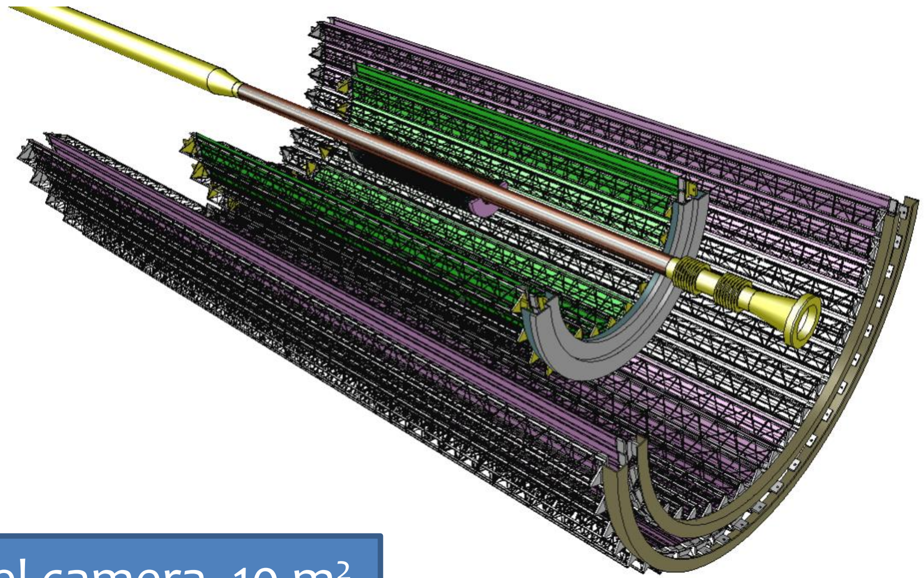
Includes safety factor ~ 4

Pixels: O(20x20μm² – 50 x 50μm²)
Strips: 95 μm x 2 cm, double sided

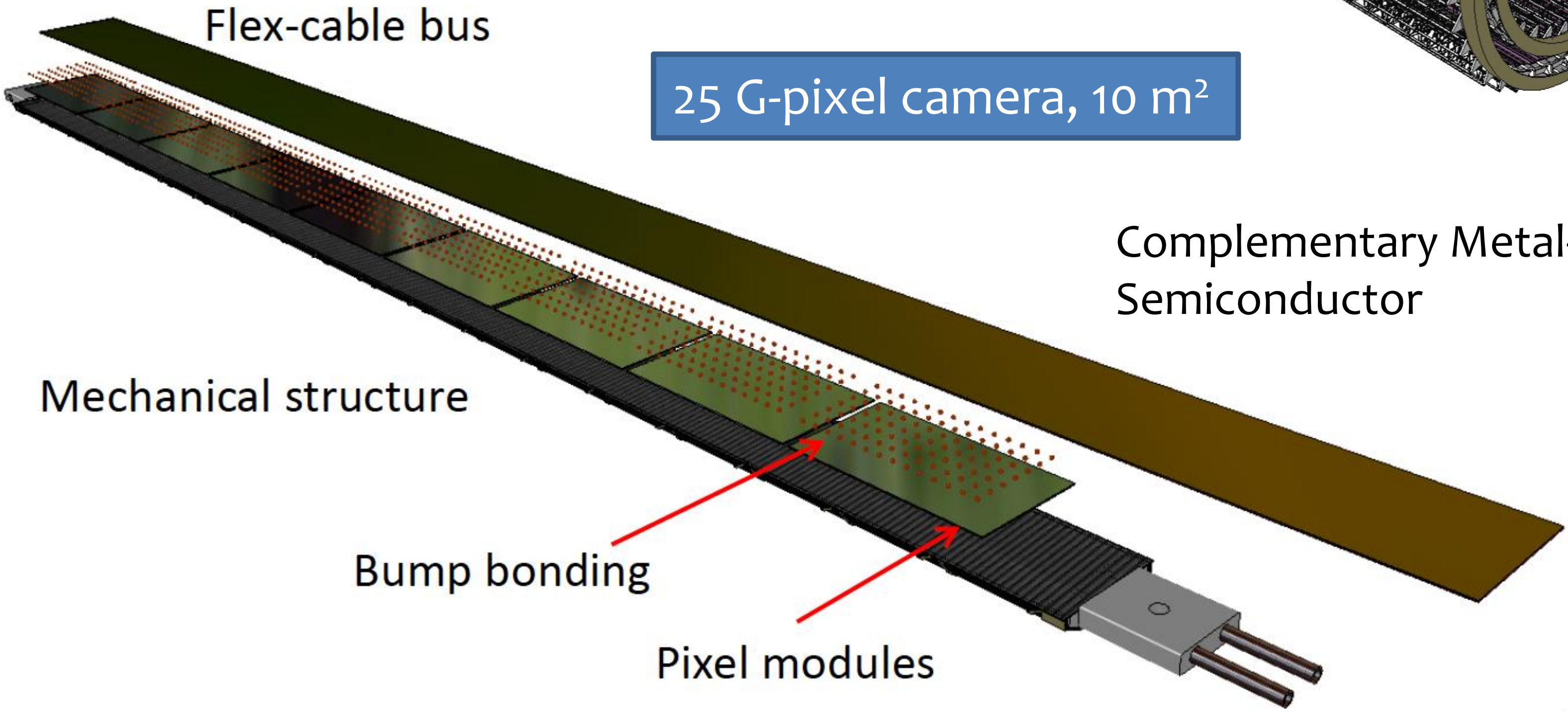
New ITS (baseline)

Inner Barrel: 3 layers
Outer Barrel: 4layers

Detector module (Stave) consists of
- Carbon fibber mechanical support
- Cooling unit
- Polyimide printed circuit board
- Silicon chips (CMOS sensors)



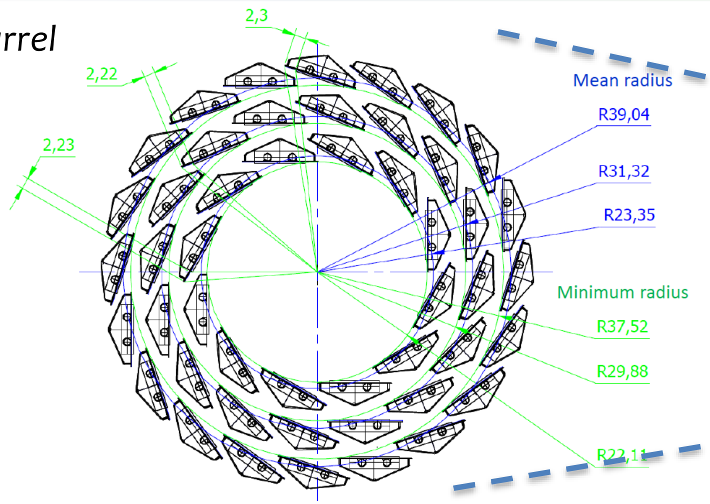
25 G-pixel camera, 10 m²



Complementary Metal-Oxide-Semiconductor

ITS Barrel Layers

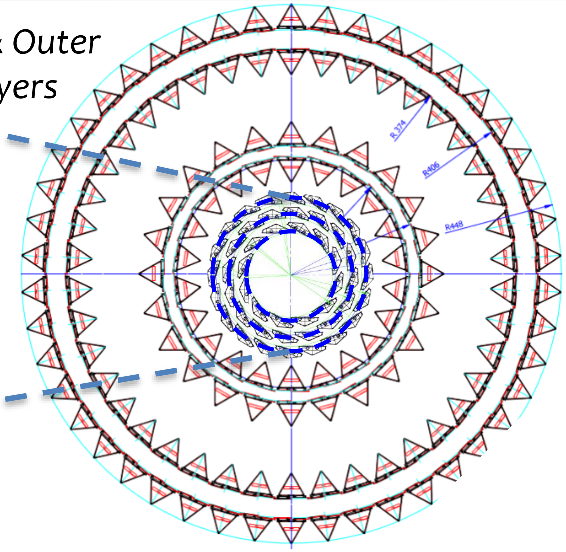
Inner Barrel layers



- *3 innermost layers at r= 22, 28 and 36 mm*
- *Same z-length: 27 cm*
- *Assumed chip size: 15 mm x 30 mm*
- *9 chips/module*
- *$X/X_0 \leq 0.3\%$*

	Modules	Chips
Layer 1	12	108
Layer 2	16	144
Layer 3	20	180
Total	48	432

Middle & Outer Barrel layers



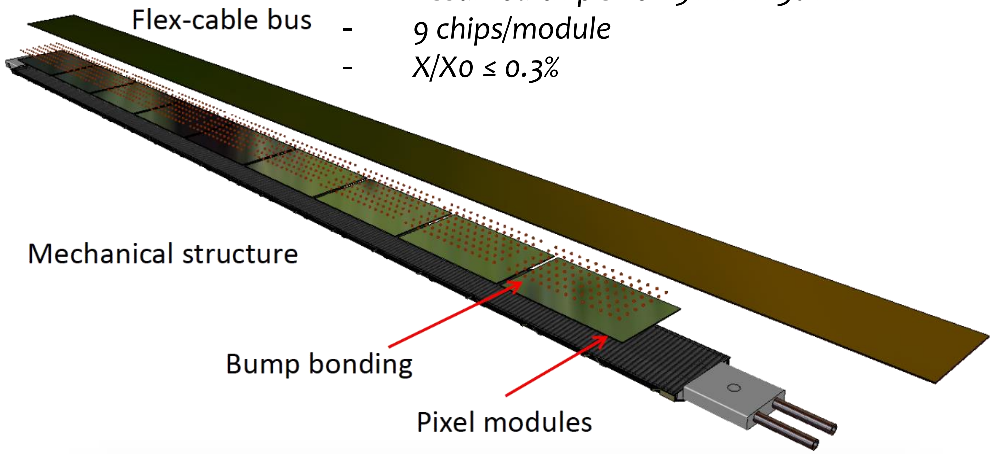
- *4 outermost layers at r= 48, 52, 96, 102 mm*
- *84 cm < z-length < 150 cm*
- *Double chip rows per module*
- *$X/X_0 \leq 0.8\%$*

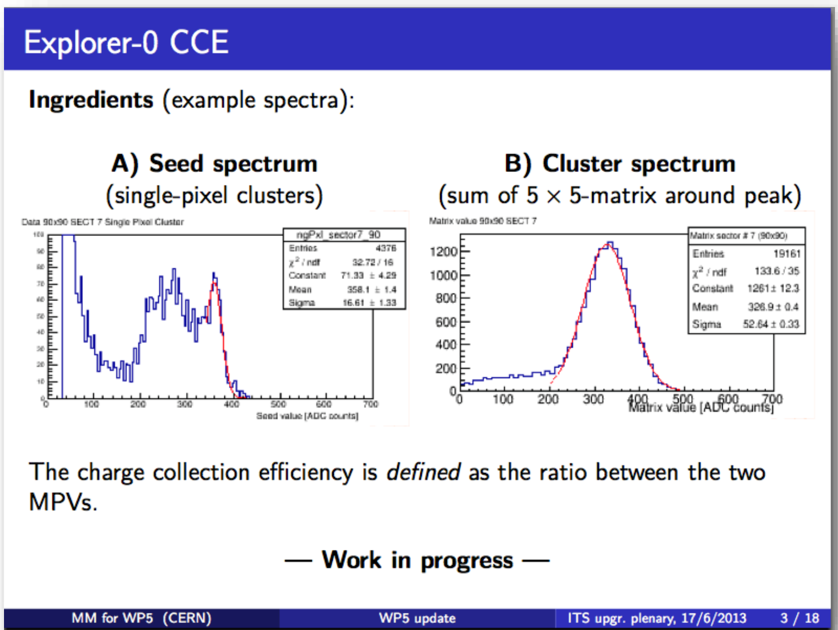
	Modules	Chips
Layer 4	48	2688
Layer 5	52	2912
Layer 6	96	9600
Layer 7	102	10200
Total	298	25400

Hybrid Pixel Detector – 'Expolrer-0/1'

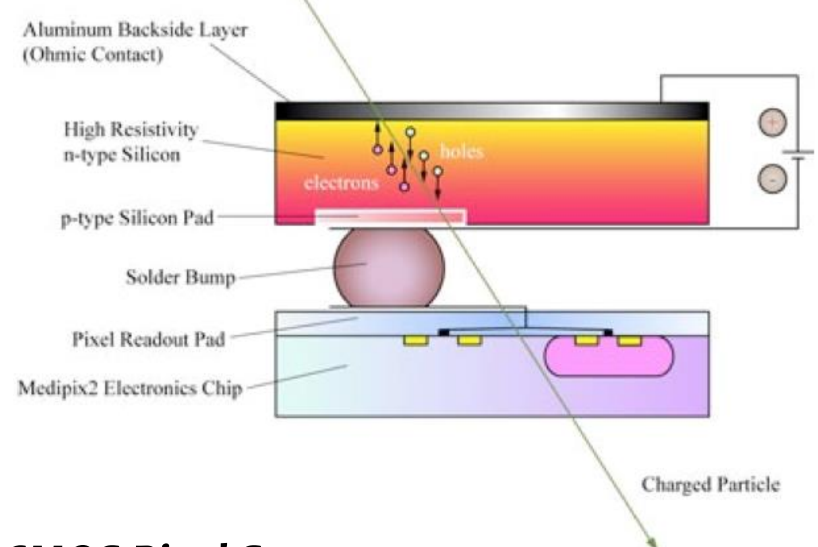
Assembly layout

- Assumed chip size: 15 mm x 30 mm
- 9 chips/module
- X/X0 ≤ 0.3%

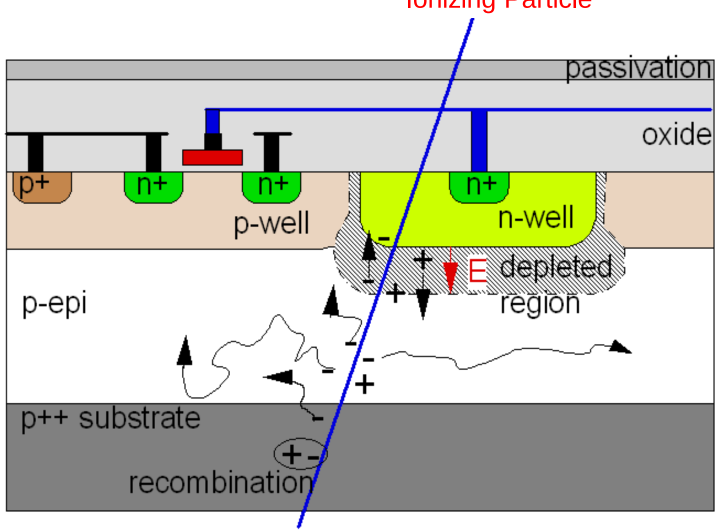




Hybrid Pixel Layout

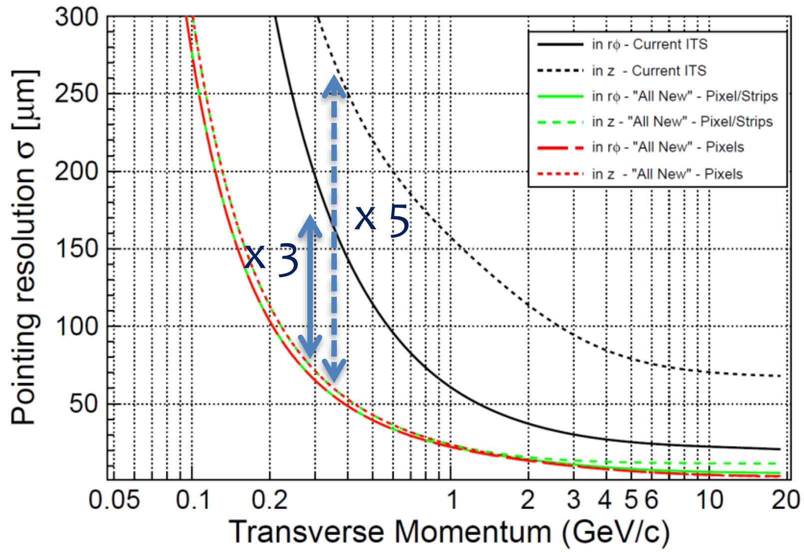


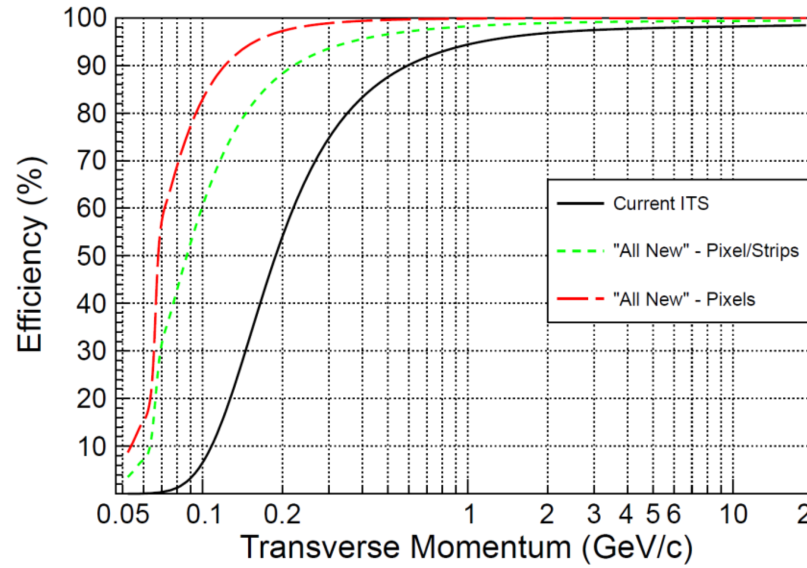
CMOS Pixel Sensors



Physics Performance Study

Motivation : Improvement of impact parameter resolution





Simulations for two upgrade layouts

Key !!

Option A: 7 pixel layers

- *Resolutions:* s_{rf} = 4 mm, s_z = 4 mm for all layers
- *Material budget:* X/X_0 = 0.3% for all layers

radial positions *(mm): 22, 28, 36, 200, 220, 410, 430*

Same for both layouts

Option B: 3 layers of pixels + 4 layers of strips

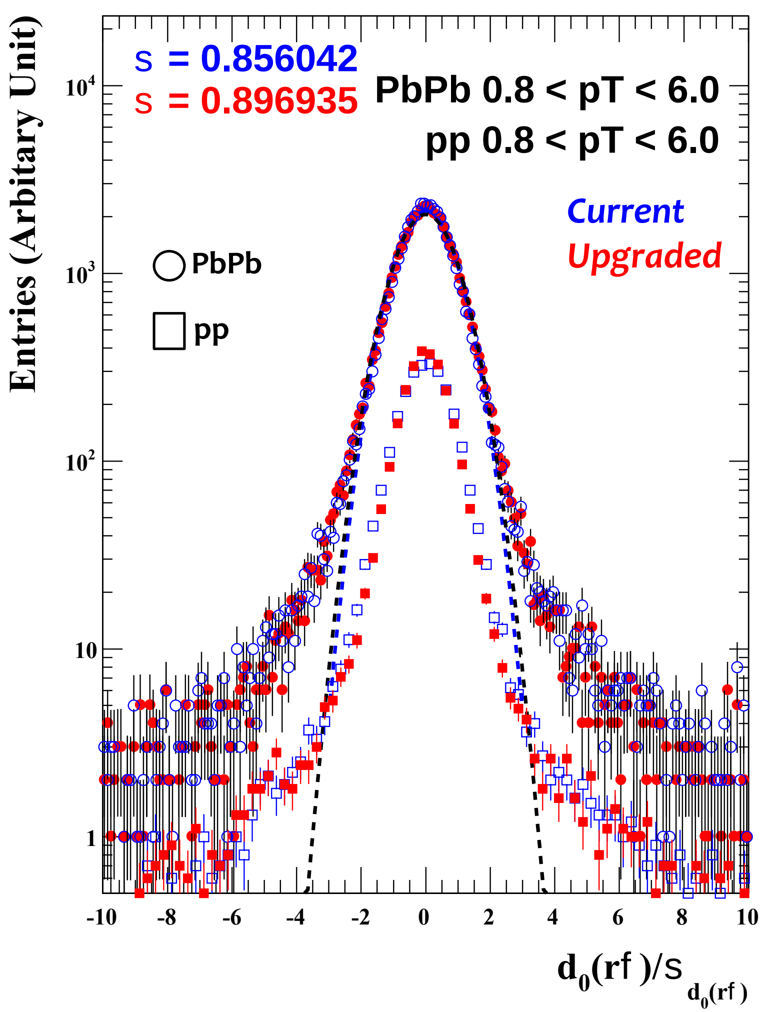
- *Resolutions:* s_{rf} = 4 mm, s_z = 4 mm for pixels s_{rf} = 20 mm, s_z = 830 mm for strips
- *Material budget:* X/X_0 = 0.3% for pixels X/X_0 = 0.83% for strips

Physics Performance Study

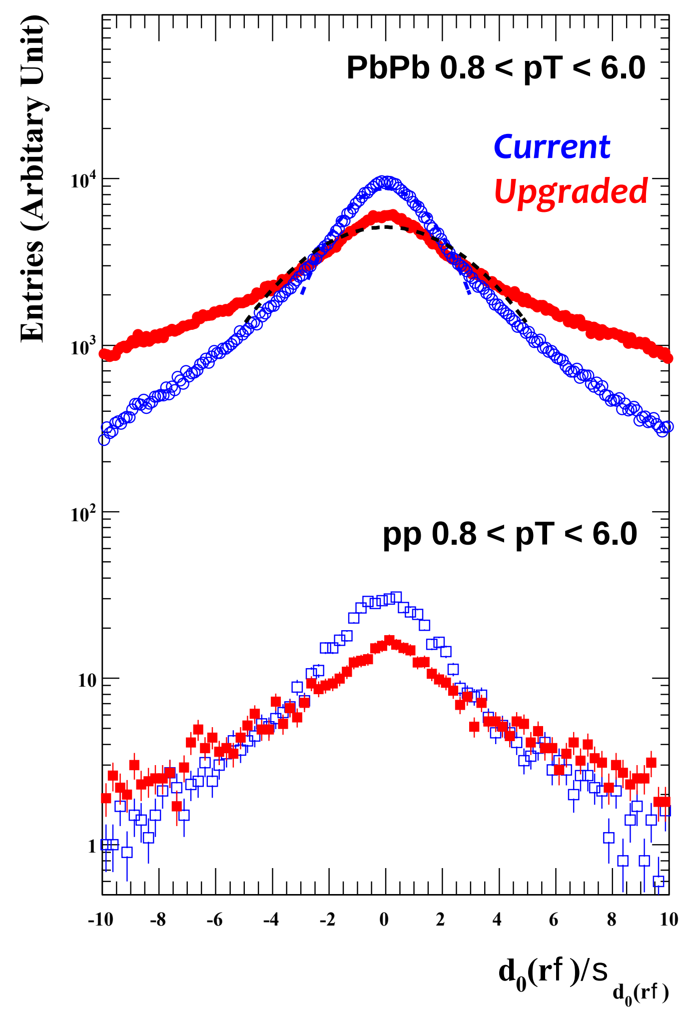
An Example : Impact parameter distribution for,

work with Prof. M.Kweon
K.Choi, K,Oh

Dielectron and Dalitz electrons



electrons from B meson



Task Organization of Asian groups

Activity	Participants	Comments
Detector simulation and reconstruction, physics performance	Inha, SUT, CCNU (?)	WP physics (A. Dainese) WP simul. and rec. (M. Masera, J. Belikov)
Design of pixel chip	CCNU, Yonsei, TMEC	WP chip design (W. Snoeys)
Characterization of pixel chip (radioactive source, test beam)	CCNU , Inha, Pusan, SLRI	WP characterization and qualification (M. Mager)
Characterization of pixel chip (laser)	Yonsei	WP characterization and qualification (M. Mager)
Pixel chip mass test	CCNU, Yonsei, TMEC	WP wafer pp and test (P. Riedler)
Assembly and qualification of hybrid structures	CCNU, Pusan, Inha	WP middle/outer layers (other institutes involved: Berkeley/INFN-Nikhef)

Outlook : PNU Task for ITS upgrade

- *2013/15*
  : Characterization & Qualification of pixel chips.
  - *This July/August : Learn Test System (Procedure, Device)*
  - *In advance : Build a Test System in Pusan*

  : Physics Performance study (with Inha Univ.)

- *2015/2017 : Assembly and qualification of hybrid structures (pixel chips + kapton printed circuit board)*
  - ***Test environment preparation:***
    - *Probing (including mechanical tooling, probe-card design, …)*
      Visual inspection system
      Define test areas (clean room)
  - ***Automatisation of test-system:** movements, pattern recognition.*
  - *Define **Database** for test-results*
  - ***Component tracking** – investigate technical options*

Back Up

PROJECT ORGANIZATION

Institute Board
(PL, DPL, SPL, TC, Team Leaders)

Project Coordination
(PL, DPL, SPL, TC, RC, Upgrade Tasks Coordinators)

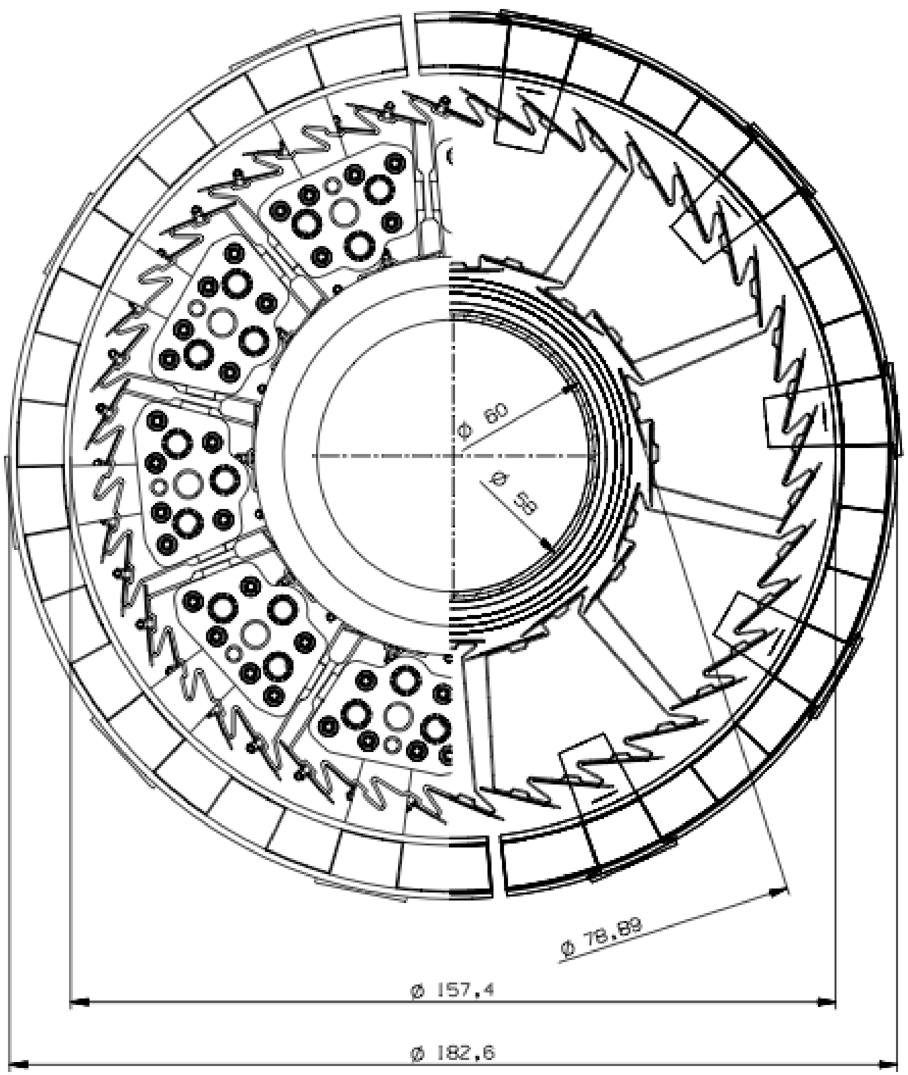
ITS Operation
(RC, PL, DPL, SPL, TC, QAC, CC, experts)

UPGRADE

1. Physics
2. Simulation and Reconstruction
3. Pixel chip design
4. Wafers post-processing and
5. Characterization and Qualification
6. Inner Layers Module
7. Middle Layers Module
8. Outer Layers Module
9. Layers Integration/Commissioning
10. Readout Electronics
11. Mechanics and Cooling
12. DCS and Database

■ Conveners nominated (green boxes: 1–5, 10–11)

Current Layout (SPD)

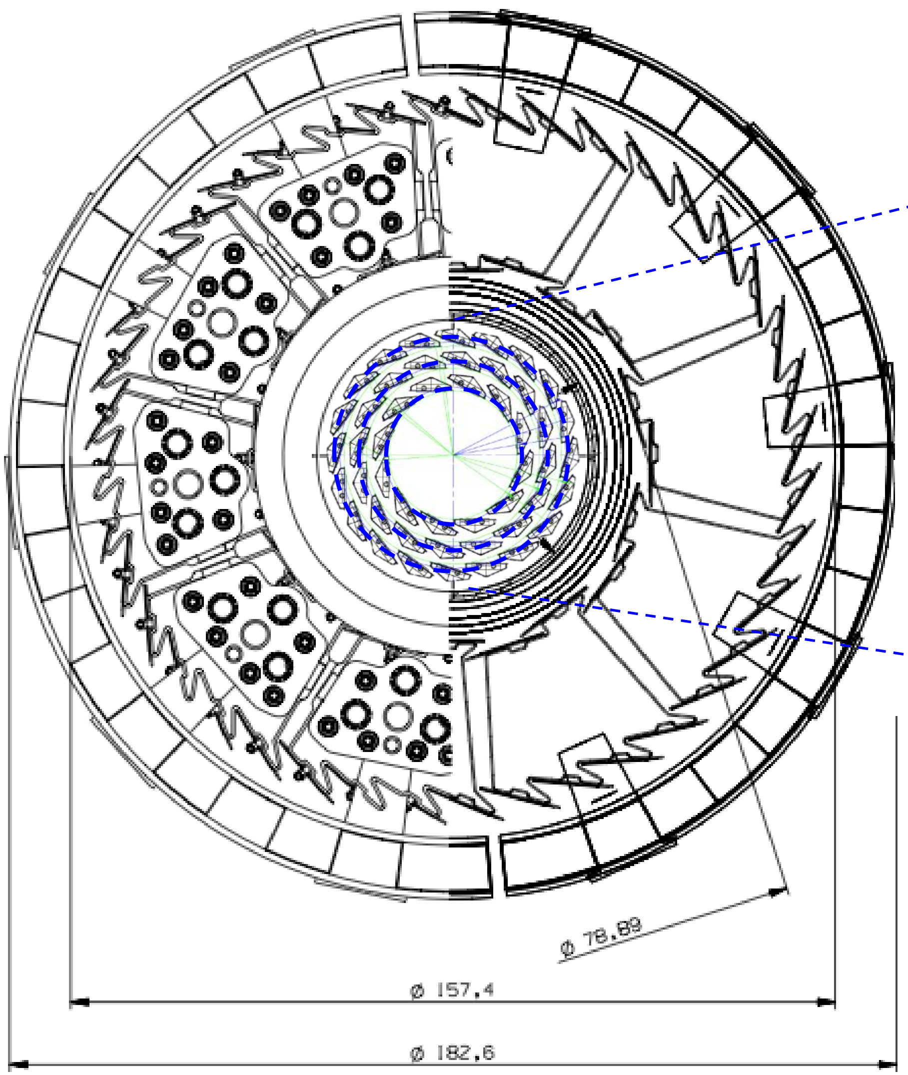


Inner Radius

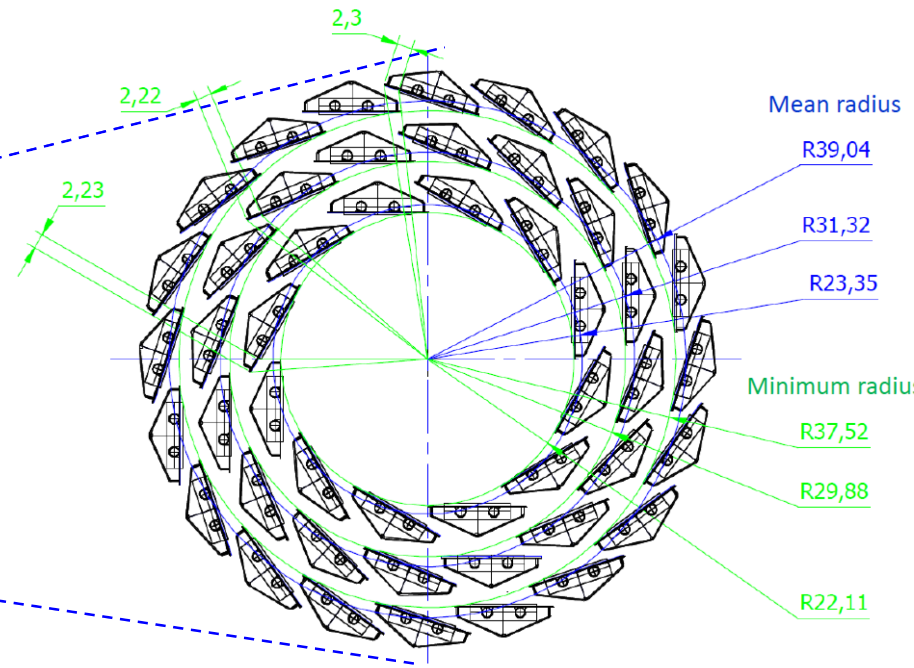
- ***R 50***
- ***R 78.89***
- ***R 157.4***

ALICE ITS Upgrade layout

Current Layout (SPD)



Upgrade Layout (Inner)

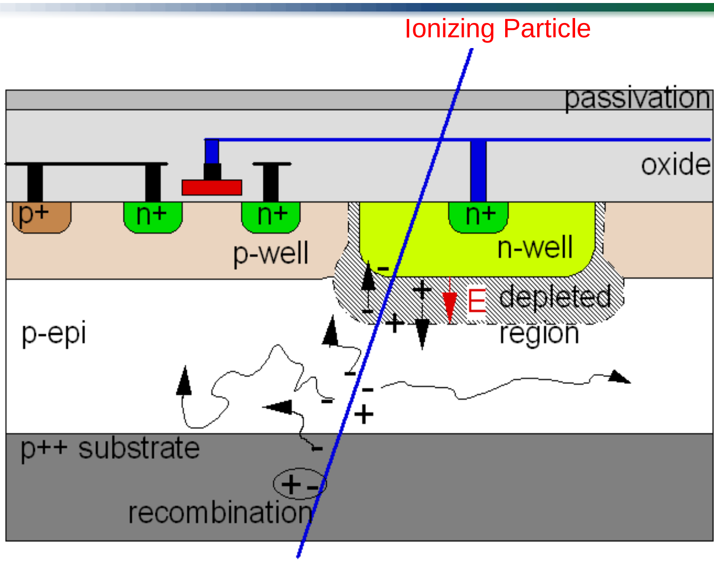


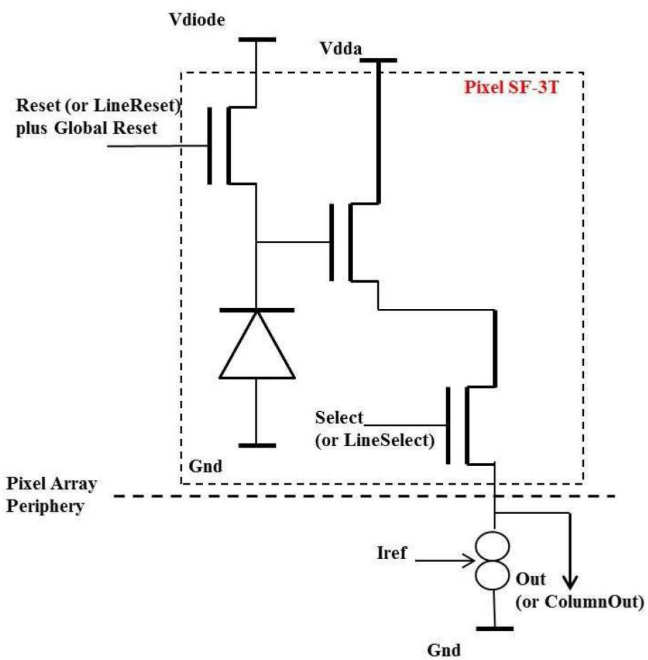
Inner Radius
- R 50
- R 78.89
- R 157.4

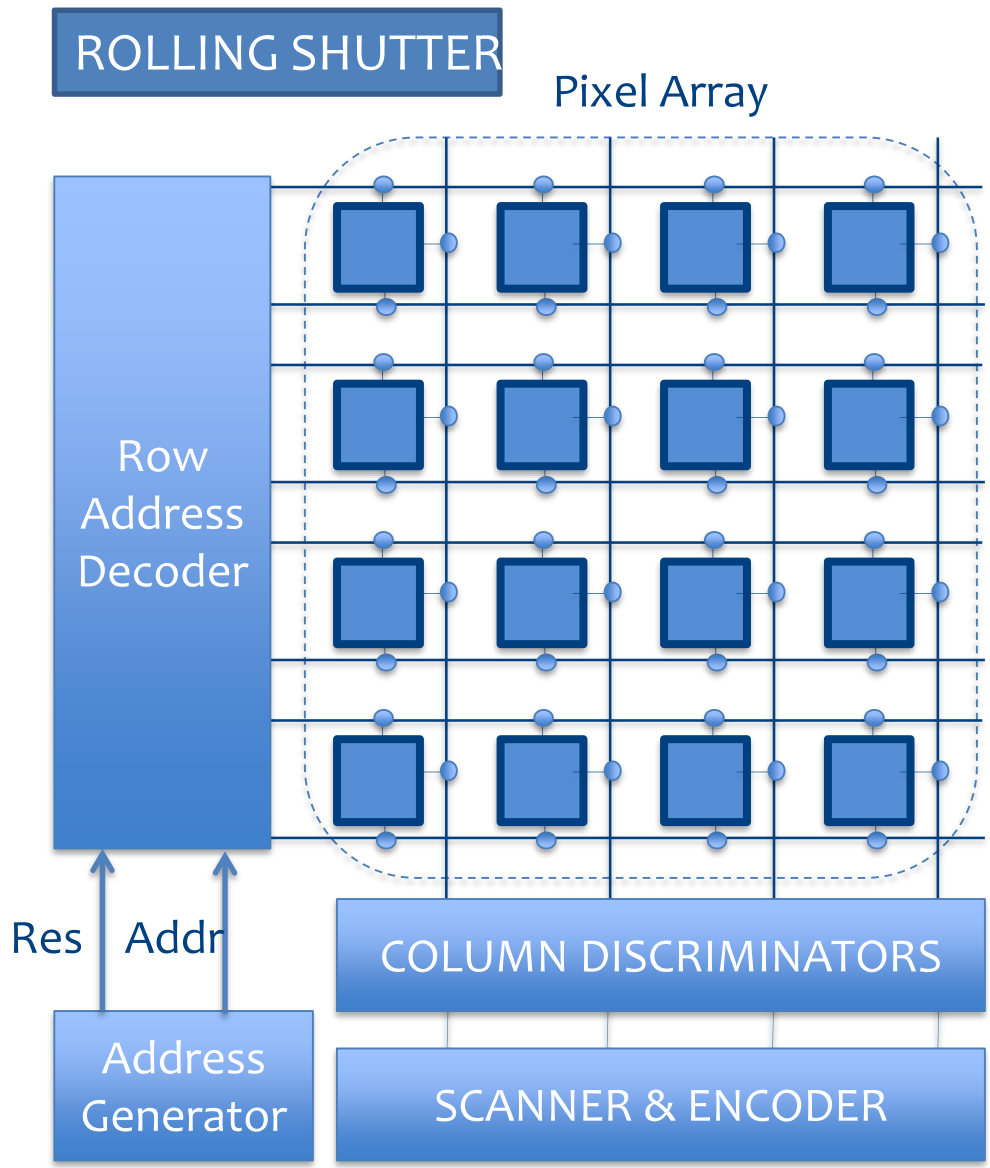
+

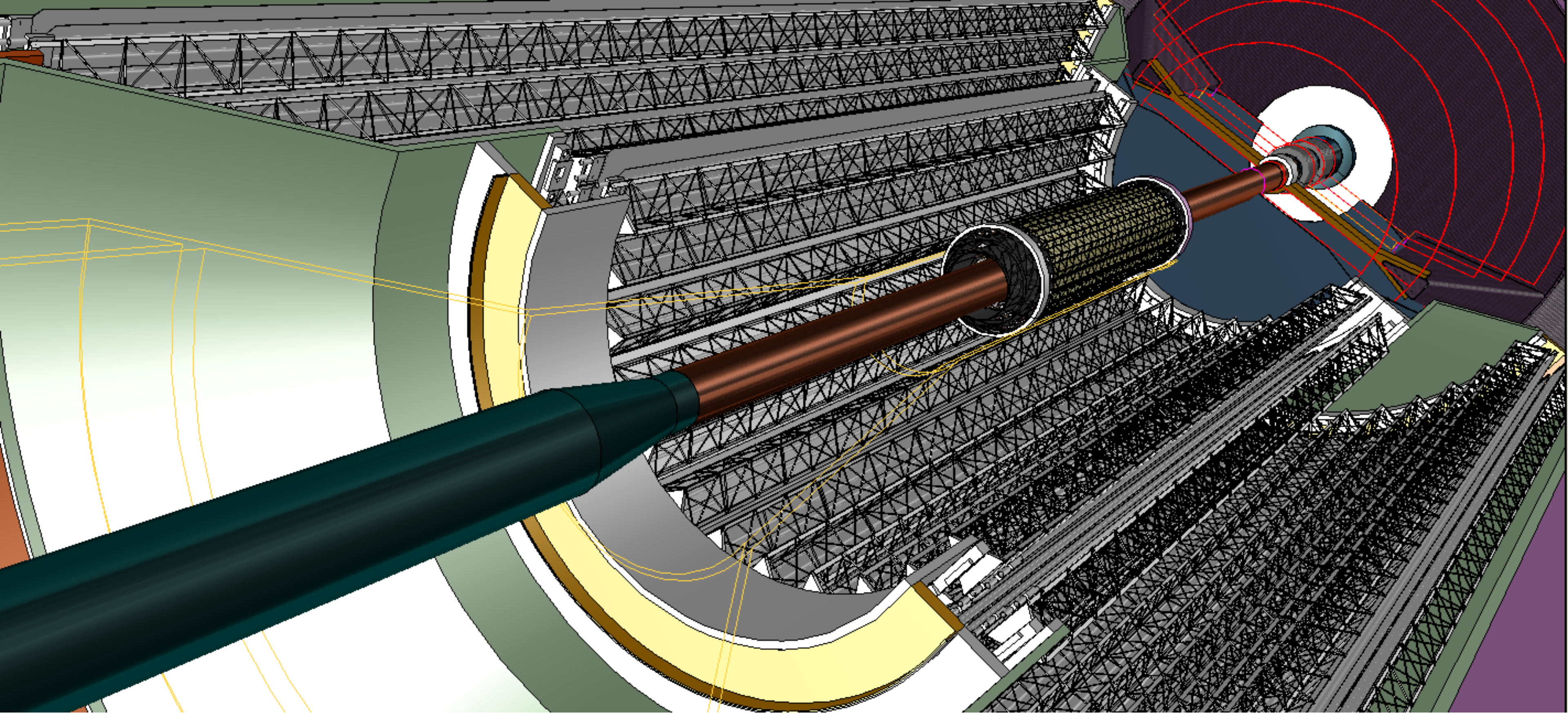
Mean Radius
- R 39.04
- R 31.32
- R 23.35

CMOS Pixel Sensors









Inner Barrel (IB): 3 layers pixels

Radial position (mm): 22,28,36

Length in z (mm): 270

Nr. of modules: 12, 16, 20

Nr. of chips/module: 9

Nr. of chips/layer: 108, 144, 180

Material thickness: ~ 0.3% X_0

Throughput: < 200 Mbit / sec•cm^2

Outer Barrel (OB): 4 layers pixels

Radial position (mm): 200, 220, 410, 430

Length in z (mm): 843, 1475

Nr. of modules: 48, 52, 96, 102

Nr. of chips/module: 56, 56, 98, 98

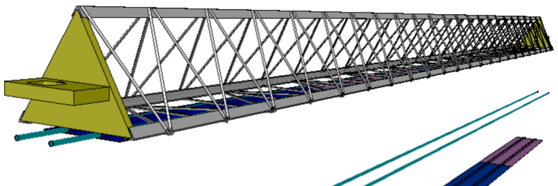
Nr. of chips/layer: 2688, 2912, 9408, 9996

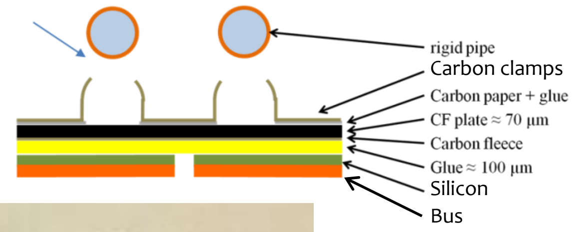
Material thickness: ~ 0.8% X_0

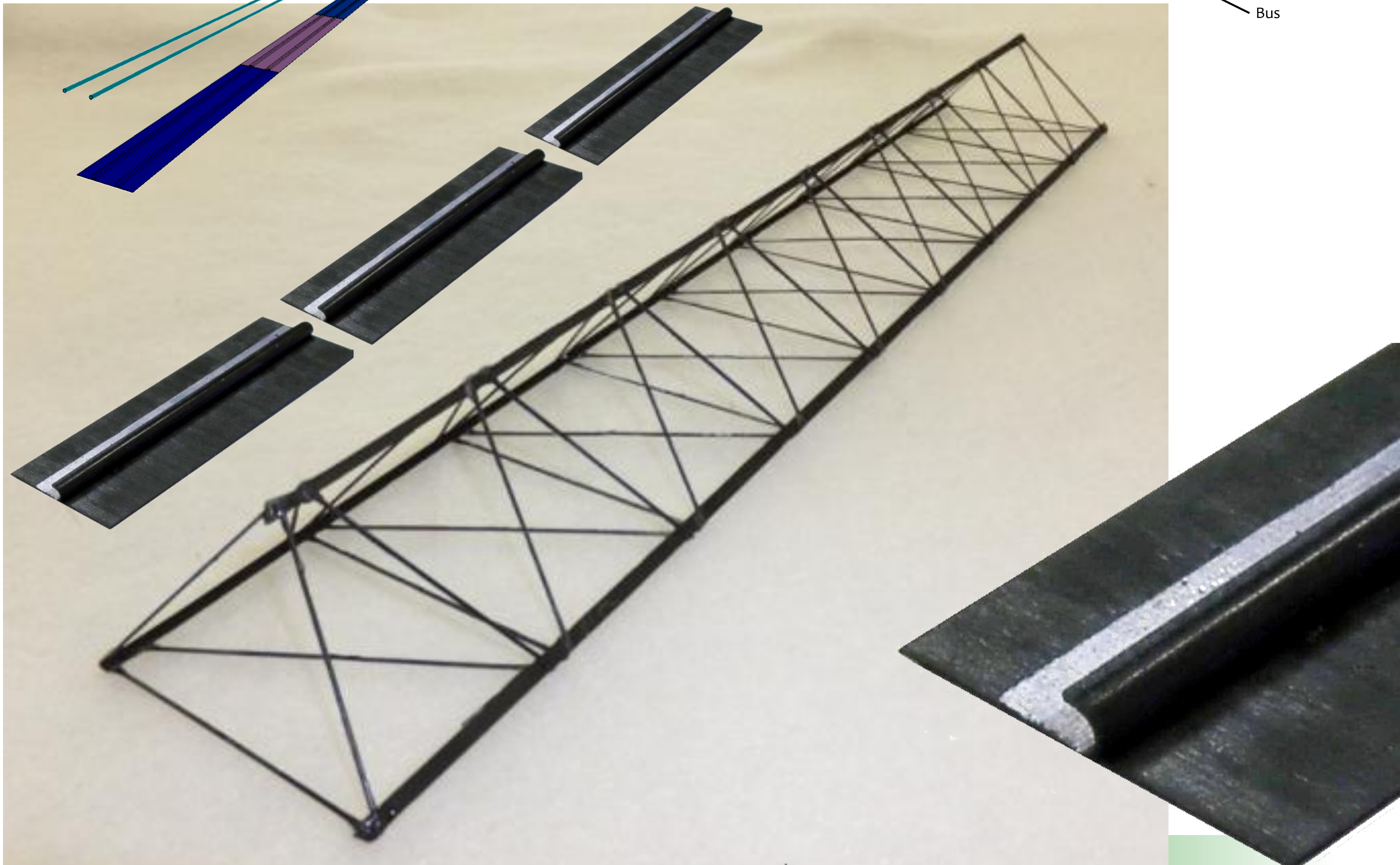
Throughput: < 6 Mbit / sec•cm^2

PROTOTYPE

CLAMP







Chip aligner and gluing machine