

Pixel sensor for ALICE ITS upgrade & CIS

Y. Kwon
(Yonsei Univ.)



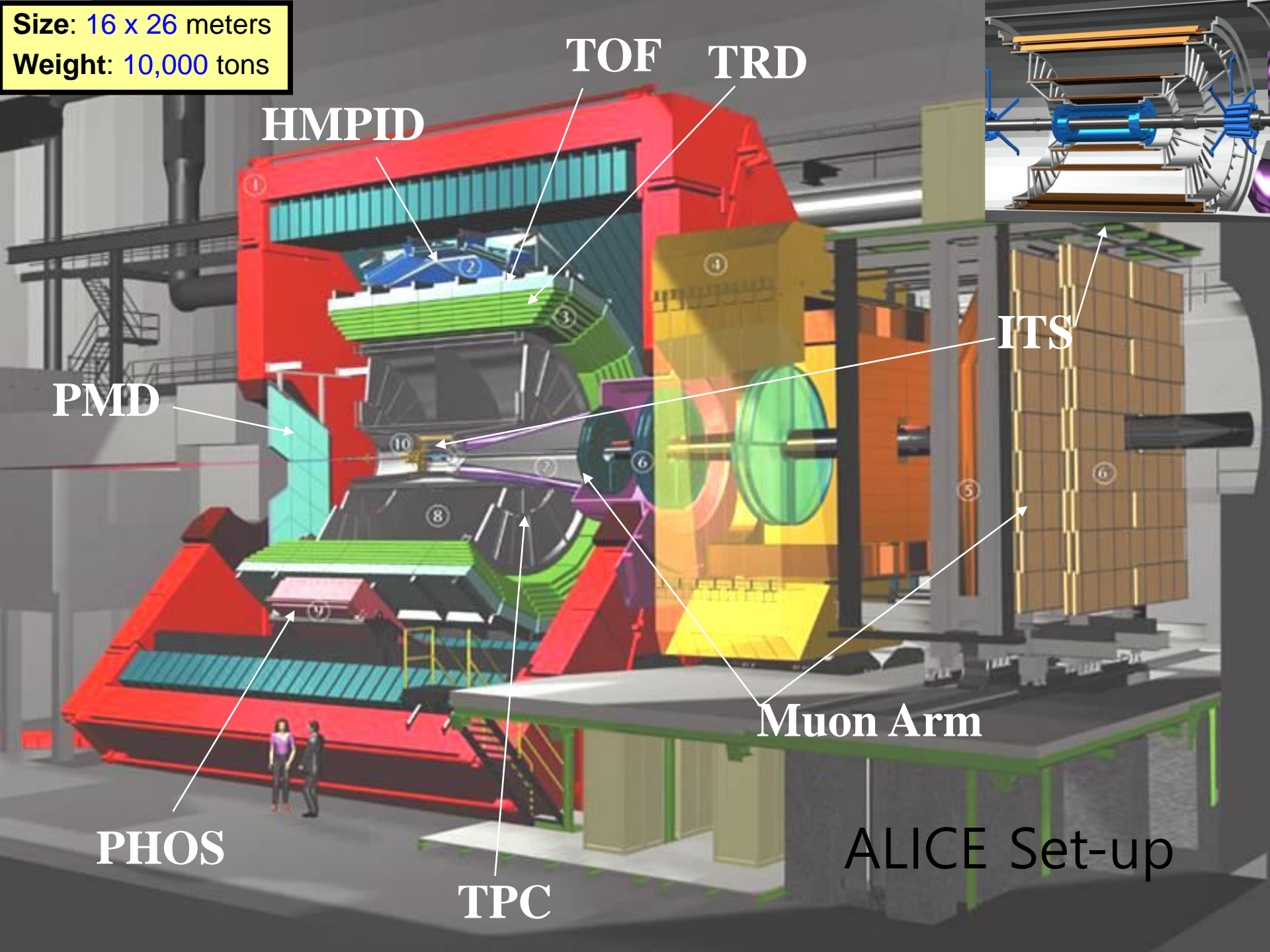
LHC

ALICE

NA

SPS

Size: 16 x 26 meters
Weight: 10,000 tons



TOF

TRD

HMPID

PMD

ITS

Muon Arm

PHOS

TPC

ALICE Set-up

ALICE (Participation)

35 countries, 120 institutes, 1300 members

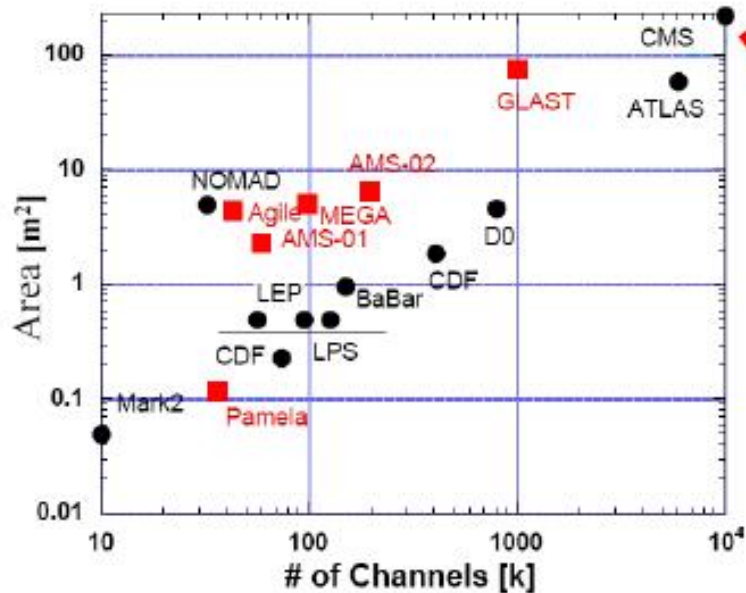
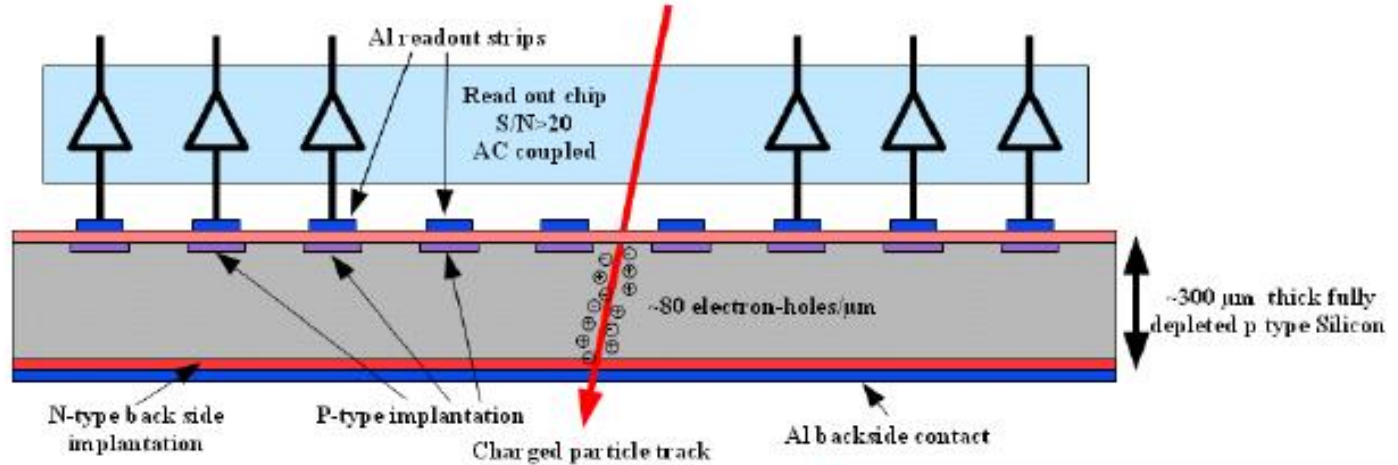


A possibility in Korea

Si sensor in general

- Mature technology
- Reliable performance
- Fine granule
- Higher energy and time resolution (than gaseous ionization detectors)
- Key burden is cost.

Microstrip silicon sensors in particle physics: a success story!



CMS Silicon Inner Tracker:
223 square meters of silicon!!!



Typical PIN-type Si sensor

R&D environment



6 inch fabrication line



8 inch fabrication line

MEMORANDUM

- (1) Youngil Kwon, Mann-Ho C
- (2) Edward Kistenev, Andrey S
- (3) John Lajoie, Physics and As
- (4) Yongsun Yoon, BT division,
- (5) Kwun-bum Chung, Electrop
- (6) Zheng Li, SDDPL, Instrum

- (7) Jinsoo Kim, National Nano

I. Purpose & Scope⁴⁾

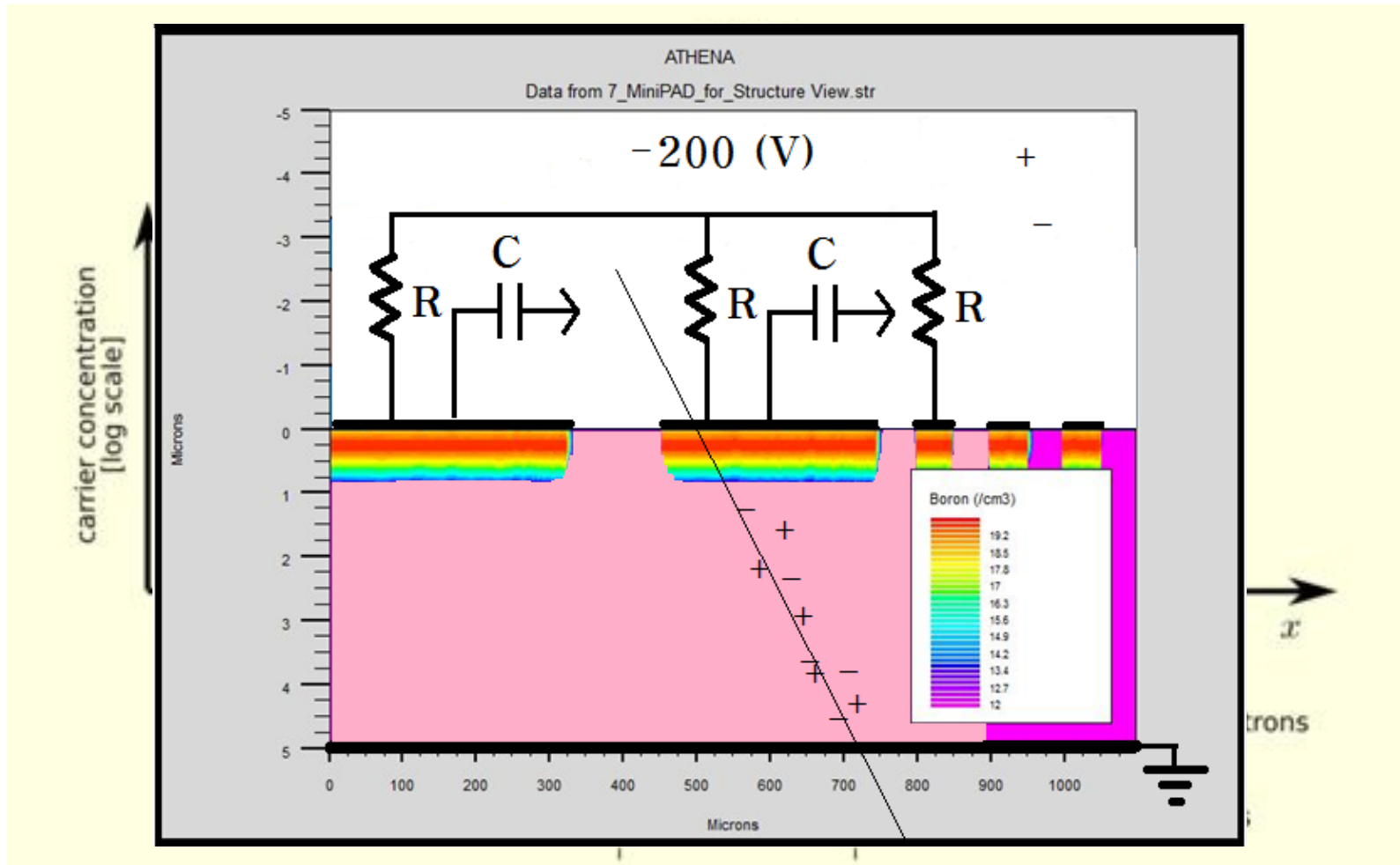
The purpose of this MOU is to... the 'Radiation damage and... planning to contribute their ov... studies. This MOU clarifies the areas of pa... collaborate by sharing their expertise and se... parties for the stated academic goal. ⁴⁾

300 cm² ~ \$ 500 ^{rties will ticipating}

II. Responsibilities Under this MOU⁴⁾

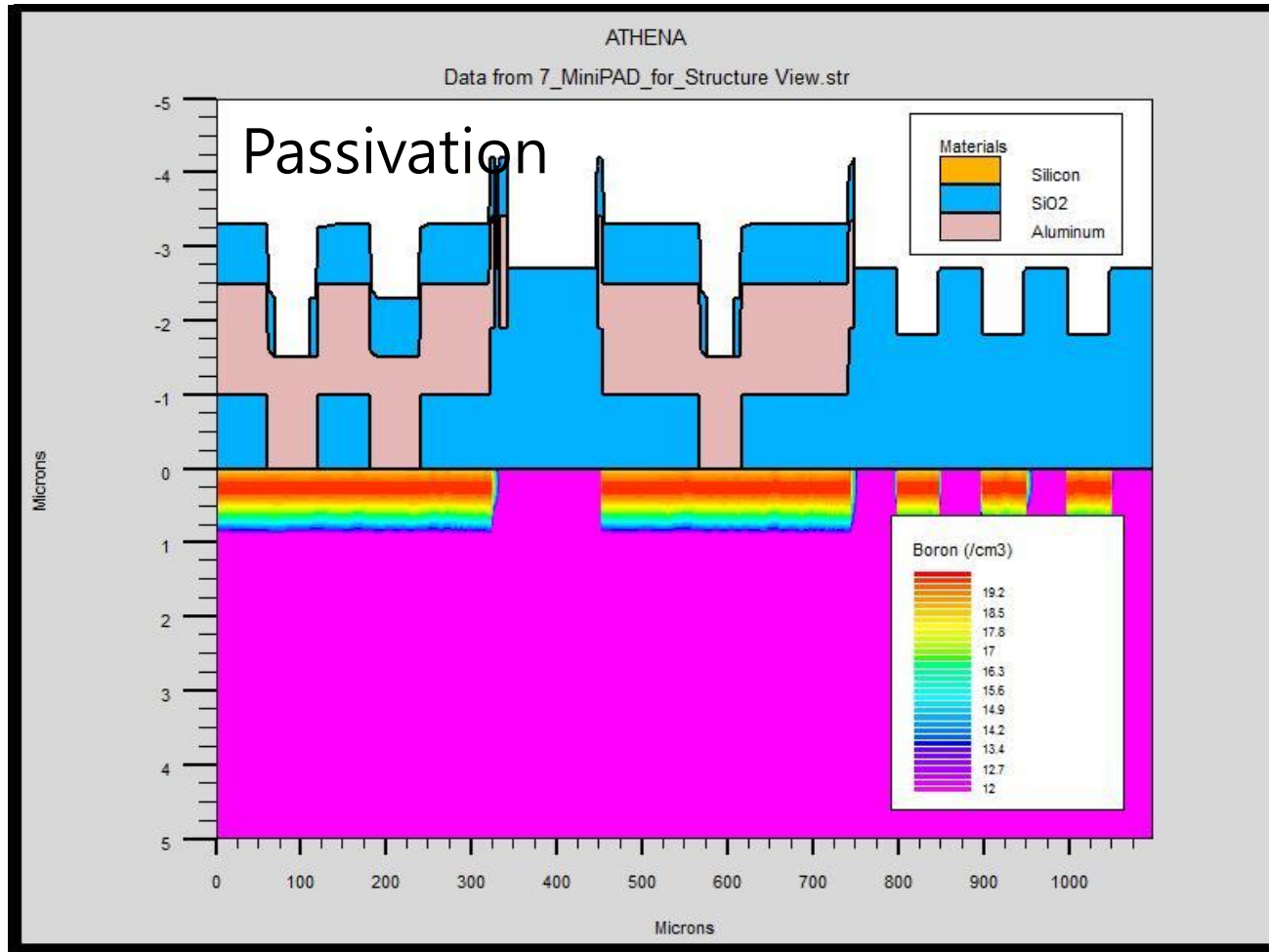
- A. Dr. E. Kistenev, and Prof. J. Lajoie, and Prof. Y. Kwon will propose silicon semiconductor detectors/devices to achieve academic goals in their field of interest in the experimental nuclear and high energy physics.⁴⁾
- B. Dr. Z. Li will design the proposed silicon semiconductor detectors/devices using standards approved by industry for large area radiation hard Si devices and will advise on the radiation induced defects in Si devices. ⁴⁾
- C. Dr. A. Sukhanov will advise on the electronic design and implementation of the readout electronics for silicon semiconductor device testing.⁴⁾
- D. Dr. Yoon will inspect designs of the proposed detectors/devices and advise on matching design ideas to fabrication technologies. He will also perform his own radiation hardness testing of the devices he develops.⁴⁾
- E. Prof. M.-H. Cho, Prof. G. T. Park, and Prof. K. B. Chung will advise on possible defects in silicon sensors/devices and will study radiation defects in the produced sensors/devices exposed to different kinds of radiation.⁴⁾
- F. Mr. Kim, leader of nano|patterning process team in National Nanofab Center, will assist in fabrication of the silicon sensors/devices with university discount program and consult on details of silicon detector/device fabrication process.⁴⁾

Traditional Si sensor operation

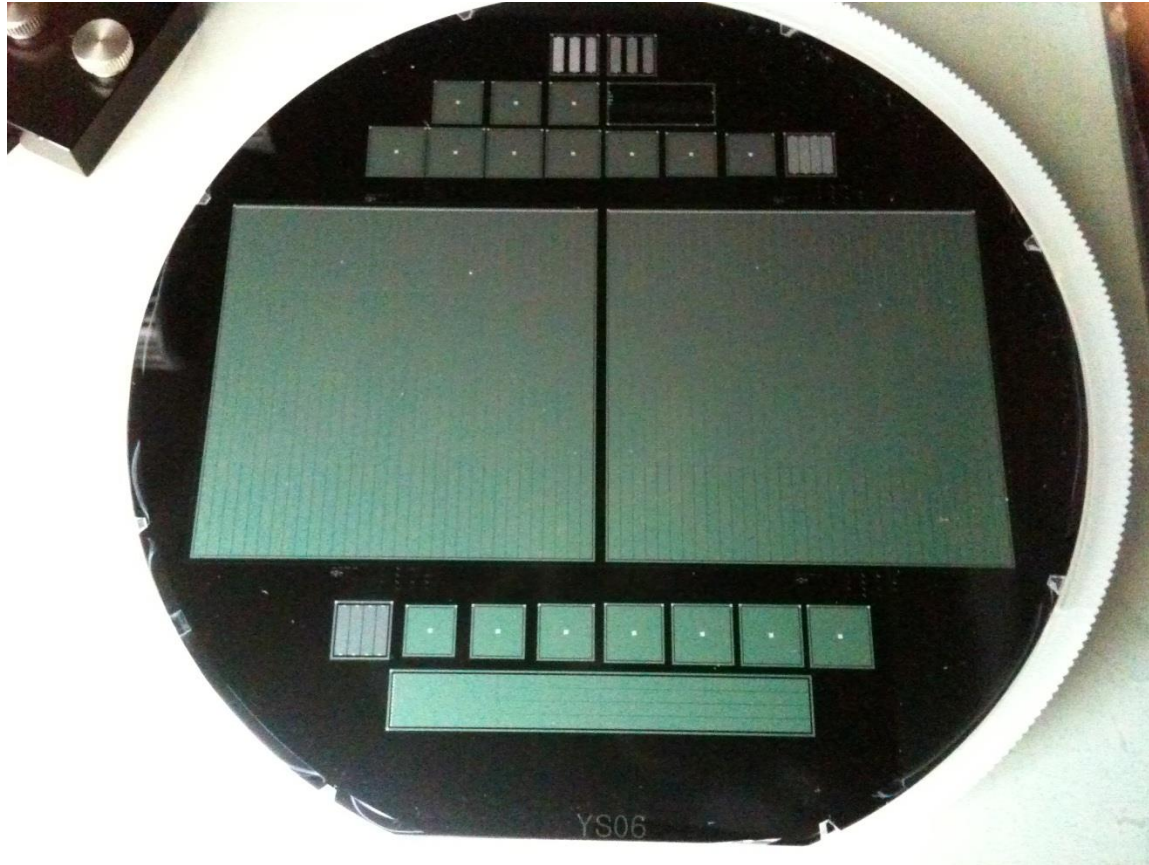


$$d = \sqrt{2\rho\mu\varepsilon(V + V_{bi})}$$

How do we make it? (CMOS process)

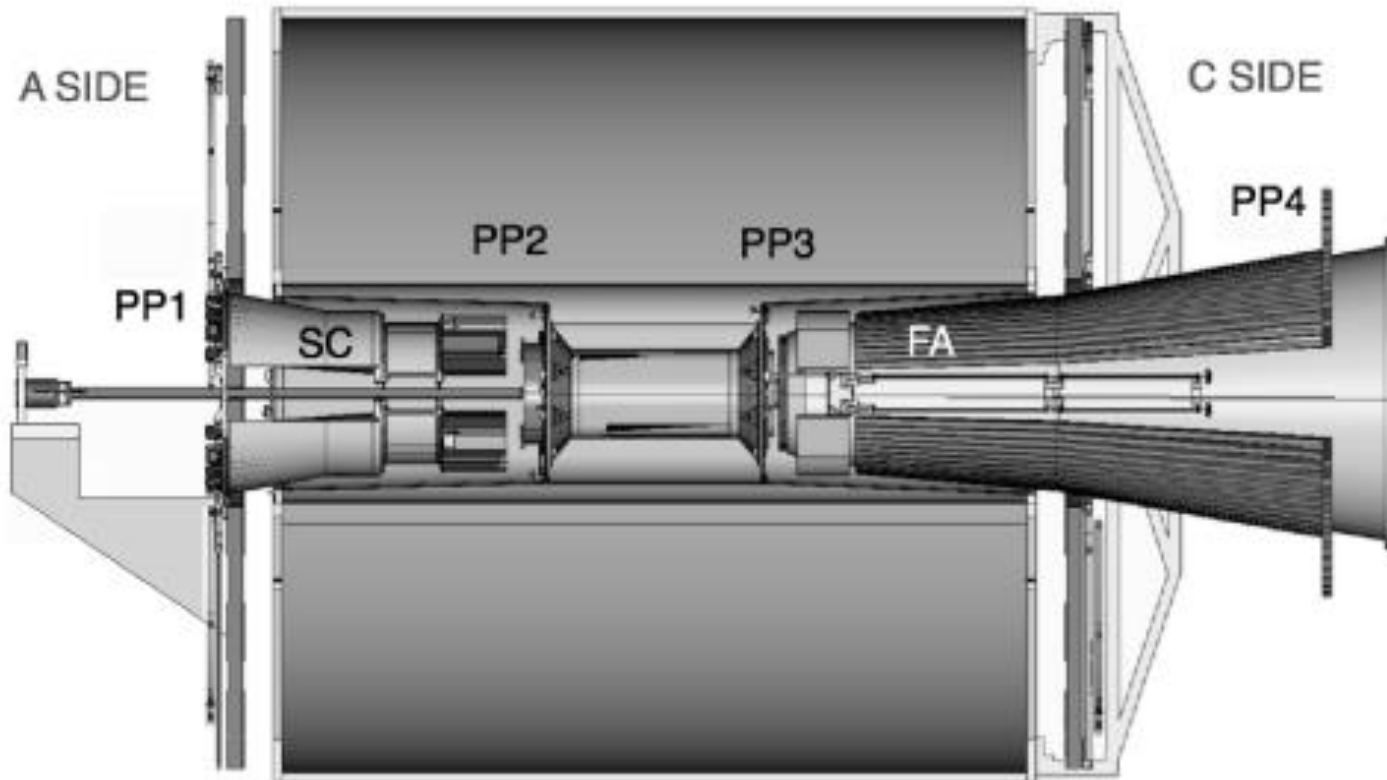


Processed Wafer



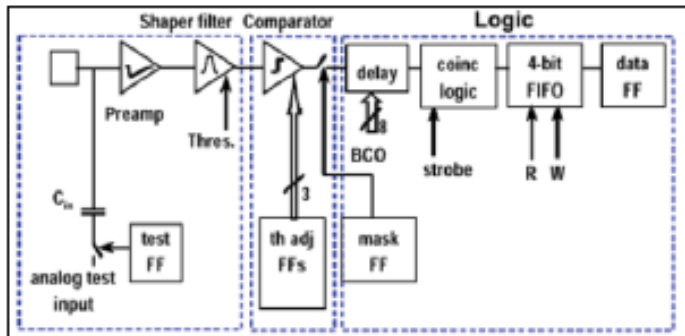
New challenge

Current ALICE ITS



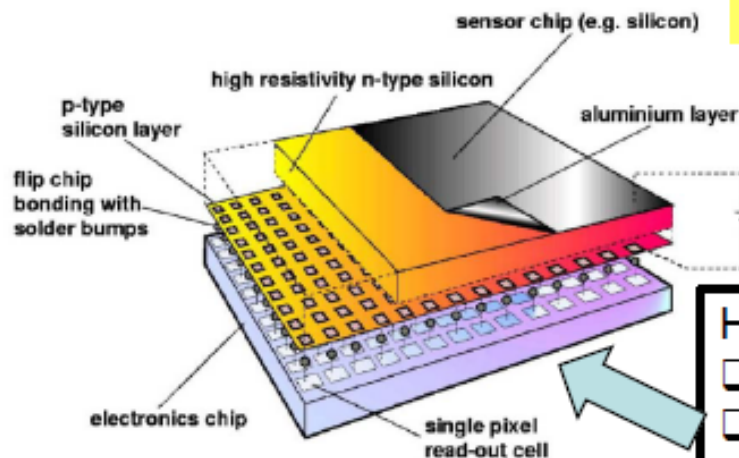
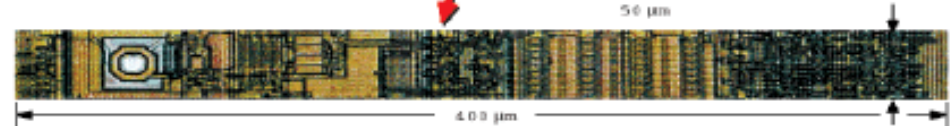
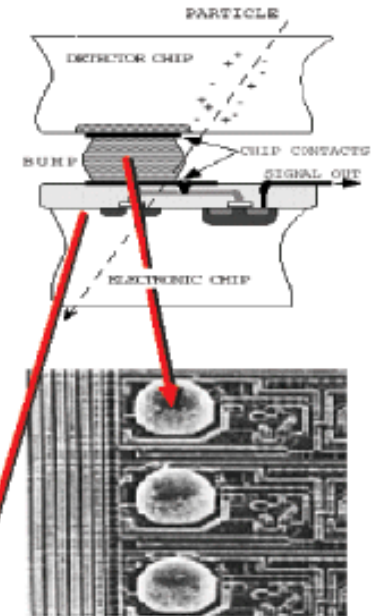
Hybrid pixel for high energy physics application: the **ATLAS** case

ATLAS pixel readout cell



ATLAS pixel structure

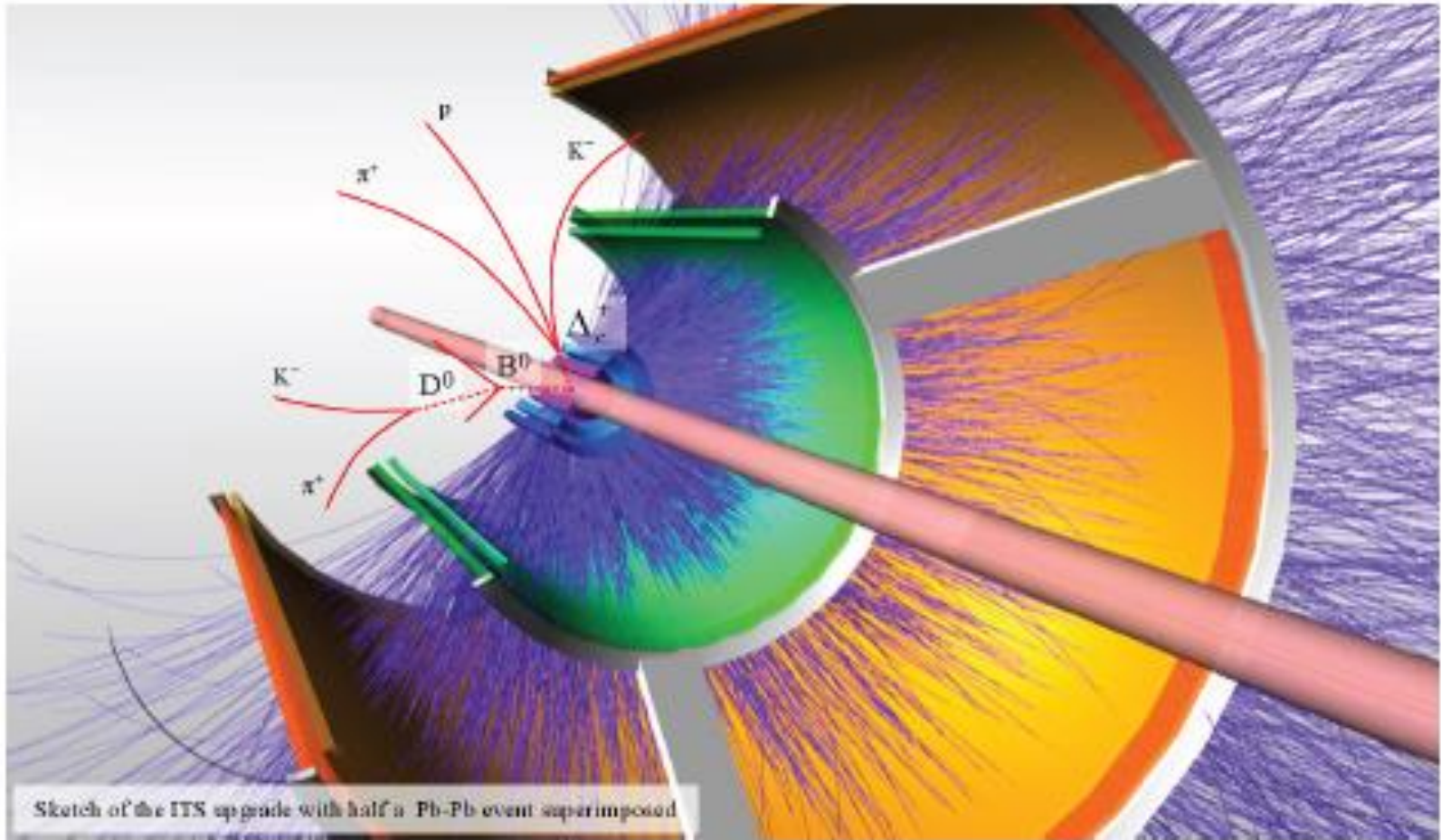
- ❑ Pixel $50\mu\text{m} \times 400\mu\text{m}$
- ❑ fully depleted silicon layer $\sim 300\mu\text{m}$
- ❑ one dedicated readout chip with complex architecture possible
- ❑ pixel pitch limited by bump bonding



Hybrid pixel general structure:

- ❑ sensor layer (detector grade fully depleted silicon)
- ❑ bump bonding ($50\mu\text{m}$ pitch)
- ❑ read out chip (standard ASIC chip)

ALICE ITS Upgrade



Main Physics Goal

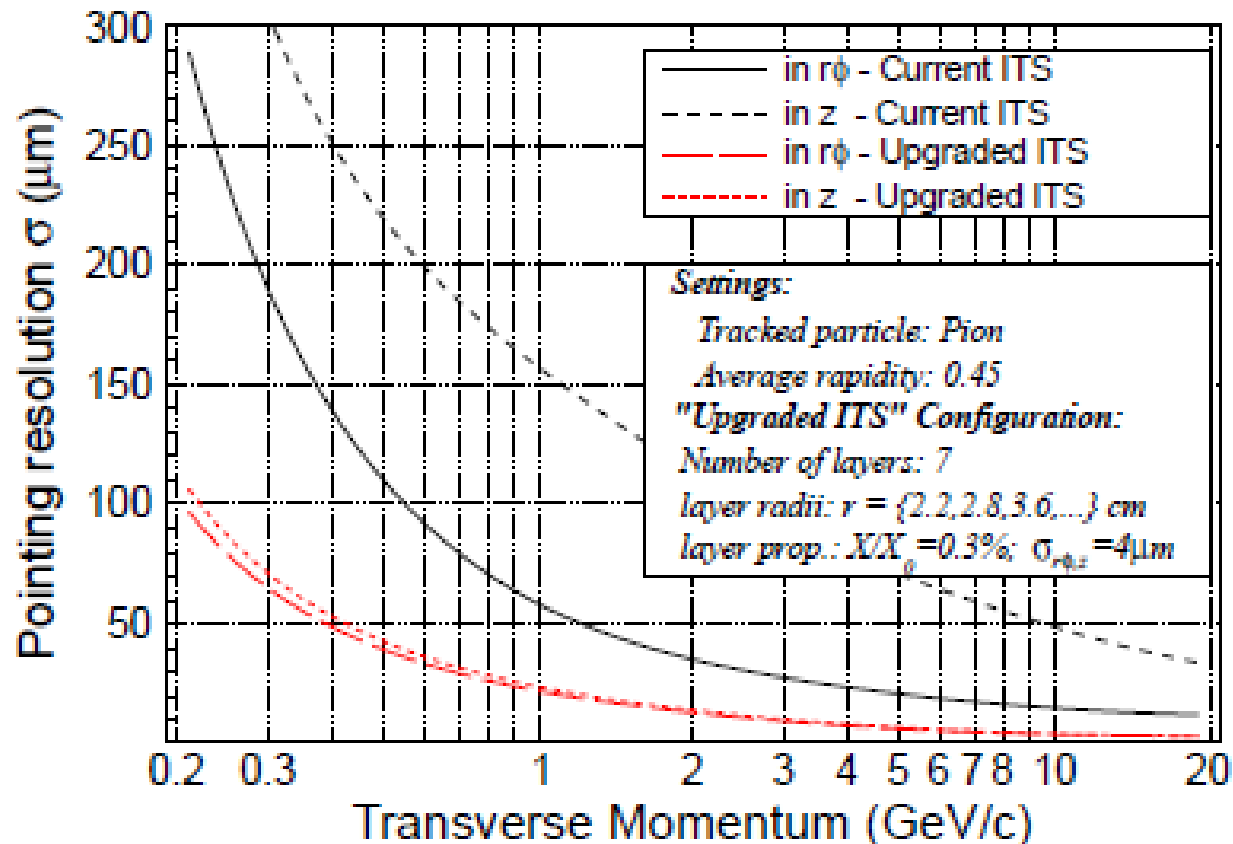
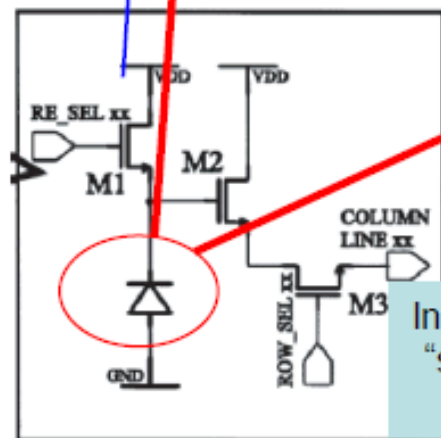
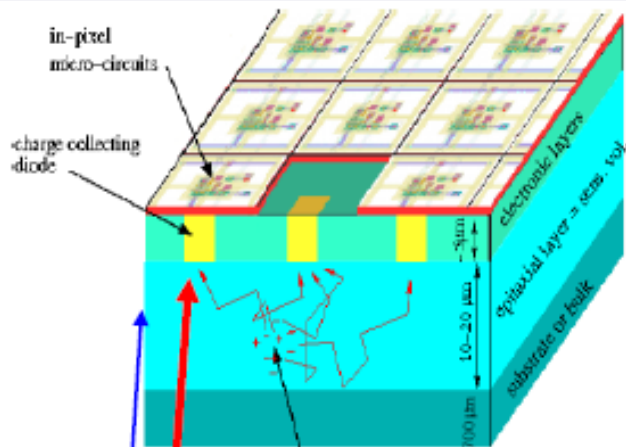


Figure 2.10: Track impact parameter resolution in $r\phi$ and z (current and upgrade).

The MIMOSA (Minimum Ionizing MO nolithic Active pixel Sensors) idea

Working principle: Use of the epitaxial layer of **STANDARD CMOS** microelectronic processes as detecting sensitive volume.

R. Turchetta, et al. , "A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology", NIM A 458 (2001) 677-689



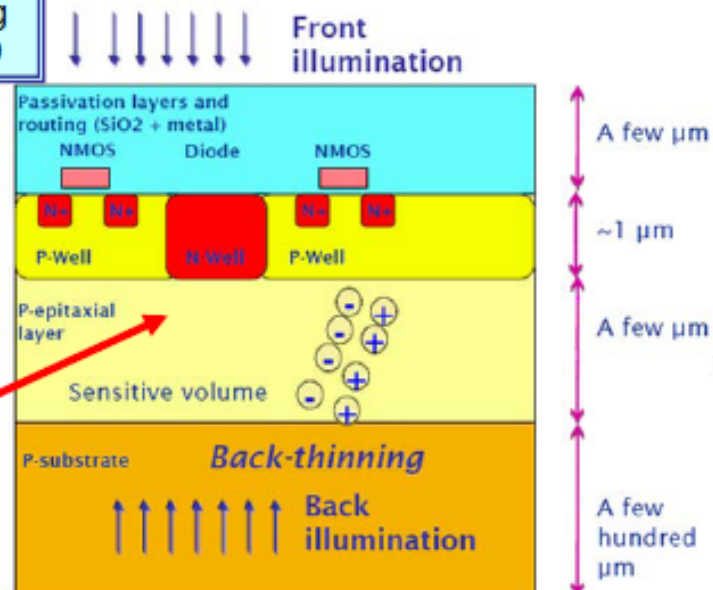
In pixel 3 transistor "standard" MAPS configuration

Recombination time:

$\sim 1 \mu s$

$\sim 10 \mu s$

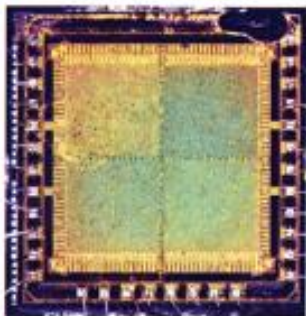
$\sim 10 ns$



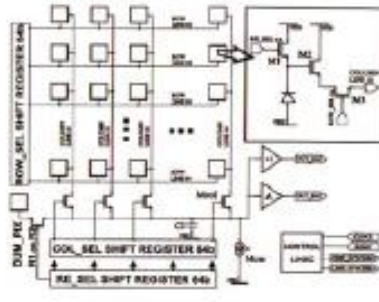
- ❑ small signal $\sim 80 \text{ e-h}/\mu\text{m}$, epi 2-14 μm
- ❑ **Undepleted** detecting volume, charge collected by diffusion and **not** by drift, cluster size $\sim 50\text{-}100 \mu\text{m}$, collection time $\sim 150 \text{ ns}$
- ❑ 3T basic readout allows noise: $\sim 15\text{-}20$ electrons
- ❑ **only N-MOS** transistors allowed in pixel area
- ❑ easy access to technology through multiproject runs: $\sim 5\text{-}50 \text{ Keuro}$

First MIMOSAs implementation (IreS and LEPSI, IN2P3/ULP), Strasburgo, (2001)

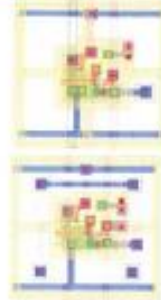
Mimosa I



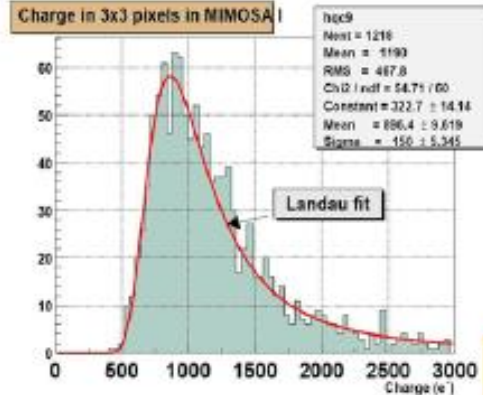
MIMOSA I die photo



MIMOSA I block schematic diagram



MIMOSA I pixels layouts



- standard 0.6 μ m CMOS (t_{ox} =12.7nm)
- 14 μ m thick EPI layer (10^{15} cm $^{-3}$)
- 4 arrays 64x64 pixels
- pixel pitch 20x20 μ m 2
- diode (nwell/p-epi) size 3x3 μ m 2 - 3.1fF
- serial analogue readout
- max. clock freq.: 5MHz
- die size 3.6x4.2mm 2
- technology 3M+2P
- power supply 5V

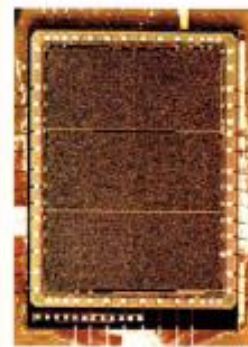
Signal-to-noise (mean):

MIMOSA I: 1 diode	42
4 diodes	32
MIMOSA II: 1 diode	21

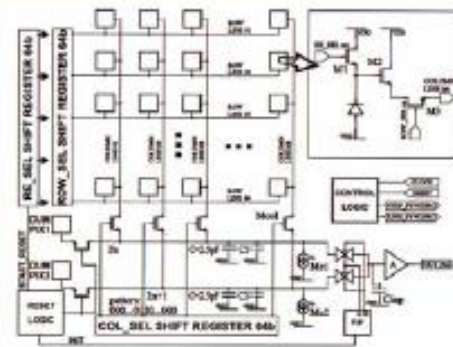
Efficiency (%)

MIMOSA I: 1 diode	99.5 +/- 0.2
MIMOSA I: 4 diodes	99.2 +/- 0.2
MIMOSA II: 1 diode	98.5 +/- 0.3

Mimosa II



MIMOSA II die photo



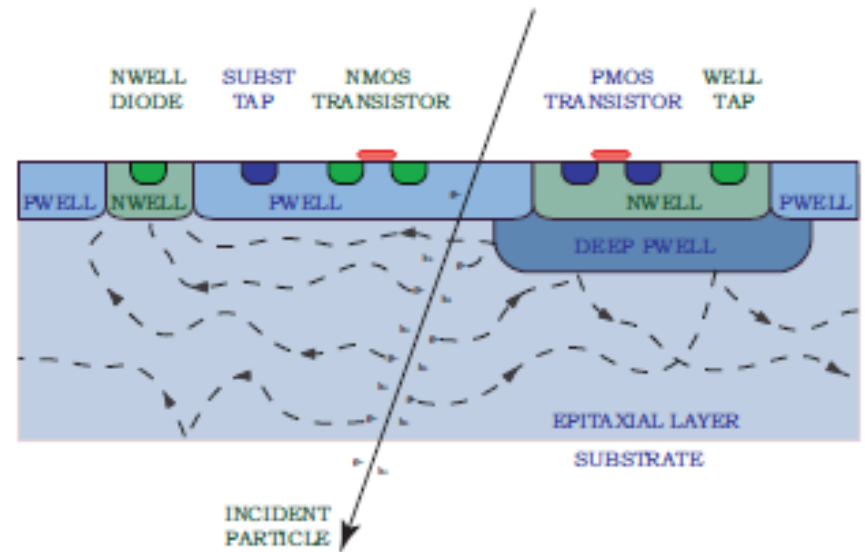
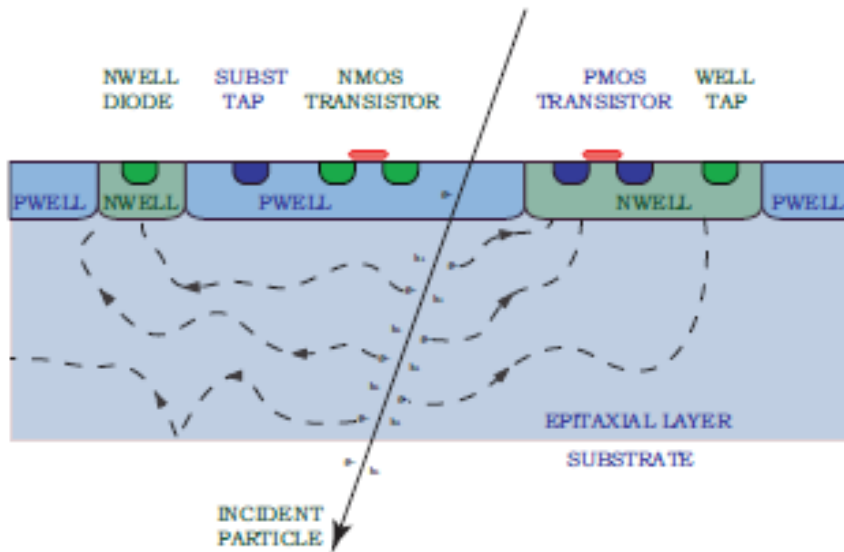
MIMOSA II block schematic diagram



MIMOSA II pixels layouts

- standard 0.35 μ m CMOS (t_{ox} =7.4nm)
- 4.2 μ m thick EPI layer (10^{15} cm $^{-3}$)
- 6 arrays 64x64 pixels
- pixel pitch 20x20 μ m 2
- diode (nwell/p-epi) size 1.7x1.7 μ m 2 - 1.65fF
- serial analogue readout
- max. clock freq.: 25MHz
- die size 4.9x3.5mm 2
- technology 5M+2P
- power supply 3.3V
- radiation tolerant
- transistor design

Sensor + Digitization



Samsung S5K8AA

Ultra thin HD image sensor for compact mobile application

HD 1/8" 1.4um BSI Pixel Image Sensor provides;

- HD sensor integrated Image Signal Processor suitable for slim mobile phone, tablet and notebook
- High speed HD 30fps and VGA 60fps
- BSI sensors providing clear and sharp still images in low light, YSNR10 86 Lux



SK하이닉스 M8라인, 시스템반도체 전환 완료

애플을 최대 고객사로 확보

서울시민신문



<http://www.seoulnewspaper.com>

▲ SK하이닉스 M8라인. © 서울시민신문

SK하이닉스가 청주 M8 라인을 거점으로 시스템반도체 생산을 본격화했다.

10월 25일 유경동 SK하이닉스 상무는 '국제반도체컨퍼런스 2012'에서 청주 소재의 자사 M8 공장을 메모리에서 시스템반도체로의 전환 작업을 성공적으로 끝냈다고 밝혔다.

M8 공장은 CMOS 이미지 센서(CIS)와 DDI, 전력반도체(PMIC), 고주파(RF), 메모리 반도체를 생산한다. CIS의 경우 90나노미터(nm) 공정 기반으로 터치스크린과 드라이버칩



CIS (CMOS Image Sensor) | SPECIALIZED FOUNDRY

Design Toolkits, 웨이퍼 가공, 패키지, 테스트 등 턴키 서비스 제공



CMOS 이미지 센서는 렌즈를 통해 들어오는 빛을 전기적 신호로 전환하는 디지털 제품의 핵심 부품으로, 저전력·초소형·저비용이라는 제품의 특성 때문에 캠코더, 디지털 카메라, PC용 카메라, 이동전화, PDA, 스캐너, 팩스 등에 널리 쓰이는 등 제품의 수요가 급증하고 있는 첨단 기술 분야입니다.

동부하이텍은 국내외 Fabless 등 고객사들에게 보다 저렴한 비용과 편리한 서비스를 제공하기 위해 CIS 제품 개발에 필요한 디자인 툴킷(Design Toolkits)을 제공하고 있으며, 웨이퍼 제조공정, 패키지, 테스트 등 이미지 센서 양산에 필요한 모든 공정들을 일괄적으로 서비스하고 있습니다.

동부하이텍이 제공하는 CIS(CMOS Image Sensor)기술은 0.18 μ m 와 0.13 μ m급 기술을 기반으로 하고 있으며, CIS 공정기술의 경우 N+/PW Photo Diode와 Color Filter, Microlens 등을 제공하여 CIF, VGA, Mega-Pixel 등 다양한 형태의 CIS 칩을 양산하고 있습니다.

As of now

- Would it work?
 - In physics?... ITS upgrade is approved and is also top priority.
 - Technically?... Probably, R&D might be initiated.
 - Financially?
 - Politically?