Pixel sensor for ALICE ITS upgrade & CIS

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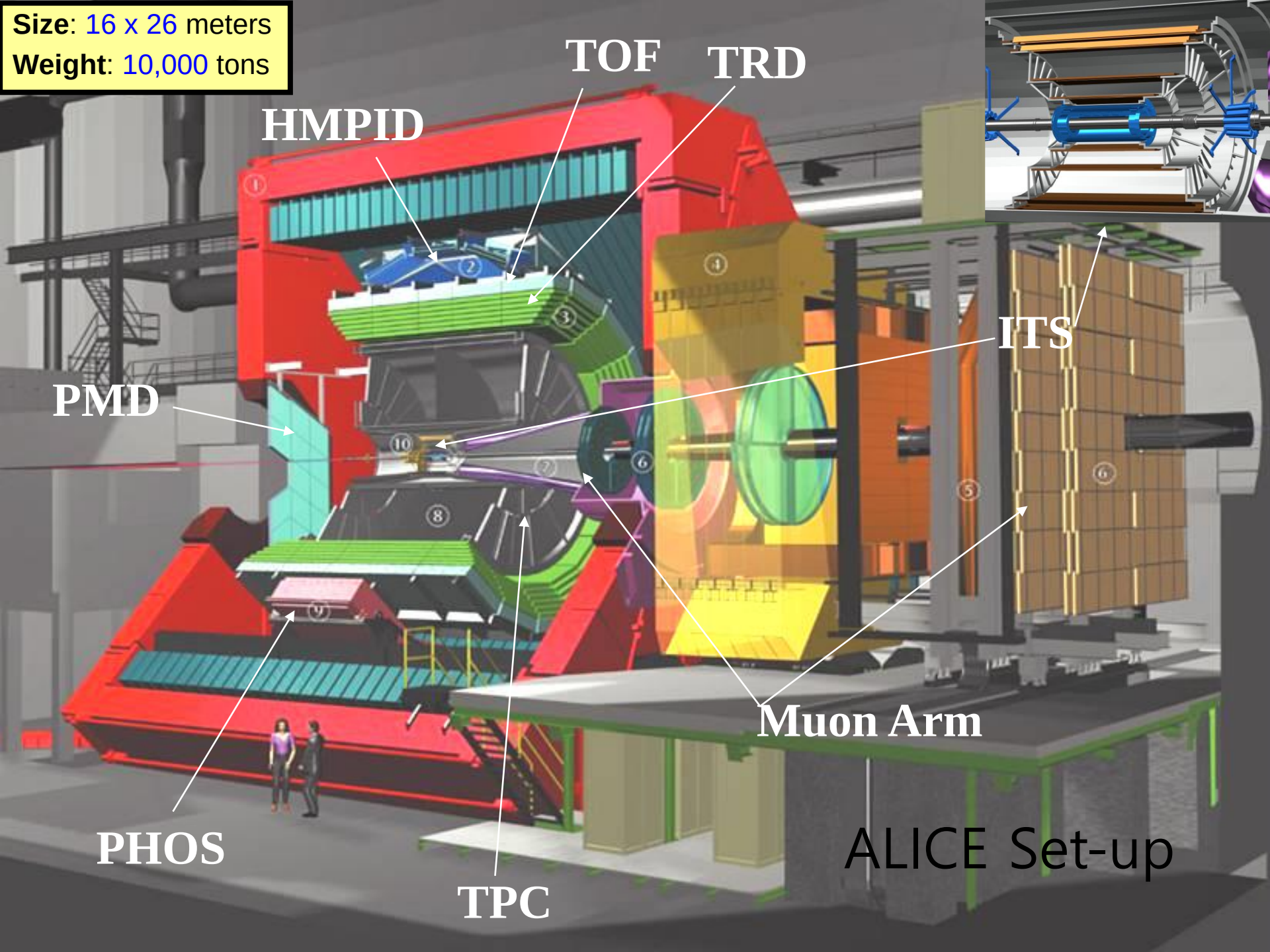
(Yonsei Univ.)


NA
LHC
SPS
ALICE


Size: 16 x 26 meters
Weight: 10,000 tons
TOF
TRD
HMPID
ITS
PMD
Muon Arm
PHOS
TPC
ALICE Set-up

ALICE
(Participation)

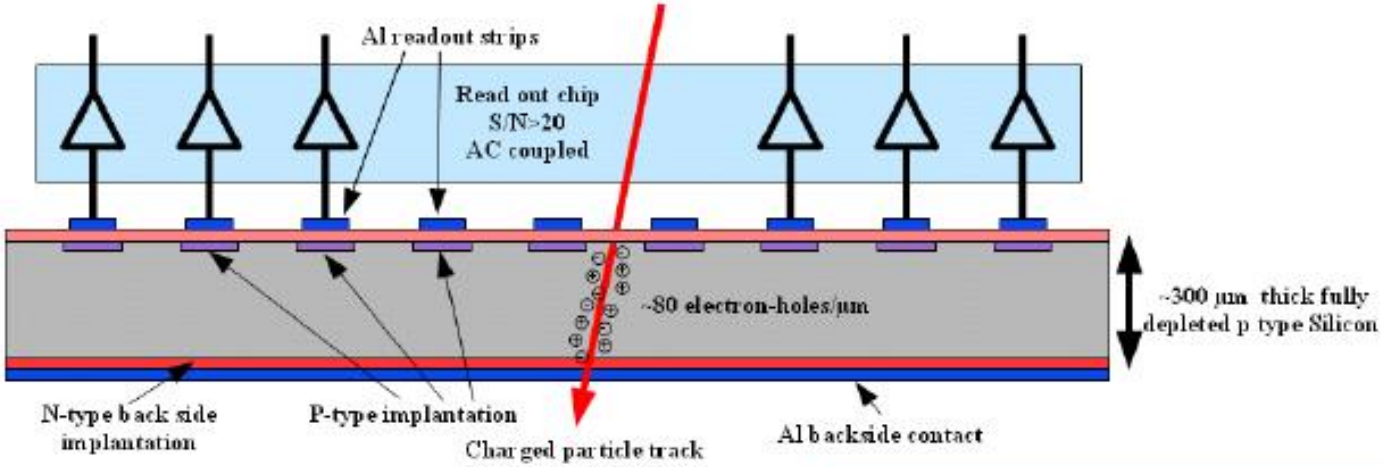
35 countries, 120 institutes, 1300 members

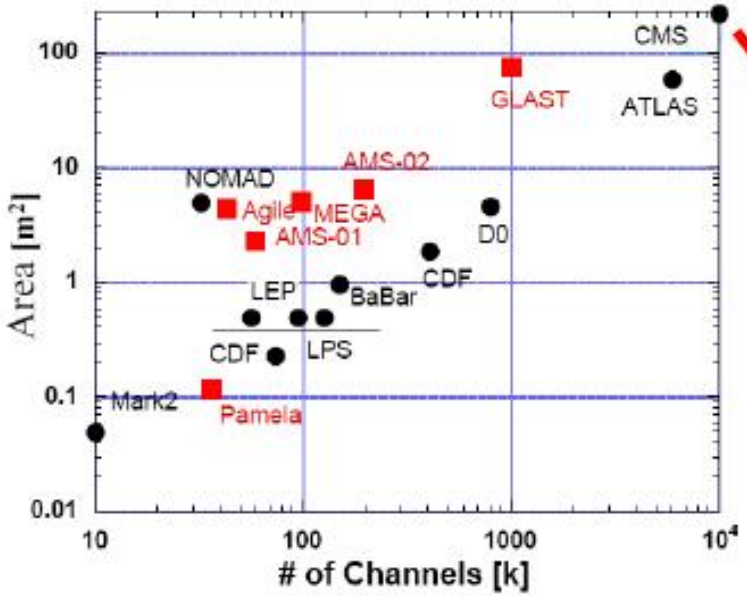
A possibility in Korea

Si sensor in general

- Mature technology
- Reliable performance
- Fine granule
- Higher energy and time resolution (than gaseous ionization detectors)
- Key burden is cost.

Microstrip silicon sensors in particle physics: a success story!



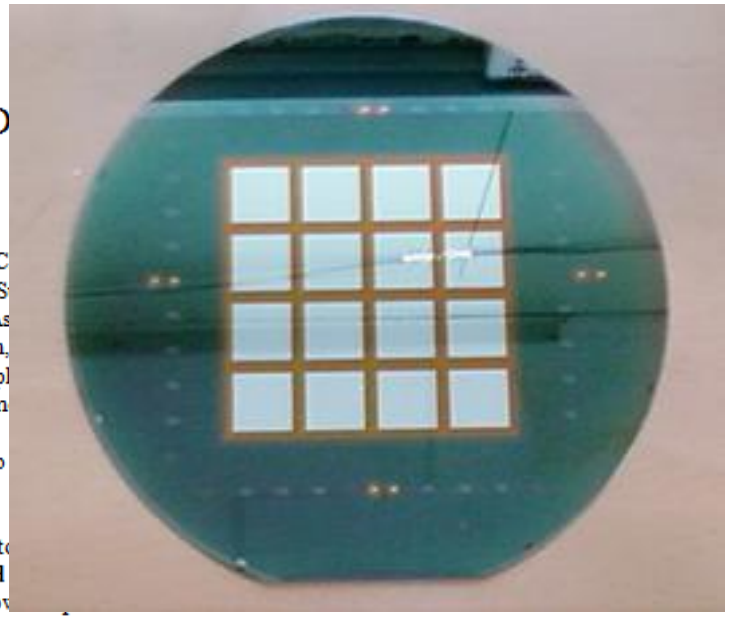


CMS Silicon Inner Tracker:
223 square meters of silicon!!!

Typical PIN-type Si sensor

R&D environment

6 inch fabrication line



300 cm^2 ~ $ 500

8 inch fabrication line

MEMORAND

(1) Youngil Kwon, Mann-Ho C
(2) Edward Kistenev, Andrey S
(3) John Lajoie, Physics and As
(4) Yongsun Yoon, BT division,
(5) Kwun-bum Chung, Elecropl
(6) Zheng Li, SDDPL, Instrum

(7) Jinsoo Kim, National Nano

I. Purpose & Scope

The purpose of this MOU is t
the '**Radiation damage and**
planning to contribute their ov
studies. This MOU clarifies the areas of pa rties will
collaborate by sharing their expertise and se ticipating
parties for the stated academic goal.

II. Responsibilities Under this MOU

A. Dr. E. Kistenev, and Prof. J. Lajoie, and Prof. Y. Kwon will propose silicon semiconductor detectors/devices to achieve academic goals in their field of interest in the experimental nuclear and high energy physics.

B. Dr. Z. Li will design the proposed silicon semiconductor detectors/devices using standards approved by industry for large area radiation hard Si devices and will advice on the radiation induced defects in Si devices.

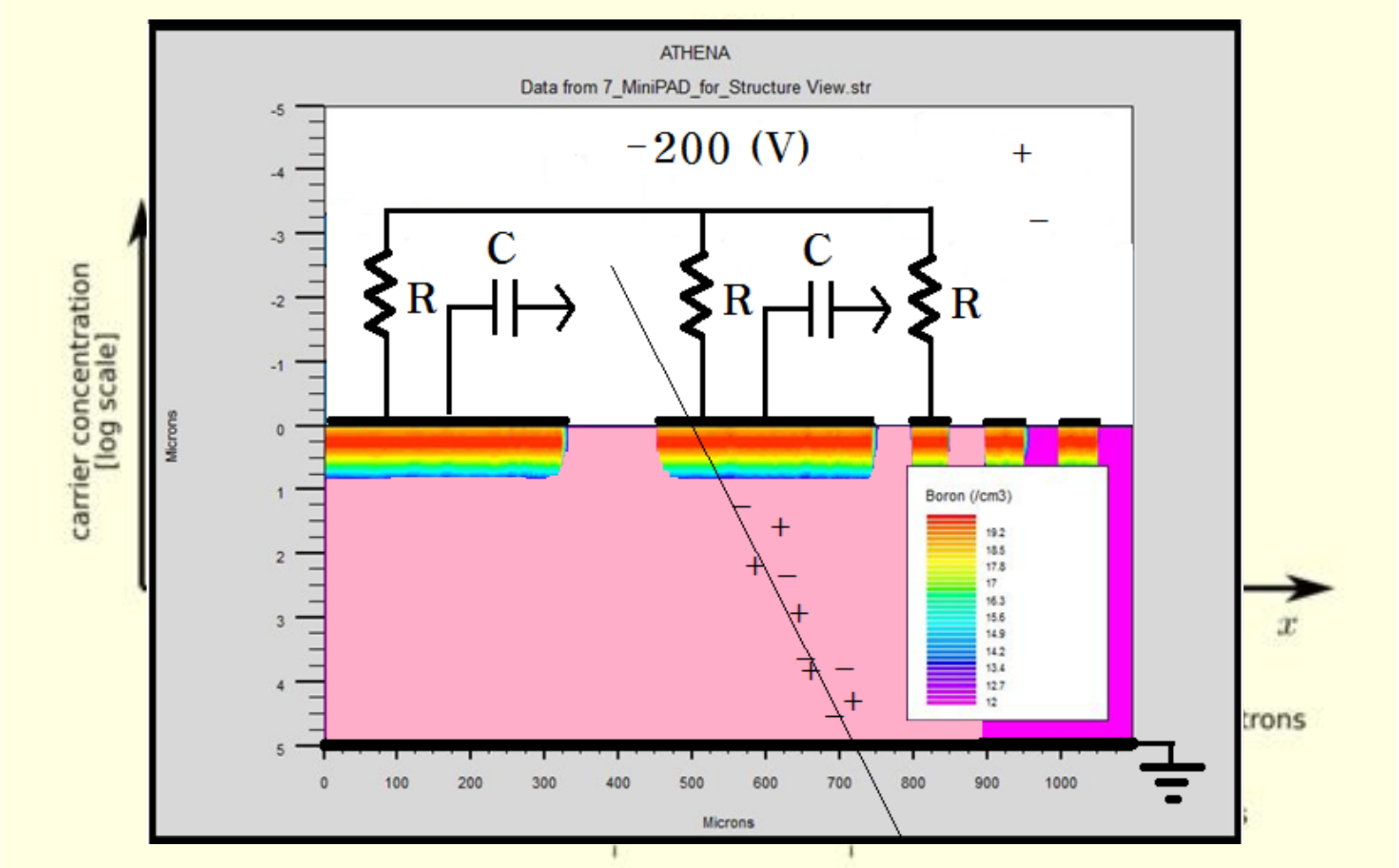
C. Dr. A. Sukhanov will advice on the electronic design and implementation of the readout electronics for silicon semiconductor device testing.

D. Dr. Yoon will inspect designs of the proposed detectors/devices and advise on matching design ideas to fabrication technologies. He will also perform his own radiation hardness testing of the devices he develops.

E. Prof. M.-H. Cho, Prof. G. T. Park, and Prof. K. B. Chung will advise on possible defects in silicon sensors/devices and will study radiation defects in the produced sensors/devices exposed to different kinds of radiation.

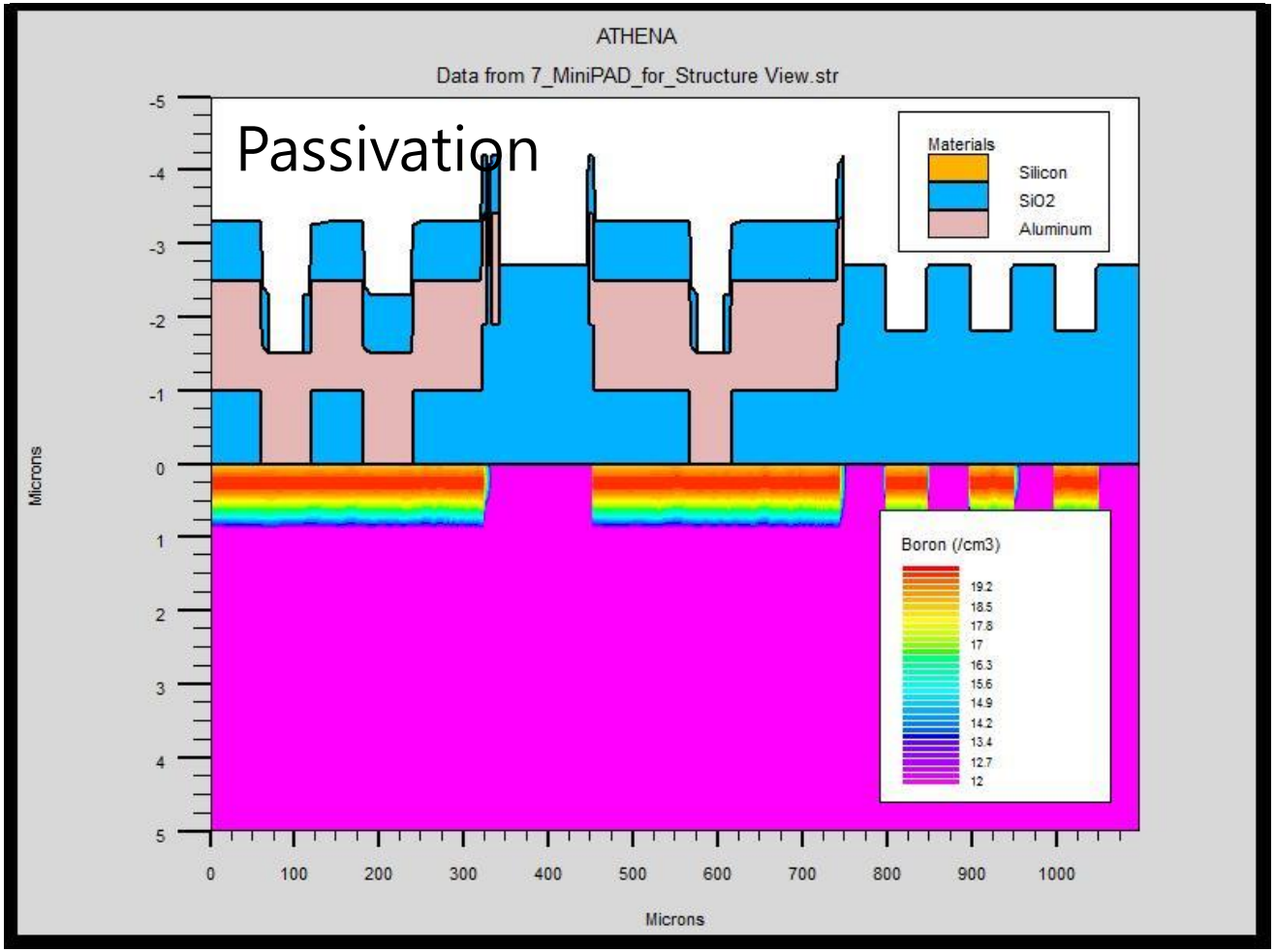
F. Mr. Kim, leader of nano patterning process team in National Nanofab Center, will assist in fabrication of the silicon sensors/devices with university discount program and consult on details of silicon detector/device fabrication process.

Traditional Si sensor operation

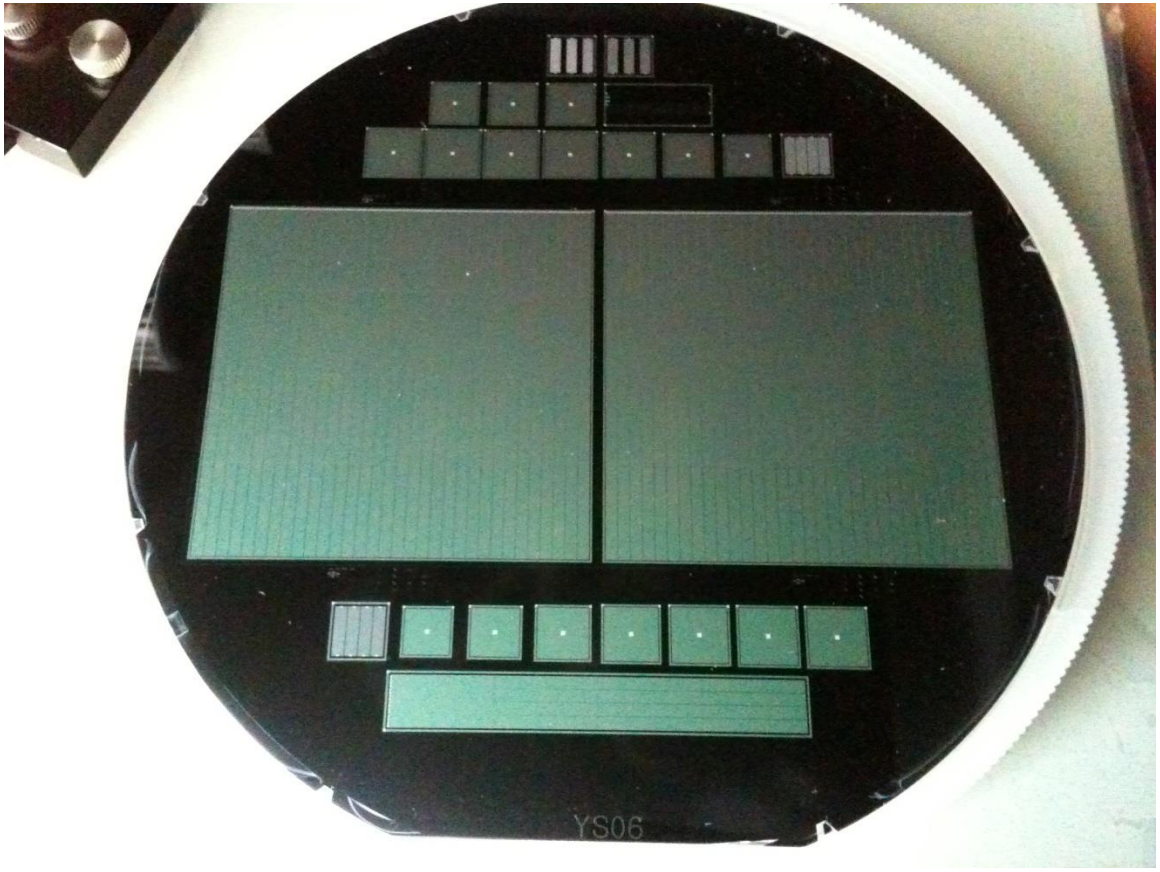


$$d = \sqrt{2\rho\mu\varepsilon\left(V + V_{bi}\right)}$$

How do we make it? (CMOS process)

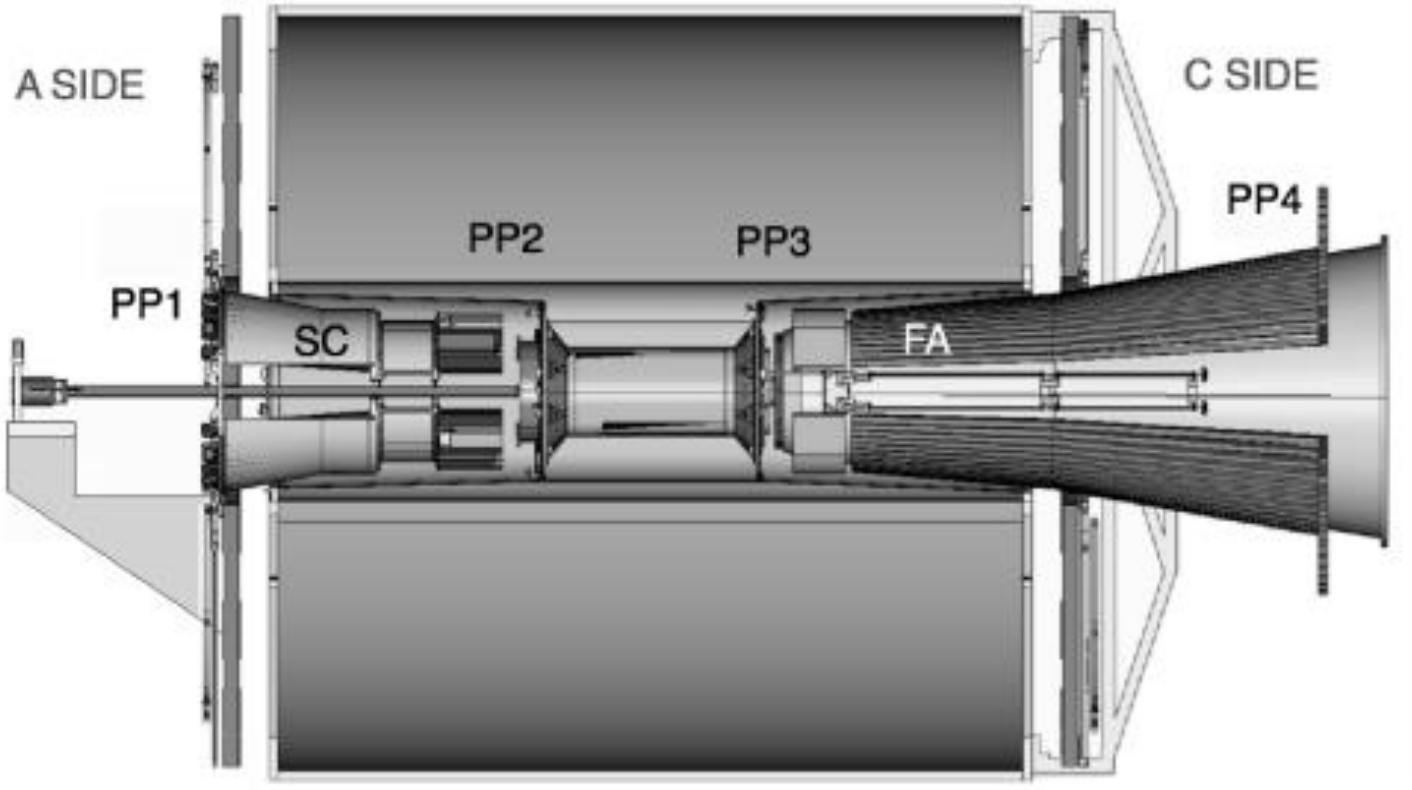


Processed Wafer



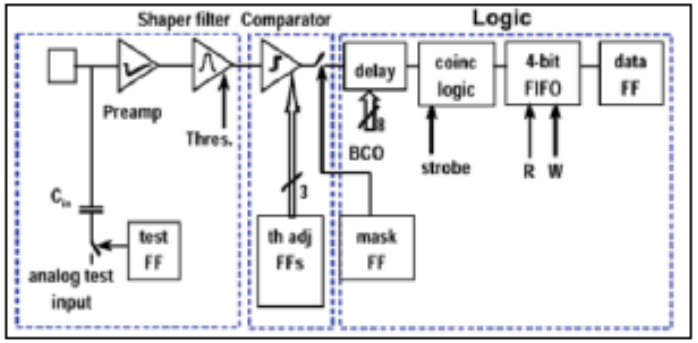
New challenge

Current ALICE ITS



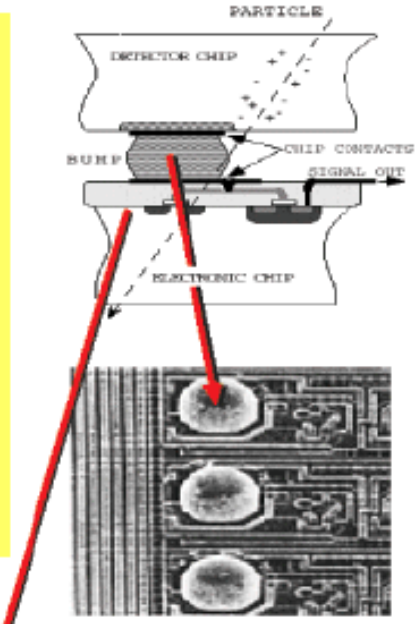
Hybrid pixel for high energy physics application: the ATLAS case

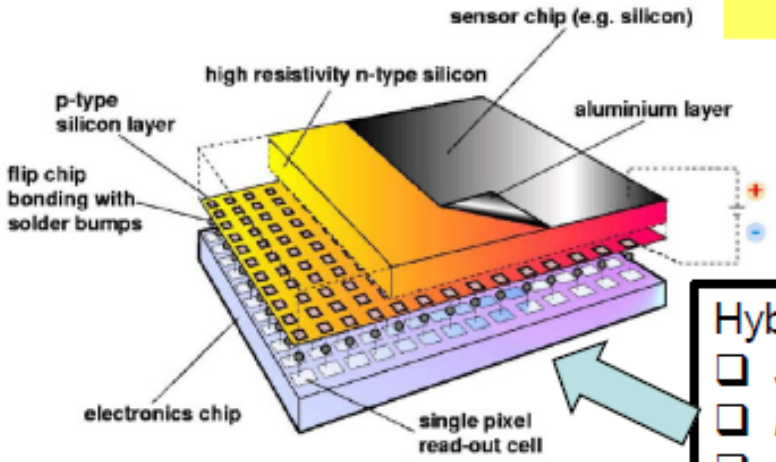
ATLAS pixel readout cell

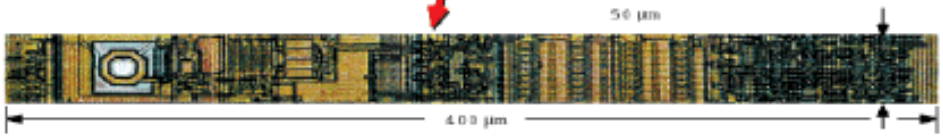


ATLAS pixel structure

- Pixel 50μm x 400μm
- fully depleted silicon layer ~300 μm
- one dedicated readout chip with complex architecture possible
- pixel pitch limited by bump bonding



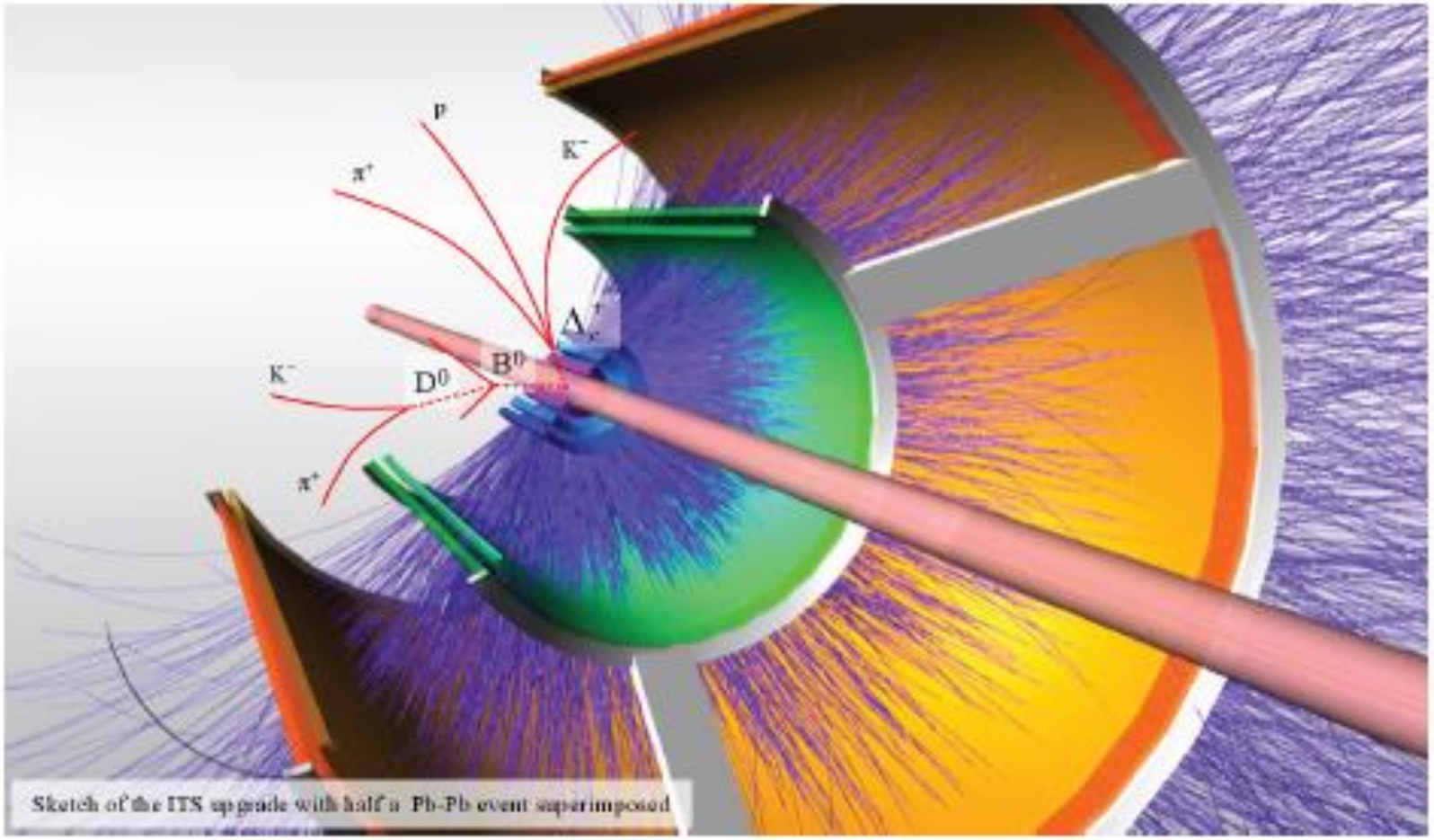




Hybrid pixel general structure:

- *sensor layer (detector grade fully depleted silicon)*
- *bump bonding (50 μm pitch)*
- *read out chip (standard ASIC chip)*

ALICE ITS Upgrade



Main Physics Goal

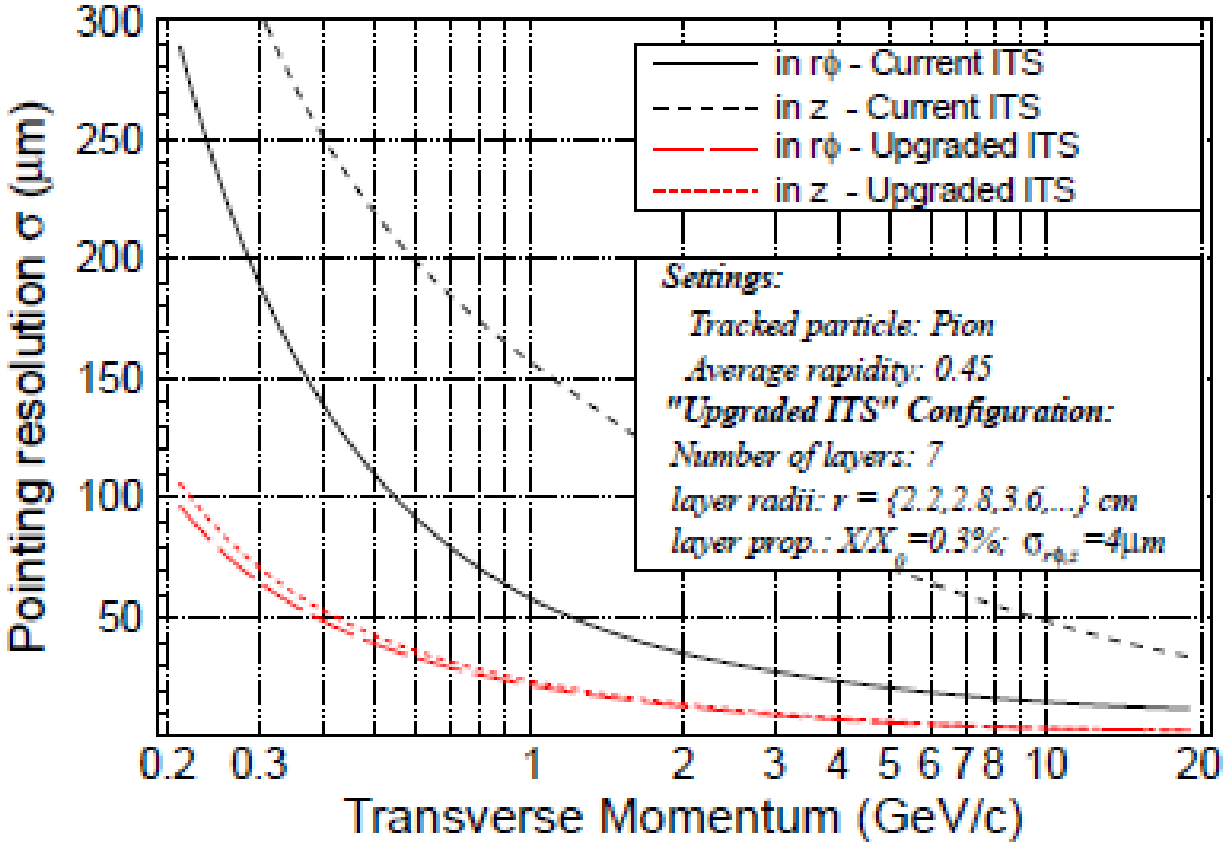
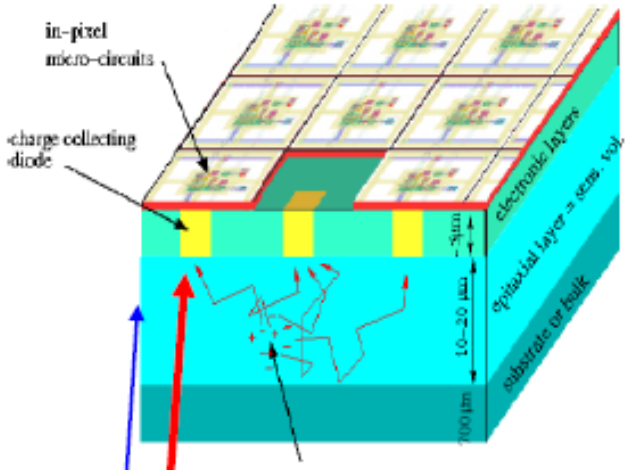
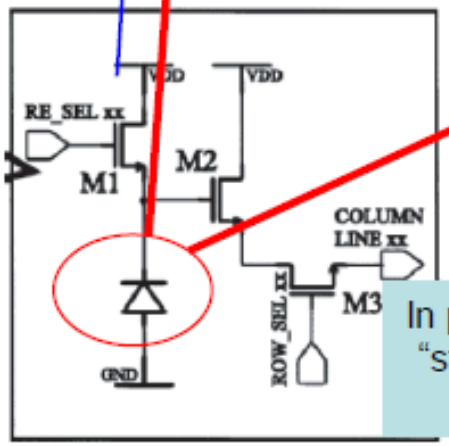


Figure 2.10: Track impact parameter resolution in $r\phi$ and z (current and upgrade).

The MIMOSA (Minimum Ionizing MOnolithic Active pixel Sensors) idea Working principle: Use of the epitaxial layer of STANDARD CMOS microelectronic processes as detecting sensitive volume.

R.Turchetta, et al. , "A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology", NIM A 458 (2001) 677-689





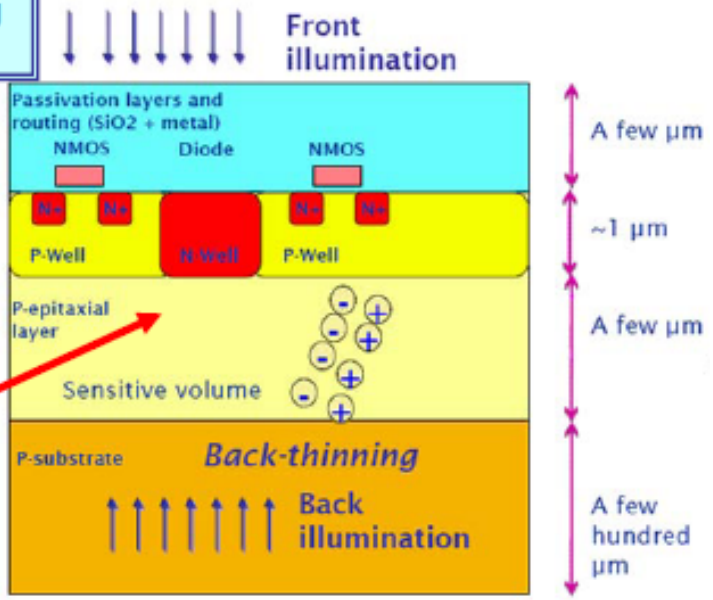
In pixel 3 transistor "standard" MAPS configuration

Recombination time:

~1 *μs*

~10 *μs*

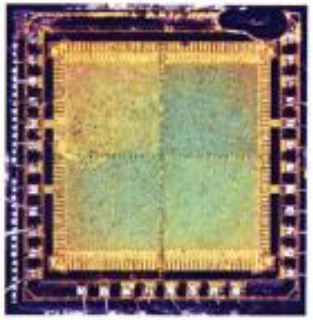
~10 *ns*



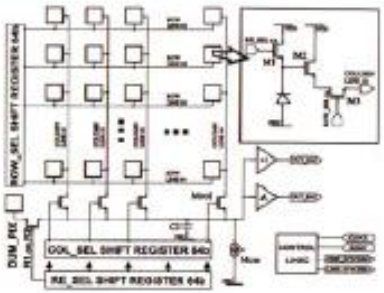
- small signal ~80 e-h/ μm, epi 2-14 μm
- Undepledet detecting volume, charge collected by diffusion and not by drift , cluster size ~ 50-100 μm, collection time ~ 150 ns
- 3T basic readout allows noise: ~ 15-20 electrons
- only N-MOS transistors allowed in pixel area
- easy access to technology through multiproject runs: ~5-50 Keuro

First MIMOSAs implementation (IreS and LEPSI, IN2P3/ULP), Strasburgo, (2001)

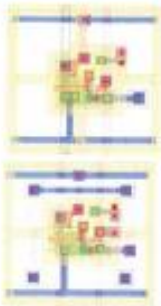
Mimosa I



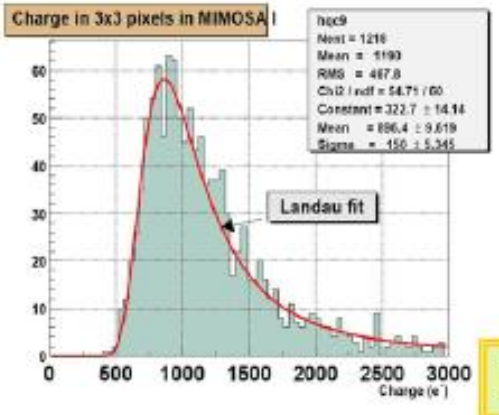
MIMOSA I die photo



MIMOSA I block schematic diagram

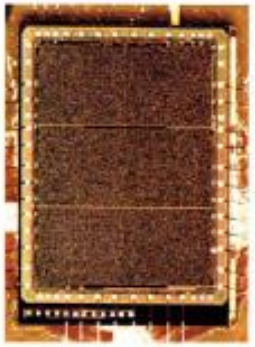


MIMOSA I pixels layouts

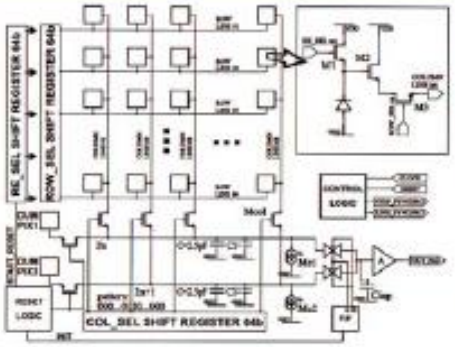


- standard 0.6µm CMOS (tox=12.7nm)
- 14µm thick EPI layer (10^{13}/cm^3)
- 4 arrays 64x64 pixels
- pixel pitch 20x20µm^2
- diode (nwell/p-epi) size 3x3µm^2 - 3.1fF
- serial analogue readout
- max. clock freq.: 5MHz
- die size 3.6x4.2mm^2
- technology 3M+2P
- power supply 5V

Mimosa II



MIMOSA II die photo



MIMOSA II block schematic diagram

MIMOSA II pixels layouts

- standard 0.35µm CMOS (tox=7.4nm)
- 4.2µm thick EPI layer (10^{13}/cm^3)
- 6 arrays 64x64 pixels
- pixel pitch 20x20µm^2
- diode (nwell/p-epi) size 1.7x1.7µm^2 - 1.65fF
- serial analogue readout
- max. clock freq.: 25MHz
- die size 4.9x3.5mm^2
- technology 5M+2P
- power supply 3.3V
- radiation tolerant
- transistor design

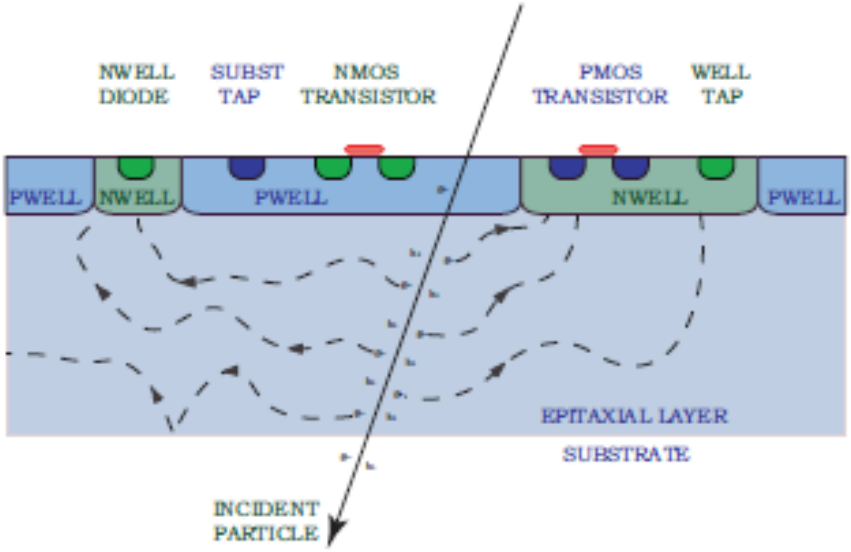
Signal-to-noise (mean):

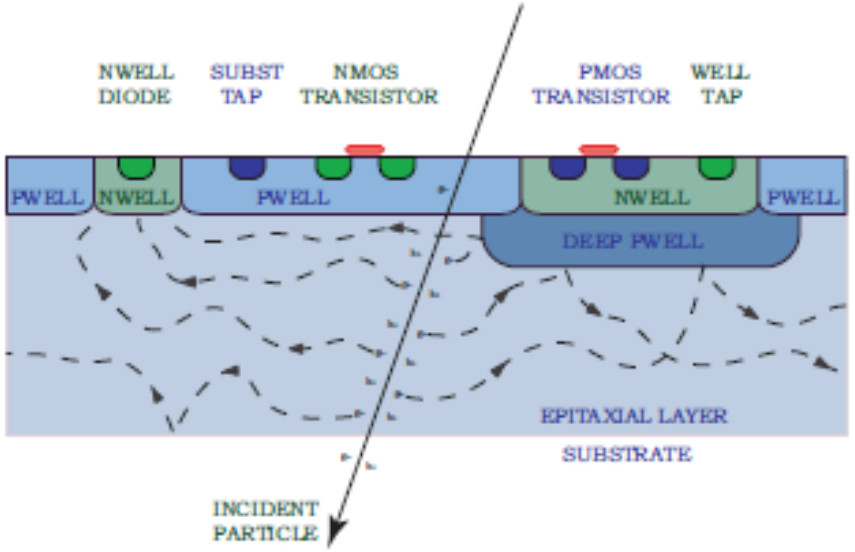
MIMOSA I:	1 diode	42
	4 diodes	32
MIMOSA II:	1 diode	21

Efficiency (%)

MIMOSA I:	1 diode	99.5 +/- 0.2
MIMOSA I:	4 diodes	99.2 +/- 0.2
MIMOSA II:	1 diode	98.5 +/- 0.3

Sensor + Digitization





SK hynix

SK하이닉스 M8라인, 시스템반도체 전환 완료

애플을 최대 고객사로 확보

서울시민신문

▲ SK하이닉스 M8라인. © 서울시민신문

SK하이닉스가 청주 M8 라인을 거점으로 시스템반도체 생산을 본격화했다.

10월 25일 유경동 SK하이닉스 상무는 `국제반도체컨퍼런스 2012`에서 청주 소재의 자사 M8 공장을 메모리에서 시스템반도체로의 전환 작업을 성공적으로 끝냈다고 밝혔다.

M8 공장은 CMOS 이미지 센서(CIS)와 DDI, 전력반도체(PMIC), 고주파(RF), 메모리 반도체를 생산한다. CIS의 경우 90나노미터(㎚) 공정 기반으로 터치스크린과 드라이버칩

As of now

- Would it work?
  - In physics?... ITS upgrade is approved and is also top priority.
  - Technically?... Probably, R&D might be initiated.
  - Financially?
  - Politically?