Analysis of QC results from the DUNE LArASIC chip testing

Antalia Ariel Rabarisoa

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Abstract

The work focuses on the analysis of some parameters of the 16-channel LArASIC PB5 version chips. The testing of the LArASIC chips is done at the room temperature (RT). The ASICs are intended to amplify and shape the pulse signals for downstream signal digitization and are implemented using the TSMC 180nm CMOS process, and have a band-gap reference in order to generate all of the internal bias voltages and currents. These chips will be used for neutrino experimental projects, designed to operate in liquid argon. The data is readout through the UDP interface of the dual FPGA mezzanine. The chips are characterized using the python scripting. The baseline measurements are made for all channels and the linearity measurement is done for the different combinations of baselines using an external pulse generator. The noise of LArASICs can be identified on the Dual-DUT test board that has been designed to carry out the characterization of two chips in a single thermal cycle. The band gap reference voltage is also evaluated and the power consumption is measured at different buffer settings.