DUNE Cold Electronics Front-end Chip Quality Control Testing and Data Analysis

By

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ABSTRACT

The Deep Underground Neutrino Experiment (DUNE) will be one of the next-generation experiments to uncover the nature of neutrino oscillations which will help understand how neutrinos play a part in the creation of the universe. The measurements will provide incredibly high statistics on the probability of neutrinos oscillating between their electron, muon, and tau flavors. The experiment will consist of a neutrino beam generator, a near detector at Fermilab in Batavia, Illinois, and the Far Detector, located thirteen hundred kilometers downstream of the neutrino beam at the Sanford Underground Research Facility. Measurements of the neutrinos will be made using Liquid Argon Time Projection Chambers (LArTPCs). Those detectors will provide analog signals, which will be processed and converted to digital data through electronic circuits, including Liquid Argon Application-Specific Integrated Circuits (LArASICs). Given that these components must remain operational for a 30-year duration without maintenance and replacement, the quality control of LArASICs is of utmost importance. The reliability of LArASIC chips is paramount for achieving the physics by DUNE. With a vast quantity of approximately 40,000 LArASICs required, there is a strong need for automating the quality control testing process. To this challenge, a Python program has been written to accept input from a directory containing multiple folders with all the tested chips. Each LArASIC's results are compiled into a CSV file (Result). Subsequently, the program processes the data, employing specific criteria to generate aggregated results from a series of the nine tests. These results serve to determine whether each chip passed or failed conclusively. The program also keeps track of how many chips passed or failed the tests. This program is an invaluable solution, eliminating the need for manual inspection and saving significant time.

1: Introduction

DUNE is designed to measure the probability that a neutrino will oscillate between any of the three flavor states. It does so by measuring the number of each flavor at one point in time, followed by another round of measurements after the neutrinos have had enough time to oscillate once. In the DUNE far detector module 1 and module 2, the signals from the neutrino interactions with liquid argon are collected by the wire planes in the Liquid Argon Time Projection Chamber (LArTPC). These signals are then shaped and amplified by the Application Specific Integrated Circuit designed for operation at Liquid Argon (LArASIC). This electronic circuit works to process the large number of signals created by DUNE and around 40,000 LArASICs will be needed to operate in the first and second modules of DUNE. However, because DUNE is anticipated to run for around 30 years without any maintenance and replacement, these LArASICs will need to remain operational for the entire length of the experiment. Therefore, Quality Control (QC) of these circuits is crucial. Performing QC tests of all 40,000 chips and analyzing the resulting data is crucial for the long run of the experiment. To facilitate the analysis of the large number of QC data, a Python program has been written to input the data from all the QC tests for the LArASICs and output their passing or failing in the 9 tests for each required to assess their quality. This program will greatly reduce the amount of time that needs to be spent on QC analysis and eventually organize the data. Statistical analysis is also done to determine the acceptance criteria of these chips. The size of one module of the DUNE far detector (10kt of LAr), however, does not allow us to replace or repair the LArASIC chips board in case of an issue once immersed in liquid argon. Therefore, a dedicated QC is required to have chips reliable during the long lifetime of the DUNE experiment and also a minimum number of dead channels in the detector (< 1%). One of the QC done by the Cold Electronics team at BNL is the LArASIC QC. The selection of the chips that passed the QC is done one by one by checking the parameters such as the Equivalent Noise Charge (ENC) noise, gain, power consumption, and baseline

selection. In the current study, we are analyzing the data of the LArASIC that passed the QC to define an acceptance range of the parameters. This report includes the results for the baseline, noise, and power measurements. Plus, the Python script which was written to help in the QC of the tested chips.

2: Methodology: Test procedures

The testing procedure starts with a quick check of all the LArASIC chips. Then once it passes the Quick check, the QC test script is run to determine the pass or fail of the chip. This is done by testing against nine parameters i.e.

Power consumption, Front End (FE) Parameter, Channel Response, Baseline (BL) Restoration, Power Cycling, Gain Measurement, and Noise measurement. When these steps are done, we check the summary of the tests and the status of the chip, then the chip is placed in the designated tray that is for the pass or failed chips.

Once the tests at room temperature are done, we use chips that pass the RT tests to be tested in the cold tests. To be able to do the actual test, we need to lower the DUAL DUT test board to liquid nitrogen until fully immersed. Then we run the quick check followed by the QC test script. When finished, we remove the board from the liquid nitrogen and check the results of the QC test. The first phase of the current study was to reproduce the results from the QC by writing a new Python script that can take all the tested chips, determine the status of the chips, then aggregate the results and count all the passed and failed chips for each batch number. The script would be a game changer in the QC analysis of the chips since it will save a huge amount of time. The second phase of the work was to perform a statistical analysis of some of the parameters tested i.e. baseline, power consumption, noise measurement, and gain measurements. Statistical analysis is done to determine the acceptance criteria of the chips.

Distribution plots for three parameters were plotted based on the results obtained. The analysis focused on data obtained from Room temperature results.

3: Results

In this section, we present only the distributions of the pedestal, noise, gain, and power measurements for the LArASIC chips. We will also present the yield rate for the tested chips at RT for batches 000,001,010 and 020. These will be results obtained from the Python script written. The script can be available here https://github.com/sgaobnl/LArASIC_QC_Statistics-

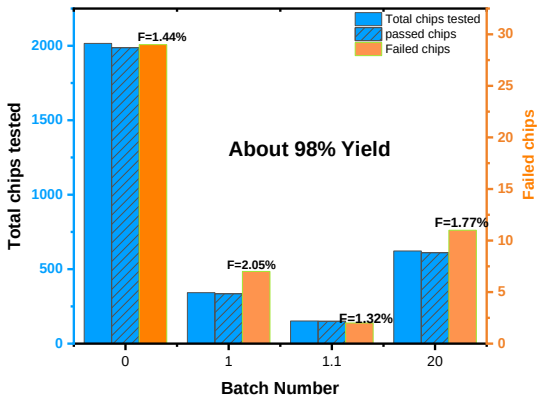
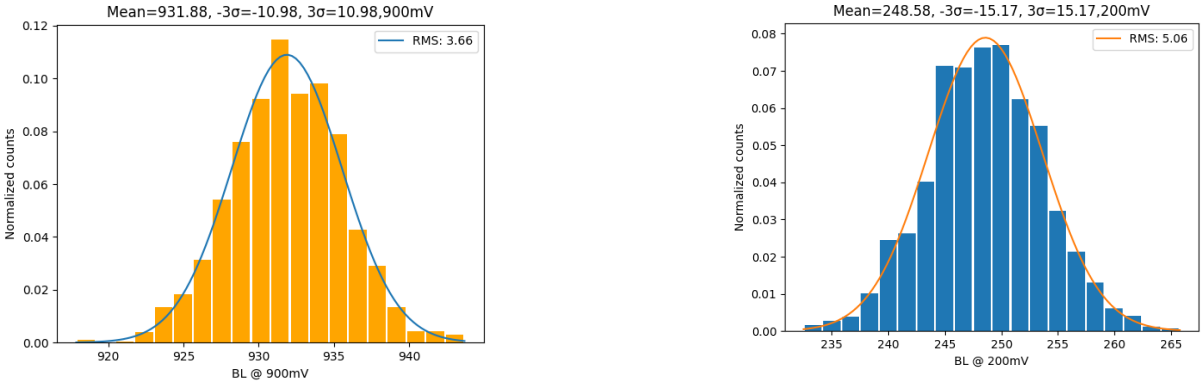


***Figure 1**: Yield Rates for the tested chips at RT*

As shown in Figure 1 above, the yield for all the batches was approximately 98% which is within the acceptance criteria. The yield can be increased if the testing process is automated to minimize mishandling of the chips especially when placing them correctly on the DUAL DUT testing board.

Baseline distribution

Figure 2 shows examples of the baseline distribution for two different configurations. From these plots, the baseline of the input signal for both 200mV and 900mV gave the expected behavior. Hence within the acceptance criteria for the LArASIC chips at RT.

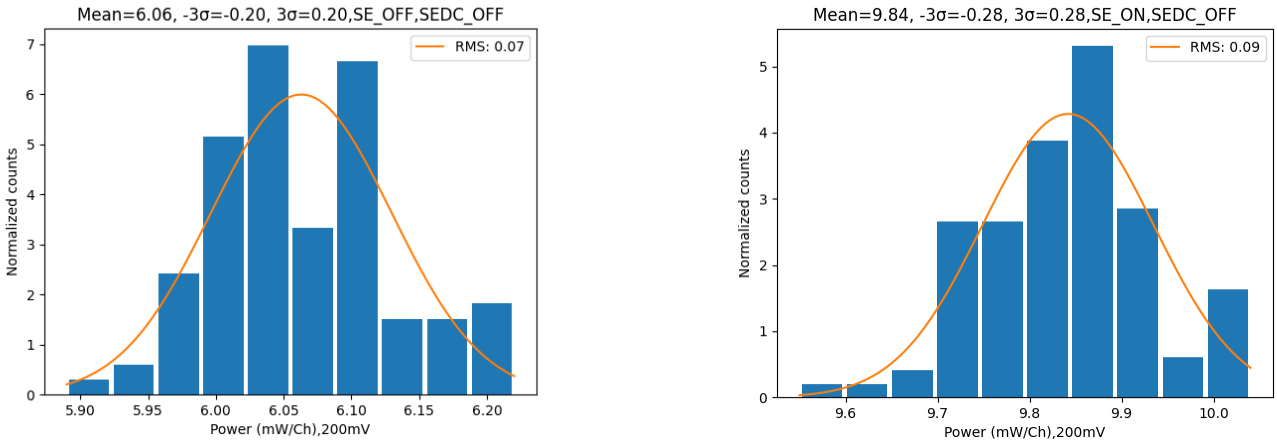


(a) (b)

***Figure 2**: Baseline Distributions for baseline 200mV (a) and 900mV (b)*

Power Consumption

The study focused on measuring LArASIC chip power under various room temperature scenarios while accounting for cable power loss. Figure 3 shows power measurements for LArASIC chips at room temperature under single-ended enabled and disabled conditions. The observed power consumption was consistent with anticipated behavior.



(a) **(b)**

***Figure 3:** Power measurement for the LArASIC chips when Single-Ended is disabled (a) and enabled (b)*

ENC noise

Figure 4 shows an example of the linearity of the Equivalent noise charge for LArASIC chips. The linearity shows the relationship between the input charge and the output signal is consistent and predictable. This is the desirable behavior of the ENC at RT since is crucial in testing the calibration of the chips before the actual deployment in a cold environment.

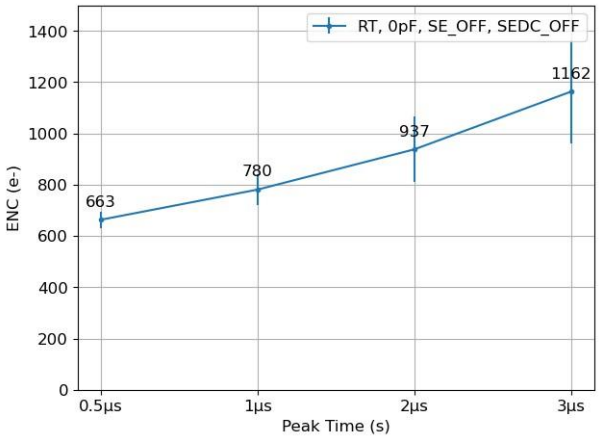


***Figure 4**: Linearity of the ENC for the LArASIC chips at RT*

Conclusion

The newly developed Python script provides a significant time-saving advantage when evaluating chip pass/fail status for the batches. The code is flexible in its application, as it can accommodate chips tested at both room temperature and liquid nitrogen. It also simplifies the calculation of yield rates across all batches. Statistical analysis determines the acceptance criteria for LArASIC chips at room temperature and liquid nitrogen. In this study, the baseline, power consumption, and noise measurements all consistently revealed the expected behavior.

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