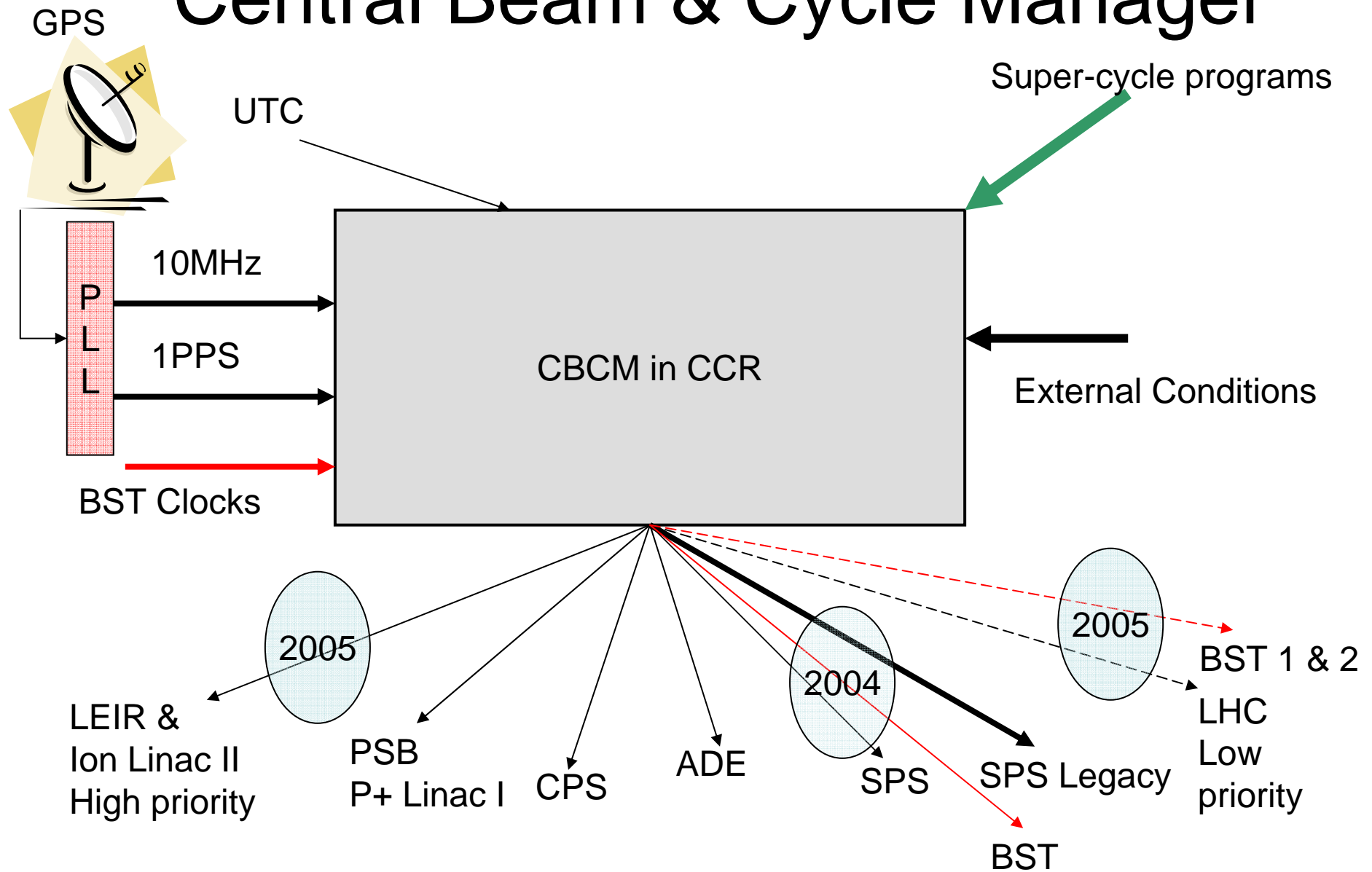
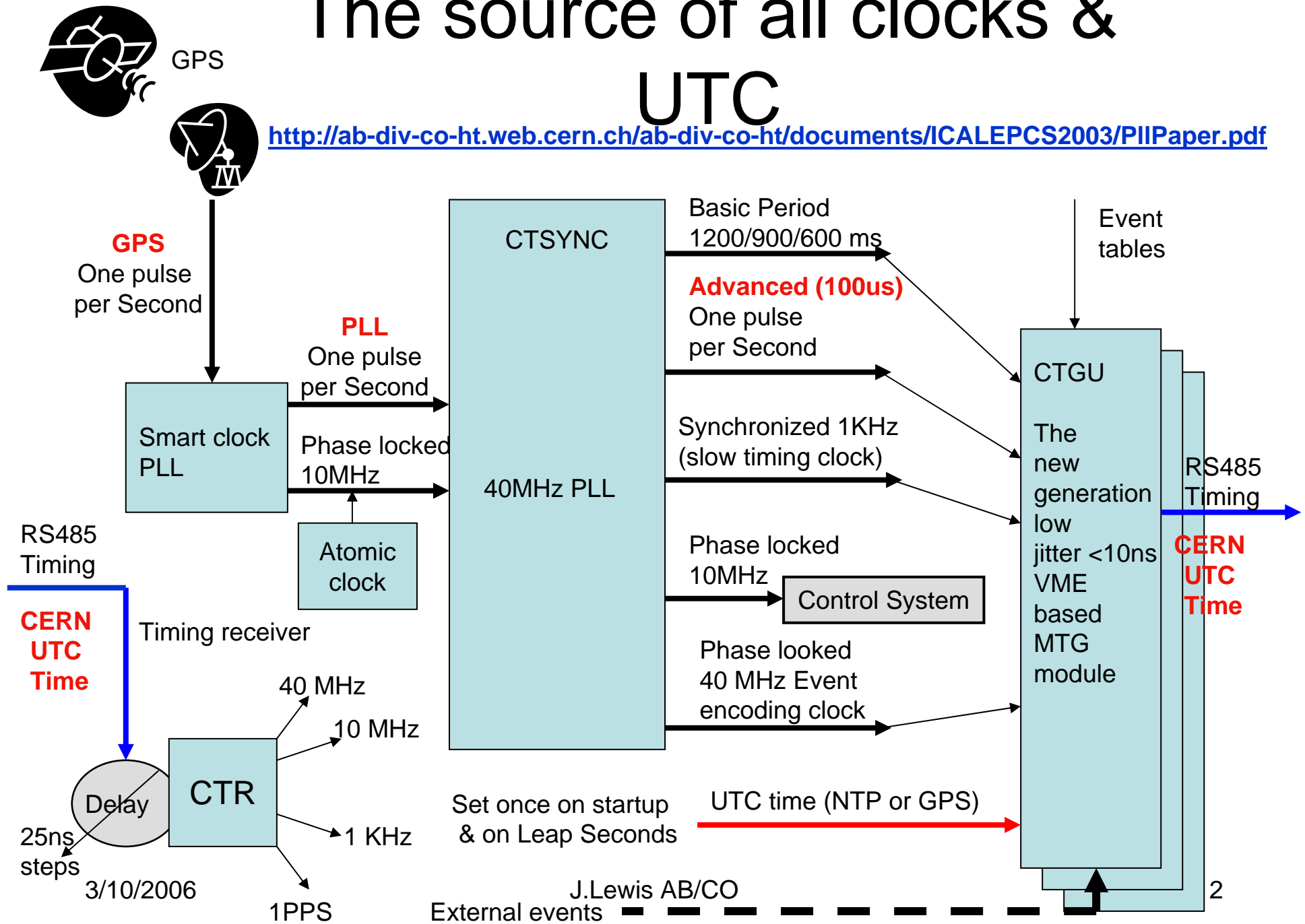


Central Beam & Cycle Manager



The source of all clocks & UTC

<http://ab-div-co-ht.web.cern.ch/ab-div-co-ht/documents/ICALEPCS2003/PIIPaper.pdf>



Controls Timing Receiver CTR

CTR-P CTR-I CTR-V CTR-G

- This device comes in formats PMC, PCI, VME, there is no CPU, its all hardware (VHDL).
- It has up to 8 x 50MHz 24-bit fully configurable counters supporting, burst mode, divide, chaining...
- Full remote counter control capabilities and event triggers
- It has two external start and two external clock inputs
- Internal wire-OR capability of counter outputs (50 Ohm TTL)
- Full telegram support and event wild-card support
- Full UTC time support with 25ns/700ps resolution (25ns/32 if HPTDC)
- Recovers the 40.000MHz encoding clock using a temperature controlled VXCO digitally controlled via a DAC, <10ns jitter.
- High precision HPTDC Time to Digital converter permitting UTC time stamping counter outputs with better than 1ns peak-peak resolution
- Adjustable transmission cable delay compensation in 25ns steps
- Trigger table containing up to 2400 entries for multi-pulse support

<http://ab-div-co-ht.web.cern.ch/ab-div-co-ht/documents/ICALEPCS2003/ctrp.pdf>

BST Master and UTC

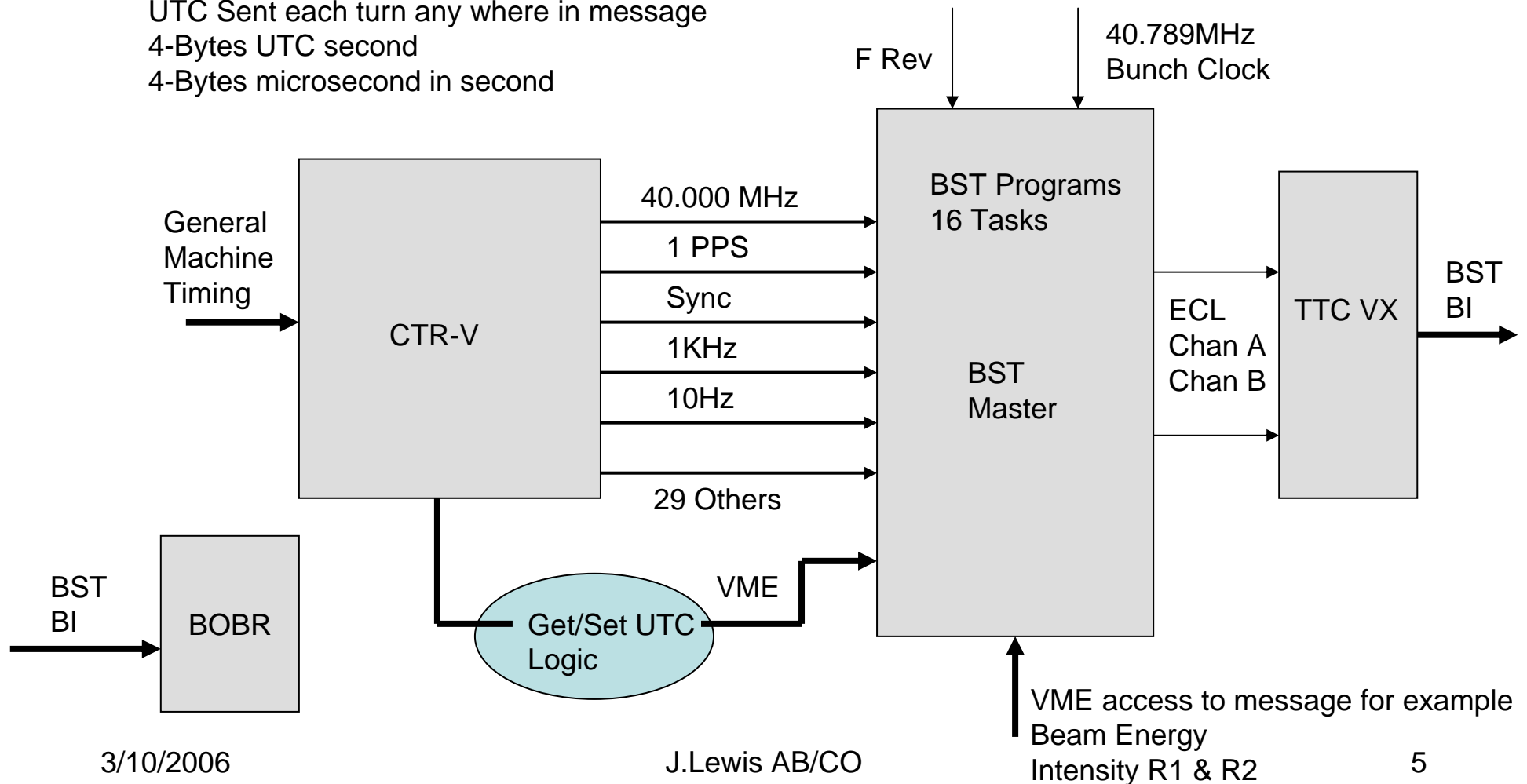
http://ab-div-co-ht.web.cern.ch/ab-div-co-ht/documents/ICALEPCS2003/BST_ICALEPCS2003.pdf

- Multi tasking CPU in FPGA up to 16 Tasks
- Same hardware as CTG card, VHDL differs
- Drives ECL outputs for TTC
- Keeps Turn number and UTC time
- Distributes BST message per turn, about 64 bytes long in the LHC
- Distributes 4/4-Byte UTC time in seconds and micro seconds
- 3 Systems envisaged for LHC, Ring 1 & 2, and Exp
- External inputs 1PPS/10Hz/1KHz + 29 others

GMT & BST Connection

http://ab-div-co-ht.web.cern.ch/ab-div-co-ht/documents/ICALEPCS2003/BST_ICALEPCS2003.pdf

UTC Sent each turn any where in message
4-Bytes UTC second
4-Bytes microsecond in second



General Machine Timing (GMT)

CTR comparison BOBR

Beam Synchronous Timing (BST)

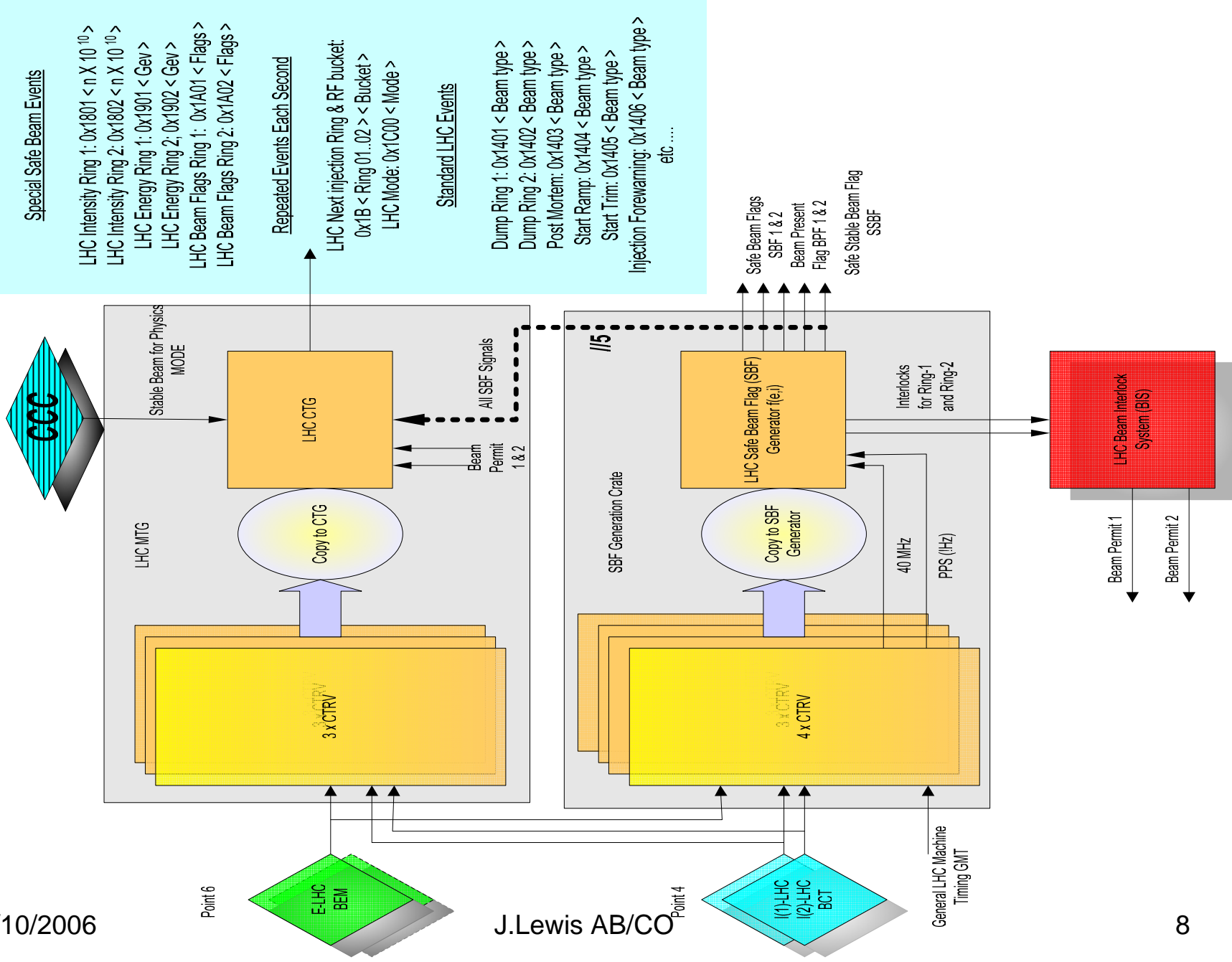
- 40.000 MHz locked to the GPS
UTC 1PPS
- 8 x 32-Bit frames per ms
continuous
- UTC Time jitter <10ns resolution
<1ns
- All key LHC and SPS timings
available
- Telegrams for all CERN
accelerators distributed each 1.2
seconds
- CTR Supports standard timing
synchronization and telegram
access libraries and CMW access
methods
- Triggers 8 fully programmable
50Mhz counters with external start
and clock inputs
- 40.789 MHz locked to bunch
frequency
- 64 Bytes per 89us beam
revolution
- UTC Time jitter <5ns, resolution
89us
- Subset of LHC timings from CTR-
V, 1KHz, 1PPS etc
- Some parameters can be
introduced from the VME
interface. There are RT
restrictions on how often.
- BOBR is provided with BI specific
software support
- Produces VME P2 Equipment
triggers

The LHC timing

- Beam Energy, Beam Intensity R1 & R2
- Target Bunch and Ring for next injection
- Machine mode, coast, ramp etc
- Particle type P+ Ions etc
- Safe beam flags
- Time stamps
- Controls information & CTR Triggers as needs become apparent, its flexible we can add things on the fly.
- User information as requested
- etc

Safe LHC Parameter distribution

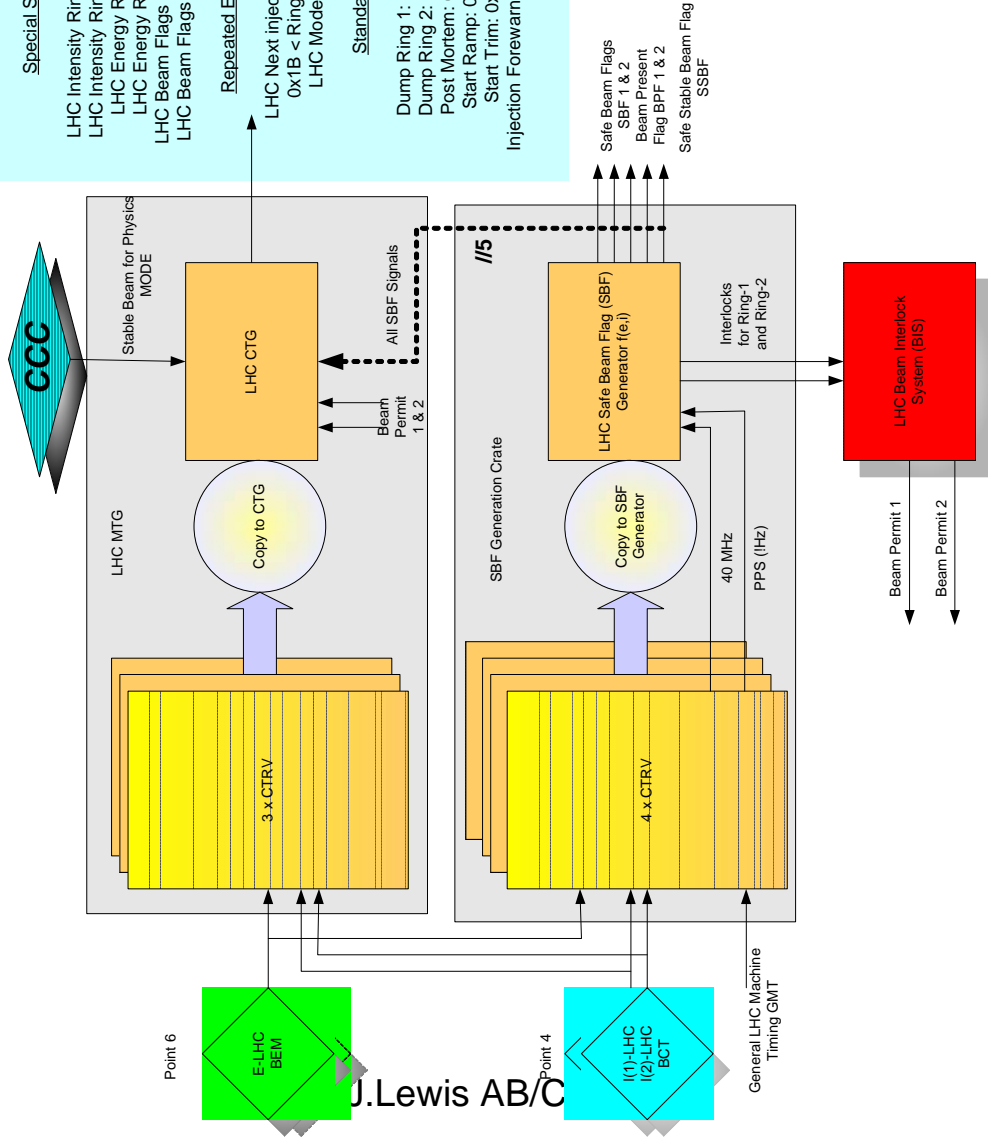
3/10/2006



J.Lewis AB/CO

3/10/2006

Safe LHC Parameter distribution



General LHC Machine Timing GMT

Special Safe Beam Events

LHC Intensity Ring 1: 0x1801 < n X 10¹⁰ >
 LHC Intensity Ring 2: 0x1802 < n X 10¹⁰ >
 LHC Energy Ring 1: 0x1901 < GeV >
 LHC Energy Ring 2: 0x1902 < GeV >
 LHC Beam Flags Ring 1: 0x1A01 < Flags >
 LHC Beam Flags Ring 2: 0x1A02 < Flags >

Repeated Events Each Second

LHC Next injection Ring & RF bucket:
 0x1B < Ring 01.02 > < Bucket >
 LHC Mode: 0x1C00 < Mode >

Standard LHC Events

Dump Ring 1: 0x1401 < Beam type >
 Dump Ring 2: 0x1402 < Beam type >
 Post Mortem: 0x1403 < Beam type >
 Start Ramp: 0x1404 < Beam type >
 Start Trim: 0x1405 < Beam type >
 Injection Forewarning: 0x1406 < Beam type >
 etc

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More info

Lots of stuff here

<http://ab-div-co-ht.web.cern.ch/ab-div-co-ht/>