ePIC Silicon Vertex Tracker

L. Gonella on behalf of the ePIC SVT DSC

ePIC collaboration meeting

Warsaw, 27 July 2023

ePIC SVT DSC

ePIC SVT Detector Subsystem Leader: Ernst

ePIC SVT Detector Subsystem Technical Coordinator: Laura

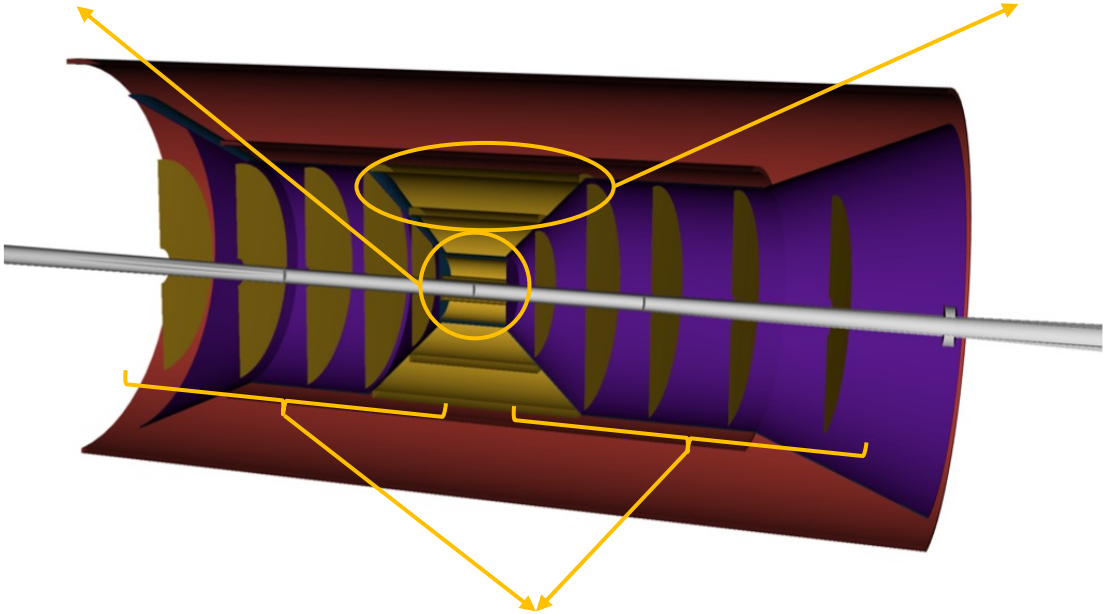
Kickoff meeting https://indico.bnl.gov/event/19823/

Work packages structure, tasks/institutes matrix being defined

ePIC SVT configuration

Inner Barrel (IB)
- 2 curved silicon vertex layers
- 1 curved dual-purpose layer

Outer Barrel (OB)
- 1 stave-based sagitta layer
- 1 stave-based outer layer



Electron/Hadron Endcaps (EE, HE)
- 5 disks on either side of the IP

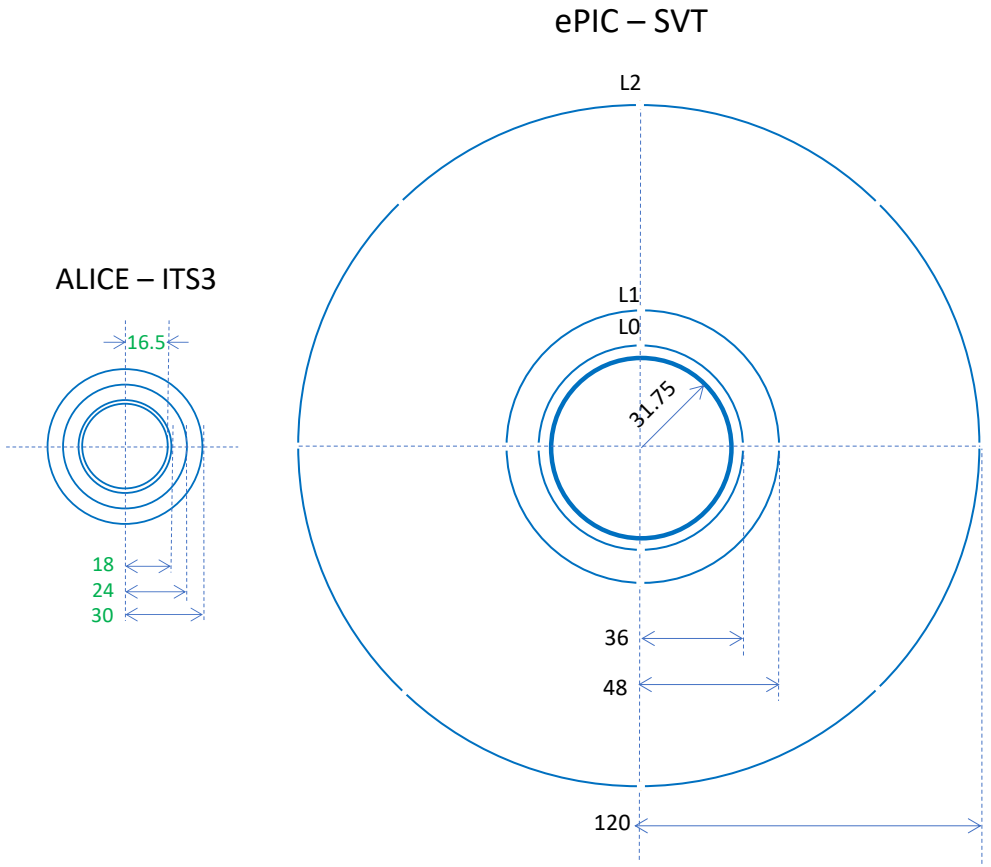
Total (active) area ~ 8.5 m^2

Inner Barrel

- Three layers of thin, bent, wafer-scale silicon sensors

- Minimal mechanical support, air cooling, no services in active area
  - ITS3 detector concept adapted to ePIC SVT radii

IB	r [mm]	l [mm]	X/X0 %
L0	36	270	0.05
L1	48	270	0.05
L2	120	270	0.05

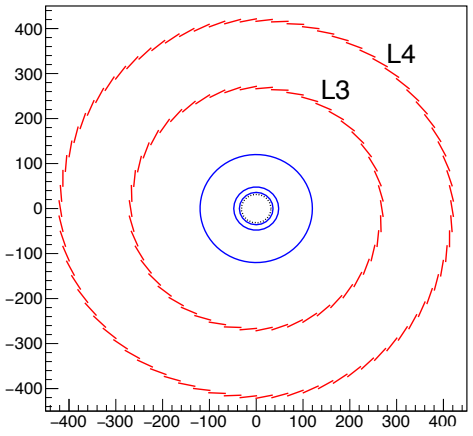


Outer Barrel and Endcaps

- Large Area Sensor (LAS) optimised for high yield, low cost, large area coverage

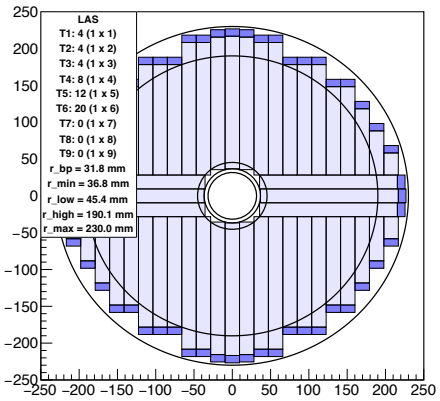
- Stave and disks support structures with integrated cooling

OB	r [mm]	l [mm]	X/X0 %
L3	270	540	0.25
L4	420	840	0.55



EE/HE	+z [mm]	-z [mm]	r_out [mm]	X/X0 %
ED0/HD0	250	-250	240	0.24
ED1/HD1	450	-450	420	0.24
ED2/HD2	700	-650	420	0.24
ED3/HD3	1000	-900	420	0.24
ED4/HD4	1350	-1150	420	0.24

Example: ED0/HD0



Sensor

- The sensor for the ePIC SVT is a MAPS sensor in 65 nm CMOS technology, developed with the ALICE ITS3 collaboration
  - IB: ITS3 wafer scale sensor
  - OB, Endcaps: EIC Large Area Sensor (LAS)

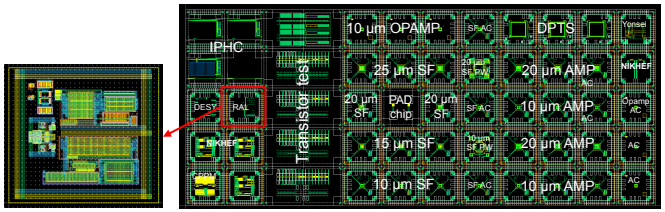
- Meeting EIC/ePIC – CERN/ALICE in April → Agreement to share sensor

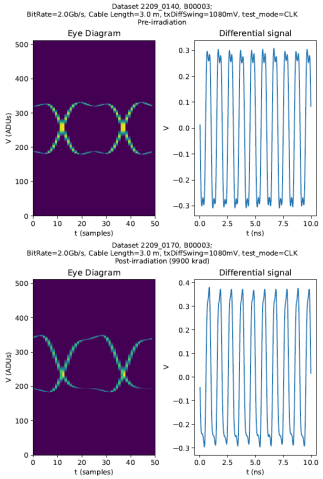
- Sensor development
  - MLR1 - Q4 2020: Technology exploration and prototype circuit blocks
  - ER1- Q4 2022: MOSS and MOST sensors, exploratory designs for proof of principle, and learning stitching methodology and yield
  - ER2 - Q1 2024: Sensor design to satisfy ITS3 requirements
  - ER3 - Q2 2025: Final ITS3 design/production

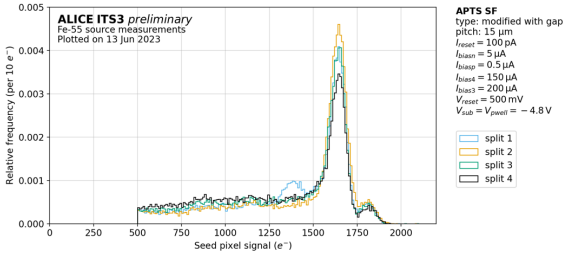
The EIC LAS sensor will be based off the ER2 and ER3 designs

MLR1 and ER1

- MLR1 – ePIC contribution
  - Design and full characterization of circuit blocks for high-speed data off-sensor transmission up to 2Gbps and 9.9 Mrad
  - Testing of analogue and digital pixel test structures (APTS, DPTS)

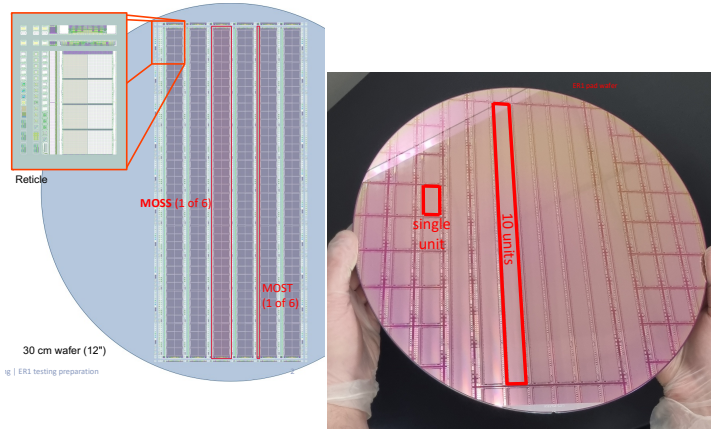






Technology validated for charged particle tracking

- ER1
  - ePIC contribution: continuation of high-speed off-sensor data transmission development, design of low-speed on-sensor data transmission; redesigned standard cells for DFM → direct contribution to MOSS/MOST
  - Sensors received in Q2 – 2023, initial testing ongoing by ITS3 groups, basic functionality verified

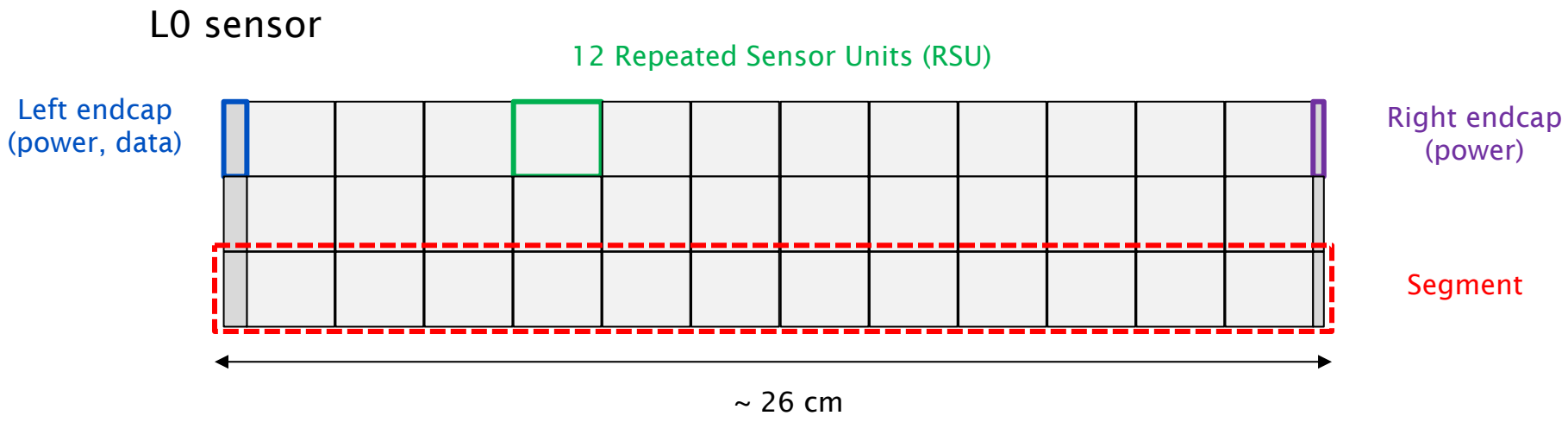


https://indico.cern.ch/event/1280150/

ER2 and ePIC IB sensor

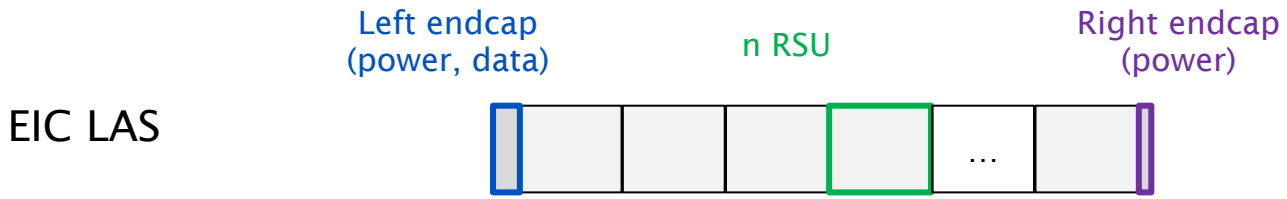
- ER2 segment = 12 RSU, left and right endcap
  - Note: ER2 design evolving rapidly; design specifications can still change (RSU and pixel size, power distribution scheme, on/off-sensor data transmission, etc.)
  - Direct impact on the overall ePIC SVT design (powering, readout, mechanics, cooling)
  - Design to converge in the next few months

- ITS3 and ePIC SVT IB sensor
  - L0: 3 segments, L1: 4 segments, L2: 5 segments



ER2 and ePIC OB, EE/HE sensor

- EIC LAS sensor = Single segment, n RSU + left/right endcap
  - If n ≤ 6, right endcap not needed



- n (i.e. sensor length) to be defined based on acceptance/coverage, yield/cost, manufacturing constraints
  - Foundry rules limit the EIC LAS sensor size to 2/3 variants
  - Impact on acceptance/coverage to be assessed in updated staves/disks tiling study

- In addition to change in RSU number, changes planned in the left endcap to accommodate the requirements of the ePIC data transmission scheme
  - Integrate multiplexing of data links for lower ePIC data rate (wrt ITS3)

ER2 and EIC LAS design

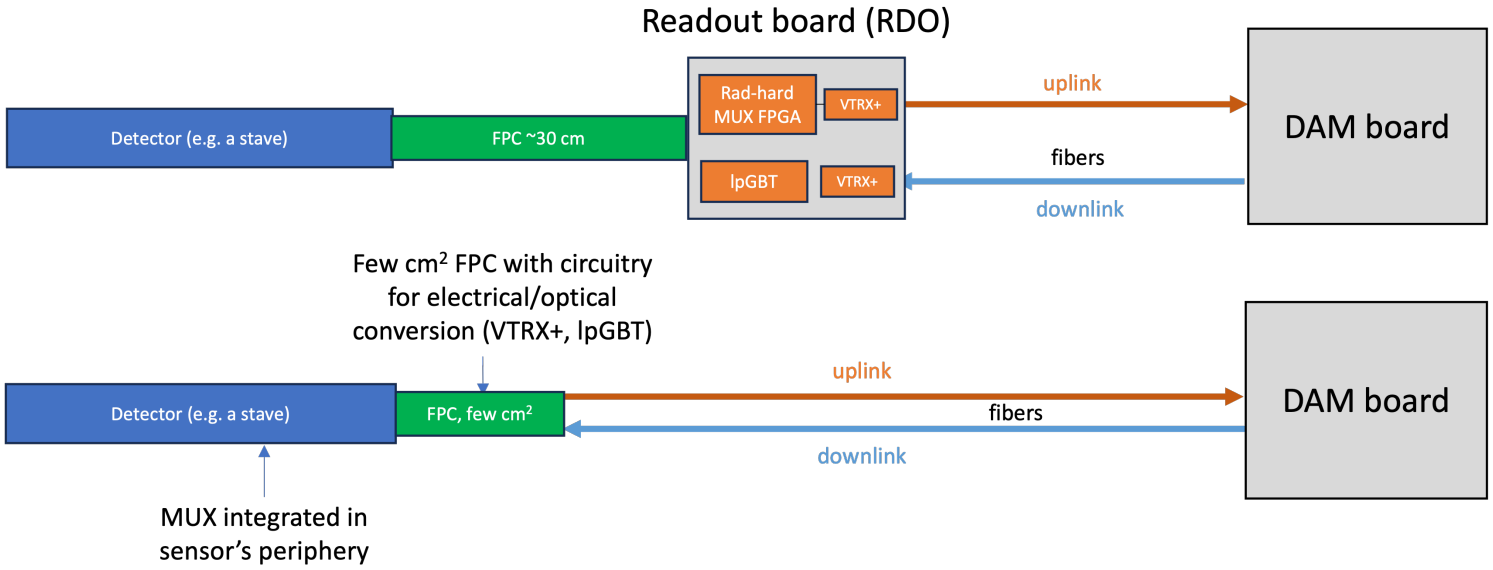
- ePIC contribution to ER2 design in under discussion with ITS3 designers
  - DFM/low power standard cells
  - Monitoring Analog-to-Digital Converter
  - SRAM design
  - Voltage regulations

- Design ongoing also on ePIC specific developments for EIC LAS
  - Integrated data multiplexing
  - Developments for current based powering scheme
    - Regulator
    - Generation of sensor bias voltage from sensor low voltage

Readout

- Development of a multiplexing strategy for the output links of the EIC LAS
  - Multiple 10 Gbps links in the ITS3 sensor, not needed for the (much lower) data rates at ePIC

- Two options under consideration
  - External multiplexing using commercial FPGA
  - Multiplexing integrated on sensor



Readout and DAQ for ePIC SVT @ https://indico.bnl.gov/event/17882/
Update on readout @ https://indico.bnl.gov/event/19390/
R&D progress in FY23 and plans for FY24 - eRD104 @ https://indico.bnl.gov/event/19740/

Powering

- A constant current powering scheme is chosen for the OB and EE/EH
  - EIC LAS sensors are powered in series by a constant current
  - Regulators convert the input current into the (analogue and digital) voltage needed by the EIC LAS

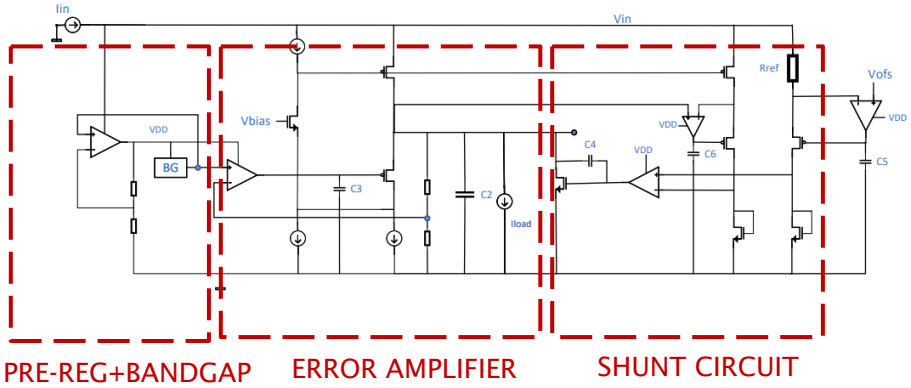
- Regulator architecture: Shunt-LDO
  - Regulator concept developed for the serial powering scheme of the ATLAS and CMS pixel systems at the HL-LHC

- The Shunt-LDO will be external to the EIC-LAS, not integrated, placed in close proximity to it
  - No change to the ITS3 sensor needed for EIC LAS powering scheme
  - Prototype and production in a cheaper technology

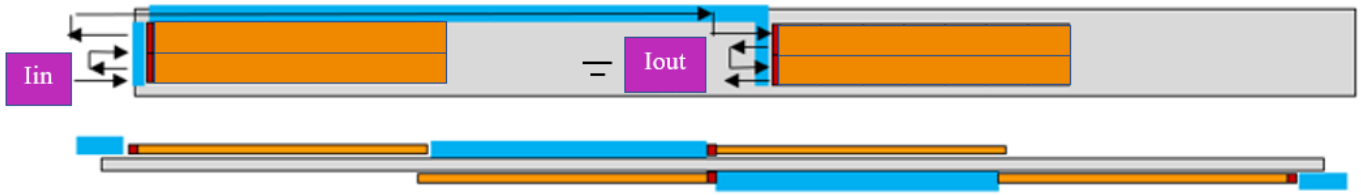
Powering scheme for the ePIC SVT @ https://indico.bnl.gov/event/18202/
Update on ePIC powering and associated services estimates @ https://indico.bnl.gov/event/18525/

Powering

- Shunt-LDO regulator design advancing
  - Submission of 65 nm prototype in Q1-24
  - Submission of 180 nm prototype in Q2-24



- Initial conceptual SP design for OB
  - 2/4 EIC LAS sensors in a serial powering chain in L3/L4
  - Assumed serial powering chains of 3 EIC LAS sensors in disks for now
  - Implications of power supply to sensor from left and right endcaps needs study



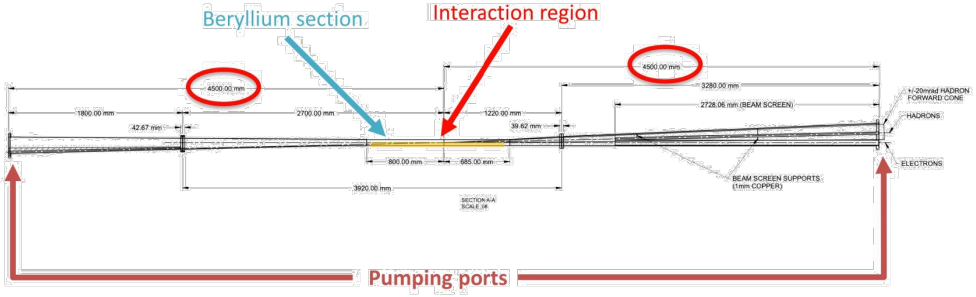
L4 serial powering scheme;
top – stave top view, bottom – stave side view

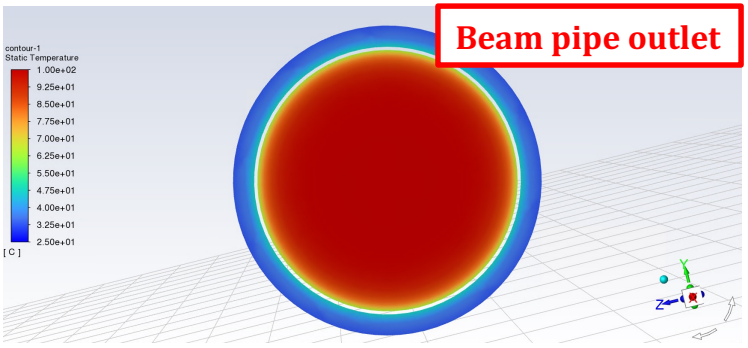
Powering scheme for the ePIC SVT @ https://indico.bnl.gov/event/18202/
Update on ePIC powering and associated services estimates @ https://indico.bnl.gov/event/18525/

Mechanics and cooling: Curved layers

- Bending and interconnections at larger ePIC SVT radii needs development
  - In particular, L2 radius is much larger than ITS3 radii; is a support cylinder between L1 and L2 needed?

- Air cooling for IB to reach 0.05% X/X0
  - How to channel air flow to vertex layers
  - Beam pipe bake-out studies ongoing; effect of air cooling on beam pipe temperature

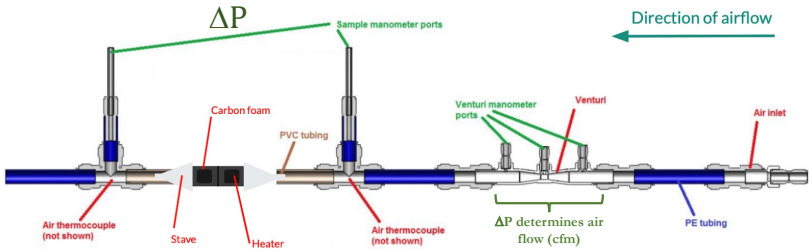


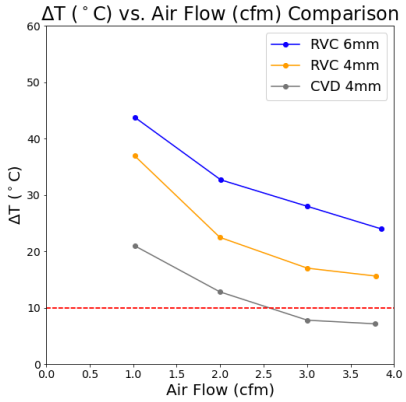


eRD111 updates https://indico.bnl.gov/event/18525/
Engineering challenges of initial ePIC SVT configuration https://indico.bnl.gov/event/17713/
R&D progress in FY23 and plans for FY24 - eRD111 https://indico.bnl.gov/event/19740/

Mechanics and cooling: Staves and disks

- Conceptual design to be updated to inform mechanical layout
  - Updated tiling study to account for impact of different sensor RSU size and manufacturing constraints on EIC LAS sizes
- Electrical interface from sensor to end of stave/disk, Flexible Printed Circuit
  - FPC designs, procedures for assembly of EIC LAS on FPC
- Cooling
  - Common cooling systems with MPGD and TOF? Monophase or 2-phase?
  - Integration in mechanical structure needs to be low mass
  - Also, initial study of air cooling through carbon fiber





Aim:

- $\Delta T < 10°C$
- $\Delta P < 1$ bar for 1m stave

CVD meets both requirements

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ePIC SVT work with the project

- Work with the project to provide inputs for the CD-3A Design Review by the DAC at the end of August and the Director's Review in October

- Services estimates
  - Three iterations documented on the project sharepoint (ePIC/Tracking/Silicon) https://brookhavenlab.sharepoint.com/:f:/s/EICPublicSharingDocs/EqFKiVvqFBFOpMyAEEtw4McBUss2SE8o9JzeJc9W44vHSA?e=NIWYDB
  - Sensor low voltage and bias schemes and cables defined (March 2023 update)
  - More recently, update on data links and cooling (July 2023 update)

- WBS, schedule, costing
  - ePIC SVT DSL and DSTC working with tracking CAM to align project WBS and ePIC SVT WP, and review schedule (by August), and costing (by October)

Conclusion

- Progress on many aspects of the ePIC SVT detector
- A lot of interesting and challenging work still to be done to deliver the ePIC SVT
- Growing interest by many institutes converging in the ePIC SVT DSC
  - The DSC remains open to more collaborators
- Finalisation of the ITS3 ER2 design in the next few months will fix crucial parameters for the ePIC SVT development
  - Sensor size, power consumption, data transmission
- The programme for FY24 is to advance designs to converge on final design choices, and scale up prototypes in preparation for the TDR

Backup