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# Barrel and Forward TOF: AC-LGAD

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## **AC-LGAD** Technology

• AC-LGAD provides not only precise timing resolution, but also ~100% fill factor and much better spatial resolution than DC-LGAD.



# **AC-LGAD TOF for ePIC**

#### **Tracking and Vertexing:**

- MAPS (3-5  $\mu m)$
- AC-LGAD (30 µm)
- MPGD (150 µm)

#### PID:

- hpDIRC
- pfRICH
- dRICH
- AC-LGAD TOF (25/35 ps)

#### **Calorimetry:**

- PbWO EEMCal
- Fe/Sc Backward HCAL
- Pb/SciFi Barrel EMCal with Imaging
- Barrel HCal (sPHENIX re-use)
- W/SciFi FEMC
- Fe/Sc&W/Sc LFHCAL

#### Far-Forward/Backward:

- AC-LGAD for B0 tracker and RPs
- ZDC ...



#### **AC-LGAD TOF for ePIC**



#### **AC-LGAD TOF Detector Specifications**



L=2.7m

Detector	Area (m <sup>2</sup> )	Channel size (mm <sup>2</sup> )	Number of channels	Time resolution (ps)	Spatial resolution (µm)	Material budget (X <sub>0</sub> )	Total Power (kW)
BTOF	~10	0.5x10	~2.4M	35	30 in r·φ	~1%	4
FTOF	~1.4	0.5x0.5 (0.7x0.7?)	~6M (3M?)	25	30 in x and y	~5% (2.5%?)	13 (7?)

#### **AC-LGAD TOF for PID in ePIC Simulation**



FTOF in DD4HEP (Nicolas Schmidt)





- BTOF with timing resolution of 35 ps provide 3*σ* π/K separation up to ~1.3 GeV/c
- FTOF with timing resolution of 25 ps provide 3*σ* π/K separation up to ~2.4 GeV/c

### **AC-LGAD TOF for Tracking in ePIC Simulation**



- BTOF with a spatial resolution of 30 µm improves momentum resolution at high p
- TOF helps track reconstruction by rejecting beam background and pileup hits in SVT

### **AC-LGAD Sensor Development**

• Goal: large area sensors that meet timing/spatial resolution requirements with minimal # of channels

Position resolution [µm]

60

50

40

30

20

10

02

- Status: prototype sensors produced by BNL IO and HPK and tested in the lab/beam by BNL/FNAL/UCSC/UIC
- Plan: new productions to optimize sensor design for better timing and less # of channels, verify irradiation tolerance validate sensor size and sensor-ASIC integration for module assembly

#### Fermilab Test Beam Facility





#### **HPK Strip Sensor for BTOF**



#### **HPK Pixel Sensor for FTOF**





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#### **Frontend Readout Electronics**

- Goal: develop ASIC and other components that meet requirements on timing/spatial resolutions and power consumption
- Status/Plan:

<u>ASIC</u>: IJCLab/Omega/CEA-Irfu EICROC0->0\_1/1; FNAL FCFDv0->1->2; UCSC HPSoCv1->2, ASROC, FAST2->3 Low mass flexible PCB: ORNL proof of concept prototypes -> full scale functional prototype

Service hybrid: BNL/Rice/UIC prototype readout boards



## **Lightweight Mechanical Structure**

- Goal: light-weight structure with cooling that meet the material budget, thermal and mechanical requirements
- Status: first BTOF prototype produced with CF sheet + form at Purdue, detailed analysis and measurement in progress
- Plan: produce BTOF/FTOF prototypes, and look into support structure and cooling system design by Purdue/NCKU



Preform of





Printed discontinuous



### **Working Packages**



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### **Summary and Outlook**

1. AC-LGAD TOF detectors will provide low p<sub>T</sub> PID and aid track reconstruction at ePIC

- BTOF at r~64 cm with 35 ps timing resolution provide  $3\sigma \pi/K$  separation upto ~1.3 GeV/c
- FTOF at z~185 cm with 25 ps timing resolution provide  $3\sigma \pi/K$  separation upto ~2.4 GeV/c
- $\circ$  Fast (<3ns) and high precision (~30 µm) spatial points provided by AC-LGAD aid track reconstruction through background rejection and momentum resolution improvements
- 2. BTOF and FTOF design based on existing detectors
  - BTOF follows STAR Intermediate Silicon Tracker with strip sensors wire-bonded to ASIC
  - FTOF follows CMS Endcap Timing Layer with pixel sensors bump-bonded to ASIC
  - Active R&D on key components with progresses made in individual components including sensor, ASIC, low mass Kapton flexible PCB, and lightweight support structure. Plan to also study sensor-ASIC integration, module assembly, readout boards, and cooling system in the coming year

Fabrication and assembly plan based on experience with multiple domestic and international institutions with strong technical capabilities and interests. No major integration issue found in initial study. More detailed study of services and integration will be done in coming months
Work on mapping institutions and work packages, fix cost estimate and schedule with CAM

### More Information about AC-LGAD TOF DSC

#### • AC-LGAD TOF DSC

- Mailing list: <u>eic-projdet-tofpid-l@lists.bnl.gov</u>
- Indico page: <u>https://indico.bnl.gov/category/414</u>
- Wiki page and task list: <u>https://wiki.bnl.gov/eic-project-detector/index.php/TOFPID</u>
- Meeting time: Tuesday 9:00am ET

#### • eRD112/eRD109/LGAD Consortium:

- Mailing list: <u>https://mailman.rice.edu/mailman/listinfo/lgads-eic</u>
- Indico page: <u>https://indico.bnl.gov/category/323/</u>
- EIC project R&D proposals: <u>https://wiki.bnl.gov/conferences/index.php?title=Proposals</u>
- Meeting time: Tuesday 9:00am ET

#### • New institutions and collaborators are very welcome to join.

#### Backup

#### **BTOF** for Particle Identification in Simulation



• BTOF with timing resolution of 35 (25) ps can achieve  $3\sigma \pi/K$  separation upto 1.6 (1.8) GeV/c

#### **BTOF Detector Layout**



#### **STAR Intermediate Silicon Tracker**



ePIC BTOF follows cylindrical silicon tracker design (e.g. STAR IST)

- Tilted stave modules overlap in phi to fully cover the azimuthal  $2\pi$  angle
- Readout boards connected to the end of staves are outside of the BTOF acceptance (see next talk)
- Cooling tubes with liquid coolant at room temperature to take the heat generated by frontend ASIC

#### **BTOF Detector Module Conceptual Design**



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### **FTOF Detector Layout**



Forward TOF layout, based on the CMS ETL design:

- Two halves DEEs made of light-weight (carbon fiber) support structure, tiled by rectangular modules of three types with different lengths
- Cooling tubes with coolant at room temperature to take the heat generated by frontend ASICs and other electronic elements

### **FTOF Detector Module Conceptual Design**



Power consumption: ~13 kW (8.5kW for ASIC, 3.5 kW for DC-DC, 1kW for sensors+cable)

- Considering  $0.7 \times 0.7 \text{ mm}^2$  sensor design, which reduces the power budget by ~50%

# **Integration and Services**



#### **Schedule and Timeline**

	2023		2024	2025	2026		2027	2028		2029			2030	2031		2032
Project Milestones																
CD2/3																
IR6 ready for																
CD-4a																
CD4																
bTOF final design																
fTOF final design																
Sensor				-												
R&D																
Pre-production																
Production																
QA																
ASIC						 		 								
R&D																
Pre-production																
Production																
QA																
Module Structure						 		 						 	 	
R&D																
Pre-production						_						<u> </u>				
Production and QA																
Module Assembly								 				<u> </u>				
R&D														 		
Pre-production														 		
Production														 		
QA																
Service						 		 	 					 	 	
R&D															 	
Production			 					 						 	 	
QA																
bTOF installation			 			 		 	 					 	 	
fTOF installation		_			_		-				_					
Software						 		 							 	
Sim. / Rec.																
Database						 		 							 	
Online																