

ePIC Electronics, Readout, & DAQ working group

Part 2 (RDO -> Data Center)

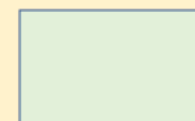
Conveners: Fernando Barbosa (JLAB)
Jin Huang (BNL)
Jeff Landgraf (BNL)

Current Efforts

- RDO
- Slow Controls
- Data Volumes
- DAQ
- Computing
- Connection to S&C
- Streaming WG

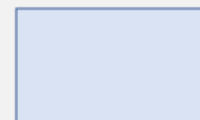
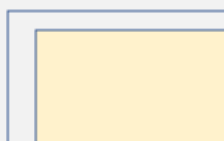
EPIC Electronics / DAQ

Standard Component Names and Functions



Global Timing Unit (GTU)

- Interface between collider, Run Control, & DAM
- Config & Control
- Clock & Timing



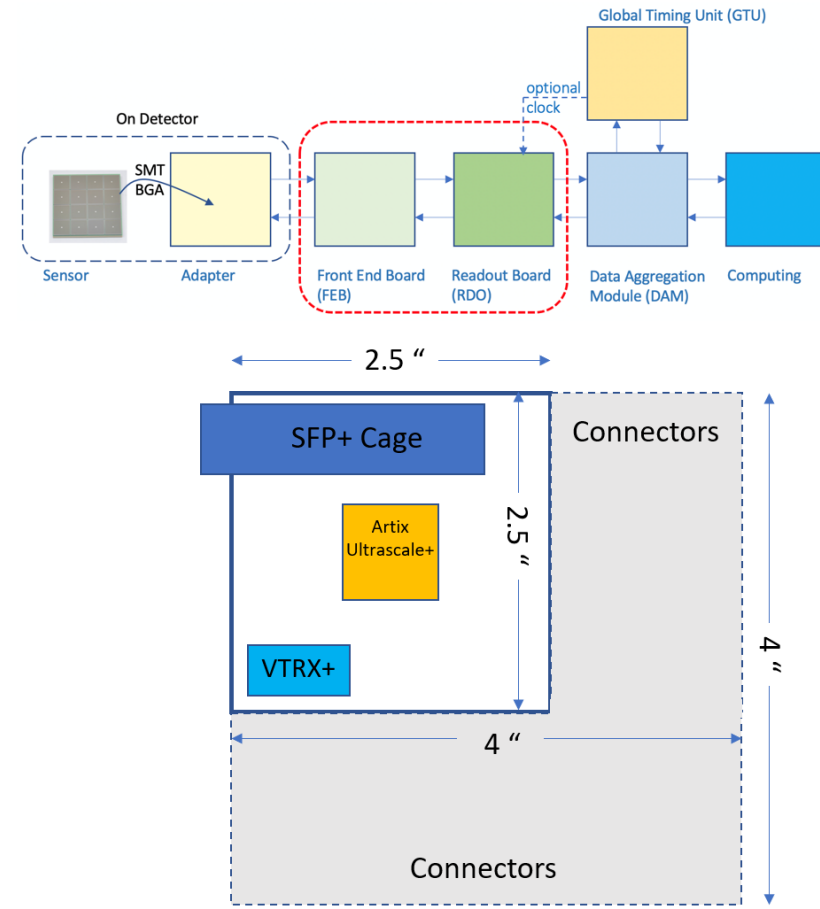
Name	Sensor	Adapter	Front End Board (FEB)	Readout Board (RDO)	Data Aggregation Module (DAM)	Computing
Sharing	Detector Specific	Detector Specific	Detector Specific	Few Variants	Common	Common
Function	-Multi-Channel Sensor	-HV/Bias distribution -HV divider -Interconnect routing	-Amplification -Shaping -Digitization -Zero Suppression	-Communication -Aggregation -Formatting -Data Readout -Config & Control -Clock & Timing	-Computing Interface -Aggregation -Software Trigger -Clock & Timing -Config & Control	-Data buffering and sinking -Run Control -Calibration Support -QA / Scalers -Collider Feedback -Event ID/Building? -Software Trigger -Monitoring
Attributes	-MAPS -AC-LGAD -MCP-PMT -SiPM -LAPPD	-Sensor Specific -Passive	-ASIC/ADC -Discrete -Serial Link	-FPGA -Fiber Link	-Large FPGA -PCIe -Potentially Ethernet	

RDO Discussions

- Physical Characteristics
 - Locations
 - Size
 - Power / Cooling
 - Radiation Requirements
 - Link distances/rates
- Optical Protocol Requirements
 - Timing (5ps / 50-100ps)
 - I2C for ASICs/FEBs
 - Real-Time Command / Control Protocol
 - Data Transfer Protocol (10Gb/s / 25 Gb/s)
- Optical Protocol Choices
 - ePIC – simple custom protocol
 - GPT in FPGA
 - Dedicated Clock/Reconstructed Clock (2 or 3 fibers/RDO?)

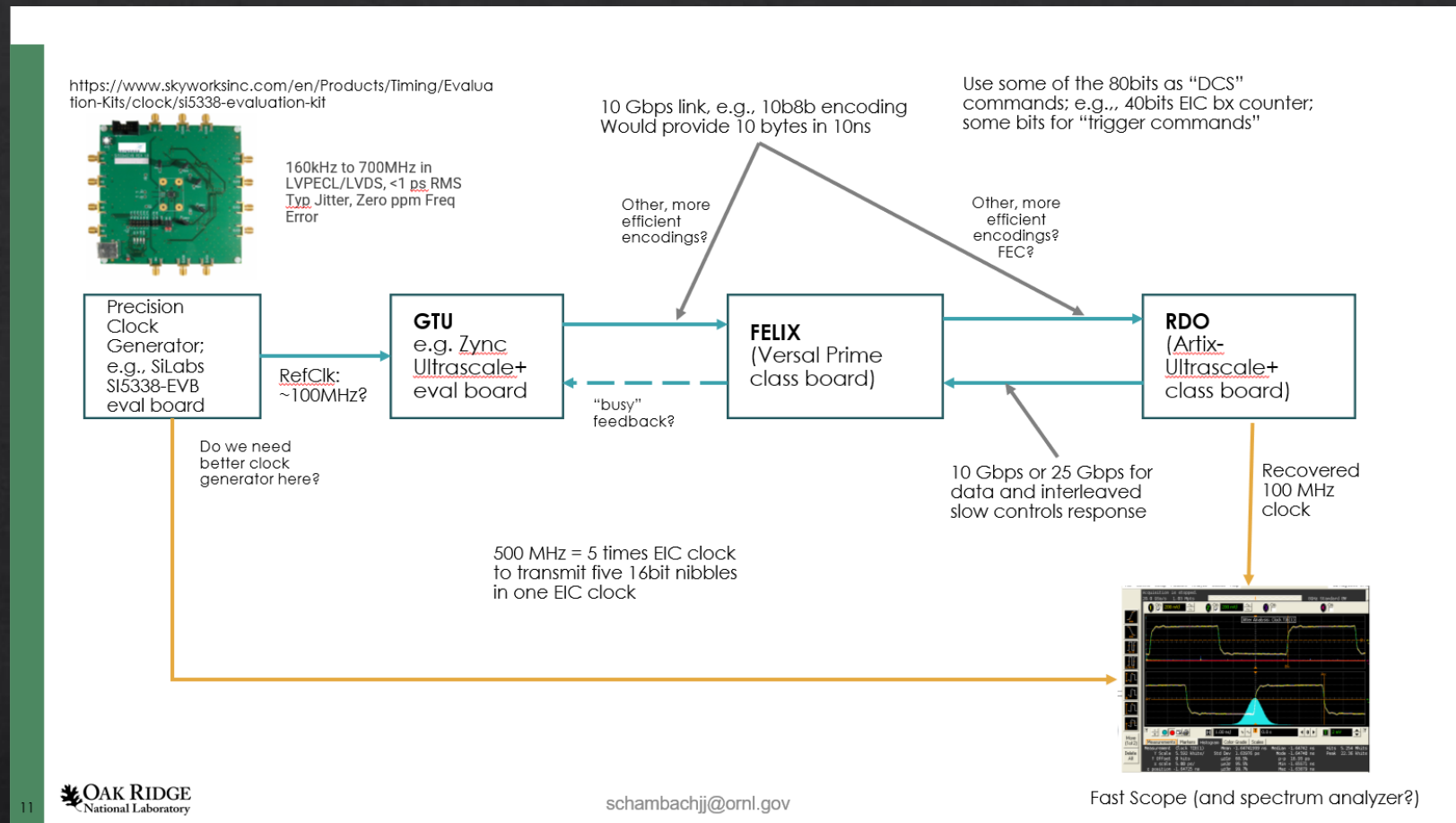
RDO Specifications/Guidance

- Nominally 2.5 in² for common RDO components including FPGA and optical link options (for example if it is integrated on the same PCB as the FEB). For standalone RDO, allow for up to 4 in² to provide space for copper-based connectors to FEBs.
- Power requirements: 3-5 Watts. Allow for at least two LV levels nominally 5V (for optics) and a lower voltage for FPGA power and ASIC signal management.
 - Consider using radiation tolerant switching voltage regulators (e.g. from CERN).
- Multiple optical link interfaces allow for flexible implementation of the RDO as either a standalone readout solution or use with the DAM boards. They can also be used for accepting an alternative low-jitter clock input.
 - Samtec Firefly connectors are also a potential option as they have a footprint similar to VTRX and also provide MTP options.



RDO Discussions

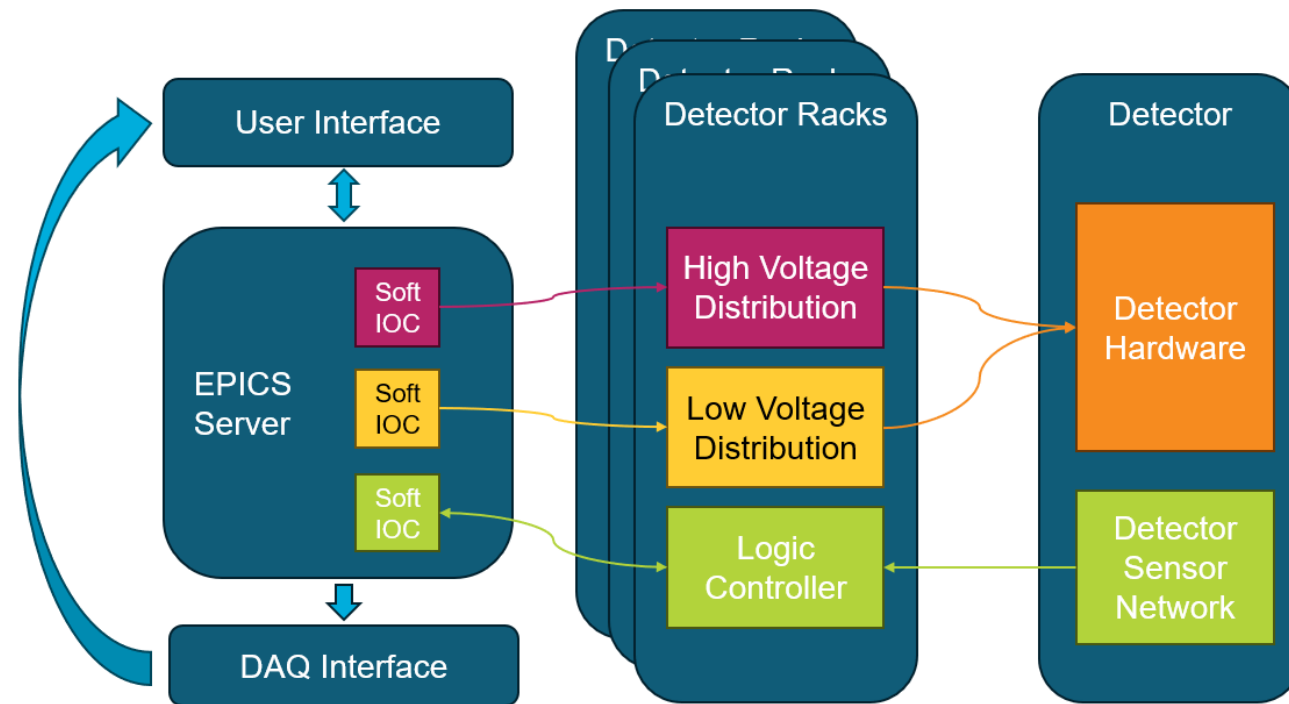
- RDO / Timing subgroup to mock up GTU/DAM/RDO to answer these questions
 - Slow startup due to time constraints of group members
 - Devkits being distributed
 - Arrangements for FELIX 182 slow but progressing
- Hope to start getting answers this fall
 - Protocol document
 - Timing measurements



Slow Controls Integration

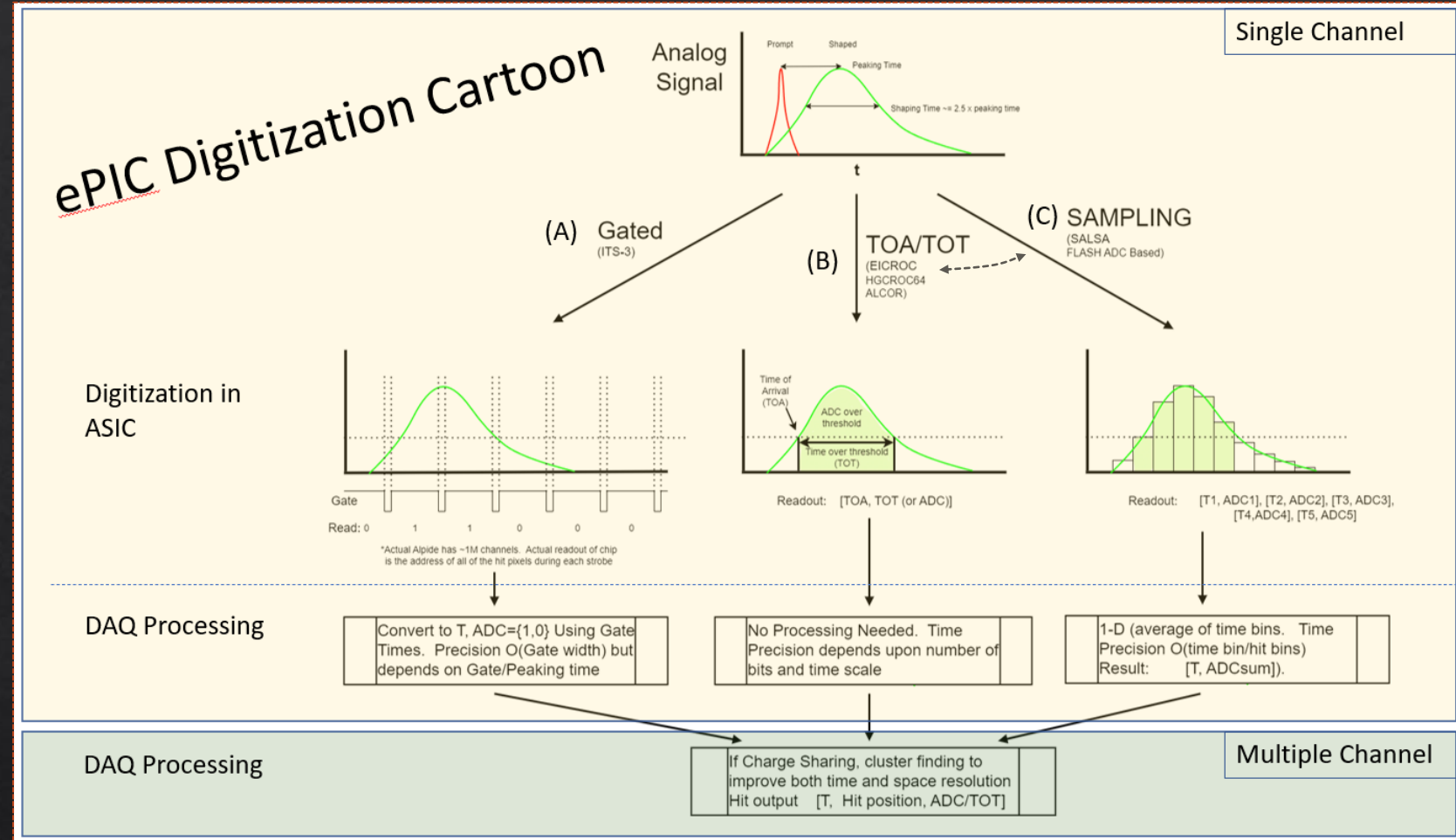
- Listed under 6.10.9 (DAQ) in the project
- The slow controls efforts for each detector listed under the detector
- Integration will
 - Coordinate with collider
 - Coordinate with detector systems (common hardware/software)
 - Provide common computing/network infrastructure
- Project hire (Lee Flader)
- Working with Norbert Novitzky on HCALs as model project
- Standardize to:
 - EPICs for control
 - Allen Bradley for PLC's

ePIC High-Level Plan



Data Volumes

- Distilled volumes from
 - Background Group Simulations provide hits/sec above detector thresholds
 - Synchrotron Radiation
 - Hadron Beam
 - Electron Beam
 - DIS (18x275 scaled to 500khz)
 - Noise estimates from
 - “digitization spreadsheet”
 - E&DAQ WG presentations
 - No charge share/time share
 - Bits / hit = $\frac{\text{Charge Sharing} * \text{Hit Duration} * \text{Bits Per Hit}}{\text{Hit Duration} * \text{Bits Per Hit}}$
 - Cluster finding (where possible) reduces hit size to BitsPerHit
 - Cluster finding (when possible) reduces noise $\times 10^{-5}$
 - Software “triggering” for Far Backward/dRICH
- Charge sharing / Time Sharing / noise estimates should be considered VERY preliminary



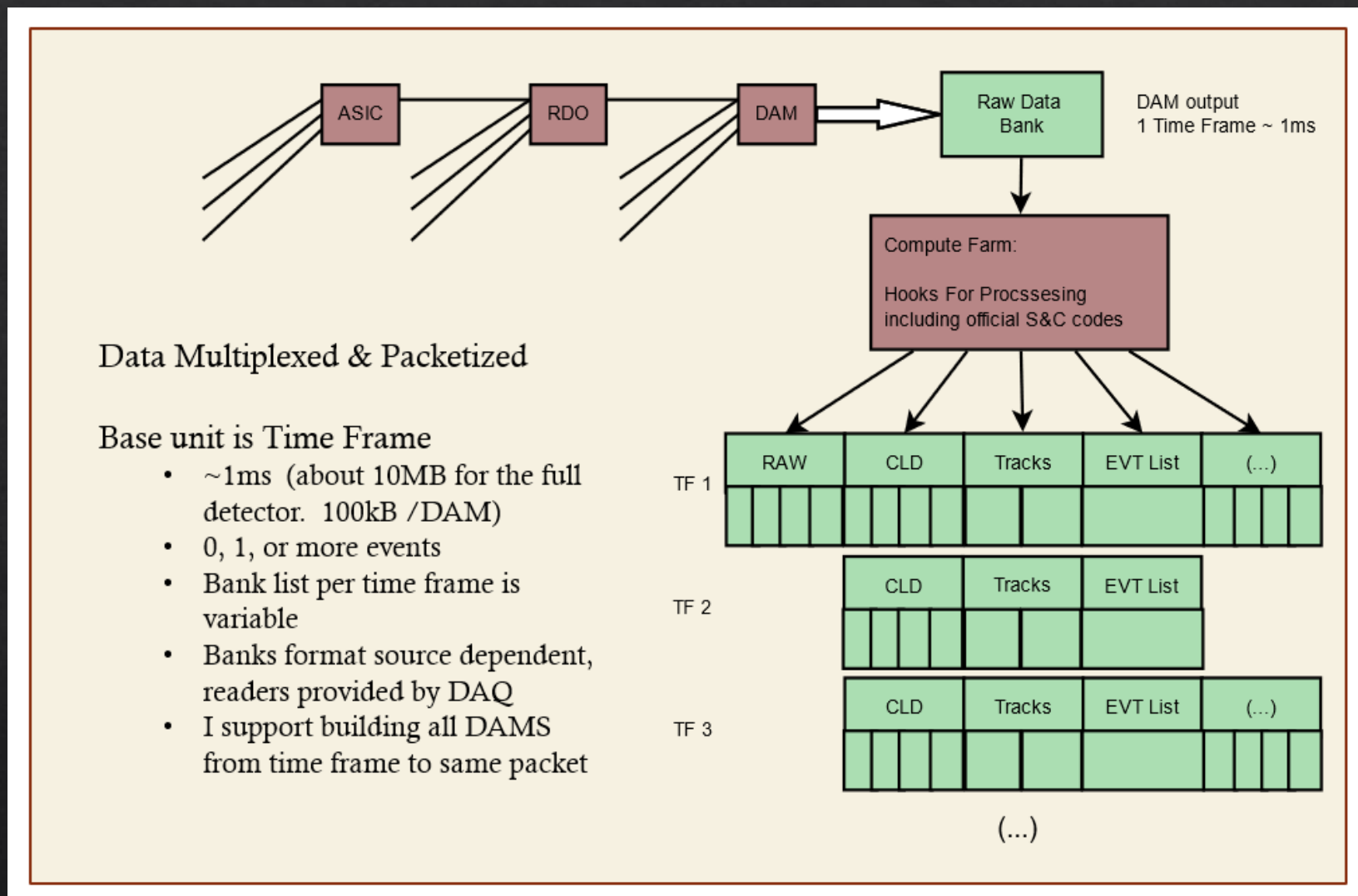
Preliminary Throughput Summary: (no surprises so far!)



See Electronics & DAQ WG indico for 7/20/23 for spreadsheet
 Need to get the granularity to specific channels / FEB / RDO
 These need to be formalized and incorporated into S&C metrics

DAQ Computing

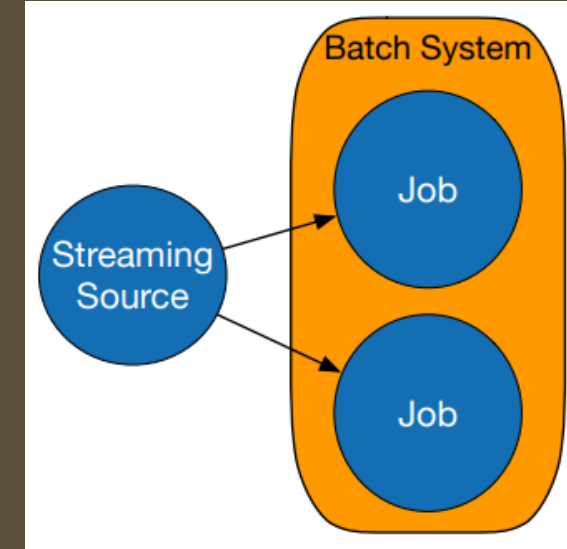
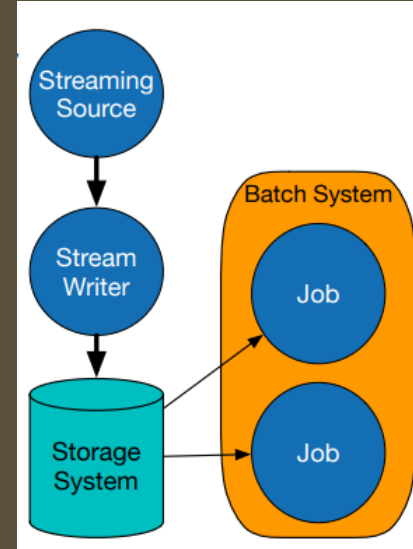
- Time Frames (~1ms)
 - Up to ~500 events
 - ~10MB output data
 - ~100kB avg / DAM
- Routing data
- Formatting data
- Processing data
 - DAM FPGA & CPUs
 - Cluster finding
 - Software triggering
 - Sanity Checkers
 - QA Monitoring
 - Metadata
 - Slow controls integration
- Scalers / continuously running DAQ components



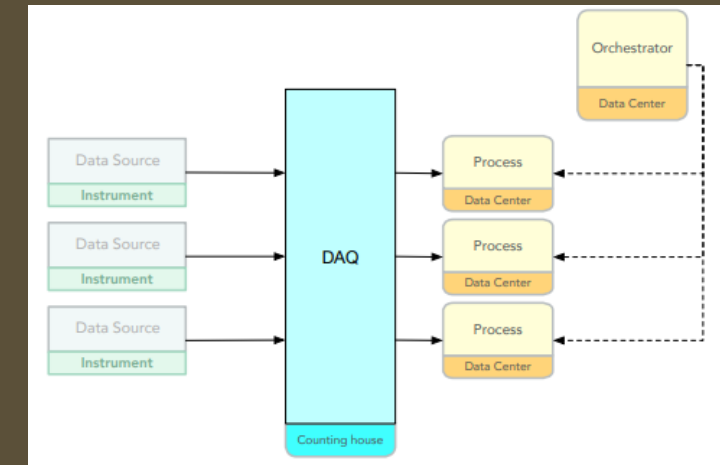
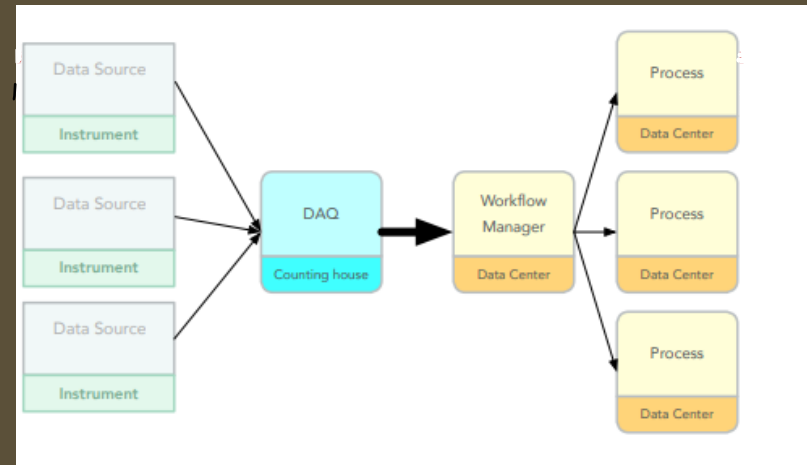
S&C Streaming DAQ WG

- Two streaming concepts
 - (Electronic) No Level-0 trigger
 - (Institutional) Rapid turn around of reconstructed data (streaming as opposed to batch processing)
- The focus of the group is the institutional requirements and organization
 - International Collaboration
 - Tasks to be done and associated institutional requirements
 - Support for streaming model
 - Automated data handling
 - Automated calibration tools
 - Automated monitoring tools
- We expect this may lead also to links between the DAQ and the streaming reconstruction for rapid turn around of critical information such as calibrations

Batch options: (reconstruction is human driven)



Streaming options: (reconstruction is data driven)



Graham Heyes

Questions?