NEEDS AND REQUIREMENTS TO A NEW TDC

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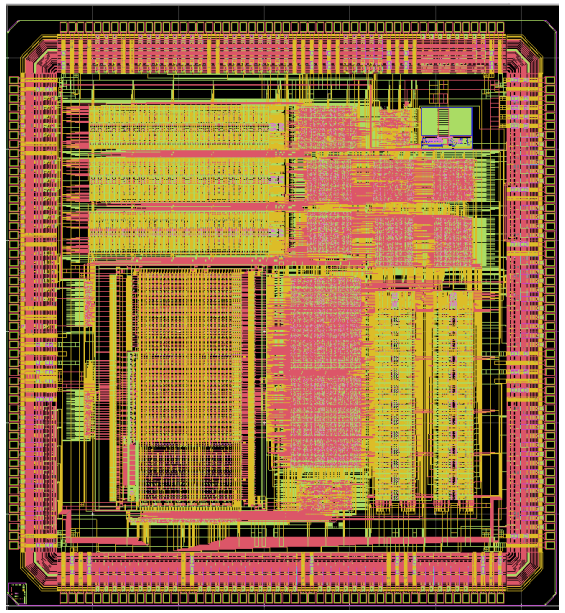
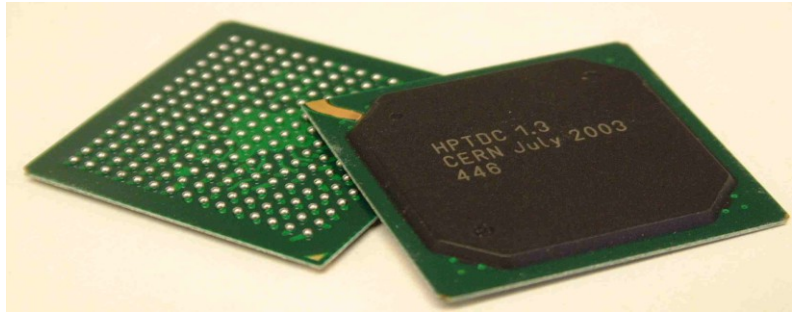
HPTDC

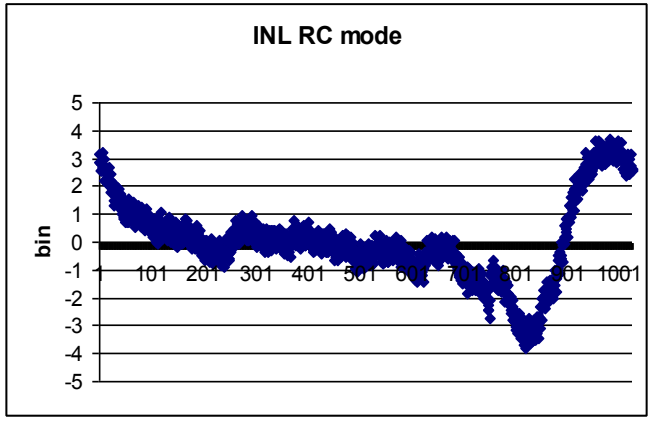
- HPTDC used in large number (>20) of HEP applications:
  - ALICE TOF, CMS muon, STAR, BES, KABES, , ,
  - Commercial modules: CAEN, Cronologic, Bluesky
- ~50k chips produced
- 250nm technology (in principle still available)
  - New production masks required.
  - Packaging problems (original company does not anymore support this package)
  - Production test based on old obsolete IC tester
  - Process trimming to get internal memories to work reliable
- Few thousand chips still on stock.
- Design and production effort:
  - ~ 6-8 man years



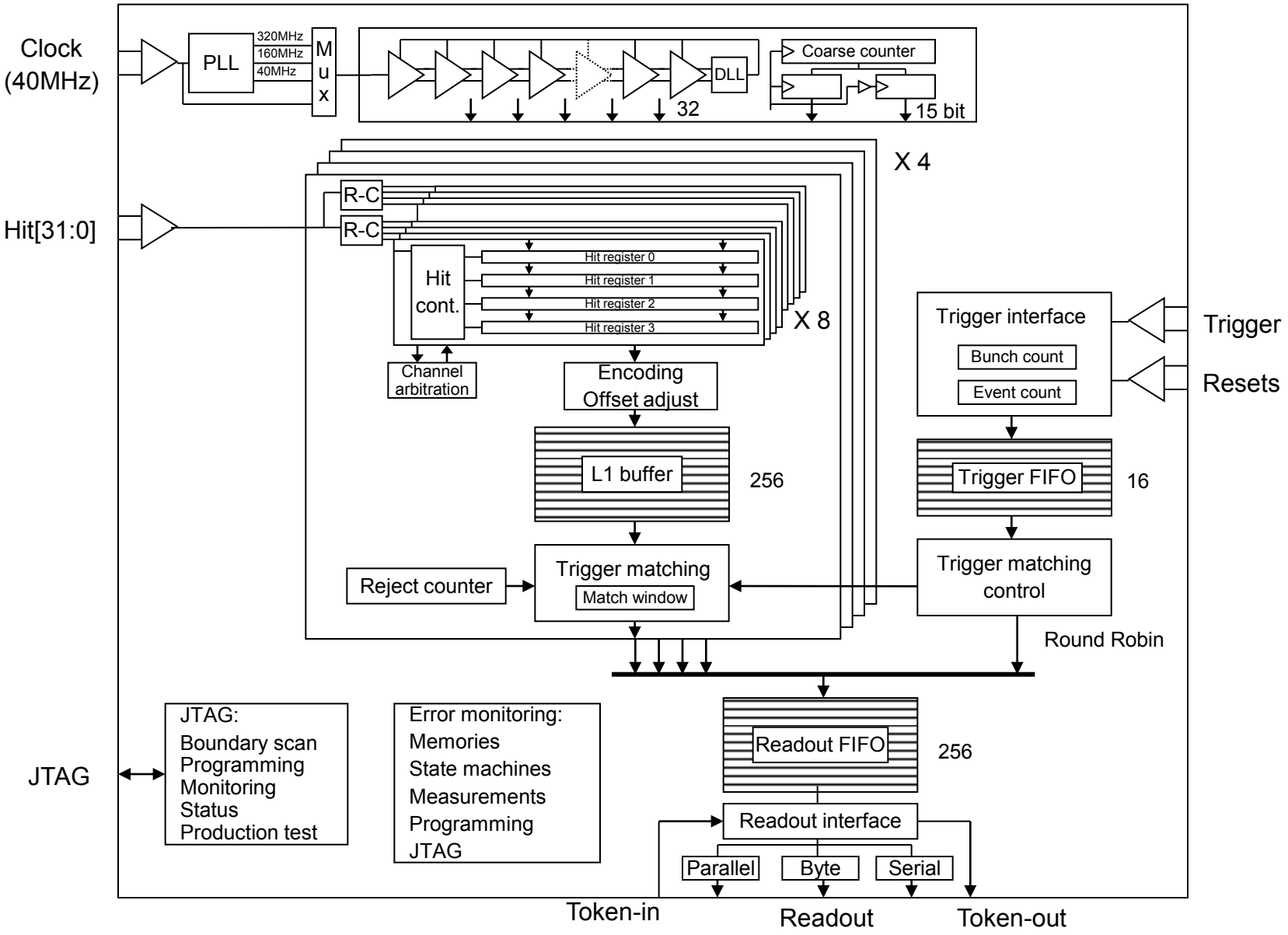


HPTDC features

- 32 channels(100ps binning) or 8 channels (25ps binning)
- LVDS (differential) or LVTTL (single ended) inputs
- 40MHz time reference (LHC clock)
- Leading, trailing edge and time over threshold (for leading edge time corrections)
- Non triggered
- Triggered with programmable latency, window and overlapping triggers
- Buffering: 4 per channel, 256 per group of 8 channels, 256 readout fifo
- Token based readout with parallel, byte-wise or serial interface
- JTAG control, monitoring and test interface
- SEU error detection.
- Power consumption: 0.5W – 1.5W depending on operating mode.
- Problems:
  - INL correction required to benefit from 25ps binning (substrate coupling from logic part of chip)
    40ps RMS without INL correction
    17ps RMS with INL correction
  - Reliability problem in on-chip memory resolved by process trimming

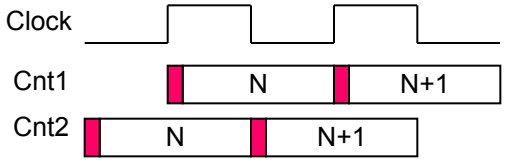


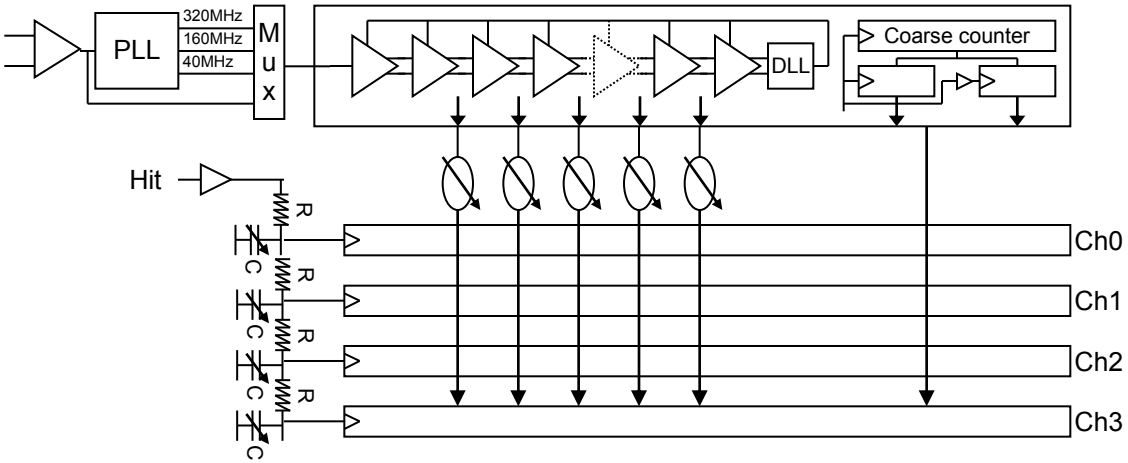
Good old HPTDC



Time measurement

- Combination of
  - Counter with PLL for clock multiplication (x1, x4, x8)
    - Double phase shifted counters to resolve possible metastability in coarse count measurement.
  - DLL with 32 taps for clock interpolation
    - Use of differential delay cell for power supply noise immunity
  - R-C delay line on hit signals for very high resolution
    - Channel reduction by factor 4 (8 channels per chip)





Low resolution: 781 ps

Medium resolution: 195 ps

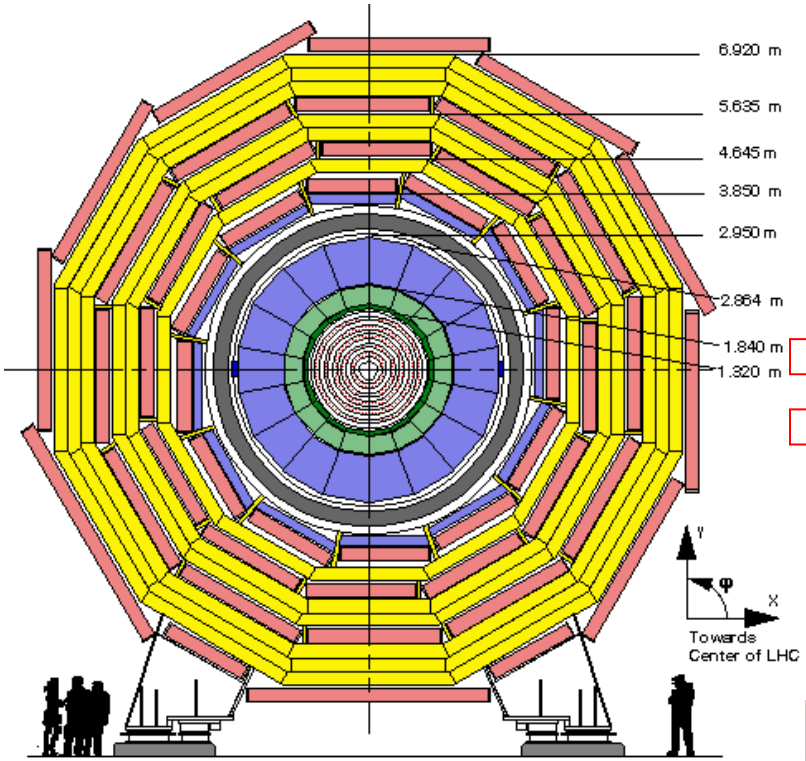
High resolution: 98ps

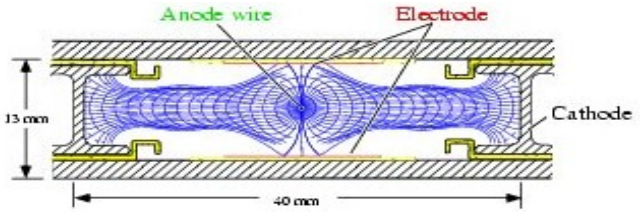
Very high resolution: 24ps (8 channels)

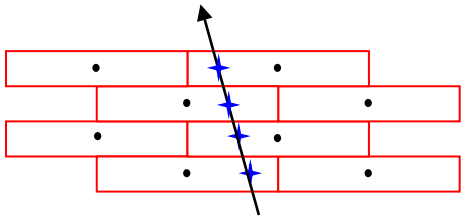
Very high resolution

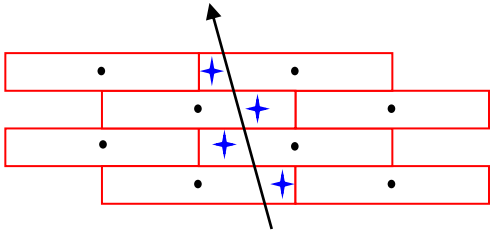
R-C delay line dependent on IC processing (Only small difference between chips seen)
R-C delay line independent of temperature in range of 20 deg
Infrequent calibration required
Calibration can be obtained with code density test with physics hits
Option of correcting integral errors from DLL
8 channels per chip
Not possible to pair leading and trailing edges

CMS muon detector (drift time)

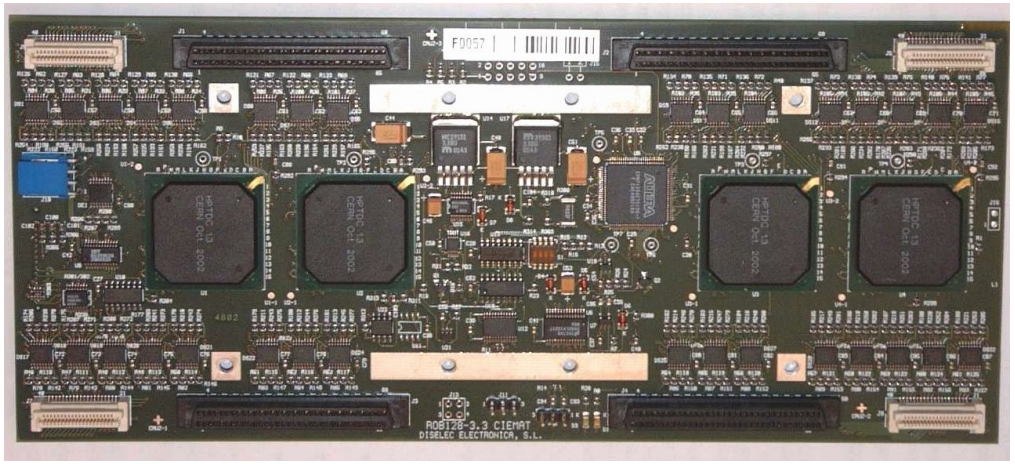




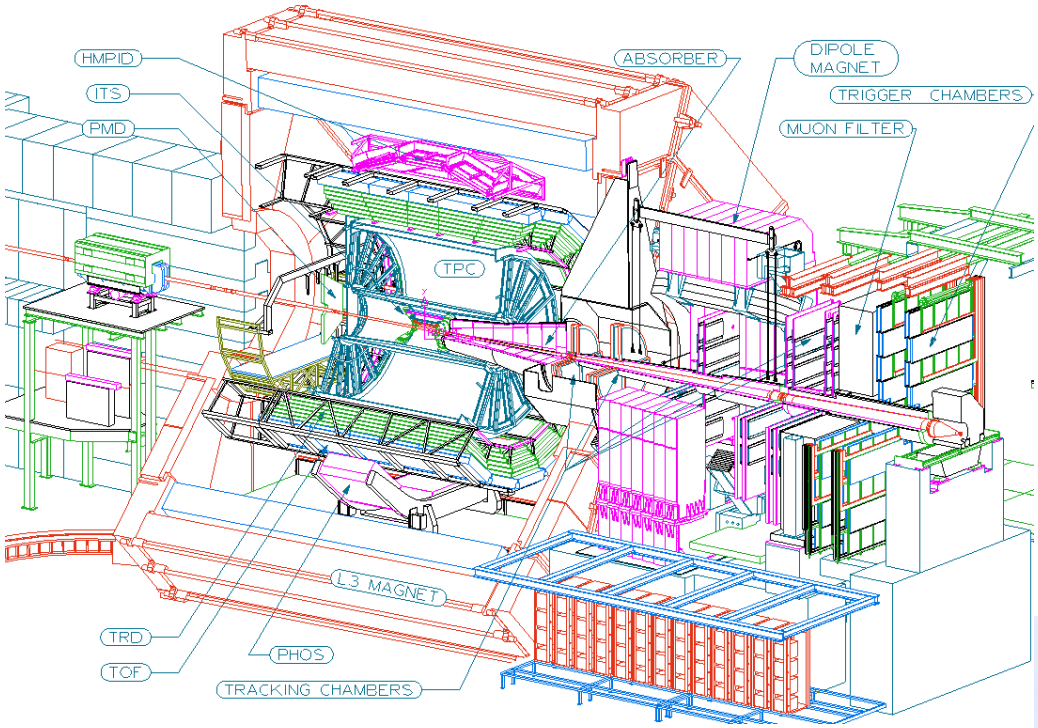


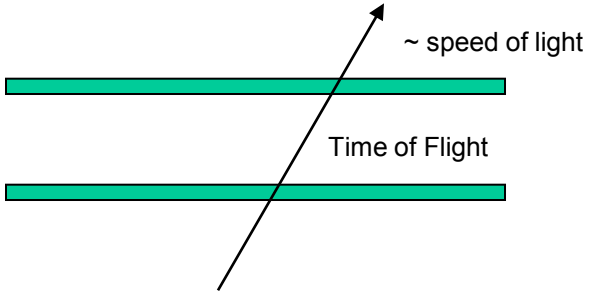


- 200.000 channels
- ~1ns resolution
- 10 – 100khz hit rate
- 100khz trigger rate
- 3.2 us trigger latency
- ~500ns trigger window

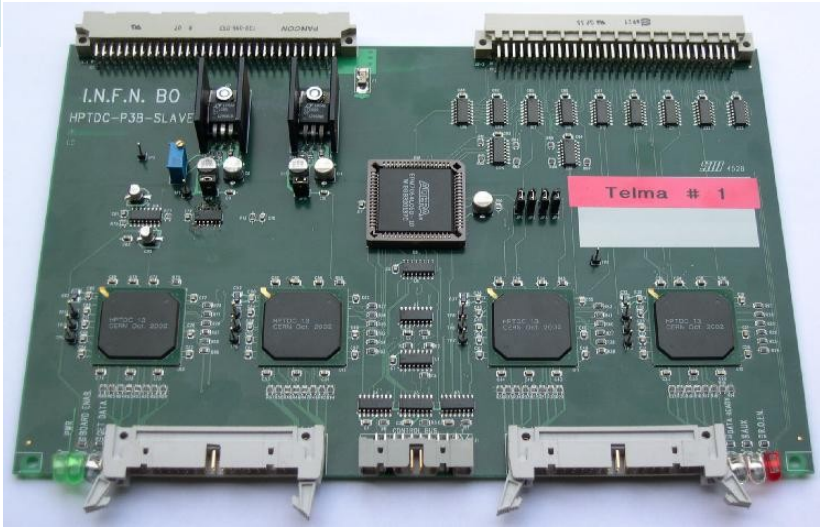


ALICE Time Of Flight (TOF)





- ~25 ps resolution
- 160.000 channels
- Low hit rate: few tens of kHz
- Trigger rate: few kHz
- Trigger latency: 6.7 us
- Trigger window: 100ns



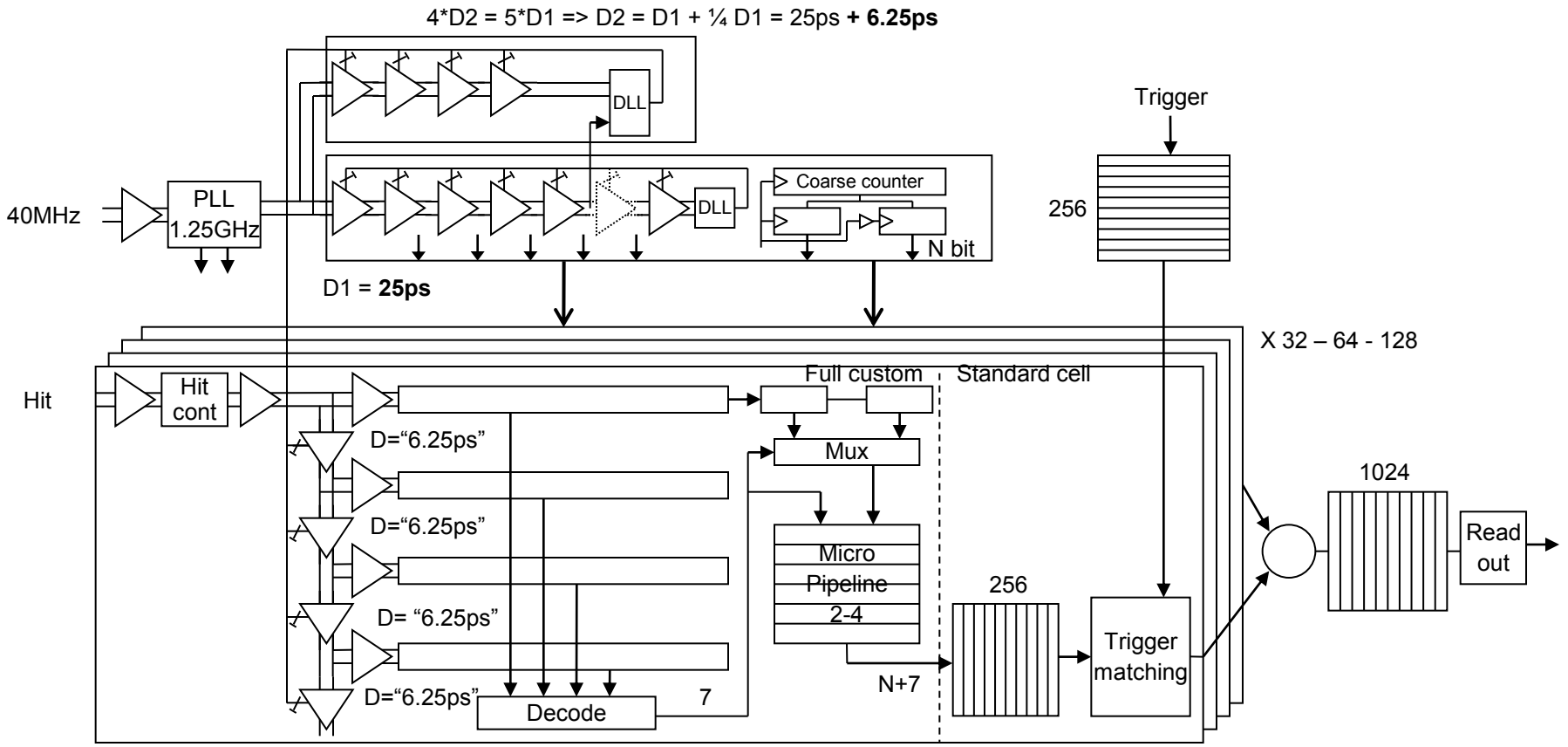
New TDC

- Needs for different HEP projects ?.
  - Especially at CERN (good justification for us)
- Requirements: time resolution, channels, triggering, buffering, readout, radiation tolerance , , ?
  - High resolution (~10ps) : TOF type applications
  - Low resolution (~1ns): Drift time measurements (can be done with FPGA's but rad tol an issue)
- Analog front-end often application specific (e.g. NINO)
- Collaboration to assemble sufficient resources (manpower and money) ?
- Other ongoing TDC developments ?

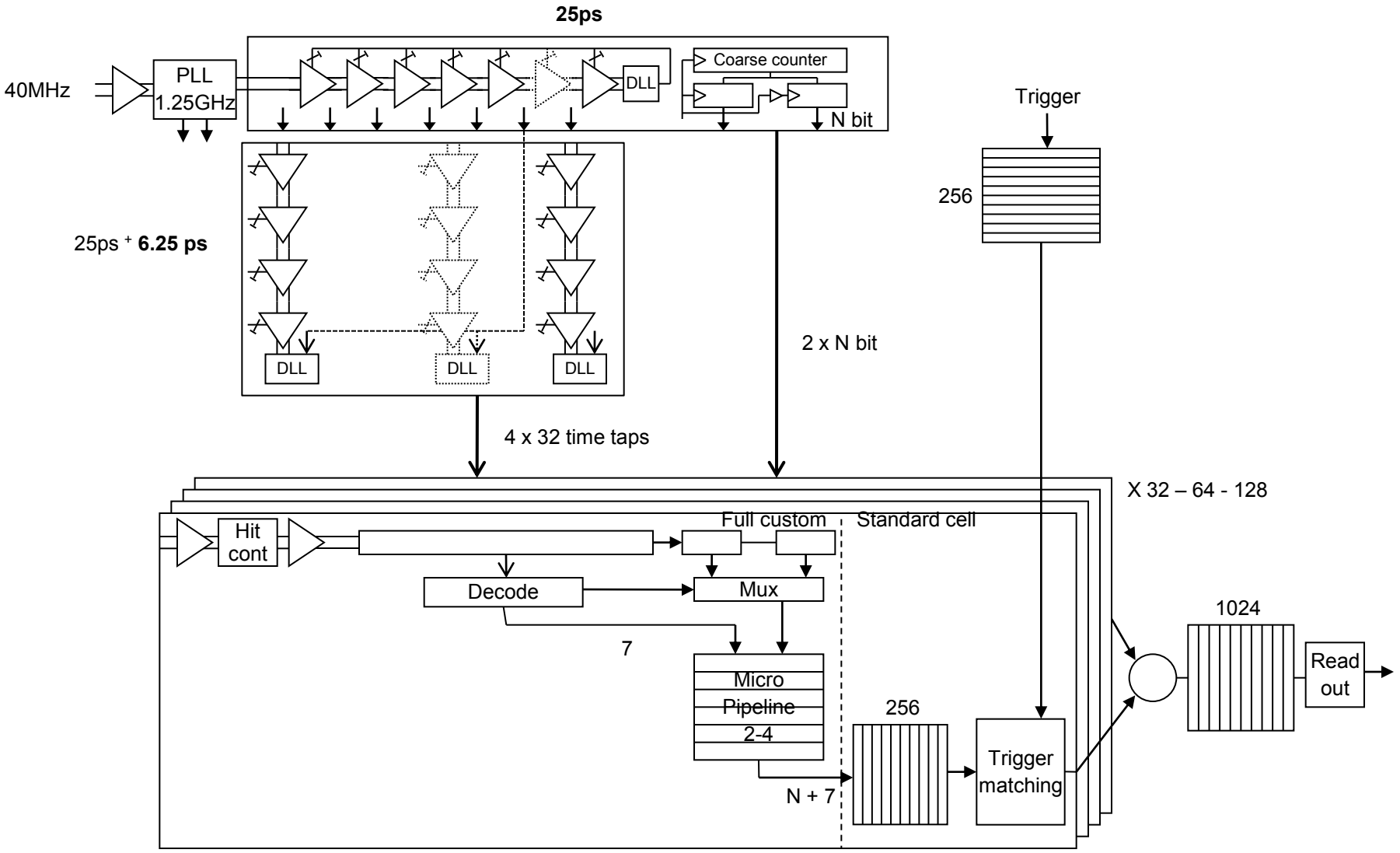
Possible spec based on HPTDC

- 32, 64 or 128 channels with 6.25ps binning
  - (ideal 6.25ps binning -> RMS resolution = 1.8ps)
  - Lower power mode for 25ps (800ps ?)
- SLVS (low voltage differential) inputs with on-chip termination.
- 40MHz time reference
- Leading, trailing, and TOT measurements.
- Features to enable TDC measurements at different thresholds on same channel (Depending on analog front-end)
- Non triggered
- Triggered with programmable latency, window and overlapping triggers.
- Buffering: 256 per channel, 1024 (or 4k) readout fifo.
- Serial readout compatible with Elink of the GBT optical link chip.
- Parallel readout.
- Control/monitoring via JTAG (or I2C) or Elink.
- SEU detection/protection.
- Power consumption: 1 – 2 W depending on operation mode.
- Implementation: 130nm CMOS (25ps delay cell possible)

Possible architecture 1



Architecture 2



Architecture 3

Way ahead

- Doctoral student designing timing core (6.25ps)
  - Test chip in 1-2 years time for test
- Verilog model from HPTDC can be adapted/modified
- Political justification to go for full chip
  - 2-3 man years for full design if working timing macro.
  - 1 man year test and qualifications
  - 1 man year to prepare production (test, packaging, etc.)
- Contributions/collaboration from others ?.
  - Design
  - Test and qualification
- Possible contributions from companies (CAEN, other) will be discussed separately.

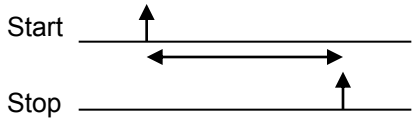
Back up slides

Outline

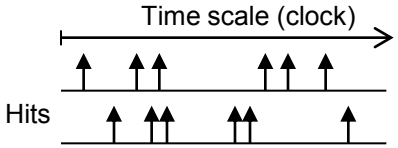
- What is a TDC and its use
- Applications of TDC's in high energy physics
- General requirements
- TDC principles
- Pipelined versus data driven
- HPTDC architecture
- Time measurement in HPTDC
- Data buffering
- SEU detection
- JTAG
- Implementation
- Timing performance
- Current status and encountered problems
- Users
- Summary

What is a TDC and its use

- TDC's are used to measure time (intervals) with high precision
  - Start – stop measurement
    - Measurement of time interval between two events:
      start signal – stop signal
    - Used to measure relatively short time intervals with high precision
    - Like a stop watch used to measure sport competitions



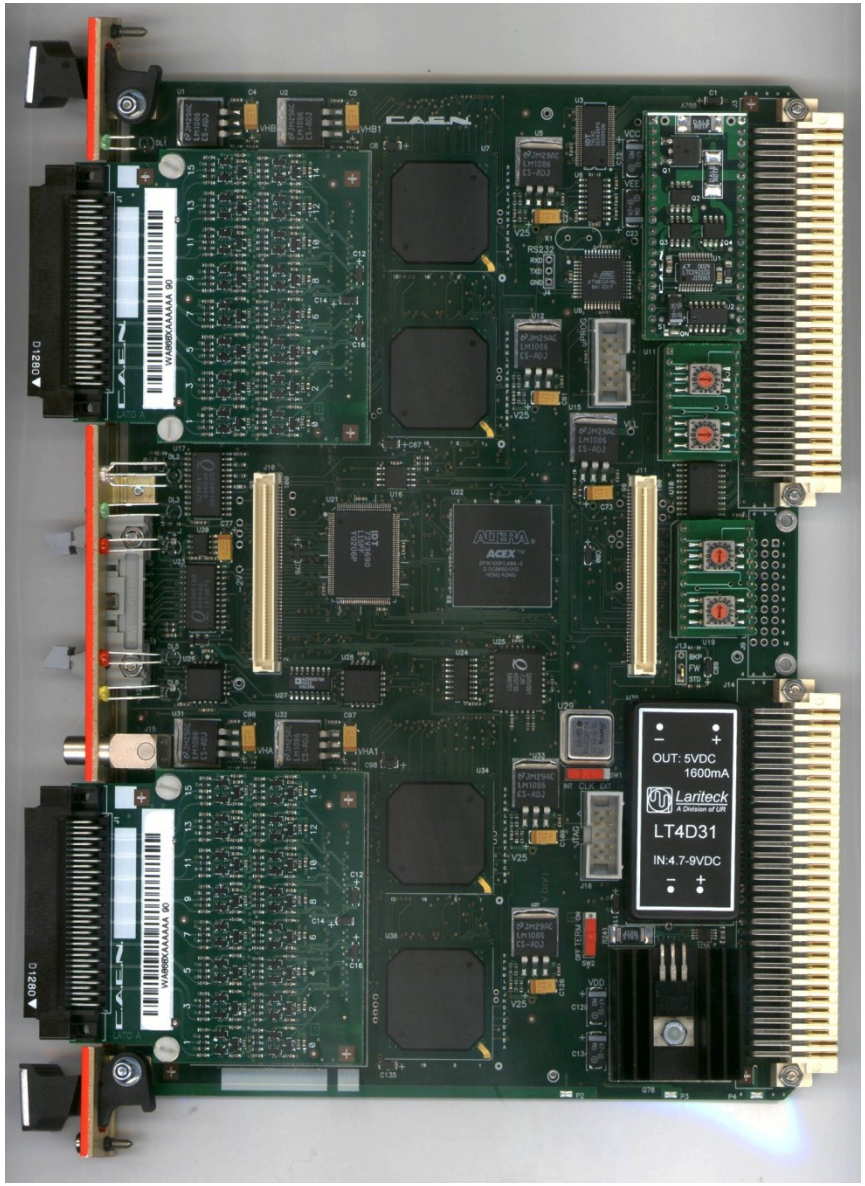
  - Time tagging
    - Measure time of occurrence of events with a given time reference
      Time reference (Clock)
      Events to be measured (Hit)
    - Used to measure relative occurrence of many events on a defined time scale
      - Such a time scale will have limited range:
        like 12 hour or 24 hour time scale on your watch when having no date and year
    - Like a normal watch



- Special needs for high energy physics
  - Many thousands of channels needed
  - Rate of measurements can be very high
  - Very high resolution
  - A mechanism to store measurements during a given interval and extract only those related to an interesting event, signaled by a trigger, must be integrated with TDC function
- Other applications
  - Laser/radar ranging (e.g. measure distance between cars, etc.)
  - Time delay reflection (TDM) to measure location of broken fiber
  - Most other applications only needs one or a few channels per system

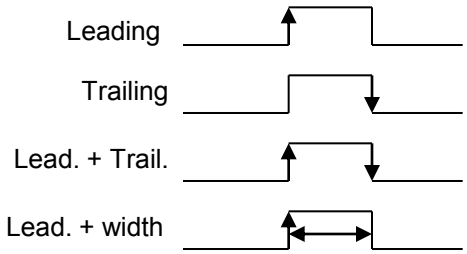
CAEN general purpose TDC board

- 128 ECL/LVDS inputs, 110 Ω impedance
- 800ps/200ps/100ps LSB selectable
  (special version for 25ps, 64 channels)
- Deadtimeless Multihit
- 5 ns double hit resolution
- Rising and falling edge detection
- Trigger Matching, Continuous Storage
- Flexible VME interface
- Embedded Data Processing mezzanine



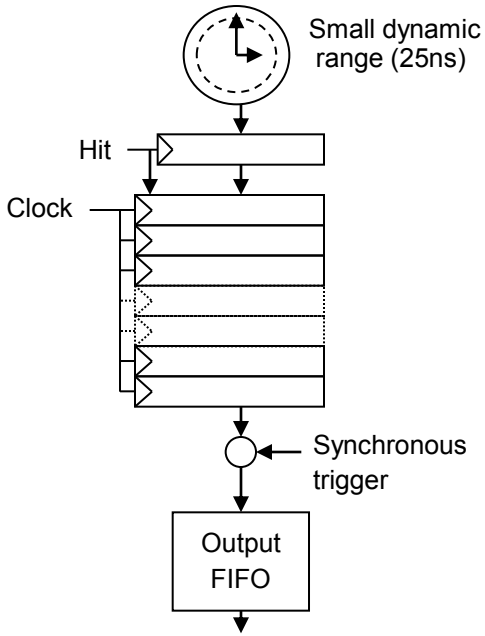
General HPTDC requirements

- High resolution for ALICE Time Of Flight (25 ps)
- Low resolution for CMS muon detector (1 ns)
- Multiple use of TDC's in other HEP experiments
- Dynamic range: One LHC machine cycle (12 bit 40Mhz counter)
- Hit rate: Few Hz - few MHz
- Leading edge and/or Trailing edge,
  or Paired leading edge + Width (not in VHR)
- High integration level (32/8 channels per TDC)
- LVDS or TTL hit inputs
- Self calibrating using 40MHz clock reference (must be low jitter)
- Triggered or not triggered
- Trigger latency: 4.0, 3.2, 2.4, 1.2 us (programmable)
- Trigger rate: Few KHz to few hundred KHz (1MHz)
- Radiation: Total dose below 10Krad, SEU detection
- Low power
- JTAG boundary scan
- **High flexibility**



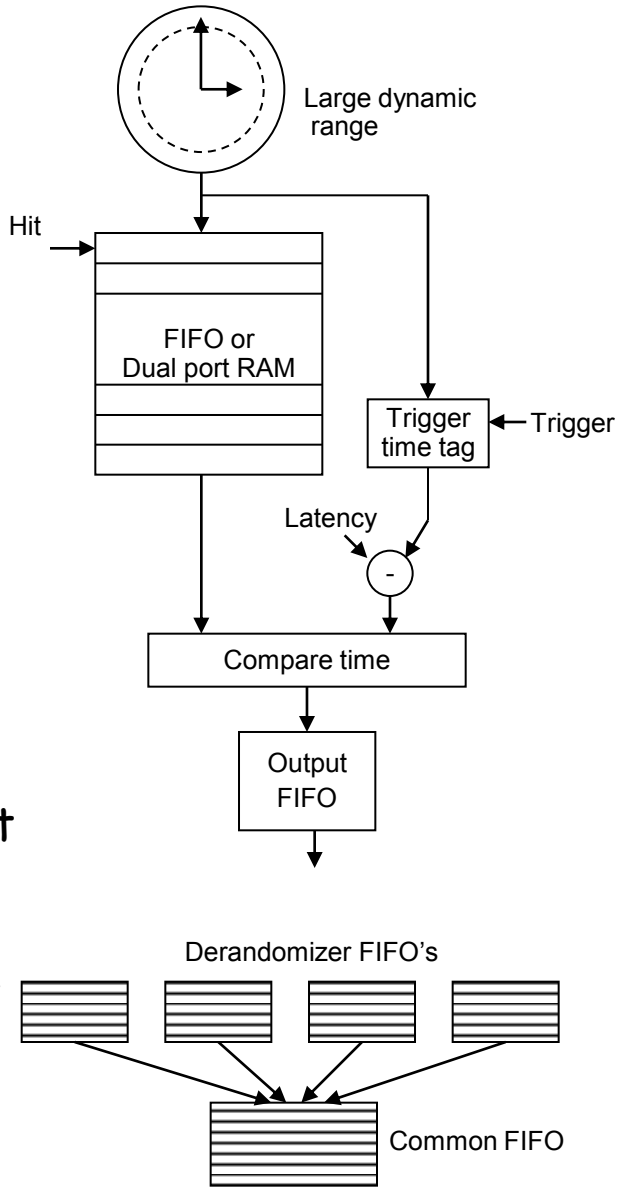
Pipelined TDC architecture

- Stores hit data every clock cycle (25ns)
- High hit rates (one per clock cycle)
- Fixed dead time
  But limited double pulse resolution
- Fixed trigger latency
  (limited by buffer size)
- Only useful in triggered mode
- Difficult to support overlapping triggers
- No problem with buffer occupancies
- Narrow but deep latency buffer
  (covers 25ns)
- Little sensitive to SEU in control part
- Simple architecture -> quick implementation
- **Limited flexibility**



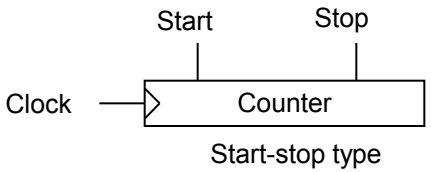
Data driven TDC

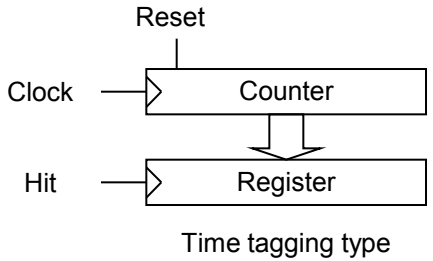
- Only stores data when hit detected
- Variable latency over full (1/4) dynamic range
  Compromise between hit rate and latency
- Triggered / non triggered mode
- Multiple overlapping triggers
- Channel merging possible via derandomizers
  Limits hit rates
- Good double pulse resolution
  But complicated dead time analysis
- Buffer occupancies must be seriously analyzed
- Buffer overflows must be handled carefully
  - Hit may be lost if marked
  - Complete events must never be lost
- Wide latency buffer (covers full dynamic range)
- More complicated architecture/implementation
  Previous data driven TDC worked well in different applications
  - Logic complication handled by logic synthesis
  - Extended verifications at behavioral/register/gate level
- High flexibility

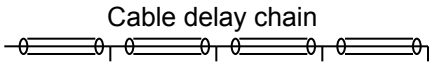


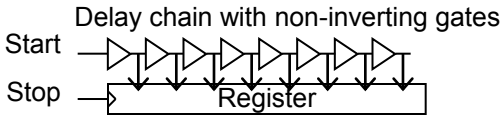
Basic TDC principles

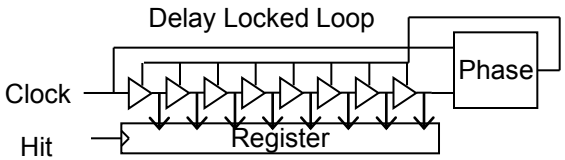
- Counter type
  - Advantages
    - Simple
    - Digital
    - large dynamic range possible
    - Easy to integrate many channels per chip
  - Disadvantages
    - Limited time resolution (1ns in modern CMOS technology)
    - Metastability (use of Gray code counter)
- Single Delay chain type
  - Cable delay chain (distributed L-C)
    - Very good resolution (5ps mm)
    - Not easy to integrate on integrated circuits
  - Simple delay chain using active "gates"
    - Good resolution (~100ps in modern tech.)
    - Limited dynamic range (long delay chain and register)
    - Only start-stop type
    - Large delay variations between chips and with temperature and supply voltage
  - Delay locked loop
    - Self calibrating using external frequency reference (clock)
    - Allows combination with counter (see later)
    - Delicate feedback loop design (jitter)
  - R-C delay chain
    - Very good resolution
    - Signal slew rate deteriorates.
    - Delay chain with losses so only short delay chain possible
    - Large sensitivity to process parameters (and temperature)

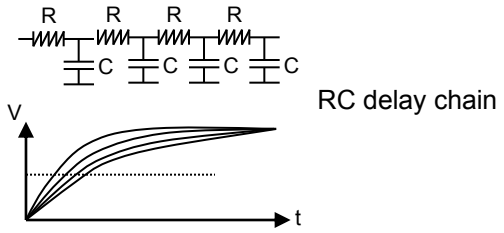




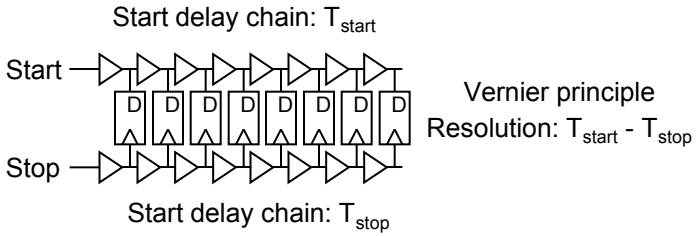


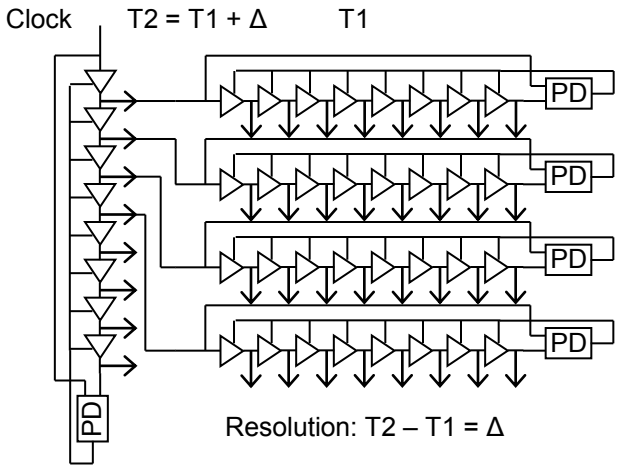




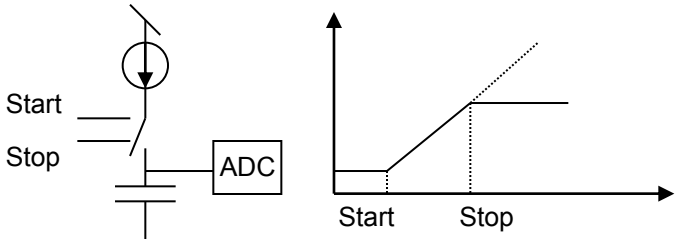


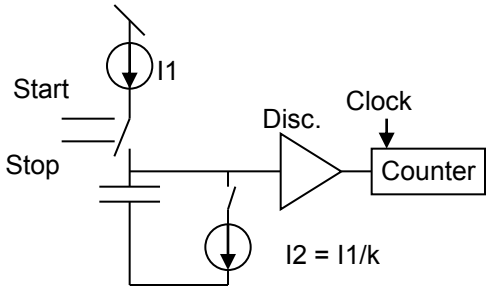
- Multiple delay chain type
  - Vernier delay chain types
    - Resolution determined by delay difference between two chains. Delay difference can be made very small and very high resolution can be obtained.
    - Small dynamic range (long chains)
    - Delay chains can not be directly calibrated using DLL
    - Matching between delay cells becomes critical
  - Coupled Delay Locked loops
    - Sub-delay cell resolution ($\frac{1}{4}$)
    - All DLLs use common time reference (clock)
    - Common timing generator for multiple channels
    - Jitter analysis not trivial

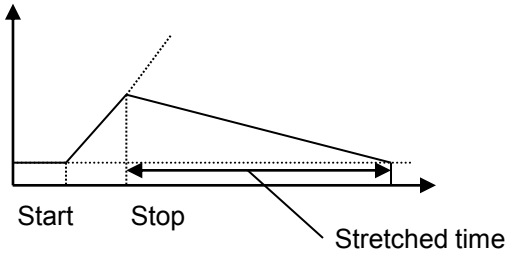




- Charge integration
  - Using ADC
    - High resolution
    - Low dynamic range
    - Sensitive analog design
    - Low hit rate
    - Requires ADC
  - Using double slope (time stretcher)
    - No need for ADC (substituted with a counter)
- Plus multiple "exotic" architectures
  - Heavily coupled Phase Locked Loops
  - Beating between two PLLs
  - Re-circulating delay loops
  - Summing of signals with different slew rates
- If any of you have a bright idea let me know !.
    - But must be implementable in IC.



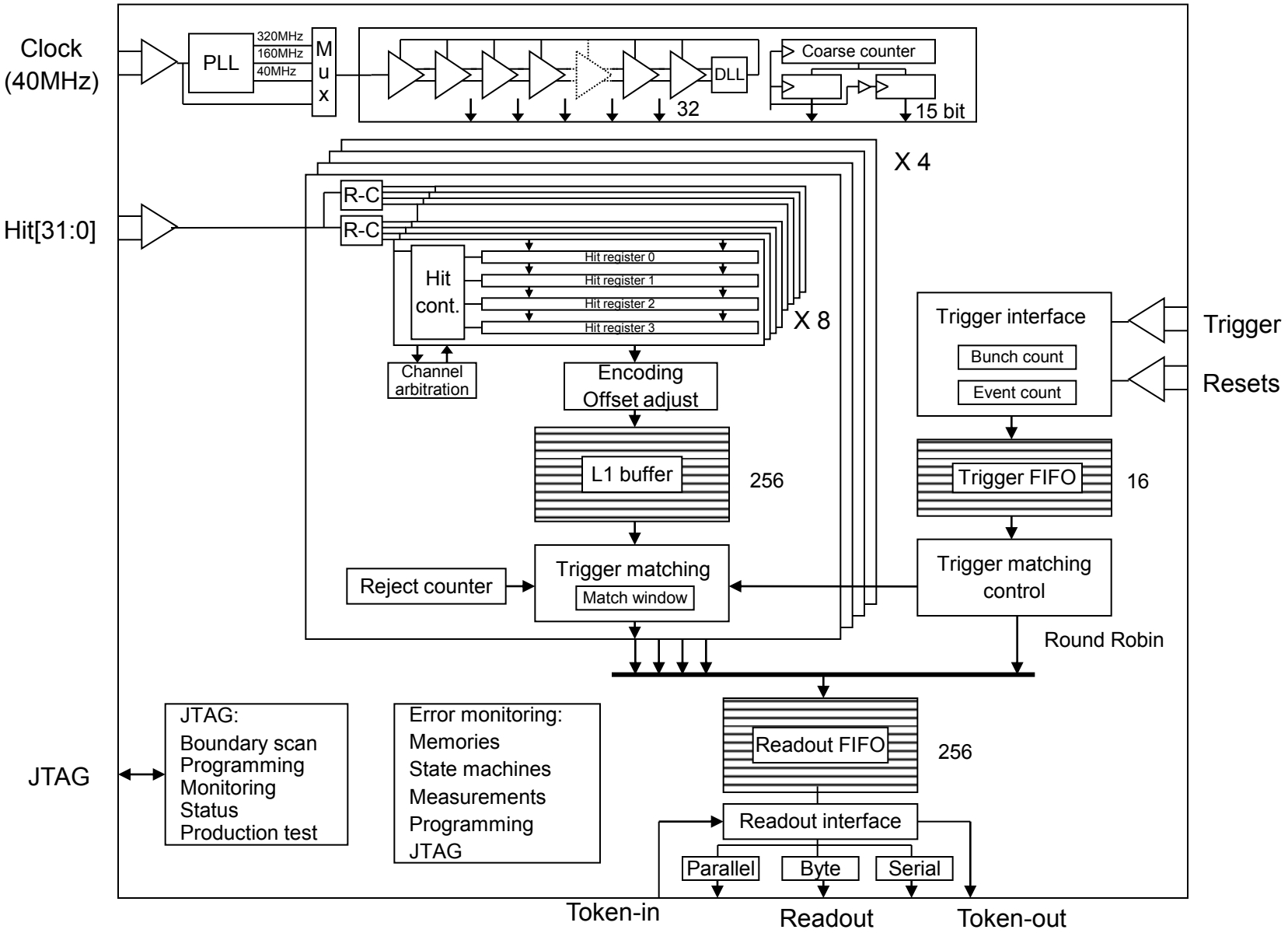




How to compare TDC's

- Merits
  - Resolution
    - Bin size
    - Effective resolution (RMS, INL, DNL)
      - I have seen many ways of giving timing performance that does not give an "honest" effective resolution measure
  - Dynamic range
  - Stability
    - Use of external reference
    - Drift (e.g. temperature)
    - Jitter
    - Noise
  - Integration issues:
    - Digital/analog
    - Noise / power supply sensitivity
    - Sensitivity to matching of active elements
    - Required IC area
    - Common timing block/ per channel
    - Time critical block must be implemented on chip together with noisy digital logic
- Use in final system
    - Can one actually use effectively very high time resolution in large systems (detectors)
    - Calibration - stability
    - Distribution of timing reference (start signal or reference clock)
    - Other features: data buffering, triggering, readout, test, radiation, etc.

HPTDC architecture



Time measurement

- Combination of
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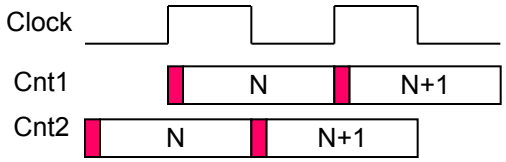
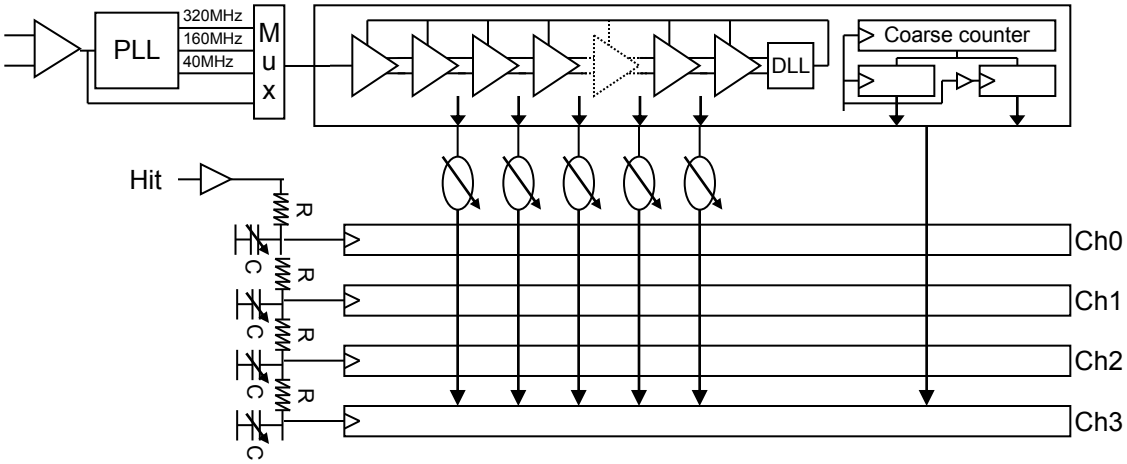
    - Double phase shifted counters to resolve possible metastability in coarse count measurement.
  - DLL with 32 taps for clock interpolation
    - Use of differential delay cell for power supply noise immunity
  - R-C delay line on hit signals for very high resolution
    - Channel reduction by factor 4 (8 channels per chip)





Low resolution: 781 ps

Medium resolution: 195 ps

High resolution: 98ps

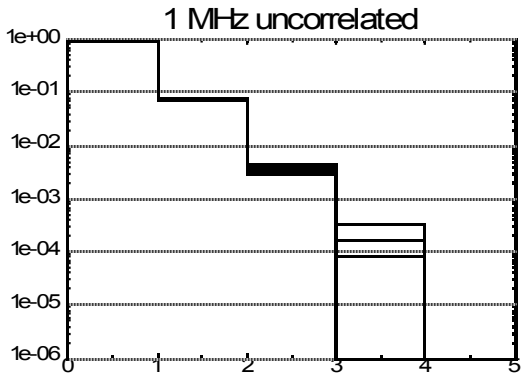
Very high resolution: 24ps (8 channels)

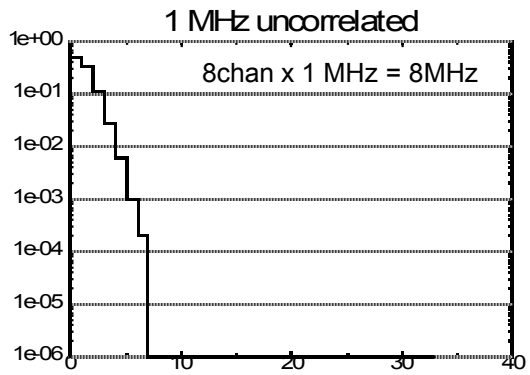
Very high resolution

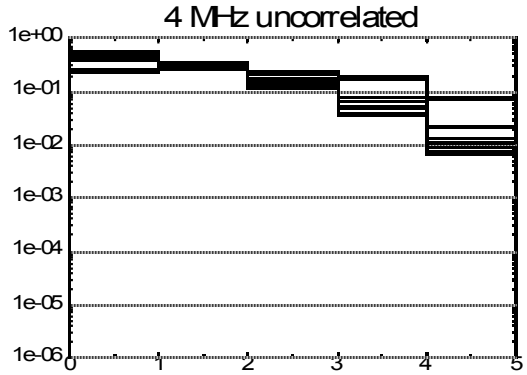
R-C delay line dependent on IC processing (Only small difference between chips seen)
R-C delay line independent of temperature in range of 20 deg
Infrequent calibration required
Calibration can be obtained with code density test with physics hits
Option of correcting integral errors from DLL
8 channels per chip
Not possible to pair leading and trailing edges

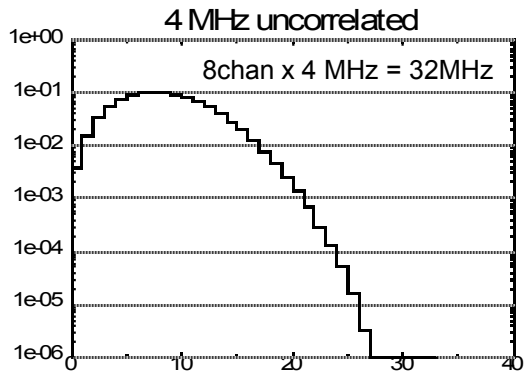
Channel merging

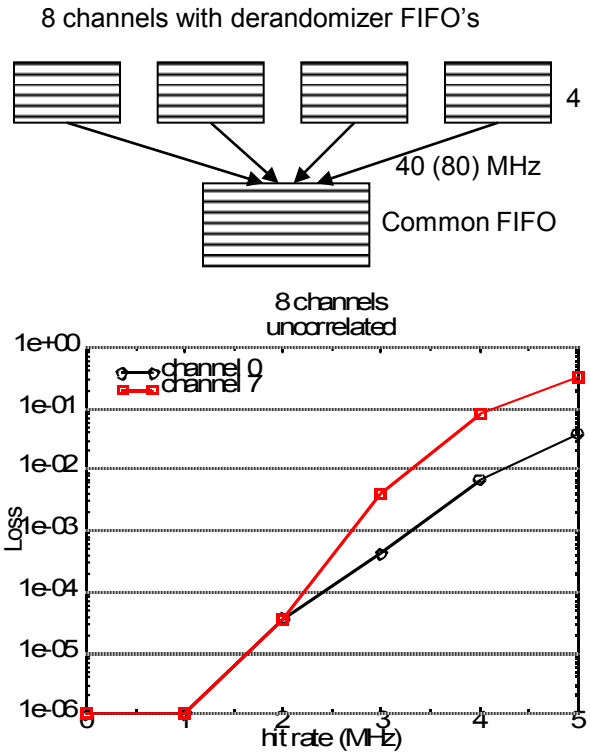
- Hit measurements are derandomized in a 4 deep asynchronous FIFO buffer
- Hits from 8 channels are merged into one L1 buffer
- Arbitration between channels made to be "reasonable" fair









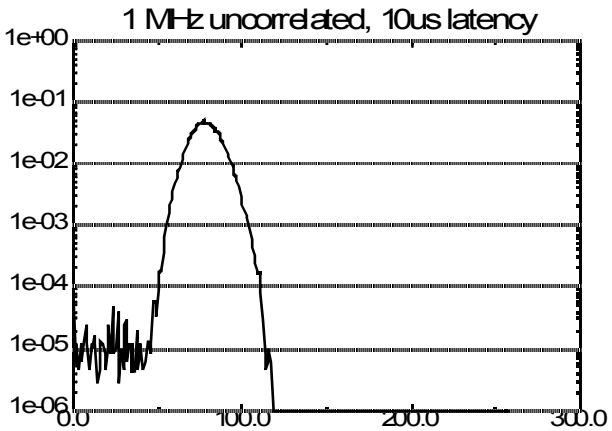


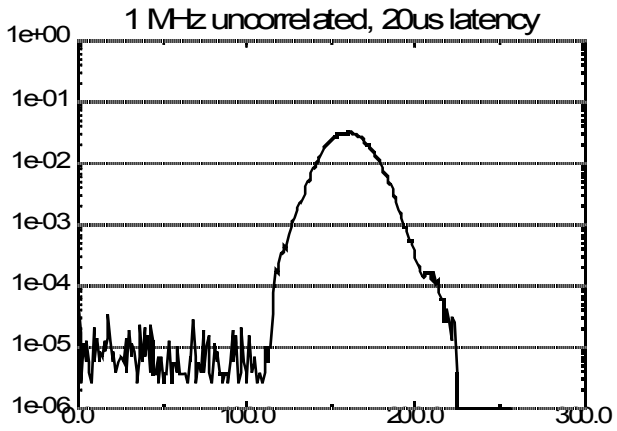
Channel buffer occupancy

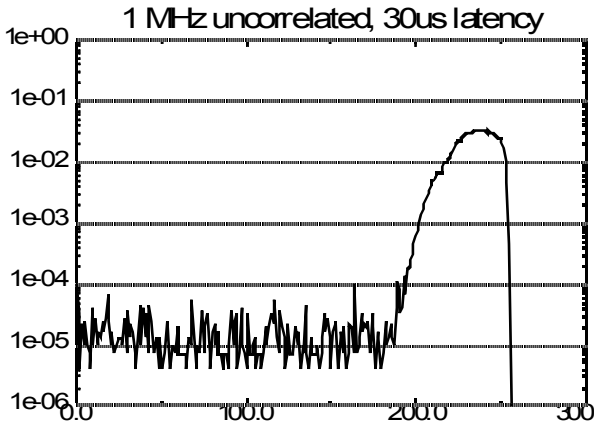
Channel group occupancy

L1 buffer

- Zero suppressed data only, max 256 hits per 8 channels
- Max latency given by dynamic range (1/4)
- High hit rate - > short latency
  Low hit rate -> long latency
- Average buffer occupancy:
  channels(8) x hit rate x latency < ~1/2 buffer size (256)
  (8channels x 1MHz x 10us = 80)
- Events with hits lost from L1 overflows marked

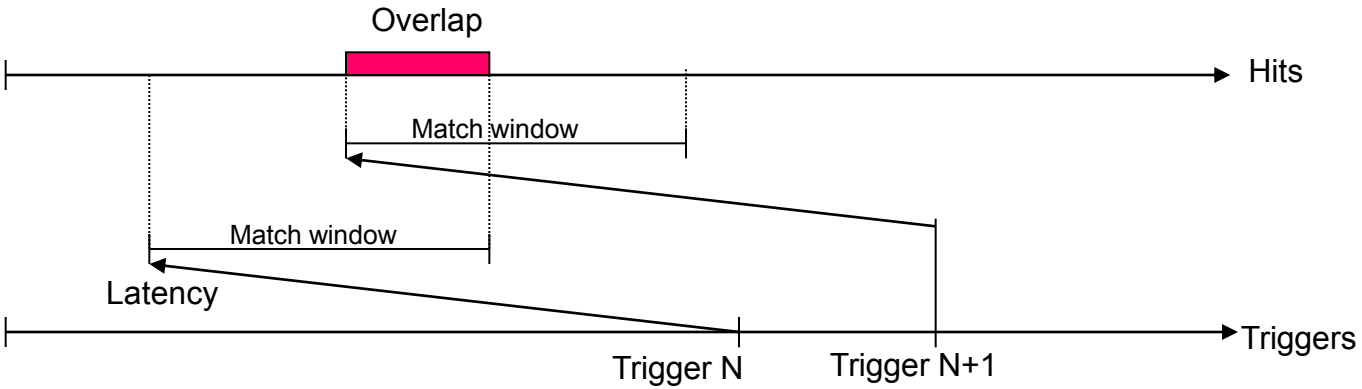






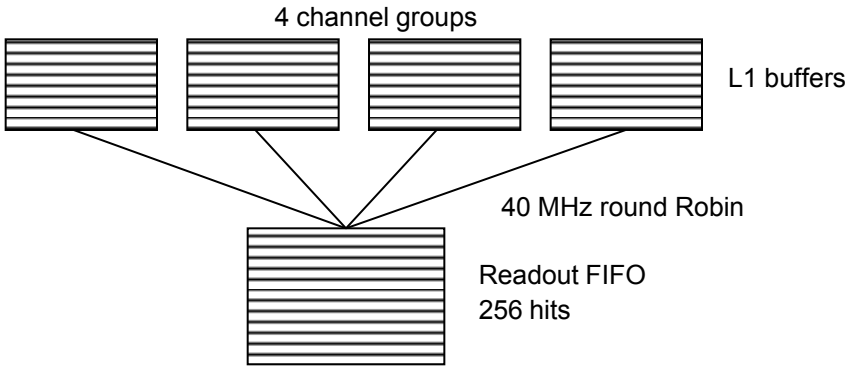
Trigger matching

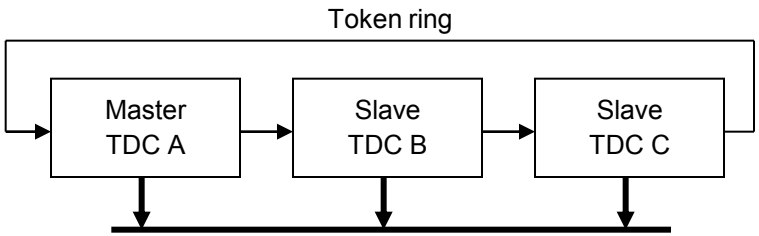
- Trigger matching based on hit measurements and trigger time tag
- 16 deep trigger FIFO to receive new triggers while matching function busy
- Trigger matching based on coarse count (25 ns resolution)
- Programmable latency and matching window
- Supports assigning hits to multiple overlapping triggers
- Reject function to remove old hits when no triggers waiting
- Works across counter overflows (3564 for LHC)
- Maximum number of hits per event programmable
- Trigger matching can be disabled



Readout

- 256 deep readout FIFO to de-couple matching and readout
- Readout FIFO can artificially be reduced to prevent data pile-up
- Token based sharing of readout port with bypass option
  - Triggered: Token only passed when all hits in event have been read out
  - Non triggered: Token must be constantly circulating to find TDC's with data
  - Bypass option skip failing chip in token chain
- Possibility to readout buffer occupancy information
- 32 bit parallel readout for high rate applications
- Byte-wise readout to drive commercial serializers
- Serial readout for low rate applications
- Readout via JTAG possible for debugging





Increasing performance

- Increasing internal logic clock frequency from 40 to 80 MHz(160):
  - Clock from internal PLL
  - Higher hit rates can be handled x2, (x4)
  - Trigger matching speed improved (for high trigger rate applications)
  - Occupancy of L1 buffer in principle NOT improved (given by latency)
  - Power consumption increases
  - IO interface kept at 40 MHz
  - Chips currently only production tested at 40 MHz
- Using fewer channels per channel group (8)
  - 4 channels (16 per chip) -> double hit rate,
  - L1 buffer occupancy reduction
  - Less than 4 channels per group does not bring significant improvement

SEU handling

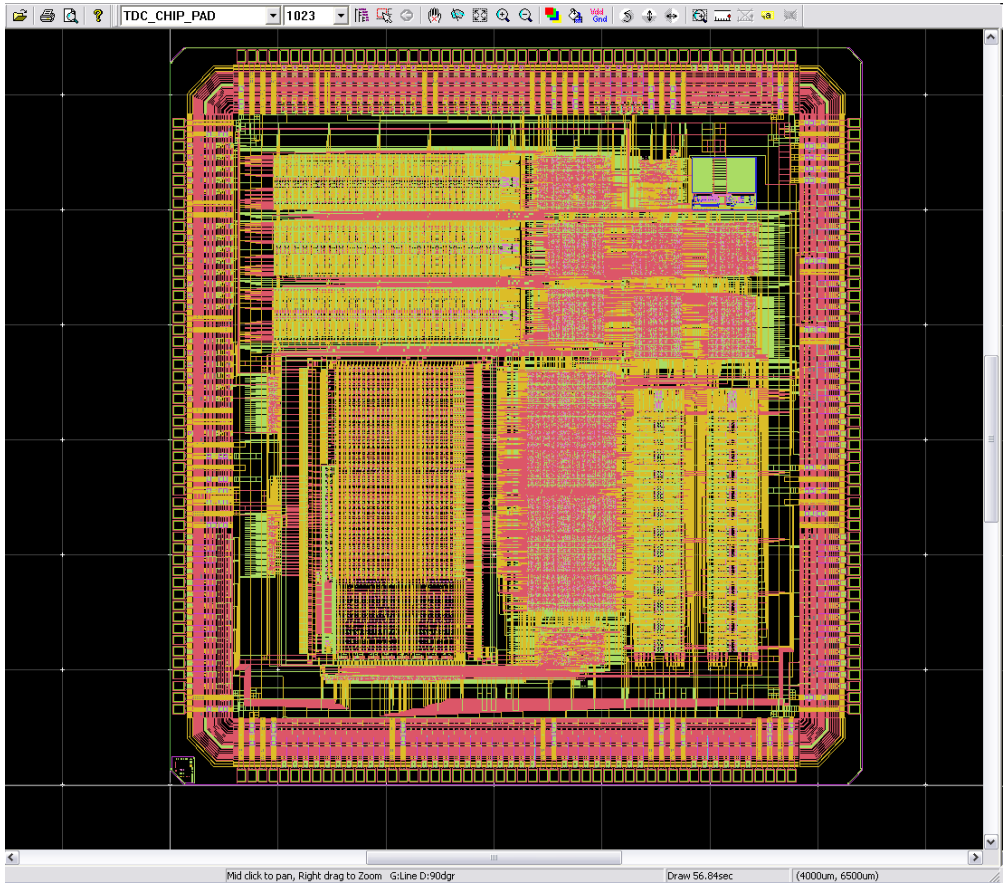
- SEU detection (not SEU immunity)
- Programming data protected with parity check
- All internal memories has parity check
- State machines implemented with one hot encoding and continuous state check.
- Measurements with parity error ignored in matching
- Error status with information about detected parity errors from different functional blocks.
- Programmable global error state which can force TDC into a passive state

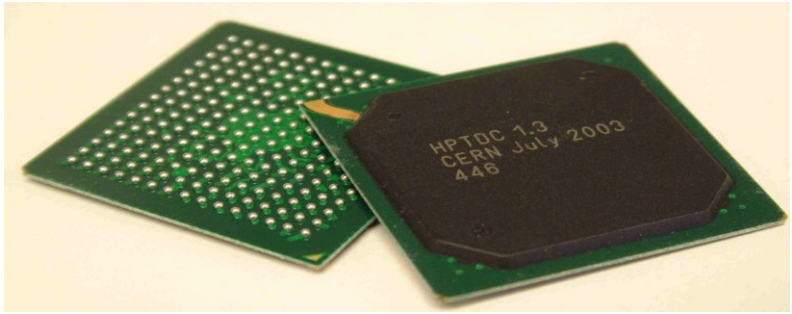
JTAG

- Programming: ~700 bits
- Status: Errors, buffer occupancies, etc. = ~60 bits
- Option of readout via JTAG
- Boundary scan for board testing
- BIST of on-chip memories
- Scan path to verify time measurements: 750 bits
- Test scan path of all internal flip-flops: 2K bits

Implementation

- Architecture simulated extensively at behavioral level
  - (Verilog simulation environment available)
- Mapped into gates (standard cells) with logic synthesis
- DLL, hit registers, RC delay and PLL implemented as full custom
- 0.25 um CMOS technology
- 6.5 x 6.5 mm
- 1 million transistors
- 225 ball grid array package





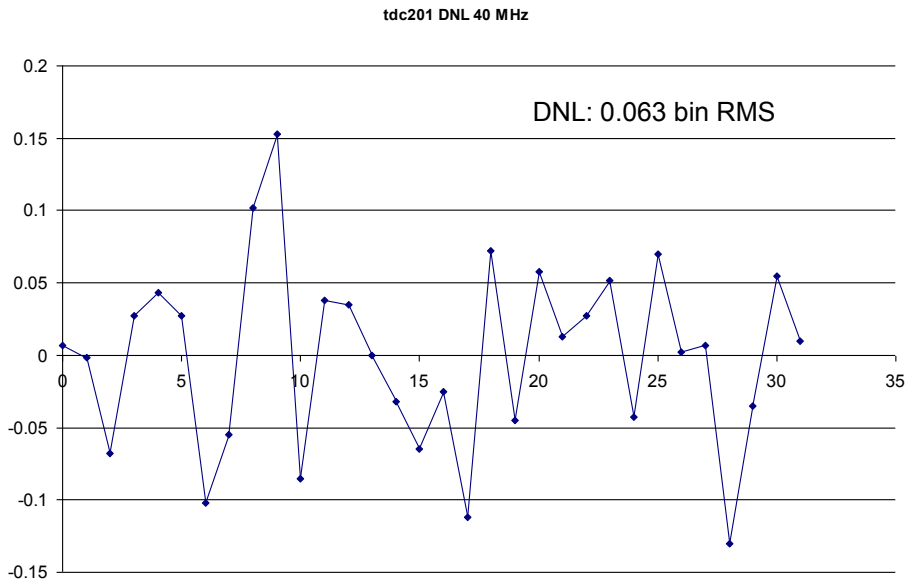
Programmable features

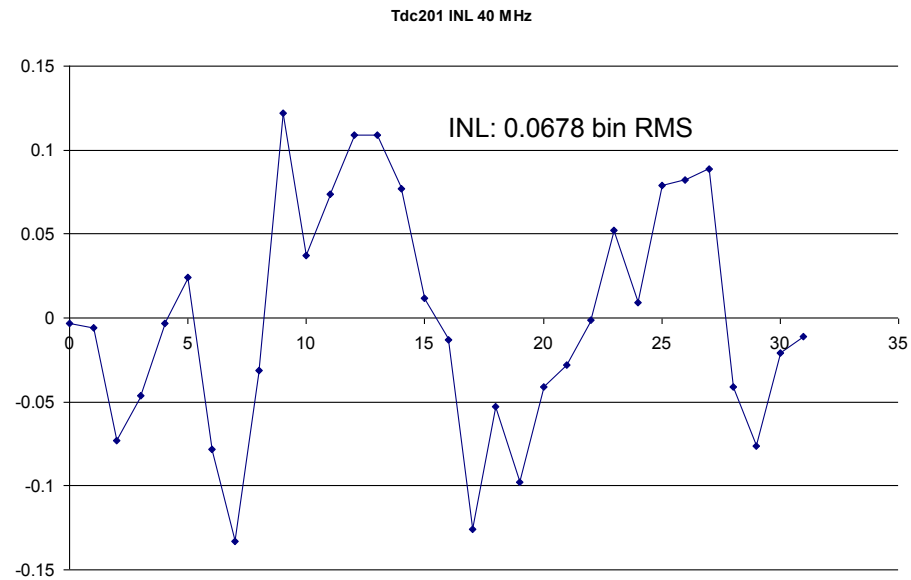
- Resolution
- Integral error correction from DLL
- Channel offsets
- Leading/trailing/pair
- Channel enable/disable
- LVDS or TTL hit inputs
- Channel dead time (5 - 100ns)
- Encoding of triggers and resets
- Trigger matching/no trigger matching
- Trigger latency
- Matching window
- Reject latency
- Roll-over and machine cycle separators
- Limiting number of hits per event
- Readout FIFO size
- Readout of buffer occupancies per event
- Buffer back propagation
- Serial, Byte, 32 bit Parallel or JTAG readout
- Force specific readout pattern
- Serial readout speed (80Mbits/s - 0.3 Mbits/s)
- Use of event headers and trailers
- Token passing scheme
- Generation of global error state
- Low power mode
- DLL and PLL control parameters
- Test modes

This large set of programmable features has made design verification very difficult

Flexibility does not come for free

Timing performance: low resolution

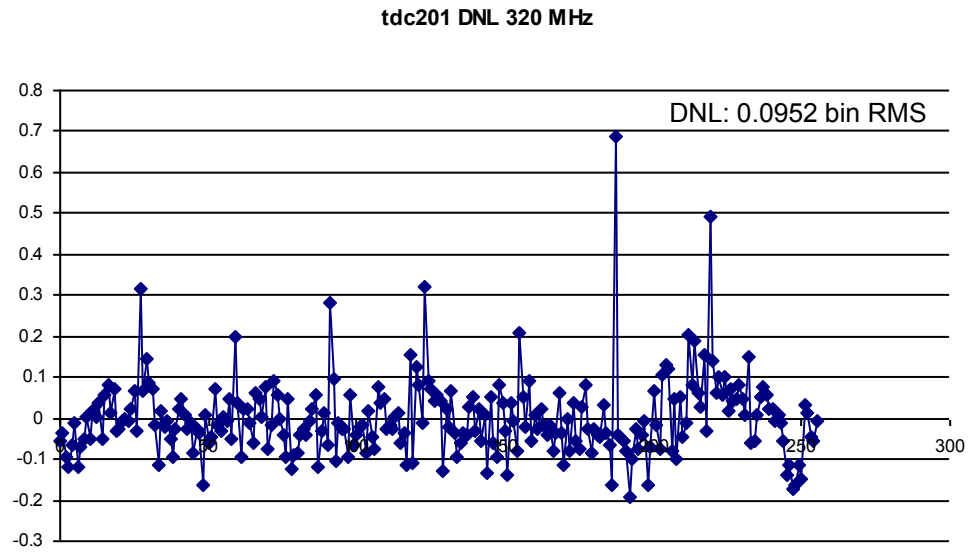




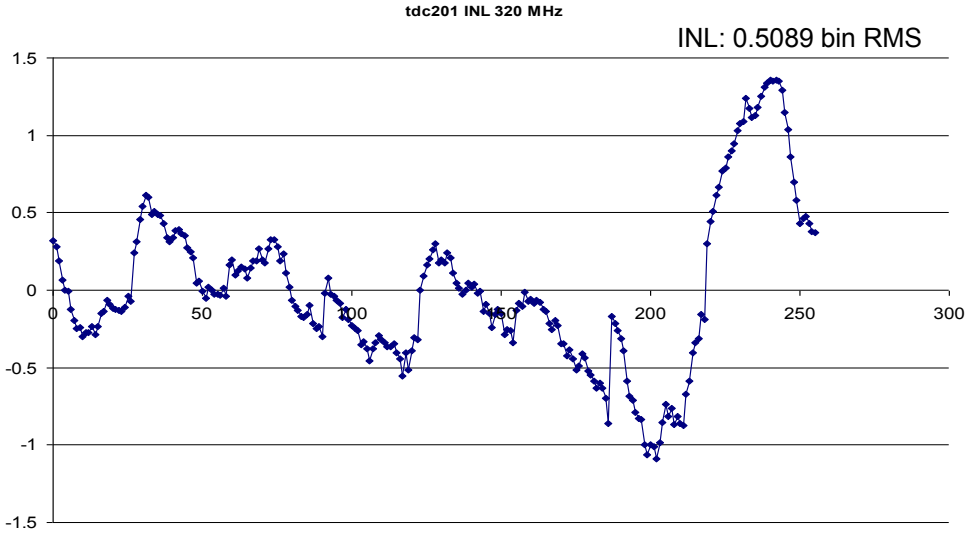
Effective RMS resolution: 261 ps

Perfect TDC gives RMS resolution of Bin/$(12)^{1/2}$ = 225ps

Timing performance: High resolution

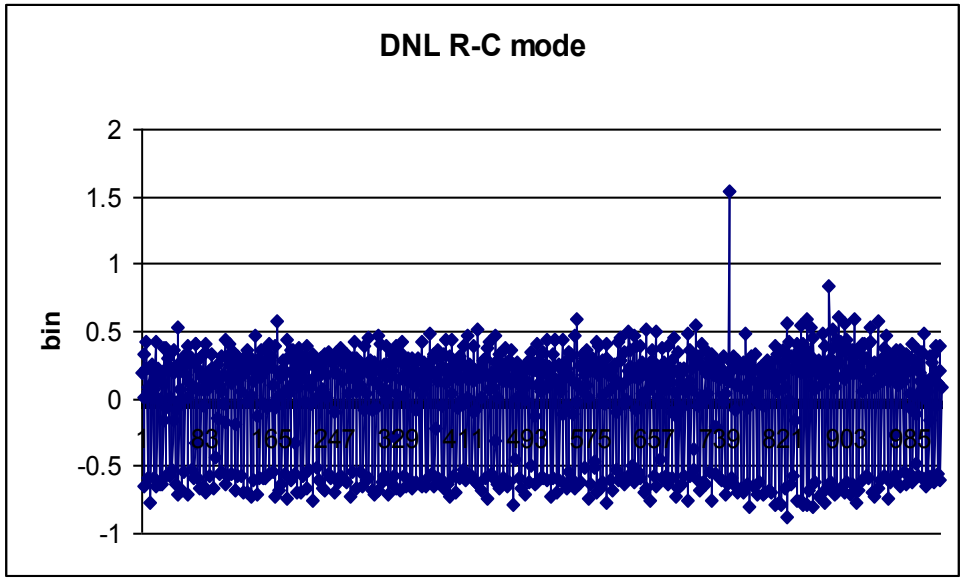


Effective RMS resolution: 48ps



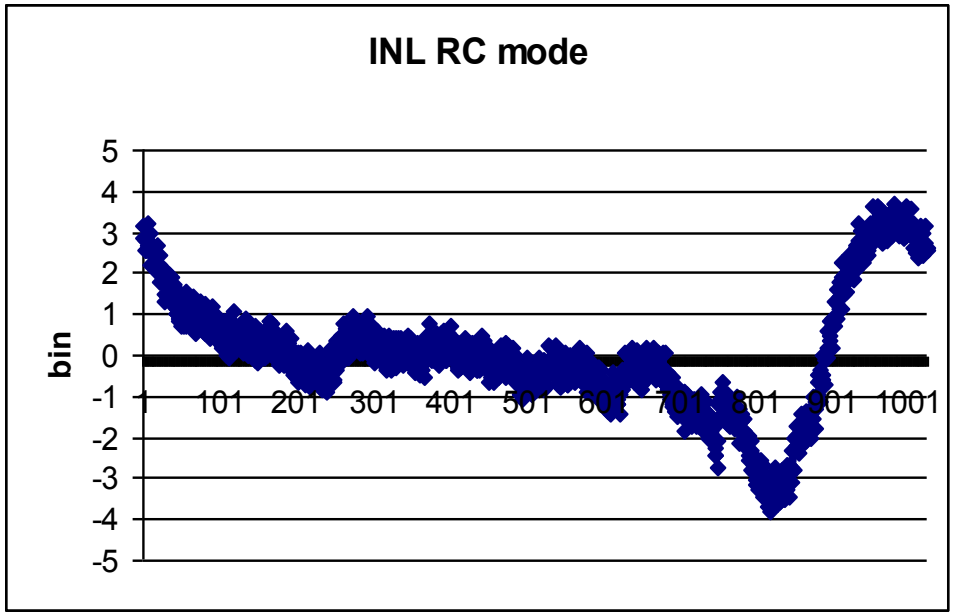
Effective RMS resolution: 34ps with simple table correction

Very high resolution (R-C mode)

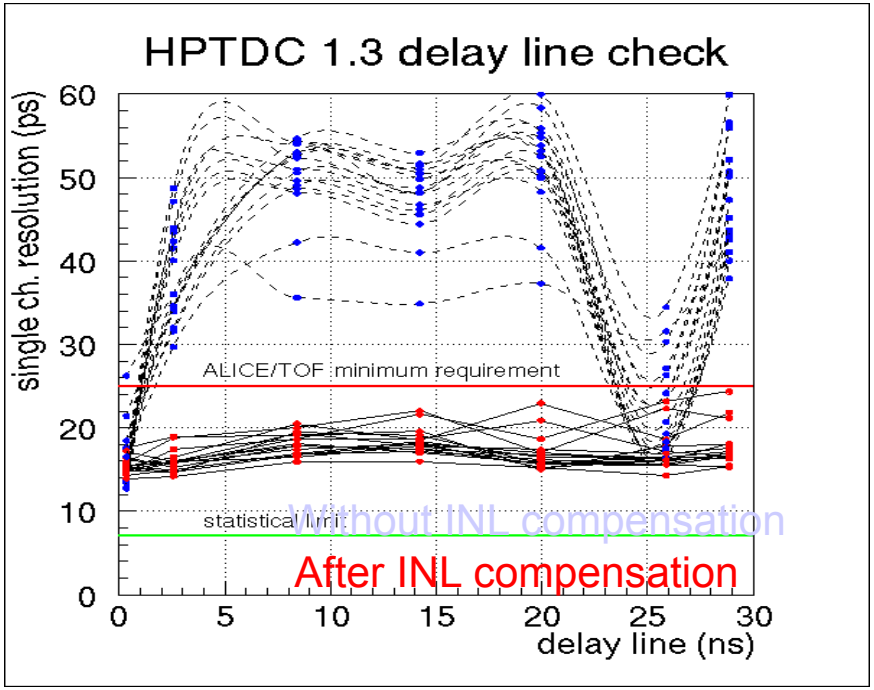


Effective RMS resolution: 40ps

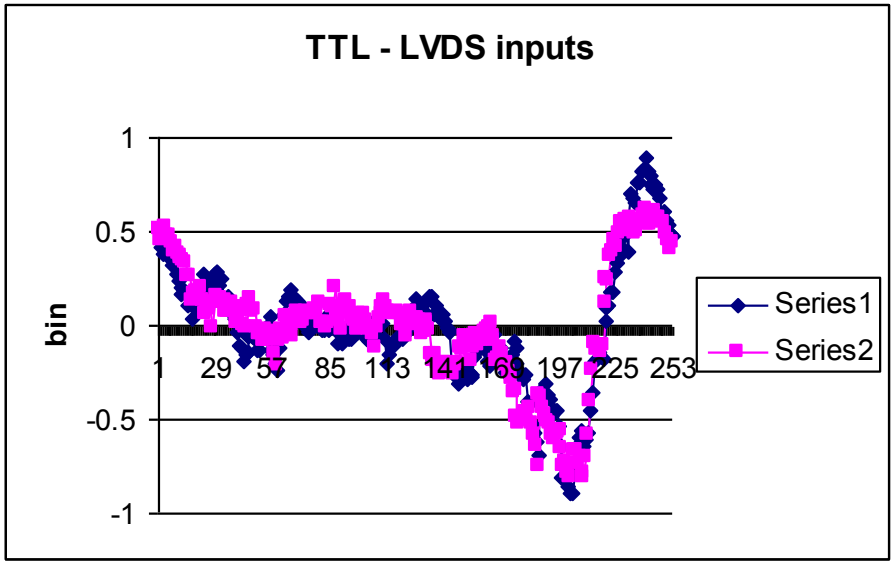
Effective RMS resolution: 17ps with table correction

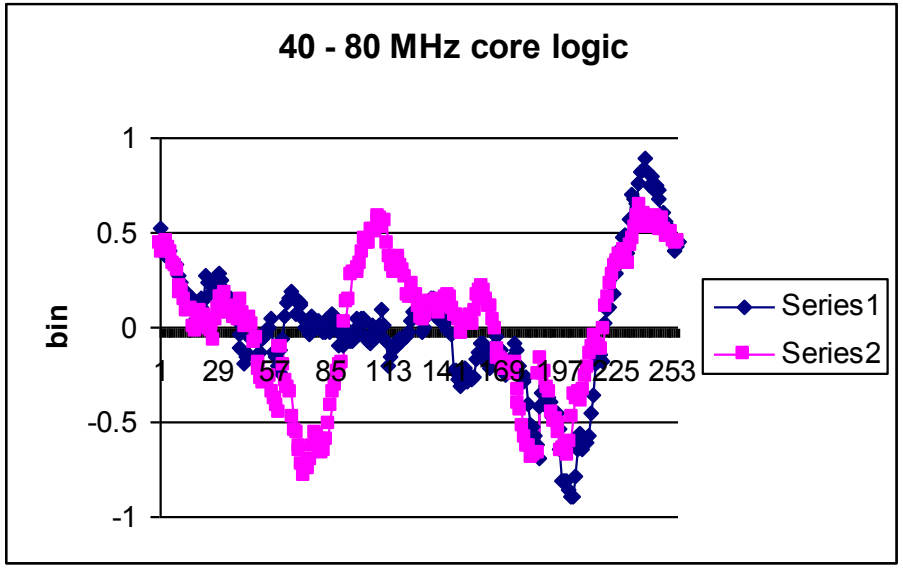


Measurements from ALICE-TOF



Cause of INL errors





It is clear that INL imperfections come from on-chip crosstalk from logic part of chip.

Several improvements have been made with limited improvement:
(special package with power/gnd plane, re-optimized signal routing, separation of power domains, etc.)

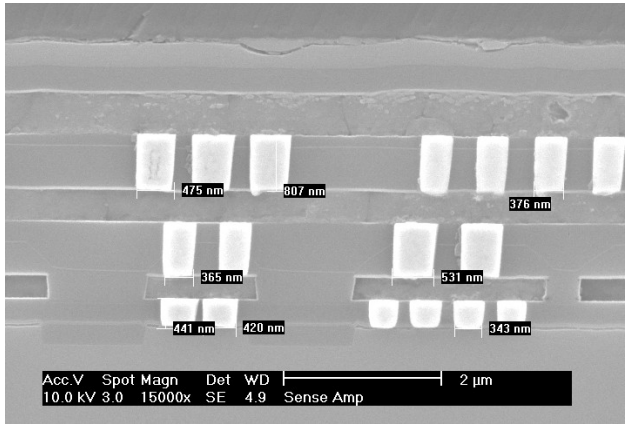
As logic clock is the same as the time reference for the time measurements this is a fixed pattern that can be compensated for if needed with a simple table look-up

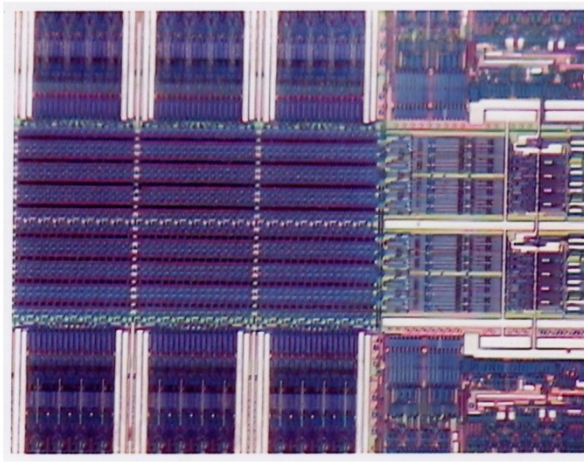
History, Problems and Planning

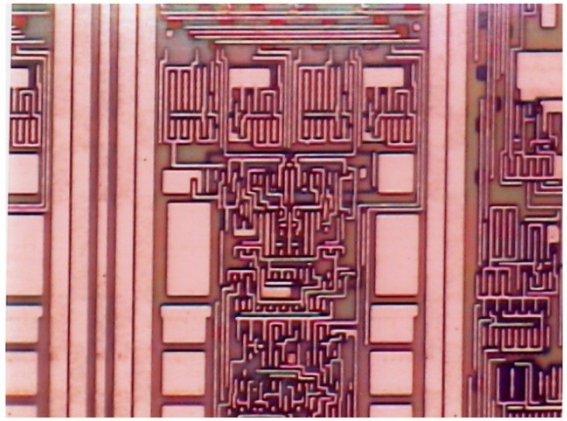
- Version 1: MPW, 2000
  - Functionally working
  - Only 2.5 volt IO levels
  - Potential problem with high power mode startup for low power applications.
  - INL problem in high resolution modes
- Version 2: Engineering run, 2001
  - 3.3 volt IO levels
  - Ensured to start up in low power mode
  - INL improved using optimized clock signal distribution and separate power supply for clock drivers. But not yet satisfactory.
  - **New**: Hit registers was in some cases found to loose hit information if Vdd decreased below 2.30 - 2.40 volt.
    Traced to possible sensitivity to relative N/P MOS parameters
  - **New**: DLL lock problem on some chips in low resolution mode at increased Vdd. Traced to possible sensitivity to relative N/P MOS parameters
  - **New**: R-C delay line adjustment in some cases problematic
- Version 3: Engineering run with few modified layers, 2002
  - Hit register problem resolved by resizing relative N/P transistors
  - DLL lock problem resolved by resizing relative N/P transistors
  - R-C delay adjust rescaled to fit observed process parameters.
  - INL improved by alternative powering scheme. Still not perfect INL in very high resolution mode but satisfactory using simple table lookup correction.
  - **New**: L1 buffer parity error at increased Vdd
- CMS production run, mid 2003
  - 25 wafers (10.000 chips)
  - L1 buffer problem only seen at Vdd out of normal working range (above 2.7 volt)
- ALICE TOF production end 2003, 48 wafers = ~20.000 chips
- Final production run for "small" users + missing chips for CMS & ALICE , begin-mid 2004

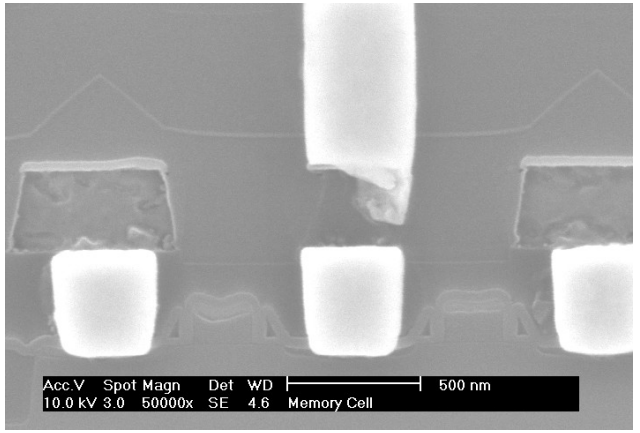
L1 buffer parity error problem

- At increased power supply voltage parity errors detected in L1 buffer (normally intended to detect SEU)
  - MPW: Above 3.0 volt (normal working range 2.3 – 2.7 volt)
  - ENG1: Above 2.8 volt
  - ENG2: Average 2.6 volt, some chips fail at 2.3volt !
  - Prod1: Average 3.0 volt, some chips (1%) fails at 2.6 volt
- Failure analysis
  - Never occurs in readout FIFO
  - In most cases L1 buffer in group3 most sensitive
  - Happens randomly -> very hard to trace cause
  - Company supplying memory macro gone bankrupt
  - Chips sent for processing failure analysis
  - 1 year spent (wasted) to try to determine cause
- Last production batch has acceptable yield when performing production test at 2.8 volt









HPTDC users

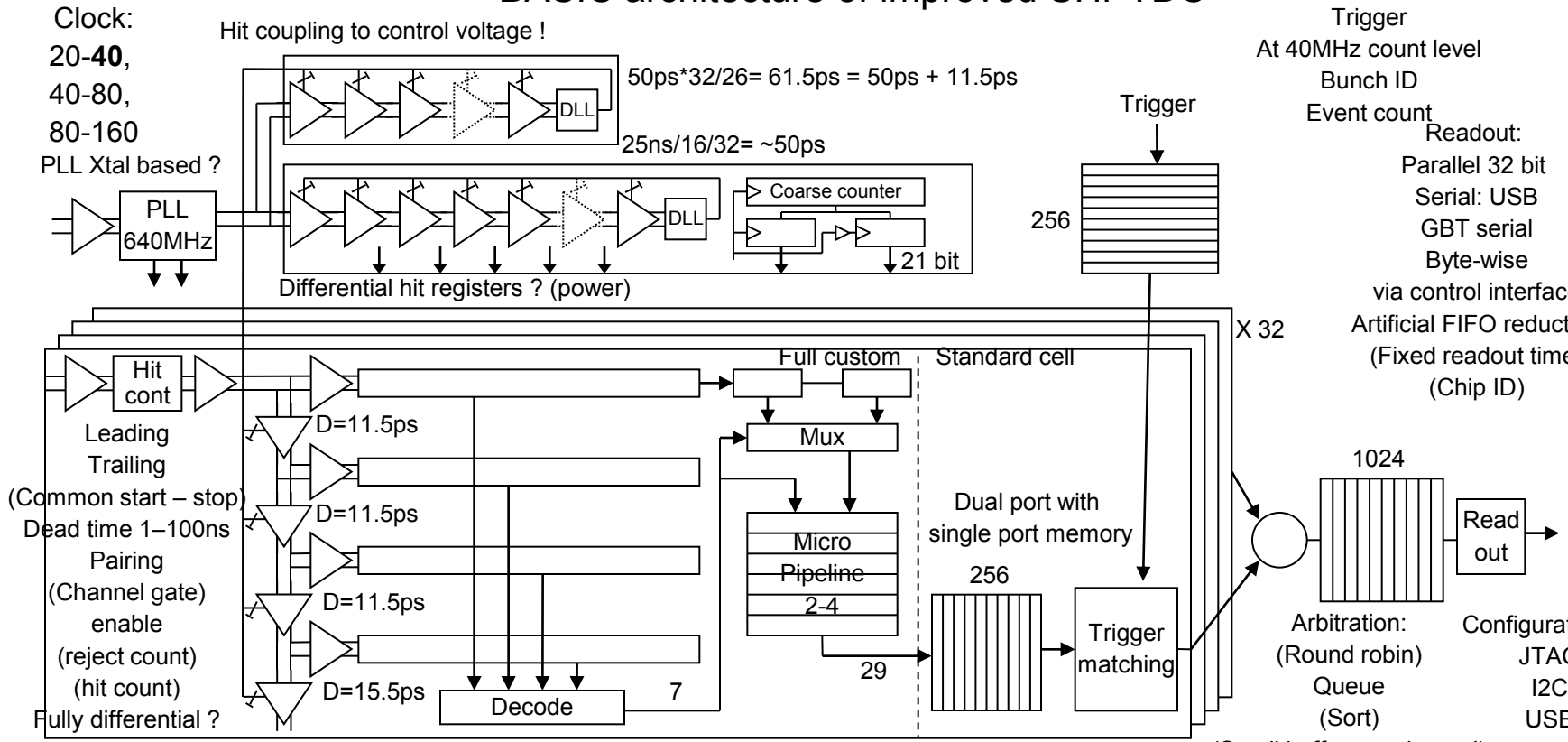
User	Contact person	Parts
CMS muon	Carlos Willmot	8000
ALICE TOF	Pietro Antonioli	24000
NA48	Sergei Basilev	50
Phobos	Andrei Sukhanov	80
CAEN	Carlo Tintori	2500
BES	Jiang Xiaoshan, Huayi Sheng	1400
RICE (STAR)	Geary Eppley	4500
Sky electronics	Lloyd bridges	800
Oku	Andrei Siderov	300
ATLAS CTP	Georges Schuler	30
HYTEC	Alan Burley	
Orsay	Robert Sellem	200
Tata institute	Suresh Tonwar	50
Upsala	Leif Gustavson	100
LHC machine	Javier Serrano	1000
Imago	Dan Lenz	100
Ionwerks	Al Schultz	1000
LHCb	Albert Zwart	
Frankfurt	Kolja Sulimma	100
Alice V0	Gwenael Morishaud	10
Struck	Mathias Kirsch	
Kopio	Pierre-Andre Amaudruz	3000
Total : ~20 users		~40.000

HPTDC summary

- Number of channels: 32 / 8
- Clock frequency: 40 MHz external
  40MHz / 80MHz / 160 MHz / 320 MHz internal
- Resolution:
  781 ps (261ps RMS) low resolution mode
  195 ps (64 ps RMS) medium resolution mode
  98 ps (48 ps RMS) high resolution mode
  24 ps (40 ps RMS) very high resolution mode
  (8 channels)
  24 ps (17 ps RMS Corrected)
- Dynamic range: 102 us
- Double pulse resolution: 5 - 10 ns depending on mode
- Hit rate: Core logic at 40 MHz, Not R-C mode
  Max. 2 MHz per channel, all 32 channels used
  Max. 4 MHz per channel, 16 channels used.
- Event buffer size: 4 x 256
- Read-out buffer size: 256
- Trigger buffer size: 16
- Power consumption: 300mW - 1500 mW depending on modes.
- Hit inputs: LVDS or LVTTL

- L1 buffer problem has been (is) a painful experience
- (too) many different users

BASIC architecture of improved SHPTDC



Support for analog front-end chip ?:
(Nino, ASDQ, etc like)
DAC + 8bit output
Process corners:
A: Conservative for normal use
B: Aggressive to get publication
(6-7ps binning, 2ps RMS !)

Prevent clock cross coupling:
Separate power domains
Differential channels
Allow fully async. for tests

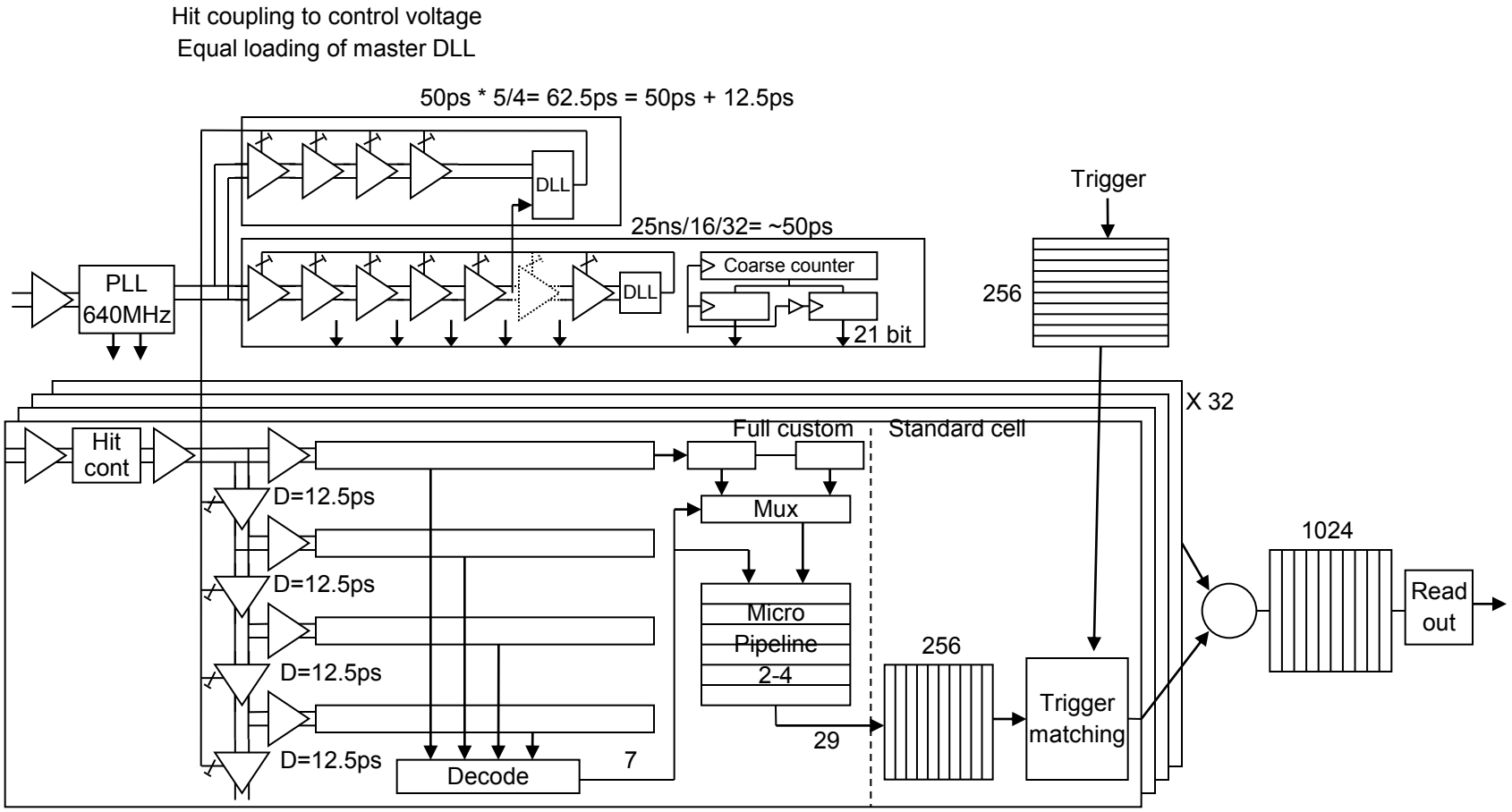
Monitoring:
PLL and DLL real time lock detect
Hit error, state error, memory error,
Hit counters,
Rejected hit count
Buffer occupancies,
(time histogram)

SEU: Immune or just checking ?
Double bit error detect in memories
Statemachine checking
Configuration protection/detection

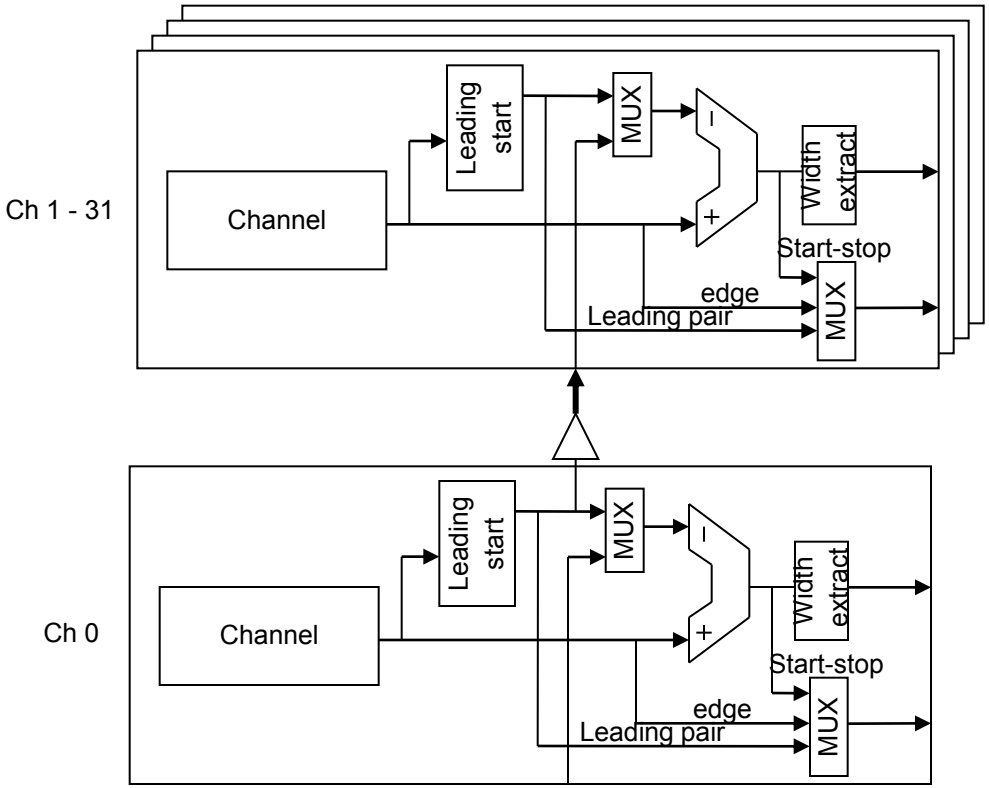
Test:
Access to raw hit data
Bypass PLL
Single clocking of logic
Test output with MUX
Internal scan
JTAG Boundary scan

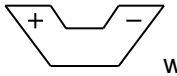
Low power mode ?
DLL always needed to select counter
Lower power mode without fine interpolation

Alternative interpolation with coupled DLL



Inclusion of pulse width and start stop modes





Subtractor with **roll-over**

Start –stop:

Channel 0 common start

Absolute common start can be read out (optional)

Relative stops can be read out

NO TRIGGER MATCHING

How to assure that start timing register is available at right time (not too slow and not too fast)

Additional pipeline stage on other channels ?.

Slower sync circuit on other channels ?.

Negative relative time could occur !

In start-stop mode Ch0 highest priority to readout FIFO ?

Channel layouts to be the same (also ch0)

Leading and width:

Hit controller must guarantee pairs (plus logic must check if leading/trailing)

Absolute leading time, relative width, Total bits to be limited !.

Trigger matching can be performed on leading edge

After trigger matching leading edge can be relative to trigger

(Width extraction could also be made at output of L1 buffer).

Width must saturate to FFF if overflow

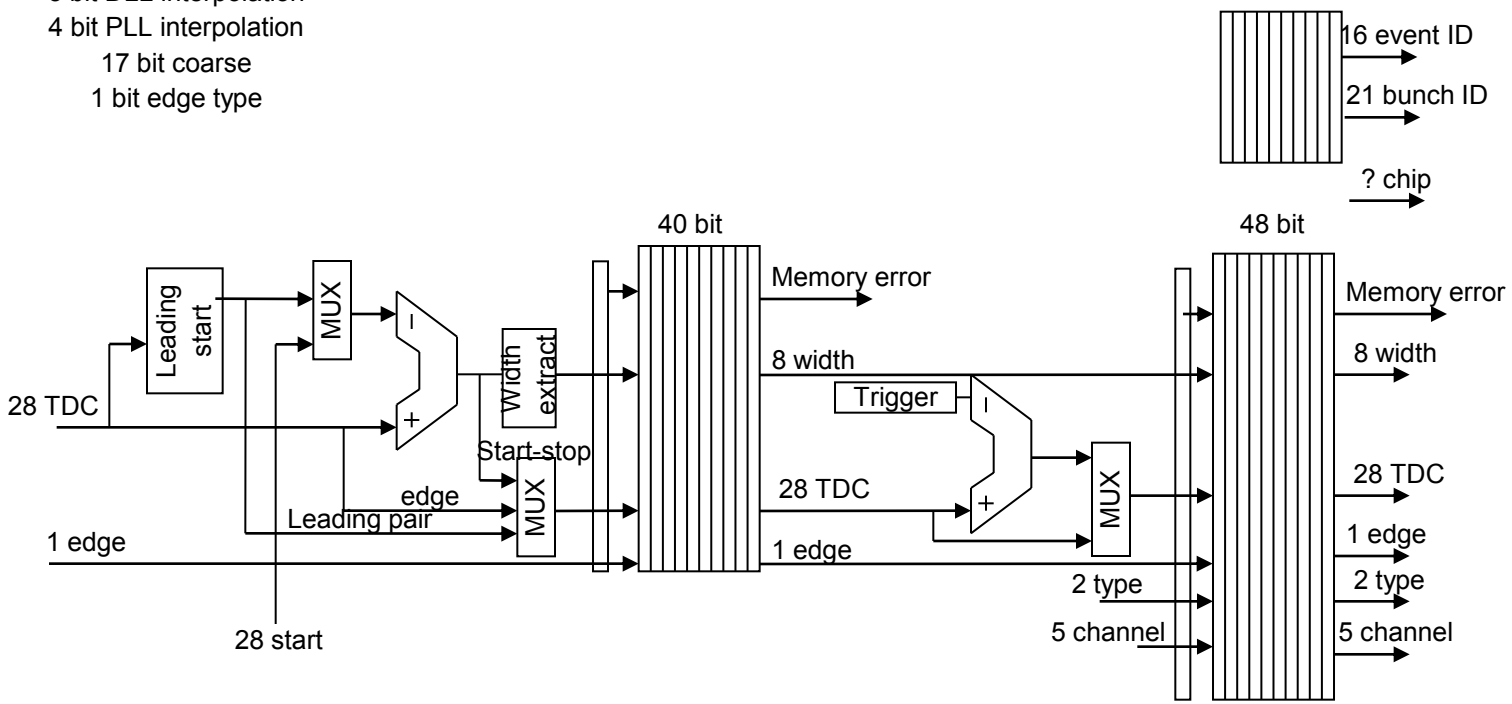
Bit widths in data path

32 bit readout:
Header: bunch ID, event ID, chip ID
Trailer: event ID, error status, word count
TDC: channel, edge, TDC with prog resolution, (width)

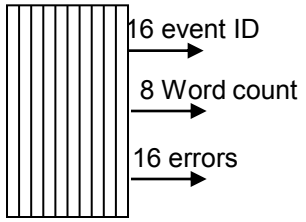
Full TDC measurement 29 bits:
2 bit fine interpolation
5 bit DLL interpolation
4 bit PLL interpolation
17 bit coarse
1 bit edge type

8 bit width measurement with programmable resolution

? bit memory protection (40 -29-8= 3)

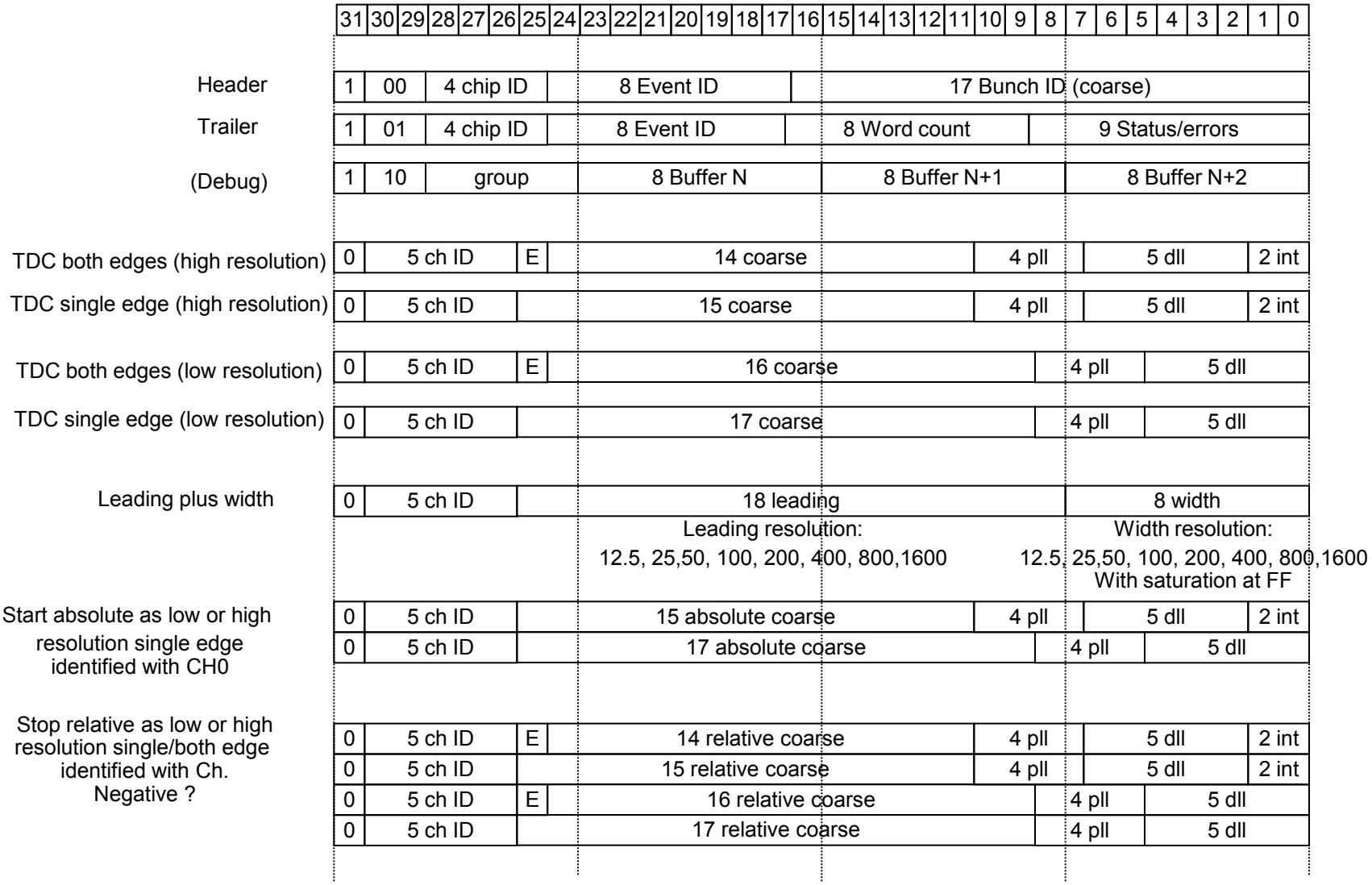


Different data types in RO FIFO:
TDC measurement
Header: Chip ID, Bunch ID, Event ID
Trailer: Event ID, words, errors
Debug: L1 buffer occupancies, RO occupancy, Trigger occupancy



Byte oriented readout: USB
Can use more freely defined parts to read out

32 bit readout formats

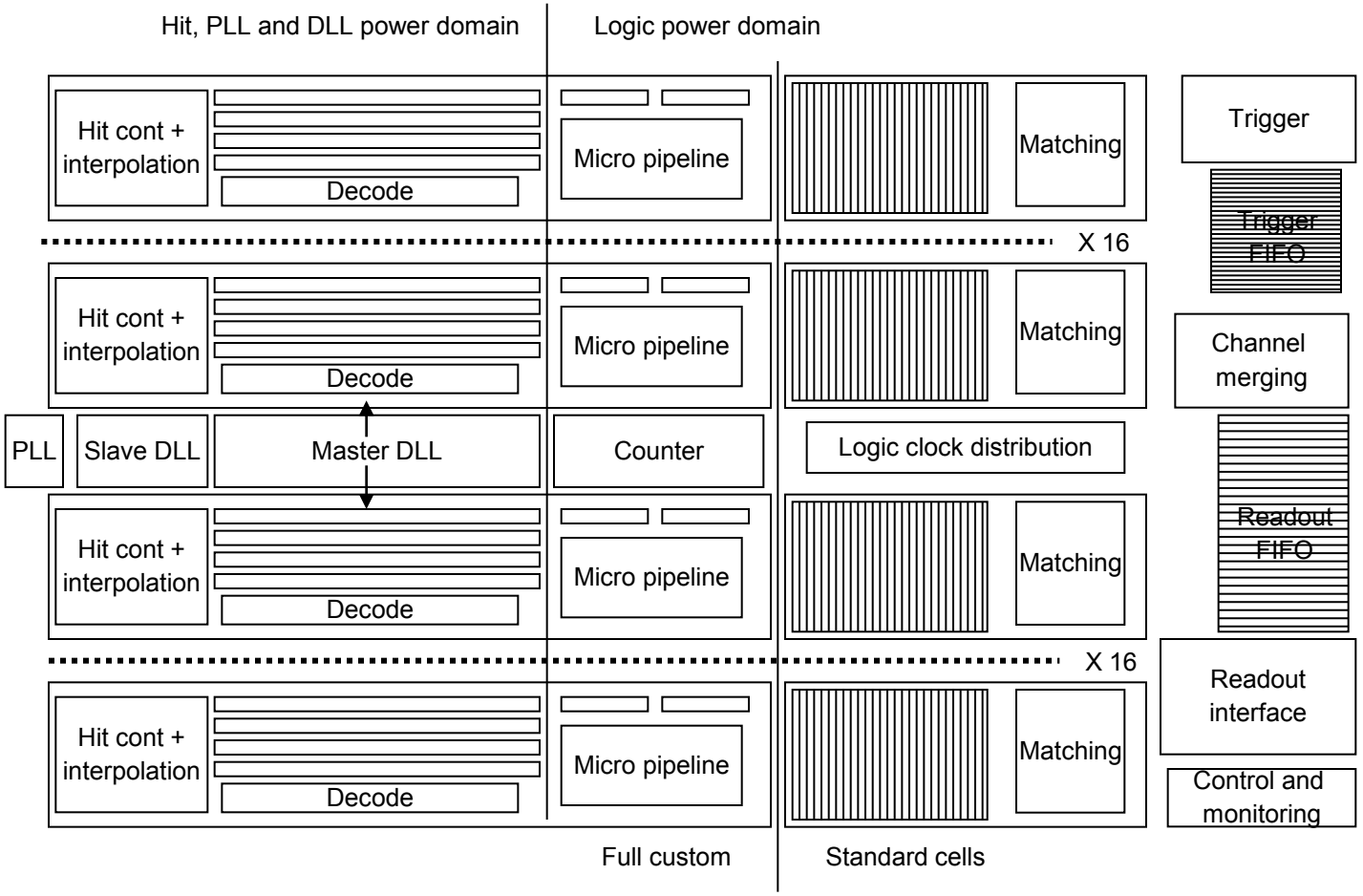


Byte oriented readout: USB

Can use more freely defined parts to read out ?

FLOOR planning (not to scale)

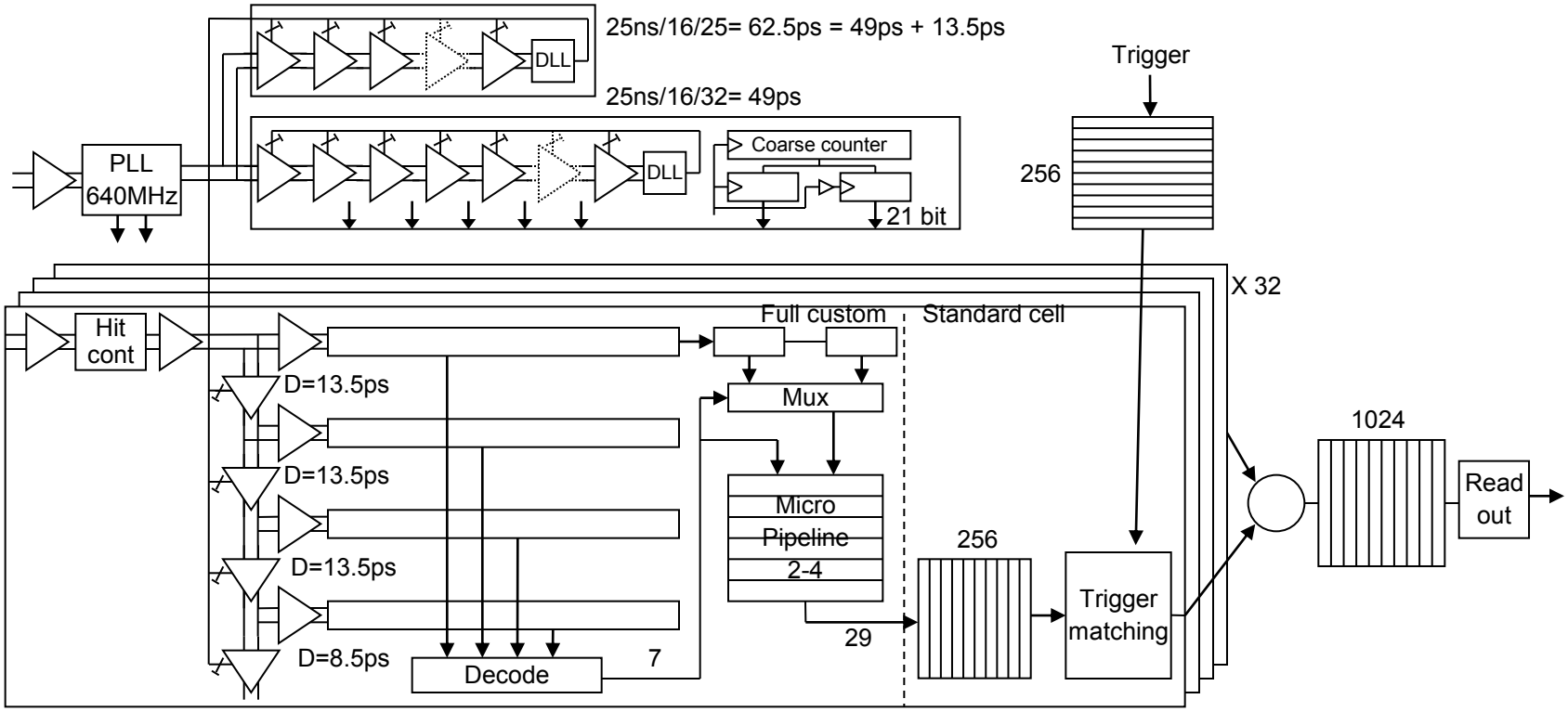
Separate power domain for sensitive part
Highly regular channel layout

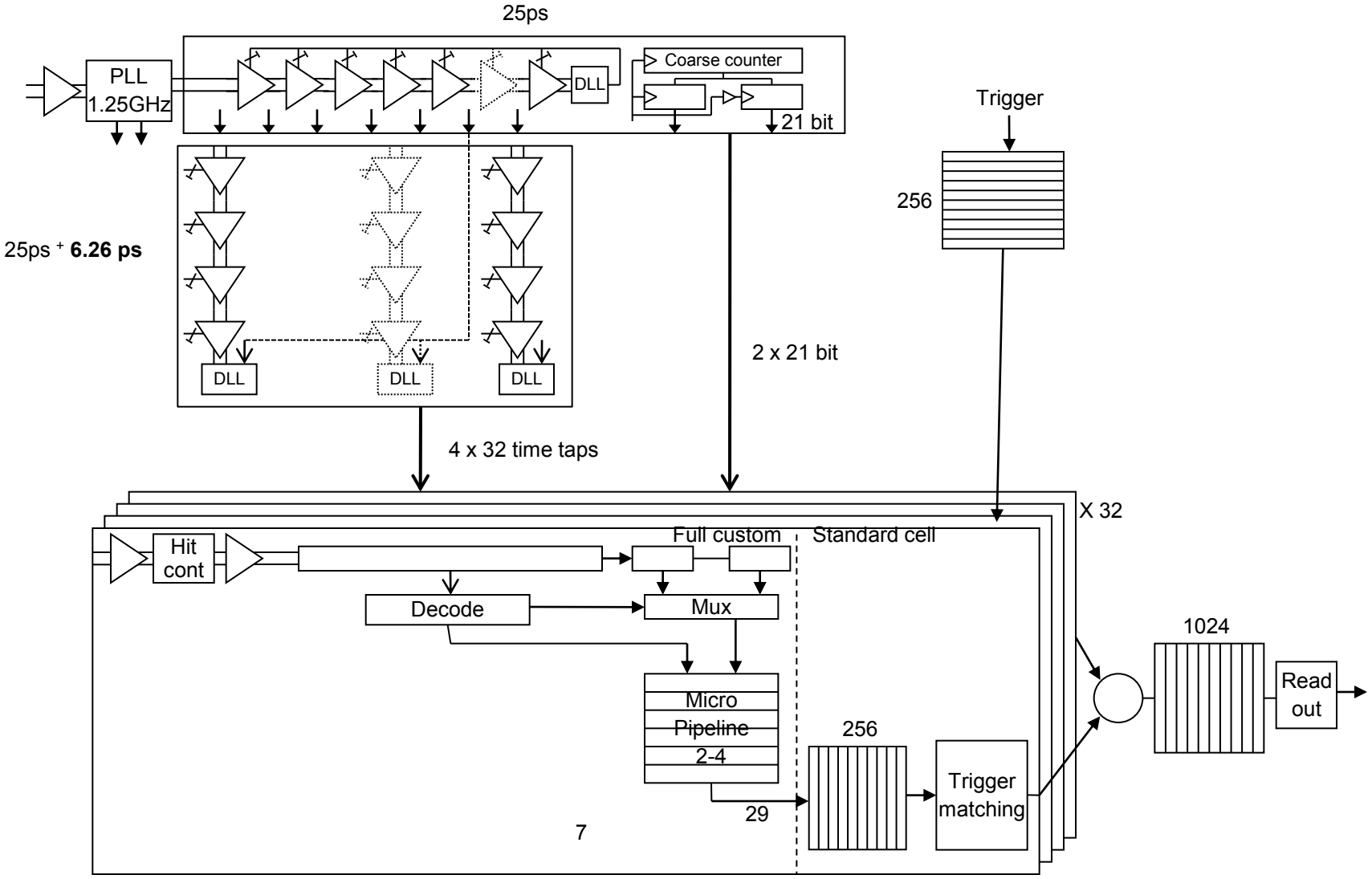


L1 buffer: 256 x 40bit = 452um x 124um (512 x 40 = 848x124)
32 channel buffers:
32 x 124um = 4.9 mm
Chip size: 6mm x 6mm

prog

- Individual per channel when some possible advantages
  - Leading on even channels , trailing on odd channels
  - Pairing in hit controller but not relative width.
  - Specific for Ch0 when start – stop mode.
    - Leading/trailing, resolution
  - Delay cell adjust for fine interpolation
  - Others ?.
- Otherwise common across channels


25ns/16/25= 62.5ps = 49ps + 13.5ps
DLL
25ns/16/32= 49ps
DLL
Coarse counter
21 bit
PLL
640MHz
Trigger
256
X 32
Hit
cont
Full custom
Standard cell
D=13.5ps
D=13.5ps
D=13.5ps
D=8.5ps
Mux
Micro
Pipeline
2-4
29
Decode
7
256
Trigger
matching
1024
Read
out


25ps
PLL
1.25GHz
DLL
Coarse counter
21 bit
Trigger
256
25ps + 6.26 ps
DLL
DLL
DLL
2 x 21 bit
4 x 32 time taps
X 32
Full custom
Standard cell
Hit
cont
Decode
Mux
1024
Read
out
Micro
Pipeline
2-4
256
Trigger
matching
29
7