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Electronic readout techniques

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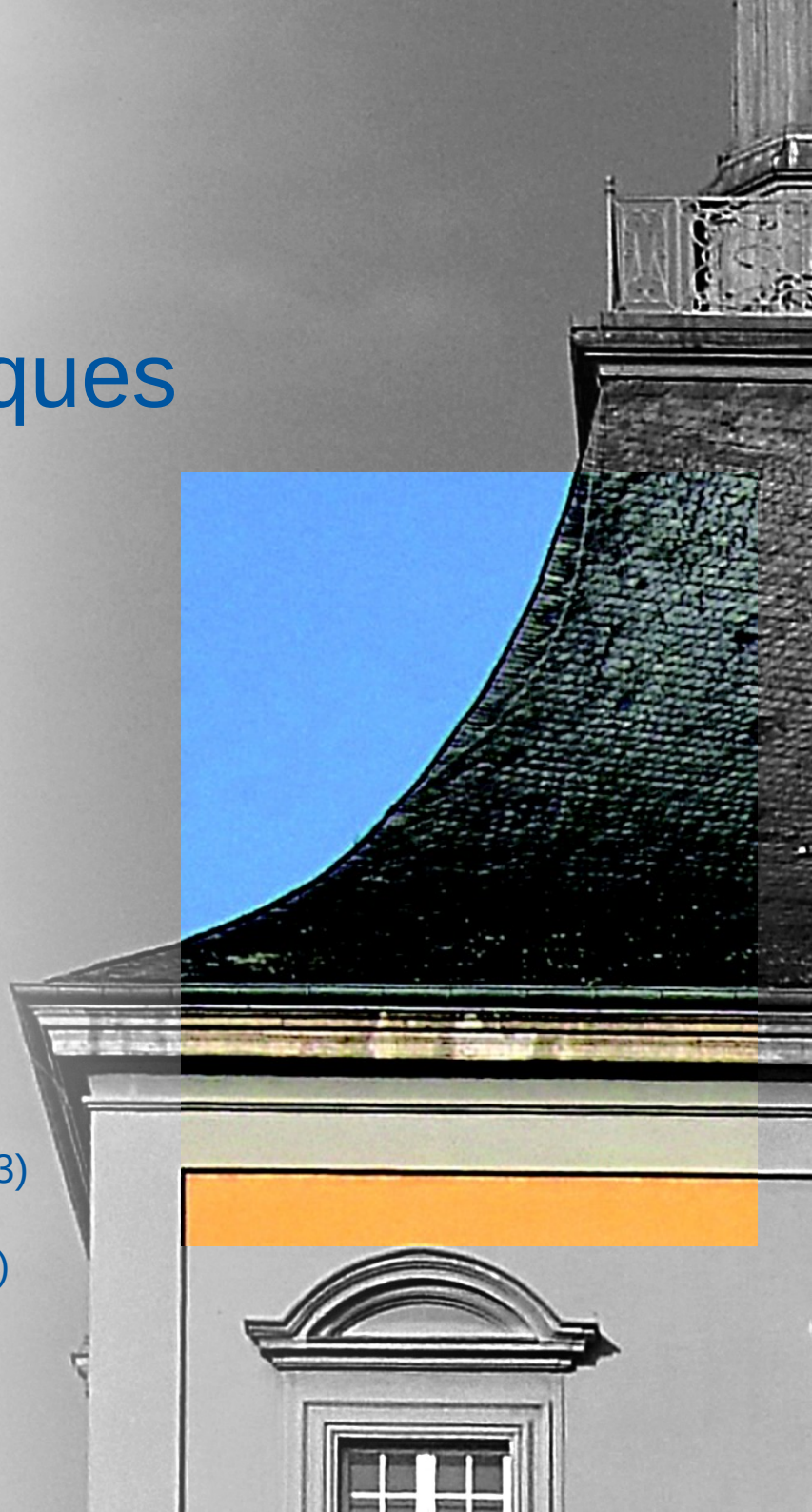
CERN 30.11.2023



With material from:
B. Ketzer & M. Lupberger
Lecture on *Physics of Particle Detectors* (2022/23)
and B. Ketzer
Lecture on Advanced Gaseous Detectors (2019)

FTD

AG Ketzer

Gas Det Bonn

RD51 Collaboration

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OUTLINE

Part 1: A brief introduction

- Recap: Signal formation and Shockley-Ramo Theorem
- Electronic readout overview
- Discrete components
- Readout concepts
- Multi-channel readout and front-end chips

Part 2: SRS demonstration

- The VMM front-end chip
- Overview on the RD51 Scalable Readout System
- SRS-VMM
- Live demo

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PART 2 – THE SRS

2011 IEEE Nuclear Science Symposium Conference Record N43-5

Front-end electronics for the Scalable Readout System of RD51

S. Martoiu, *Member, IEEE,* H. Muller, and J. Toledo

***Abstract*– Recent developments in micro-pattern gas detector technologies have considerably broadened the interest in this type of detectors, extending their application field from high-energy physics to nuclear, astrophysical, geophysical, medical or industrial applications, to name just a few. Historically, for the wide range of gas amplification schemes available, there has been an almost equally wide amount of electronic readout solutions, tailored on just one application, making it rather difficult for newcomers to employ the technology. Developed within RD51 Collaboration for the Development of Micro-Pattern Gas Detectors Technologies, the Scalable Readout System (SRS) is intended as a general purpose multi-channel readout solution for a wide range of detector types, and detector complexities, as well as for different experimental environments.**

II. The SRS Concept

The Scalable Readout System is designed around a bivalent scalability concept, which refers to both applications range and system size. Not limited to a single detector technology, the system needs to respond to a wide range of detector requirements, in terms of sensitivity, time resolution, event rate capability, trigger concept, radiation or magnetic tolerance, etc. In the same time the SRS concept has to allow the integration of small prototype detectors, as well as large area detectors in a wide range of experimental environments.

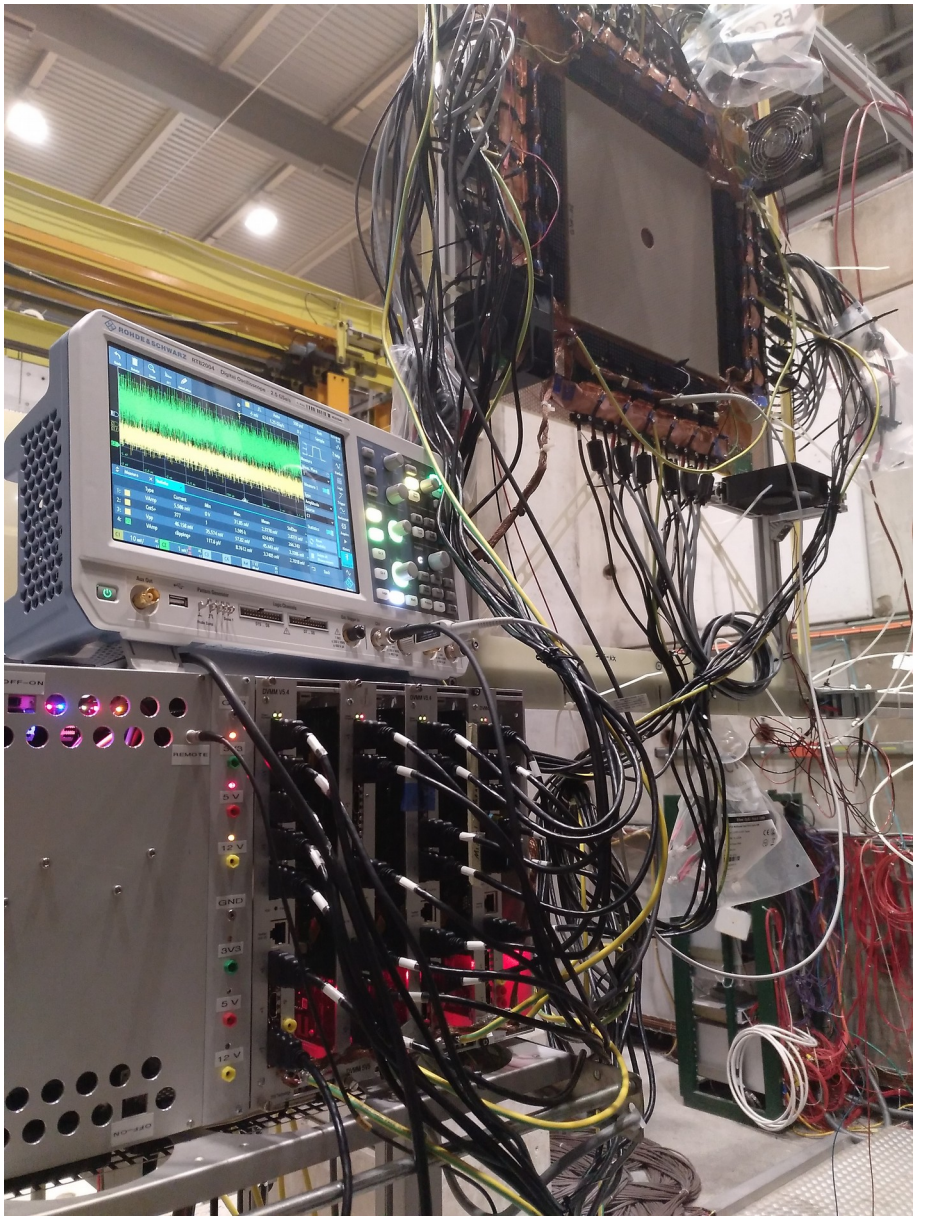
A. Application-Range Scalability

WHAT IS SRS

Scalable Readout System:

- A generic readout system for laboratory and detector instrumentation
- Developed and supported by the RD51 Collaboration since 2009 (Inventor: H. Müller)
- Standardised multi-purpose data acquisition system
- Different front-end chips supported
- Constantly extended, improved, adapted to needs from community
  by community
- Exceptional common long-term project of RD51

  ⇒ used in many MPGD groups for R&D
  and also some (upcoming) experiments



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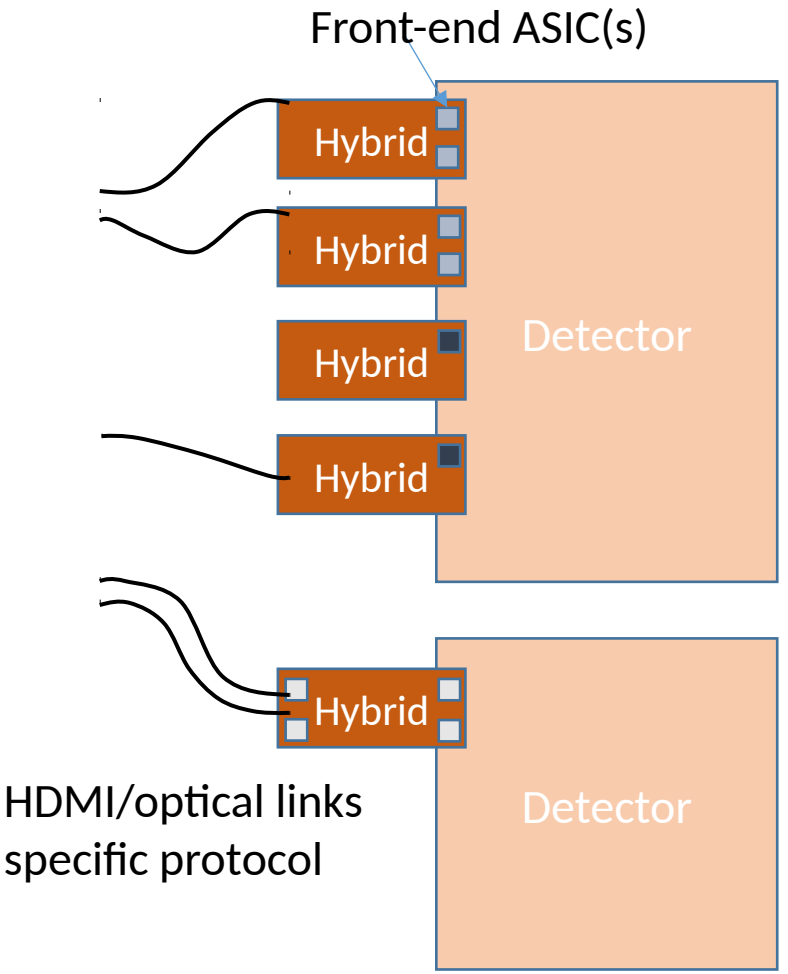
WHAT IS SRS



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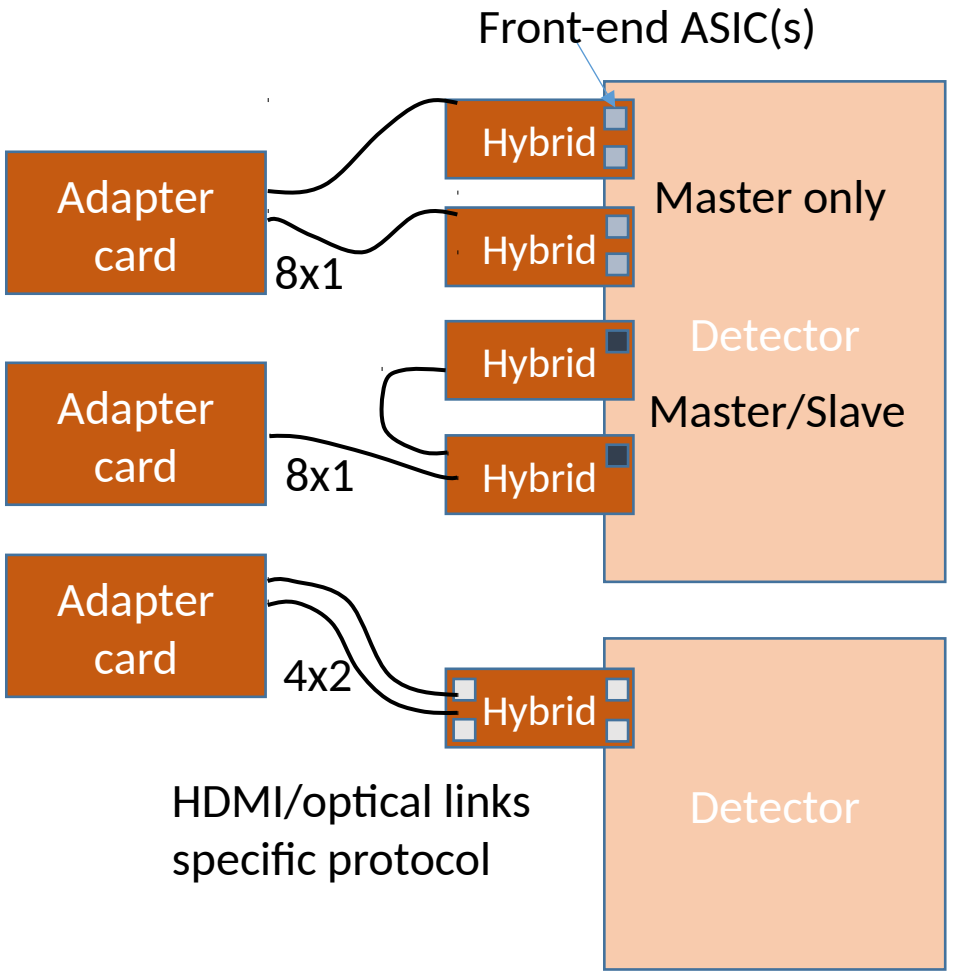

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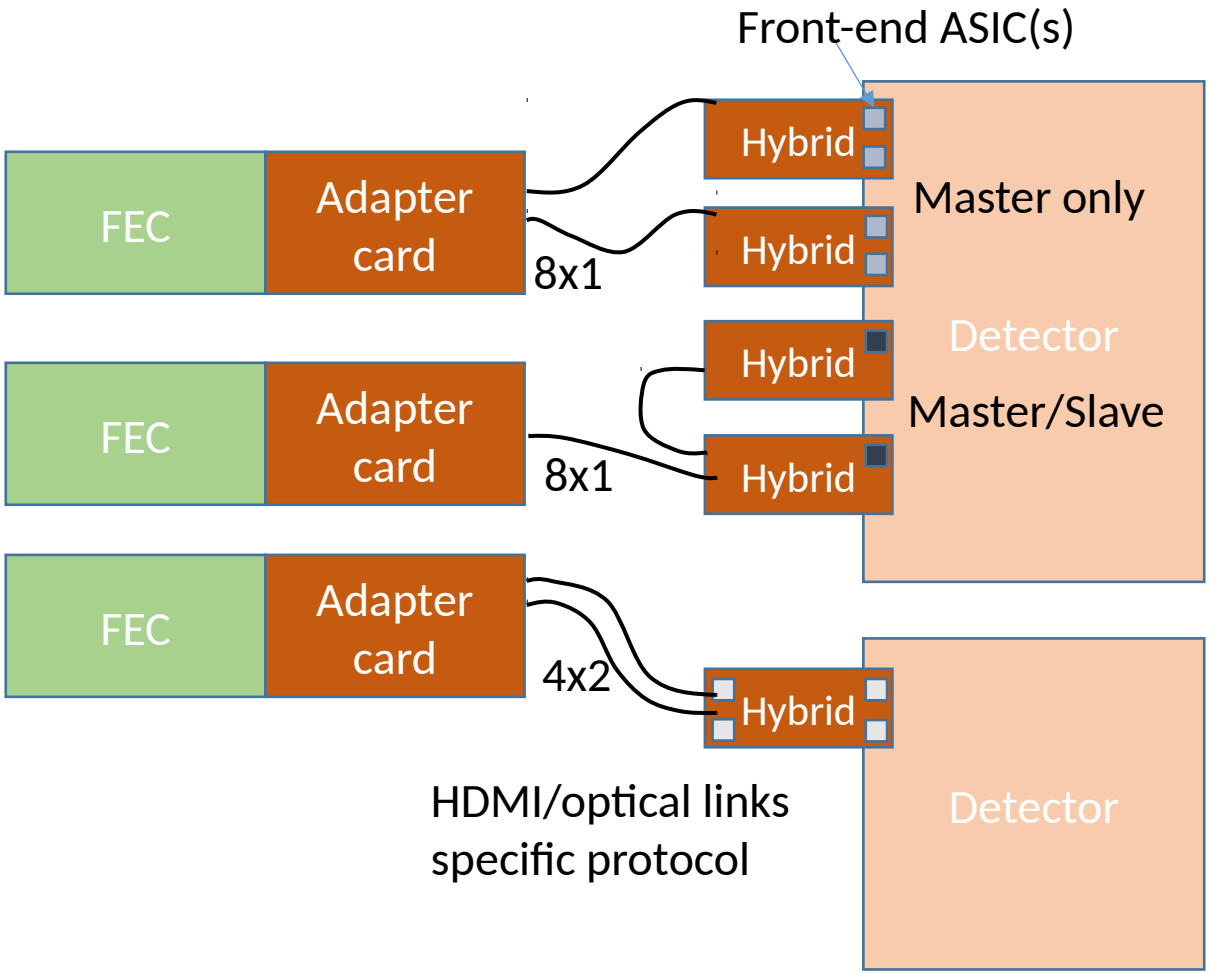

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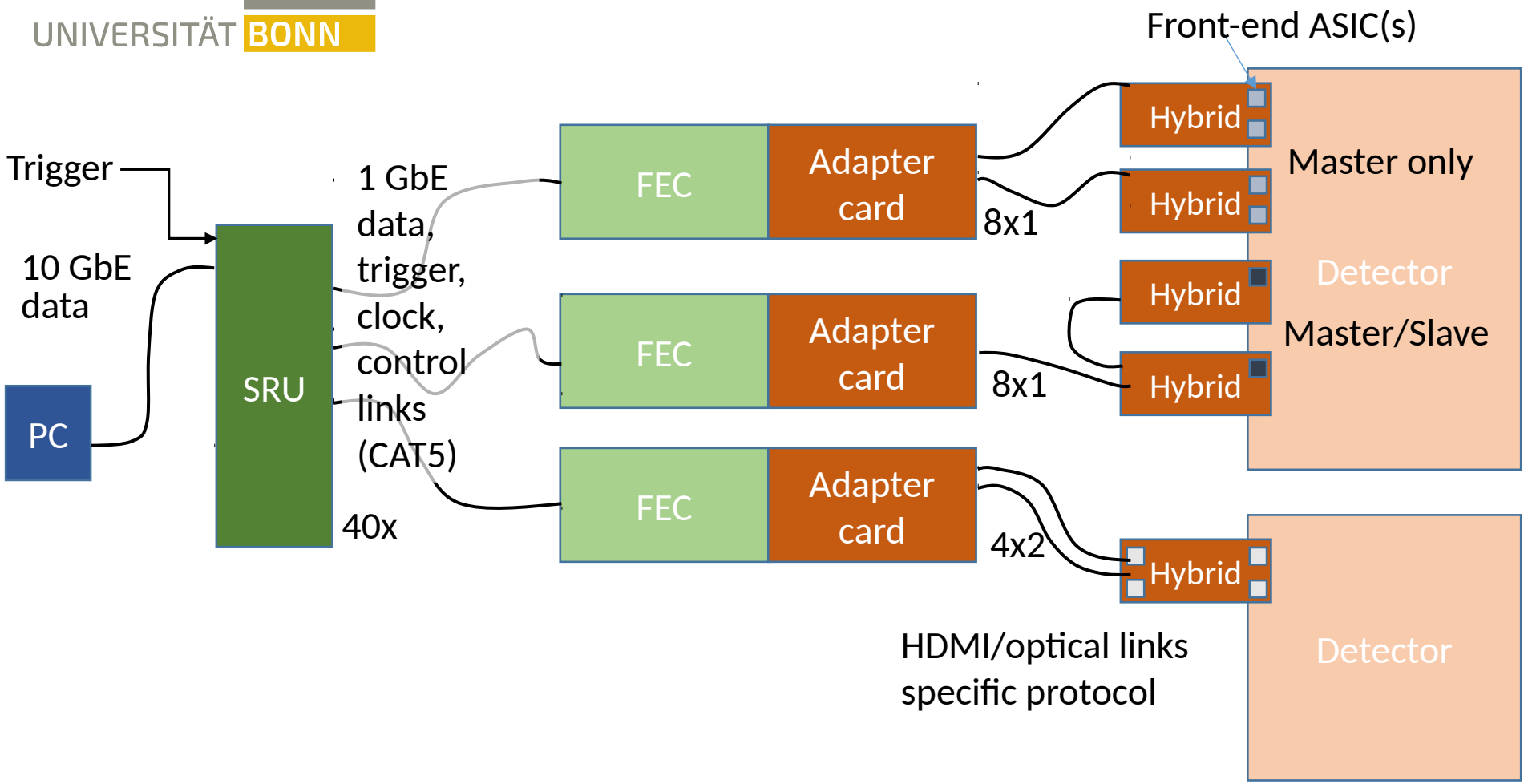
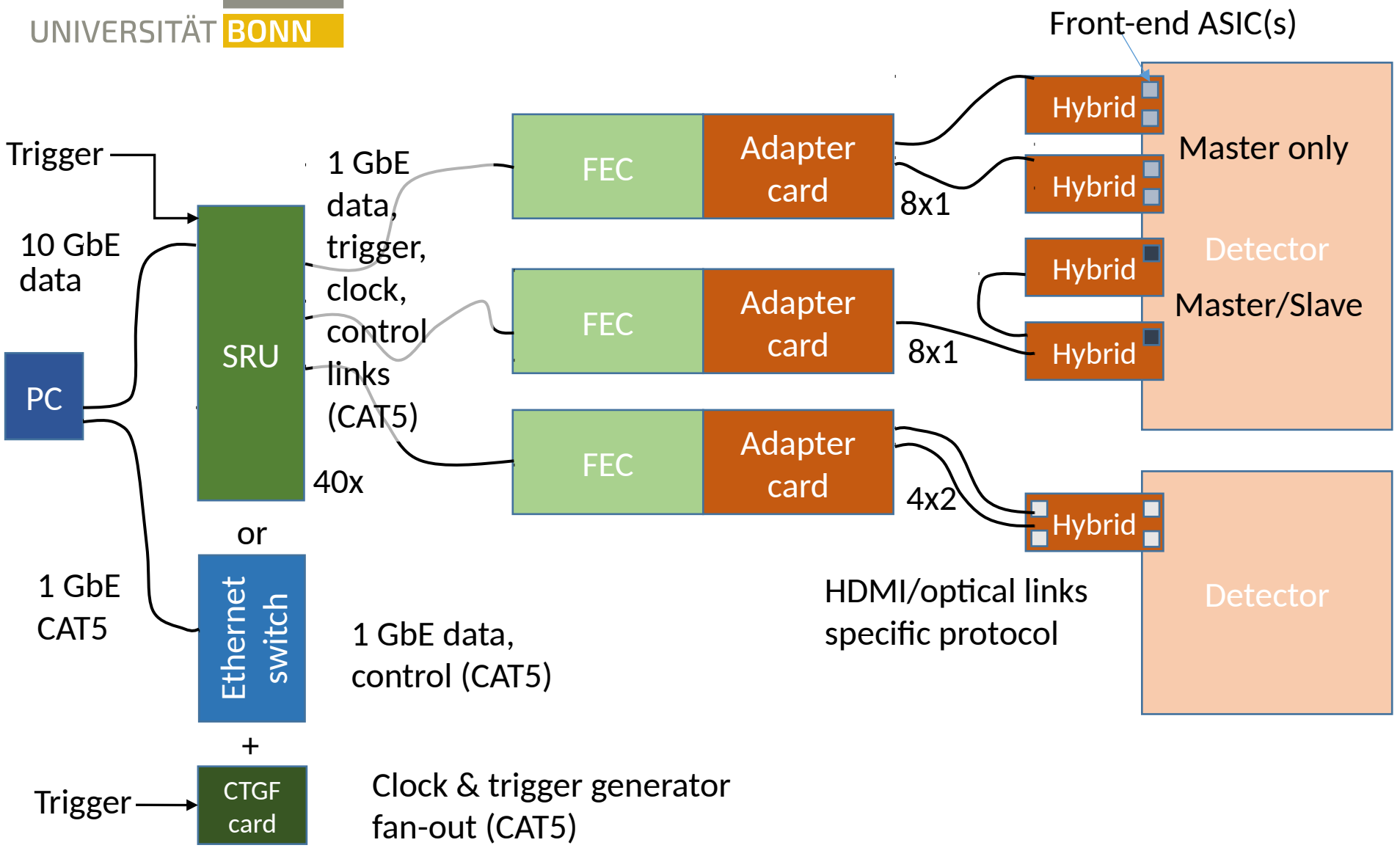
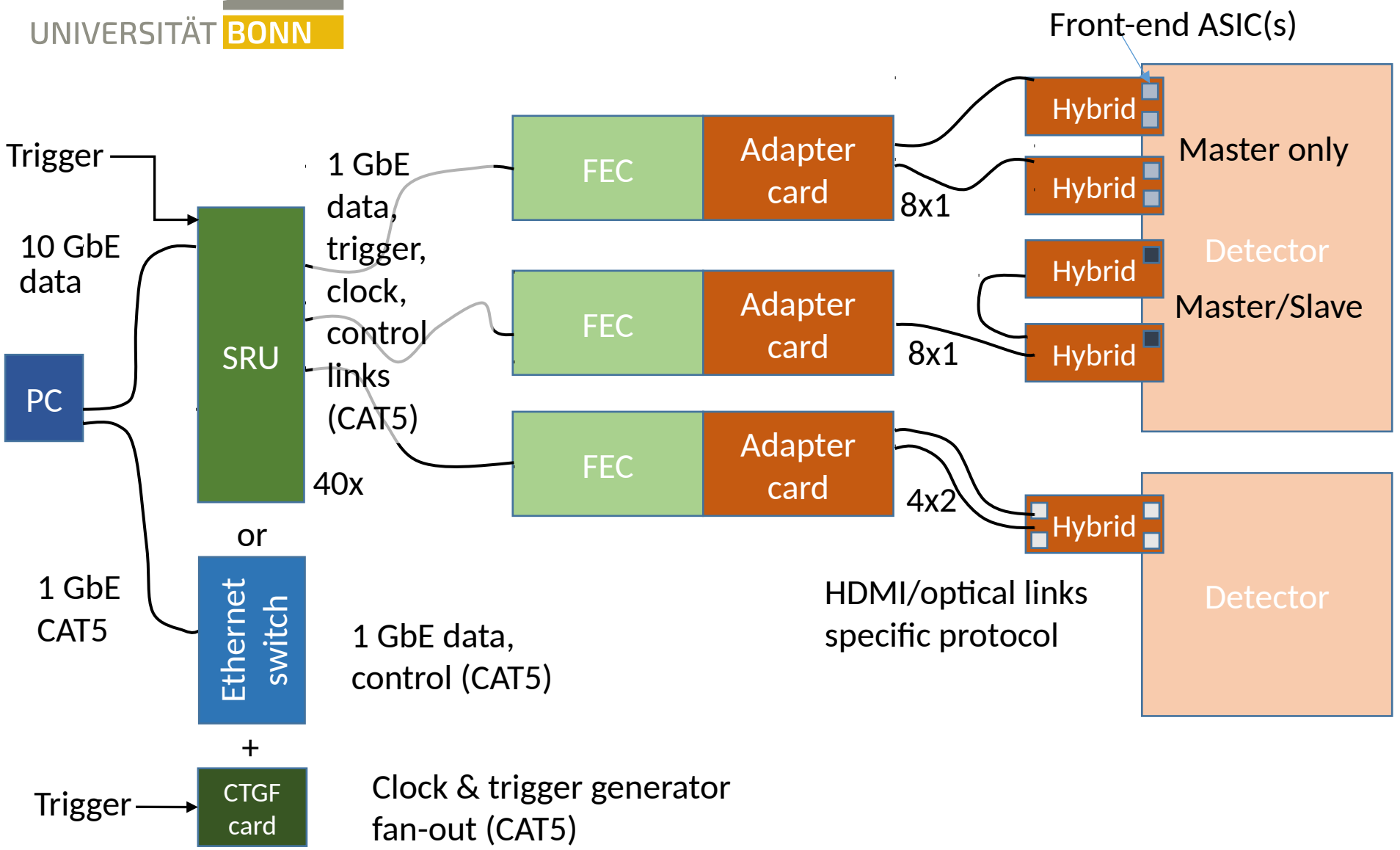

Front-end ASIC(s)
Trigger
10 GbE data
PC
SRU
1 GbE data, trigger, clock, control links (CAT5)
40x
FEC
Adapter card
8x1
FEC
Adapter card
8x1
FEC
Adapter card
4x2
Hybrid
Hybrid
Hybrid
Hybrid
Hybrid
Master only
Detector
Master/Slave
Detector
HDMI/optical links
specific protocol

WHAT IS SRS


Front-end ASIC(s)
Trigger
10 GbE data
PC
SRU
1 GbE data, trigger, clock, control links (CAT5)
40x
or
1 GbE CAT5
Ethernet switch
1 GbE data, control (CAT5)
+
Trigger
CTGF card
Clock & trigger generator fan-out (CAT5)
FEC
Adapter card
8x1
FEC
Adapter card
8x1
FEC
Adapter card
4x2
Hybrid
Hybrid
Hybrid
Hybrid
Hybrid
Master only
Detector
Master/Slave
Detector
HDMI/optical links specific protocol

WHAT IS SRS

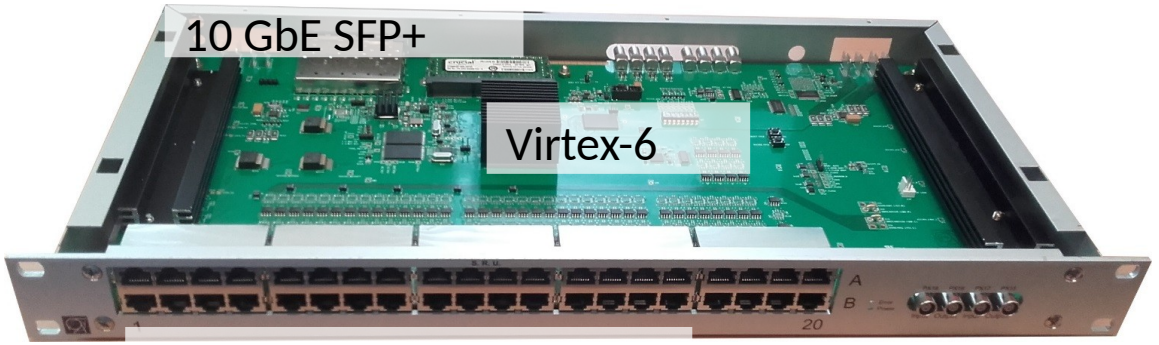


Example AVP25 (strip readout) up to:

82k ch/SRU 2048 ch/FEC 128 ch/hybrid + (master/slave)

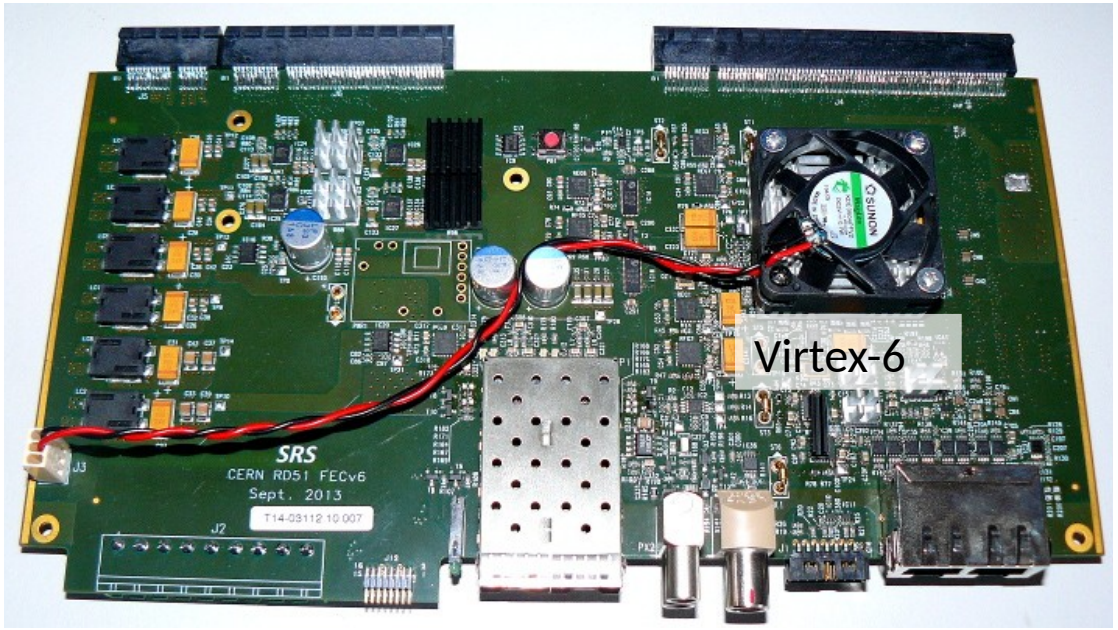
WHAT IS SRS

SRU



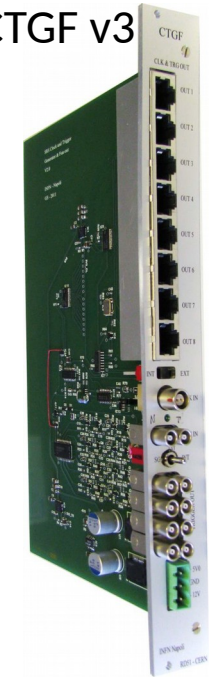
40x DDTC from FECs

FECv6 (2013)



1 GbE or DDTC to SRU

CTGF v3



FECv3 (2010)

SRS AND FRONT-END ASICS

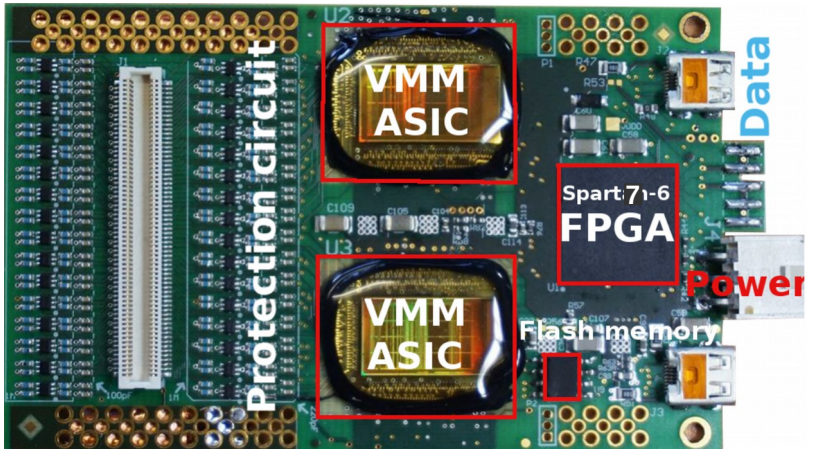
Different ASICs are implemented in SRS:
- APV25 (past backbone in MPGD R&D)
- Beetle
- VFAT
- Timepix
- SiPMs

Recently:
- Timepix3
- VMM (new backbone in MPGD R&D)

Ongoing:

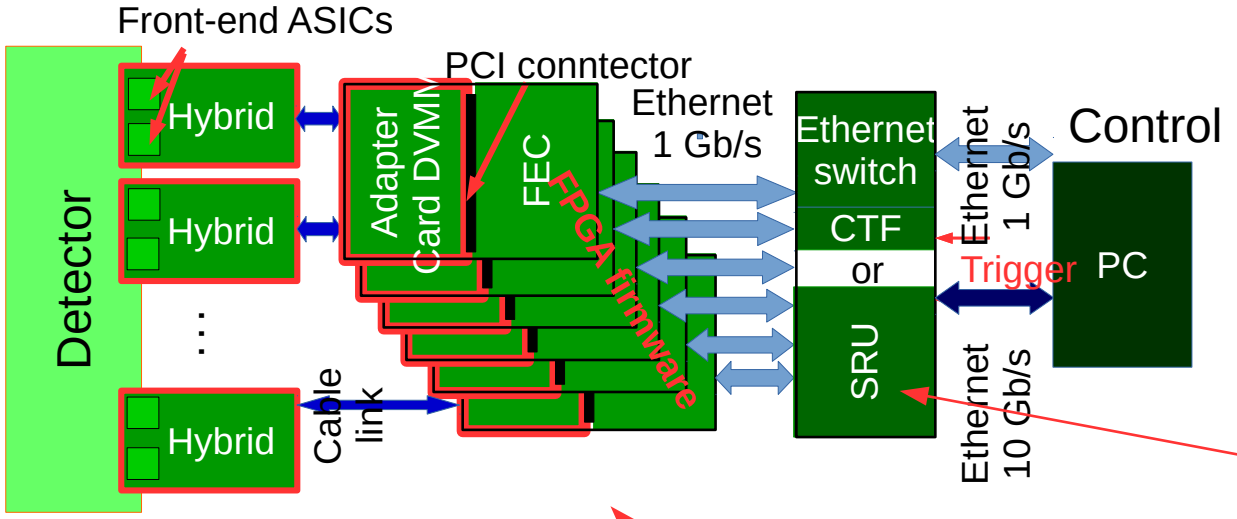
SAMPA

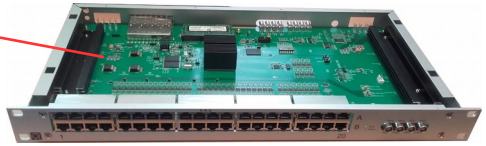
Implementation of ASIC in SRS requires: Hybrid, adapter card, FEC FPGA firmware

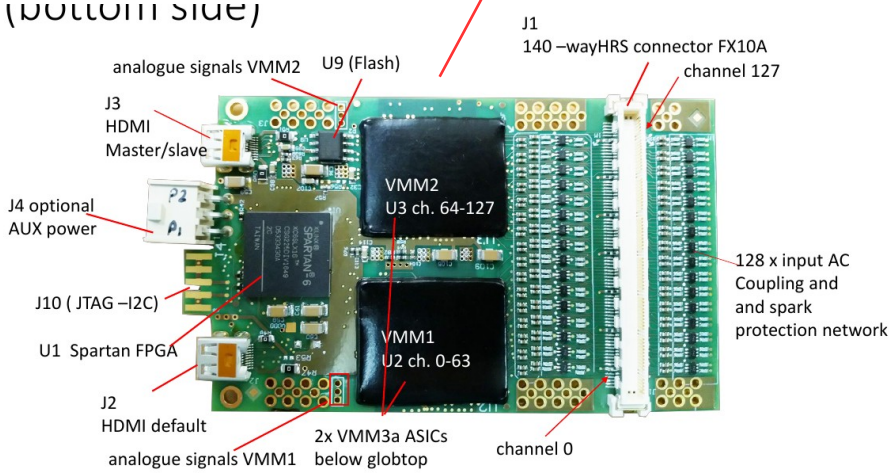


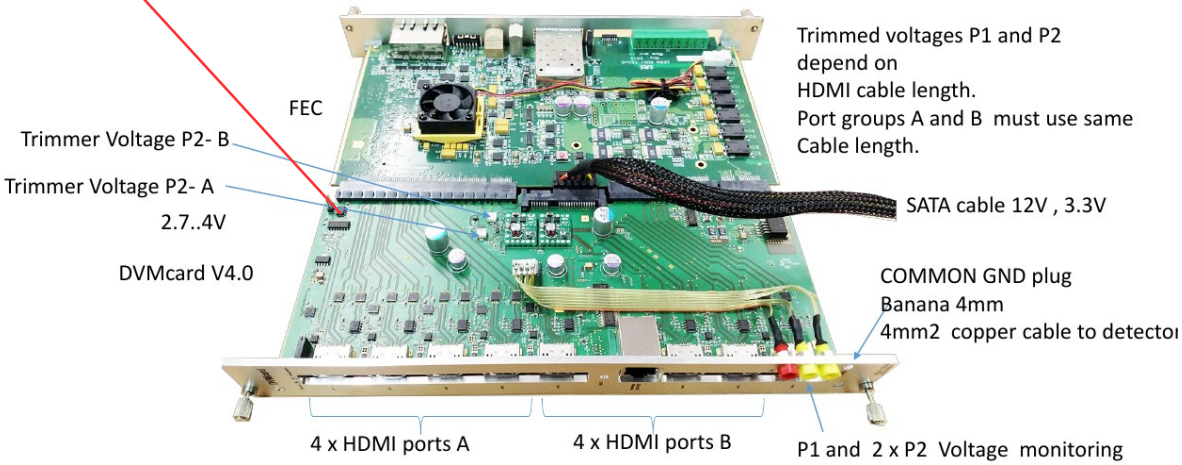
SRS VMM - DETAILS

System overview – readout chain





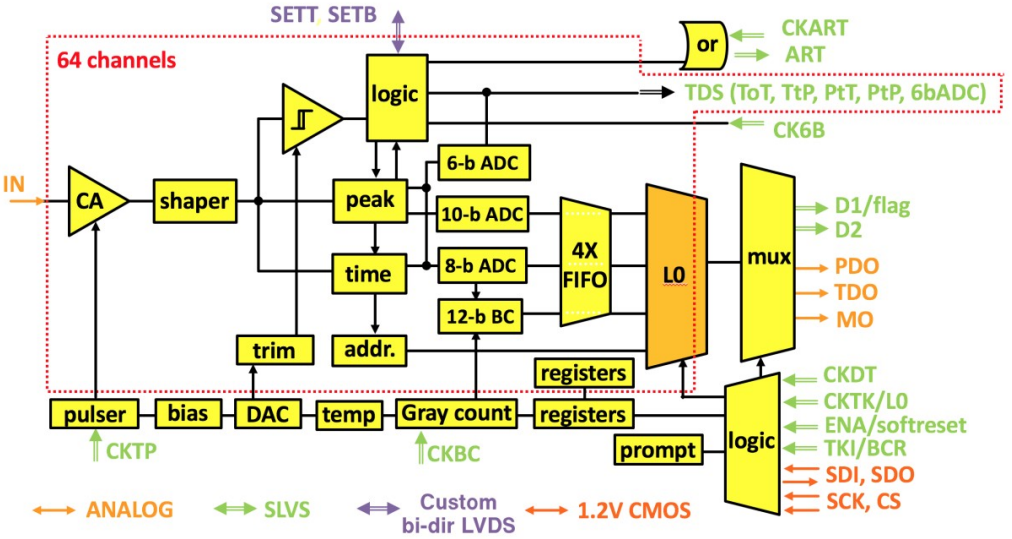




VMM FRONT-END ASIC

Developed for the ATLAS NSW upgrade by BNL

- 130 nm CMOS technology
- 64 input channels, each w/ preamplifier, shaper, peak detector, several ADCs
- Pos. & neg. polarity sensitive
- Digital block w/ neighbouring logic, FIFO, multiplexer
- Adjustable gain 0.5-16 mV/fC
- Adjustable shaping time from 25 ns – 200 ns
- Input capacitance from few pF – 1 nF



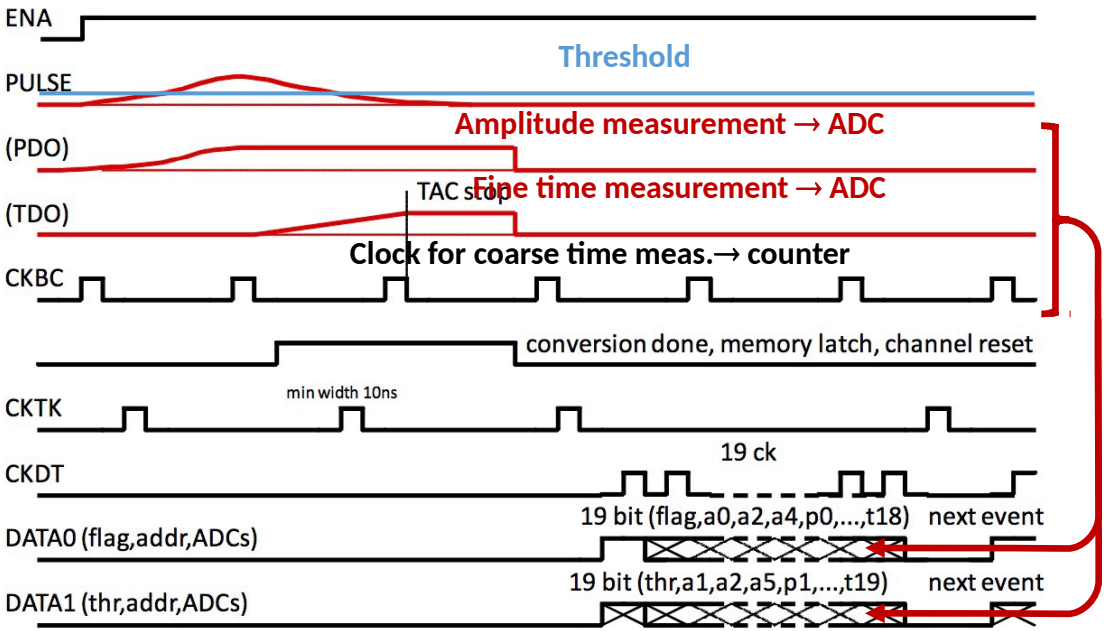
VMM FRONT-END ASIC

Developed for the ATLAS NSW upgrade by BNL

- Internal test pulser with adjustable amplitude
- Global threshold & adjustment per channel
- Self-triggered, zero suppressed
- 38 bit per hit

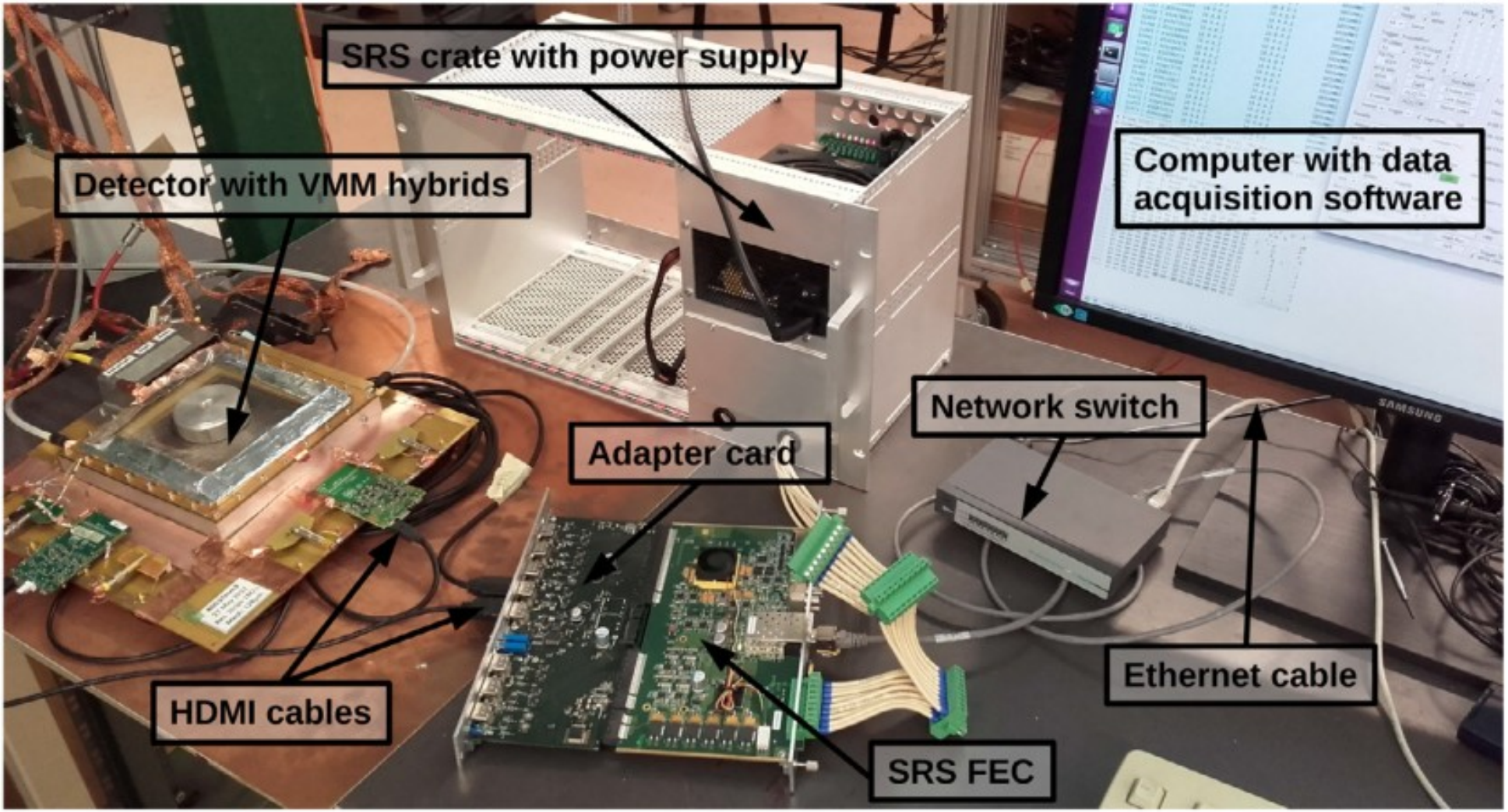
  (if input charge goes over threshold)

  1. Event flag (1 bit)
  2. Over threshold flag (1 bit)
  3. Channel number (6 bit)
  4. Signal amplitude (10 bit)
  5. Arrival time (20 bit)



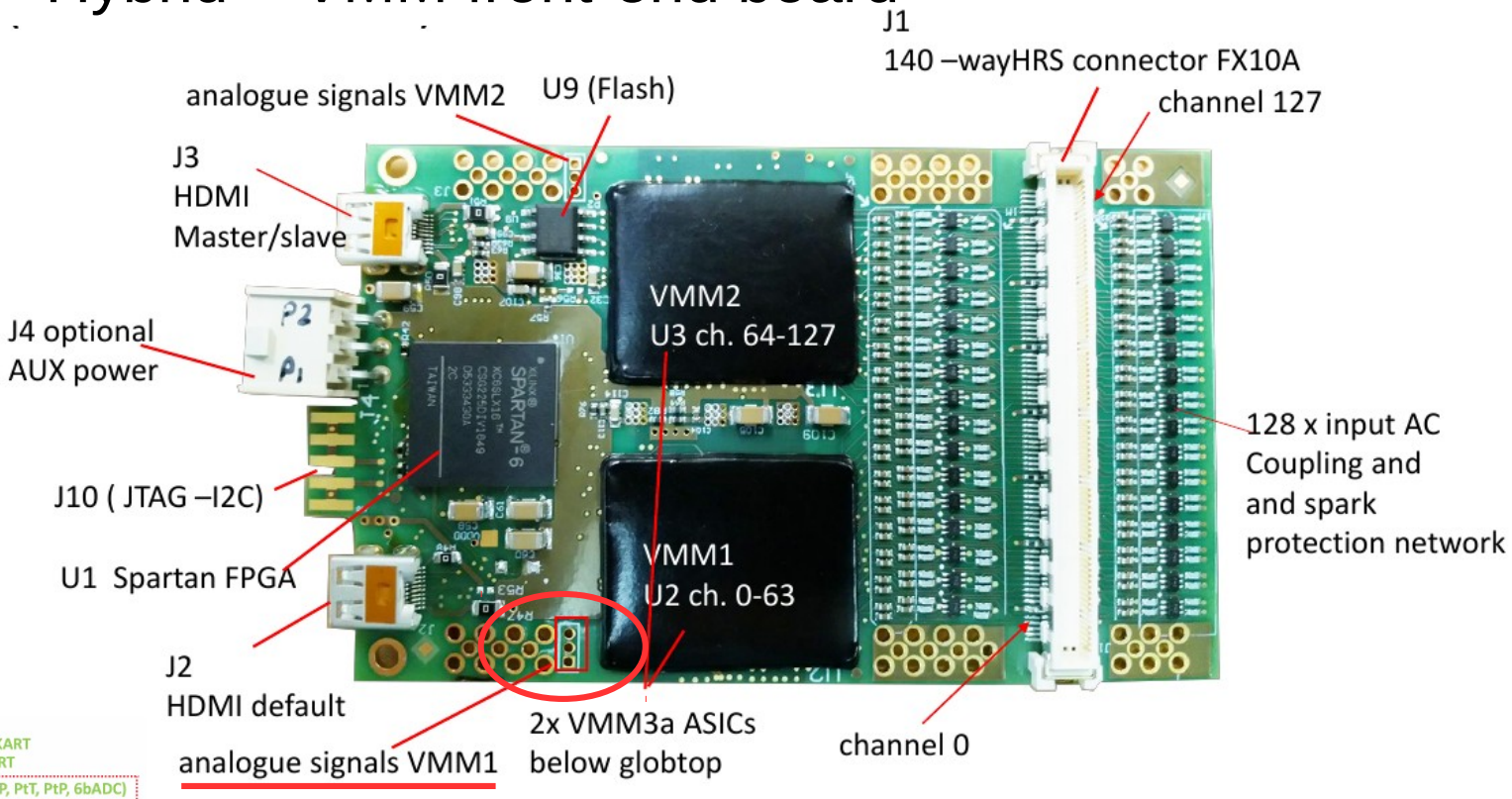
SRS VMM - DETAILS

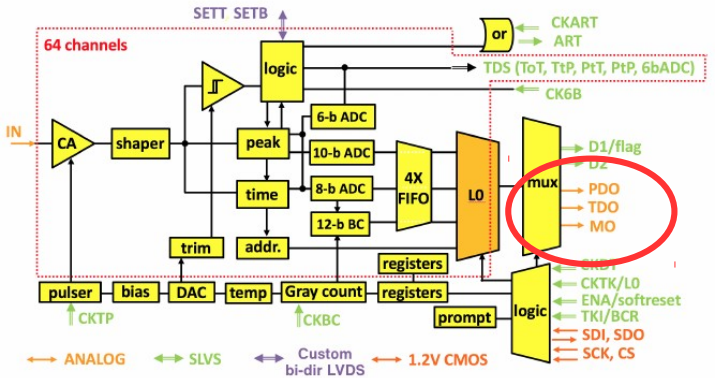
System overview – readout chain



SRS VMM - DETAILS

System overview – Hybrid = VMM front-end board





Programmable MO (Monitoring, analogue level) output:

- Global temperature sensor
- Bandgap voltage
- Pulser DAC
- Global threshold DAC
- Channel: individual threshold,baseline = shaper output

SRS VMM - DEMONSTRATION

Let’s connect to the lab