

Simulation of the Pixel readout TPC at e+e- collider

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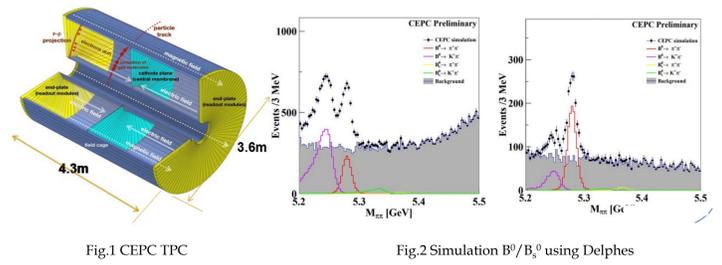
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Motivation

In some future physics experiment, such as ILC, CEPC, FCC concepts, the main tracking detectors with extremely high performance will be needed to research and develop. High precision TPCs are essential options for large-size main track detectors. The innovation of TPC technology will play a crucial role in the precise measurement of Higgs properties and the search for a variety of new physics particles.

TPC Requirement for e+e- Higgs/EW/Top Factories

- Provide decent Hits (for track finding) with high spatial resolution compatible with PFA design
 - $\delta(1/p_t) \sim 10^{-4} \text{ GeV}/c$ (TPC alone) and $\sigma_{\text{point}} < 100 \mu\text{m}$
 - Provide dE/dx and dN/dx with a resolution $< 3\%$
- ➔
- Essential for Particle Identification
 - Beneficial for Flavor Physics at Z pole



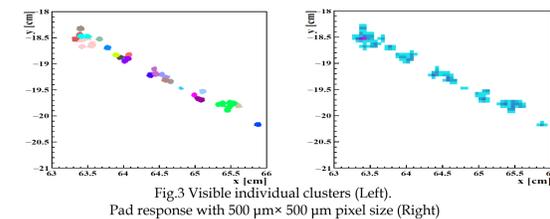
Pixel Readout TPC

Classical dE/dx Measurement by Charge

- measure charge per sample along a track
 - Key problem: sensitive to large fluctuations
- $p_T = 0.3 \text{ Br}$
 $p = \sqrt{1 + \tan^2 \gamma}$
 $p + dE/dx \rightarrow \text{PID}$
- $Sp = \frac{dE/dx(A) - dE/dx(B)}{\sigma(dE/dx)}$

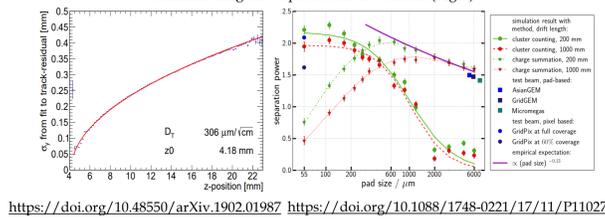
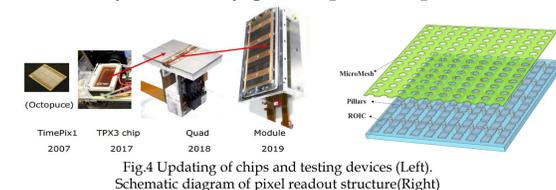
NEW dN/dx Measurement by Cluster Counting

- Pixel TPC makes cluster space measurement possible
- avoid any problems with cluster fluctuations
- $< 3\%$ dE/dx resolution by cluster counting
- Improve the particle identification ability of TPC



GridPixes Pixel TPC Readout in LCTPC

- Tests with single and quad devices have been successfully done
- $\sim 4.1\%$ resolution at $B = 1.0\text{T}$ at DESY
- For very small readout pads the cluster counting method yields a very good separation power



Advantages of Pixel Readout

- High granularity readout allows measuring every ionization cluster
- High spatial resolution under 2T or 3T
- Better momentum resolution
- High-rate operation (MHz/cm²)
- Excellent two tracks separation

Application of Pixel Readout in CEPC-TPC

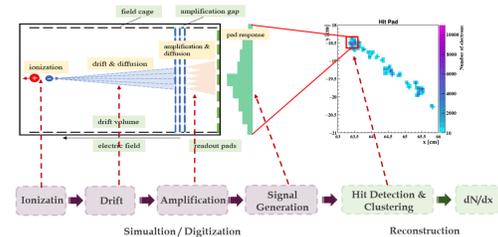
- Pixel Readout is a feasible option for CEPC
- The next steps involve optimizing the size of pixels, detector geometry, occupancy

Pad readout	Pixel readout
Readout size : $2 \times 10 \text{ m}^2$	Readout size : $2 \times 10 \text{ m}^2$
MPGD Readout	Micromegas Readout
Single Pad size : $\geq 1 \text{ mm} \times 6 \text{ mm}$	Single pixel size : $\geq 55 \mu\text{m} \times 55 \mu\text{m}$
10^6 readout units	10^9 readout units
$dE/dx < 5\%$	$dE/dx < 3\%$
Rate : kHz/cm ²	Rate : MHz/cm ²

Table.1 Comparison of Two Readout Methods for CEPC-TPC

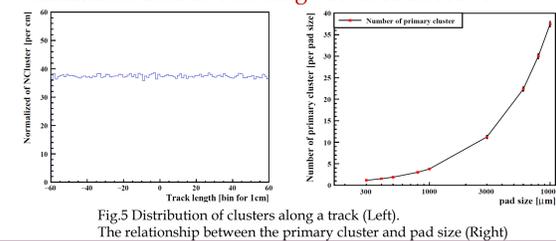
Simulation Studies on Cluster Counting

Full Simulation Framework of Pixel TPC



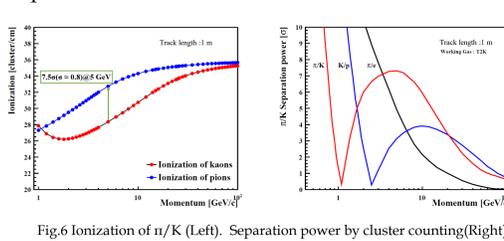
Simulation of the Primary Cluster

- Typically ~ 30 primary ionization clusters/cm in gas at 1 bar ~ 1.9 clusters/ $500 \mu\text{m}$, ~ 1.1 clusters/ $300 \mu\text{m}$
- If pad size is at the level of cluster distances of primary ionization Cluster counting becomes effective

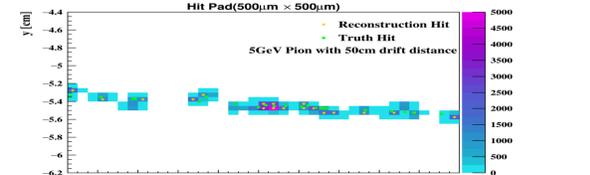


PID Improvement by Cluster Counting

- At 5 GeV, the particle separation power for π/K particles can achieve 7.5 σ
- Cluster counting exhibits excellent potential for particle identification

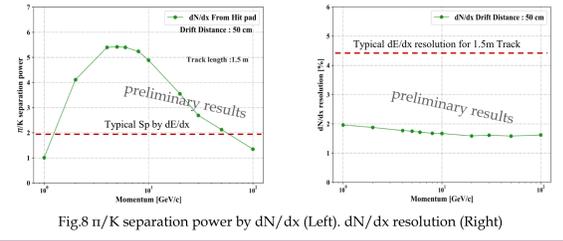


$$Sp = \frac{|\mu_A - \mu_B|}{\sqrt{\frac{\sigma_A^2 + \sigma_B^2}{2}}}$$



Preliminary PID Performance

- Investigating the π/K discrimination capability using reconstructed clusters, a 3σ separation at 20GeV with a 50cm drift distance can be achieved
- dN/dx has significant potential for improving resolution



R&D Plan & Efforts

R&D Plan

- Bump bond pixel readout with Micromegas detector
- Developed the readout chip at Tsinghua
- Developed the Micromegas detector sensor at IHEP



Fig.9 Design of Pixel TPC at IHEP

Future Plan

- Further simulations are still necessary to understand the detailed requirements of the pixel detector (e.g. More realistic simulation model; More sophisticated reconstruction; Detector optimization etc.)
- The simulation work will contribute to the upcoming release of the CEPC TDR in 2024.

Current R&D Efforts

- R&D on pixel TPC readout for CEPC
- Pixel TPC ASIC chip was started to develop in 2023 and 1st prototype wafer standalone tested in May.
 - ✓ Power consumption: $< 1.1 \text{ mW}/\text{ch}$ (1st prototype)
 - ✓ $< 400 \text{ mW}/\text{cm}^2$ (Test)
- 2nd prototype wafer design done
 - ✓ $< 100 \text{ mW}/\text{cm}^2$ (Goal and final design)

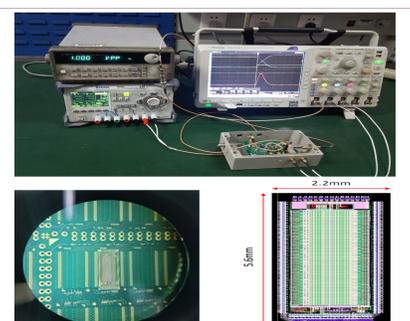


Fig.10 1st readout PCB board and the ASIC layout