Evaluation of the Radiation Tolerance of SiGe Heterojunction Bipolar Transistors Under Gamma Exposure

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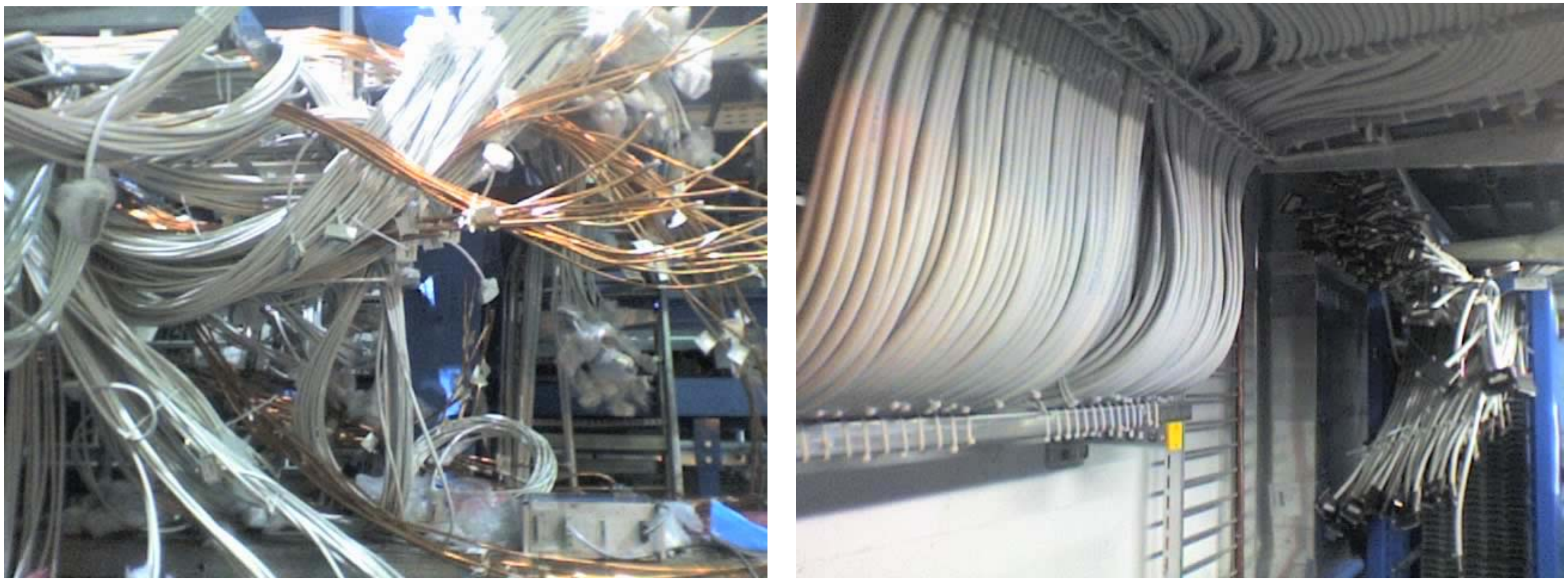
Power Constraints

ATLAS already has over 4,000 heavy copper cables for the SCT alone!

-> Need to reduce power consumption w/out sacrificing noise performance at high radiation levels for ATLAS Upgrade if we want to replace the TRT with silicon.

Target for Front-End Channel (Analog Section Only):	Current ATLAS:
<400µW @ 15pF (long strips at outer radius, 60cm)	2 mW
<160µW @ 6pF (short strips at mid-radius, 20 cm)	



Why SiGe?

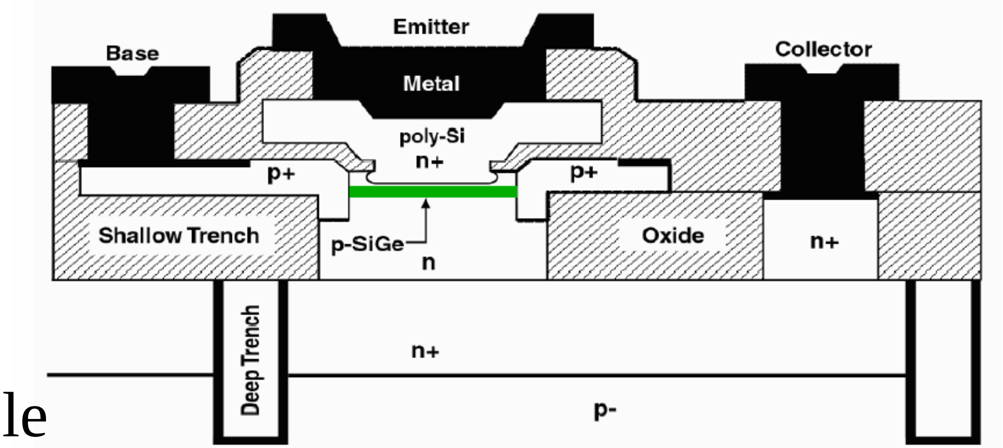
Advantages of SiGe Bipolar Over CMOS for Silicon Strip Detectors

- A key element in the design of low noise, fast shaping, charge amplifiers is high transconductance in the first stage.
- With CMOS technologies, this requires relatively larger bias currents than with bipolar technologies.
- The changes that make SiGe Bipolar technology operate at 100 GHz for the wireless industry coincide with the features that enhance performance in high energy particle physics applications.
  - Small feature size increases radiation tolerance.
  - Extremely small base resistance (of order 10-100 Ω) affords low noise designs at very low bias currents.
- These design features are important for applications with:
  - Large capacitive loads (e.g. 5-15 pF silicon strip detectors)
  - Fast shaping times (e.g. accelerator experiments with beam crossing times of tens of nanoseconds in order to identify individual beam crossing events)

SiGe Technology

Origin of radiation tolerance:

- Small active volume of the transistor
- Thin emitter-base spacer oxide (weakest spot)



SiGe Technology Readily Available

- Over 25 foundries
- Some Vendors: IBM, IHP, JAZZ, Motorola, STm…

IBM offers 3 generations (4th on the way):

- 5HP (5AM): 0.5x1 -> 0.5x20 μm^2
- 7HP: 0.2x1 -> 0.28x20 μm^2
- 8HP: 0.12x0.52 -> 0.12x8 μm^2

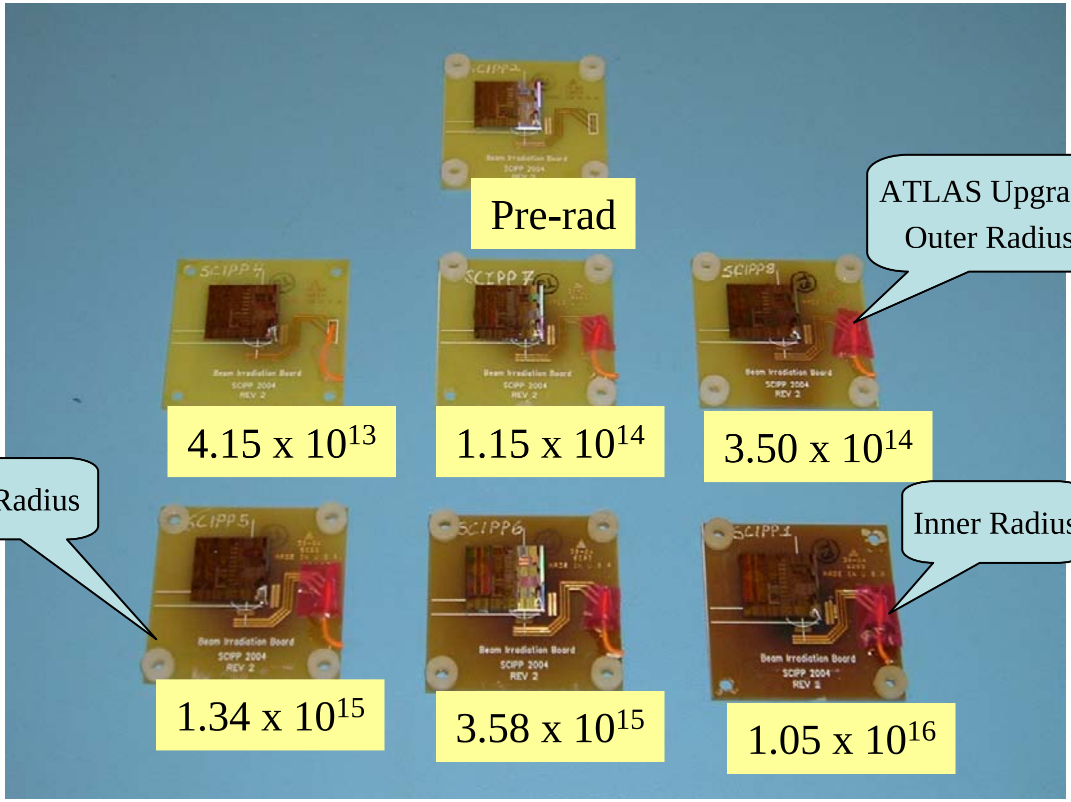
IHP SiGe Technology:

- Radiation Tolerance Study by:
  - Miguel Ullán, et al CNM, Barcelona
- Ned Spencer (SCIPP) has designed an amplifier with IHP as a proof of principle

Summary of 2004 Proton Results

Irradiation Procedure:

- 5AM devices were sent to CERN and exposed to a 24GeV proton source with the highest fluence taking 5 days to accumulate.
- The leads were grounded during irradiation --> worst case scenario.
- The transistors were annealed to improve performance.
- **Special thanks to the RD50 collaboration, especially, Michael Moll and Maurice Glaser!!**



Pre-rad

ATLAS Upgrade Outer Radius

4.15×10^{13}

1.15×10^{14}

3.50×10^{14}

Mid Radius

Inner Radius

1.34×10^{15}

3.58×10^{15}

1.05×10^{16}

Device Sizes:

$0.5 \times 1\ \mu m^2$

$0.5 \times 2.5\ \mu m^2$

$0.5 \times 10\ \mu m^2$

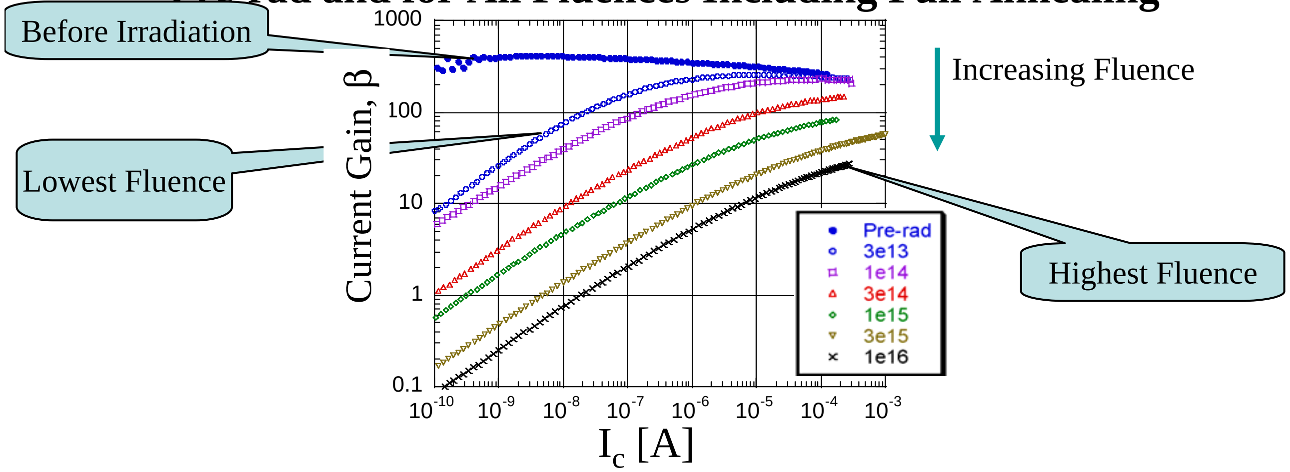
$0.5 \times 20\ \mu m^2$

$4 \times 5\ \mu m^2$

Summary of 2004 Proton Results

Current Gain, β, vs. I_c for 0.5x10 μm^2

Pre-rad and for All Fluences Including Full Annealing



Conclusions:

- @ 3x10^{14}, I_c low enough for substantial power savings over CMOS
- @1x10^{15}, I_c good for a front transistor (uses a higher current while minimizing noise)

Fluence: 3.50E14 p/cm^2 (2.17x10^{14} n$_{eq}$/cm^2)
β=50

Transistor Size μm^2	I_c irrad	I_c anneal
0.5x1	2.E-06	
0.5x2.5	4.E-06	5.E-08
0.5x10	3.E-05	8.E-07
0.5x20	5.E-05	2.E-06
4x5	9.E-06	5.E-07

Fluence: 1.34E15 p/cm^2 (8.32x10^{14} n$_{eq}$/cm^2)
β=50

Transistor Size μm^2	I_c irrad	I_c anneal
0.5x1	3.E-05	1.E-07
0.5x2.5	7.E-05	4.E-06
0.5x10	4.E-04	9.E-06
0.5x20		6.E-05
4x5	1.E-04	1.E-05

Current Investigation

Gamma, Neutron & Proton Irradiations:

Device Types:	Number Transistors Per Chip:	Number Chips:	Number Measurements:	Number Runs:
8HP HBT	8	26	7	6
7HP HBT	8	14	7	6
5HP HBT	10	3	7	6
5AM HBT	6	10	7	6
8HP Resistor	10	16	1	6
8HP Capacitor	12	15	1	6
			Total:	**22410**

Tests:

- 8HP HBT
- 8HP HBT--Biased
  - For gammas & protons
- 8HP HBT--Shield
  - For gammas & neutrons
- 7HP HBT
- 5AM HBT
- 8HP Resistor
- 8HP Capacitor

Measurements:

- Forward Gummel
  - Vcb=0V, 0.5V
- Inverse Gummel
  - Vcb=0V, 0.5V
- Early Voltage
- Neutral Base Recombination
- M-1, Avalanche Factor
- Resistance
- Capacitance

Runs:

- Characterization (Pre-Rad)
- Post-Rad (No Anneal)
- Anneal 1 (5 days @ 25C)
- Anneal 2 (1 day @ 60C)
- Anneal 3 (1 day @ 100C)
- Anneal 4 (6 days @ 100C)

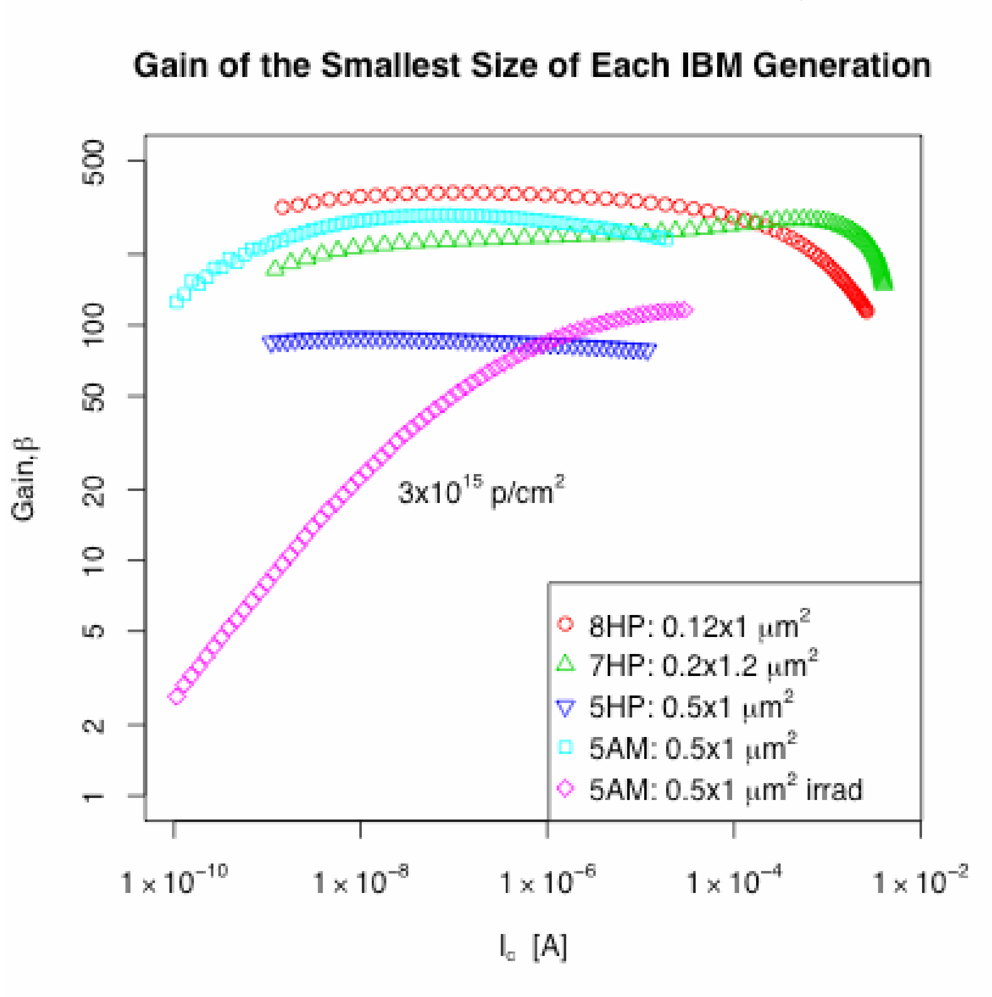
- Over 22,000 measurements planned!!!
- Developed an automatic measuring system at SCIPP and BNL

->Plug in a chip, take all measurements for all transistors at once

Will this be enough to understand the specific mechanisms for device degradation??

Current Investigation

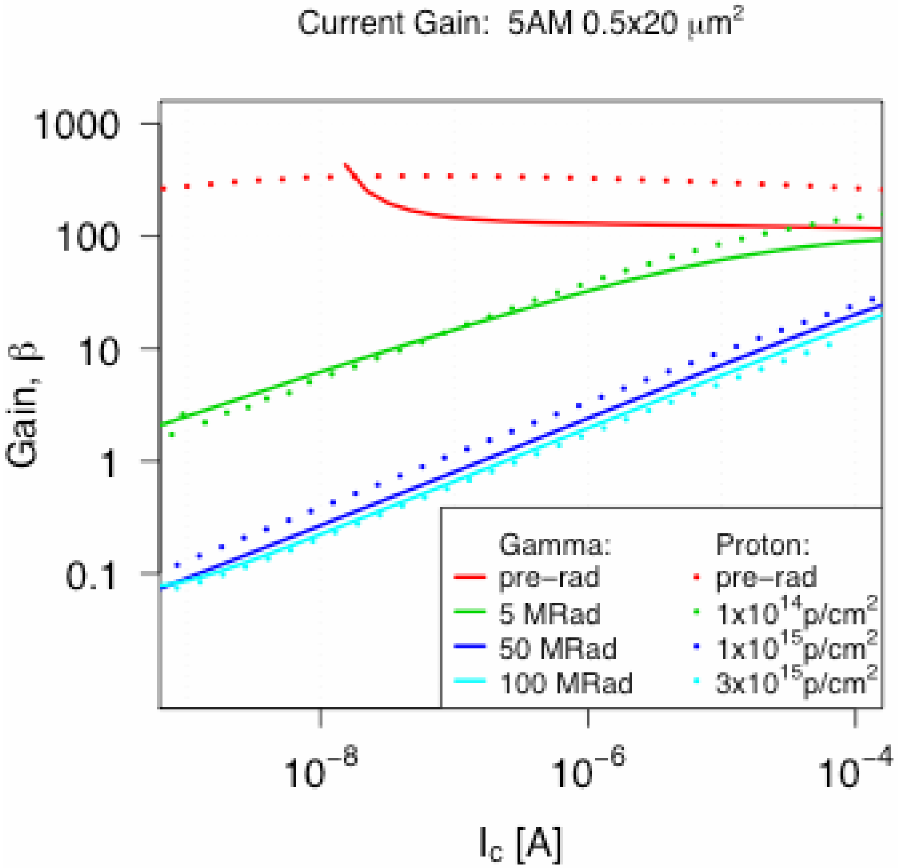
Characterization measurements:



Irrad Procedure for Gammas:

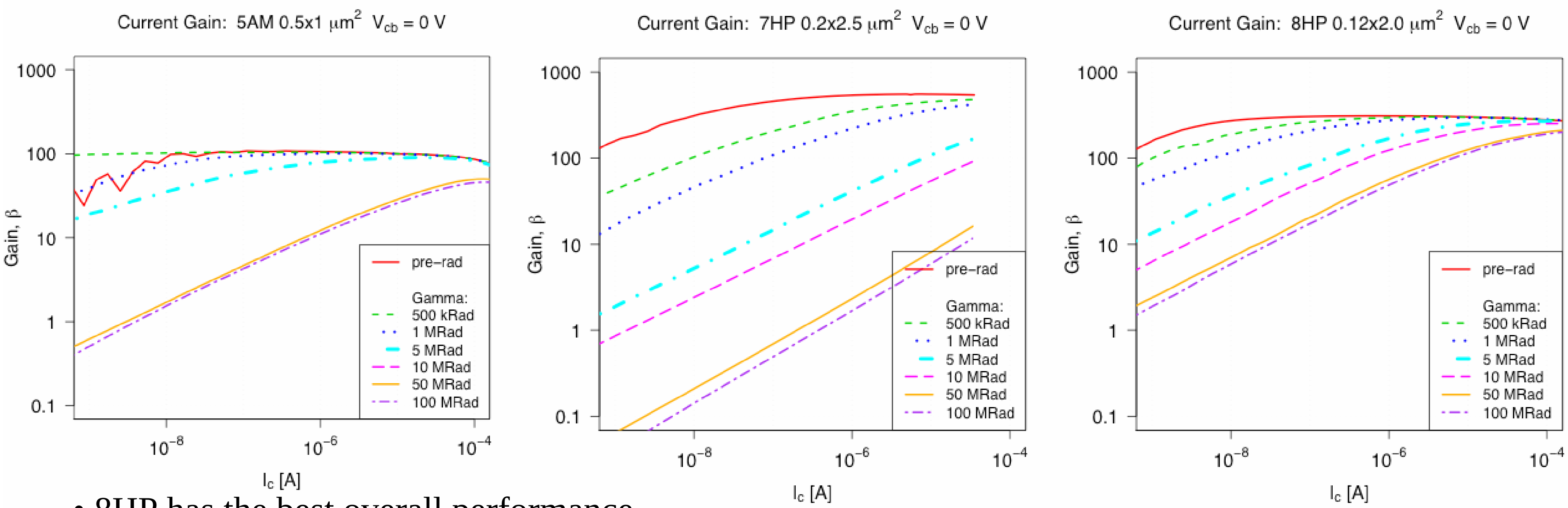
- ^{60}Co source at BNL
- Measurements performed at BNL
- Total dose of 100 Mrads
- Devices tested at steps:
  - 500 kRad
  - 1 Mrad
  - 5 Mrad
  - 10 Mrad
  - 50 Mrad
  - 100 Mrad
- Devices shorted during irrad
  - Except one 8HP HBT chip biased
- No Shield* (next round)

Preliminary Gamma Results



The damage caused by gammas and protons for comparable doses/fluences is very similar even though starting gain values are different. This <u>may</u> imply that most of the gain degradation is induced by ionization damage.

Preliminary Gamma Results

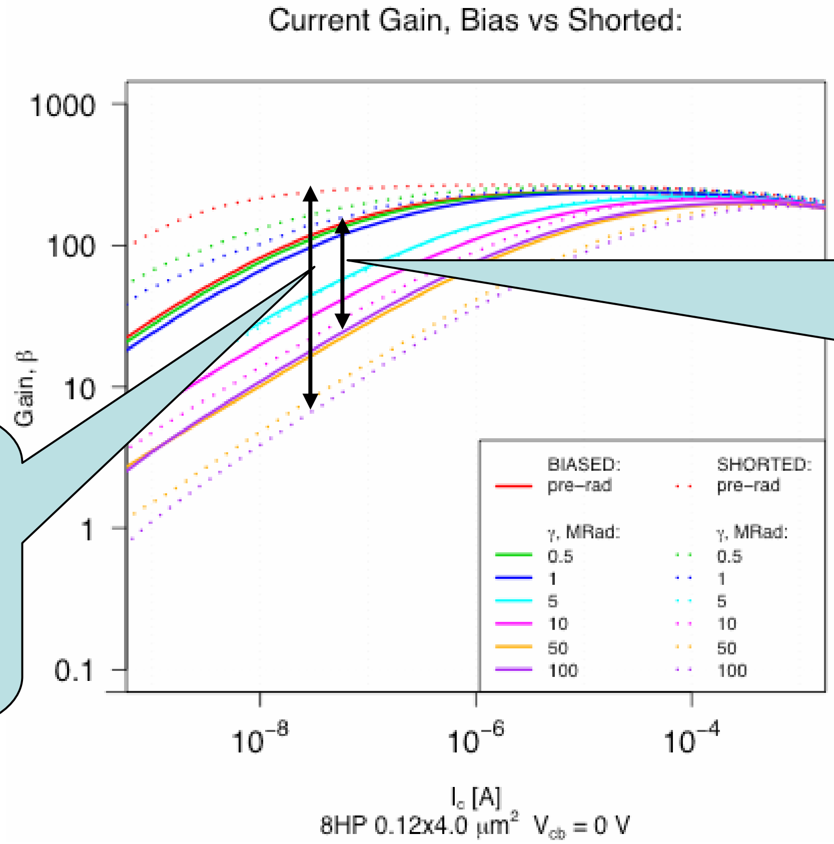


- 8HP has the best overall performance.

- The damage mechanism in the 7HP is distinctly different due to structural differences.

“ Ionizing radiation has been shown to damage the EB spacer region in these SiGe HBTs, and produce a perimeter-dependent space-charge generation/recombination (G/R) base-current leakage component that progressively degrades the base current (and current gain) as the fluence increases. …the 7HP device degrades much more rapidly than the 5HP device. This result is consistent with significantly higher EB electric field under the EB spacer region in the 7HP device, which has both more abrupt doping profiles…as well as a decreased EB spacer thickness compared to the 5HP device…” *Silicon-Germanium Heterojunction Bipolar Transistors*, Cressler, Niu

Preliminary Gamma Results

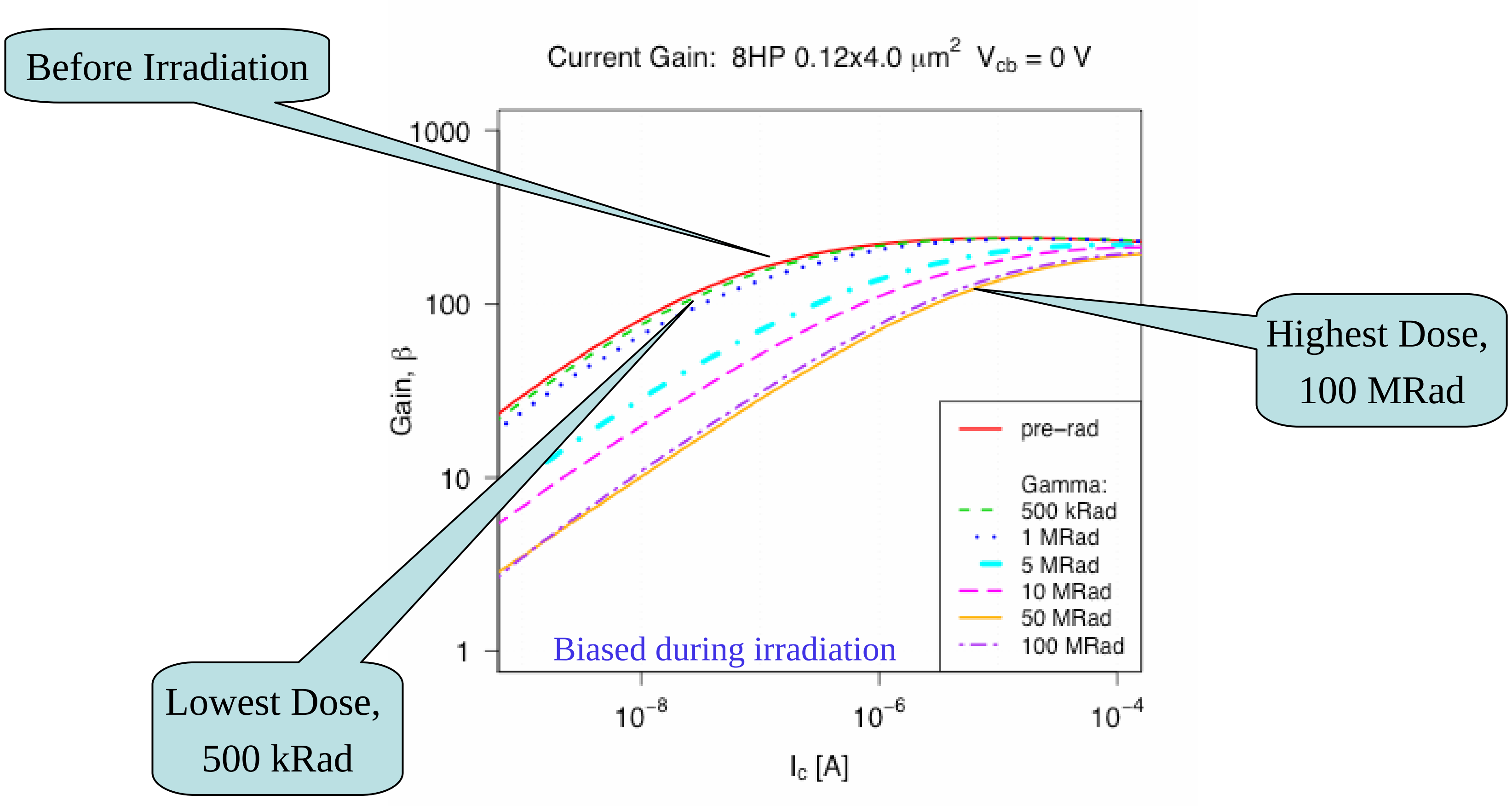


The gain of the
shorted 8HP HBT
degrades more rapidly
after 100 MRads.

The gain of the
biased 8HP HBT
performs much better
after 100 MRads, even
though it started at
a lower gain value!!

The gain for the biased transistor started at a lower gain value (normal fluctuation in starting gain), but by 5 MRads showed less radiation damage. At higher doses this effect becomes enhanced indicating that device performance at high doses for transistors shorted during irradiation will be improved.

Preliminary Gamma Results: Biased



Before Irradiation

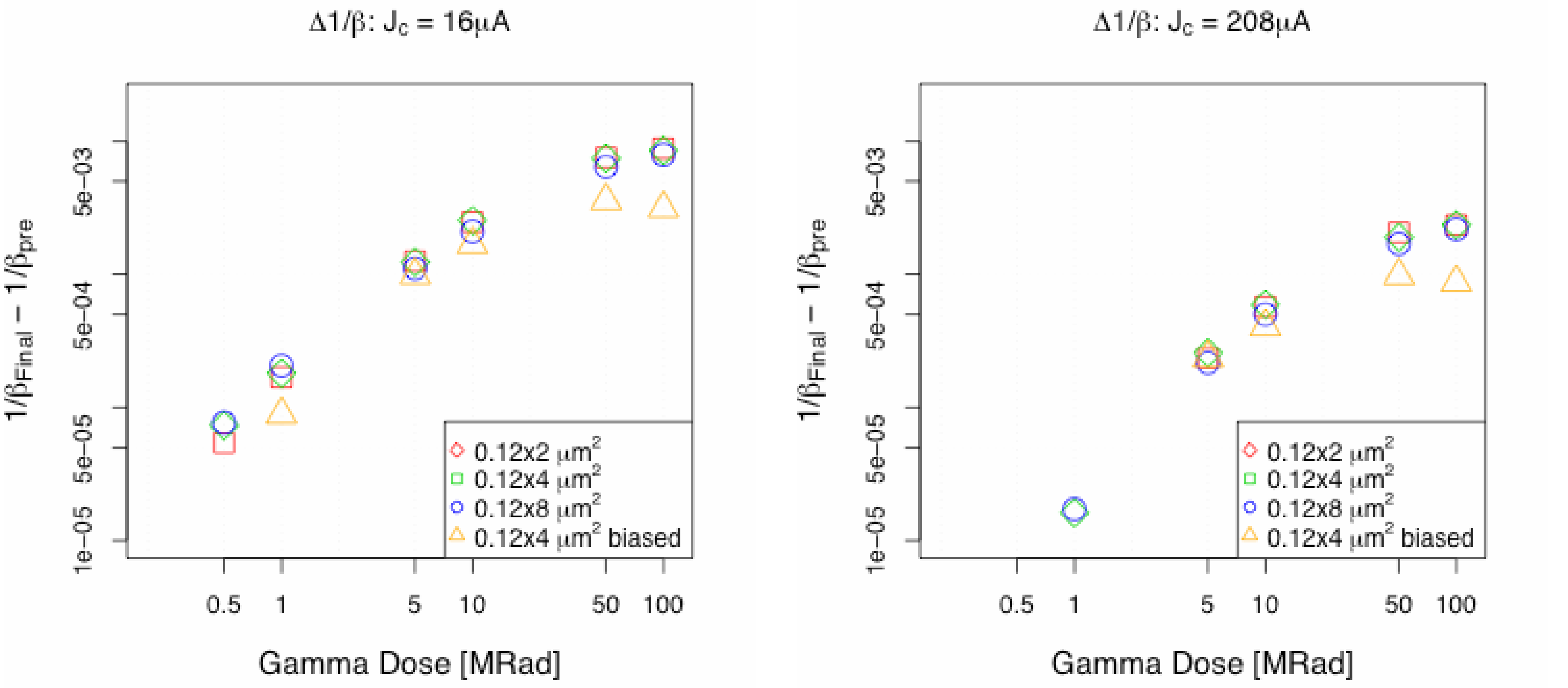
Highest Dose, 100 MRad

Lowest Dose, 500 kRad

Biased during irradiation

Transistor performance at for 8HP at 100 Mrad is very good--the current gain is still 77 at 1µA!! (No annealing yet!)

Preliminary Gamma Results



Universal behavior is independent of transistor geometry when compared at the same current density J_c and for similarly shorted or biased transistors. For a given current density Δ(1/β) scales linearly with the log of the fluence. This precise relation allows the gain after irradiation to be predicted for other SiGe HBTs for shorted devices before annealing. Hence, the operating currents can be scaled to desired device sizes for Front-End Channel simulations.

Preliminary Gamma Results

Qualifications for a good transistor:

A gain of 50 is a good figure of merit for a transistor to use in a front-end circuit design.

β=50

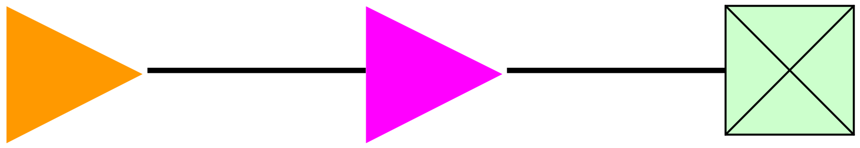
100 MRad

Type:	size (μm^2)	I_C (μA)	J_C ($\mu A/\mu m^2$)
5AM HBT Shorted:	0.5x1	145	290
	0.5x2.5	216	173
	0.5x20	179	18
7HP HBT Shorted:	0.2x2.5	217	434
	0.2x5	62	62
	0.28x5	83	30
8HP HBT Shorted:	0.12x2	1.0	4.2
	0.12x4	2.0	4.2
	0.12x8	3.8	3.9
8HP HBT Biased:	0.12x4	0.28	0.58

Requires only 0.28 μA to reach a gain of 50!!

At 100 Mrad (before annealing!), the dose reached at the mid-region of ATLAS Upgrade, very small currents can be used in the design of the front transistor and the others in a Front-End Channel design. This provides flexibility in choosing the operating current for the transistor, which allows the FEC design to optimize other factors such as matching.

Preliminary Power Savings



	Pre-Amp	Amplifier-Shaper	Comparator	Total
0.25 µm CMOS	300 µA (120 µA)*	210 µA	120 µA	1.5 mW (1.1 mW)*
SiGe IHP	150 µA (40 µA)*	13 µA	16.6 µA	0.36 mW (0.14 mW)*

* Low capacitance (7 pF) = Short strip

→ FEE Design 360 µW/Channel

SPICE simulations with IHP models predicts these currents yield a Front-End Channel design using only 360 µW!! Current ATLAS uses 2 mW!

*CMOS numbers courtesy of Kaplon

Conclusions

- Radiation damage may be primarily due to ionization damage.
- 8HP appears to be more Rad Tolerant than 5AM or 7HP.
- HBTs biased during irradiation (closer to actual conditions in ATLAS) show less damage--interesting to see after annealing.
- Preliminary results of gamma irradiations indicate that IBM 8HP SiGe Technology is sufficiently Rad Tolerant for ATLAS Upgrade SCT application. (Irradiations already underway will verify this.)
  - May be able to reduce power by 75% from 1500 μW to 360 μW!