

# New Mask and vendor for 3D detectors

R. Bates, G. Pellegrini et al. at  
Glasgow and CNM

Introduction

3D geometry

Mask design

Details of items on the mask

Fabrication at CNM

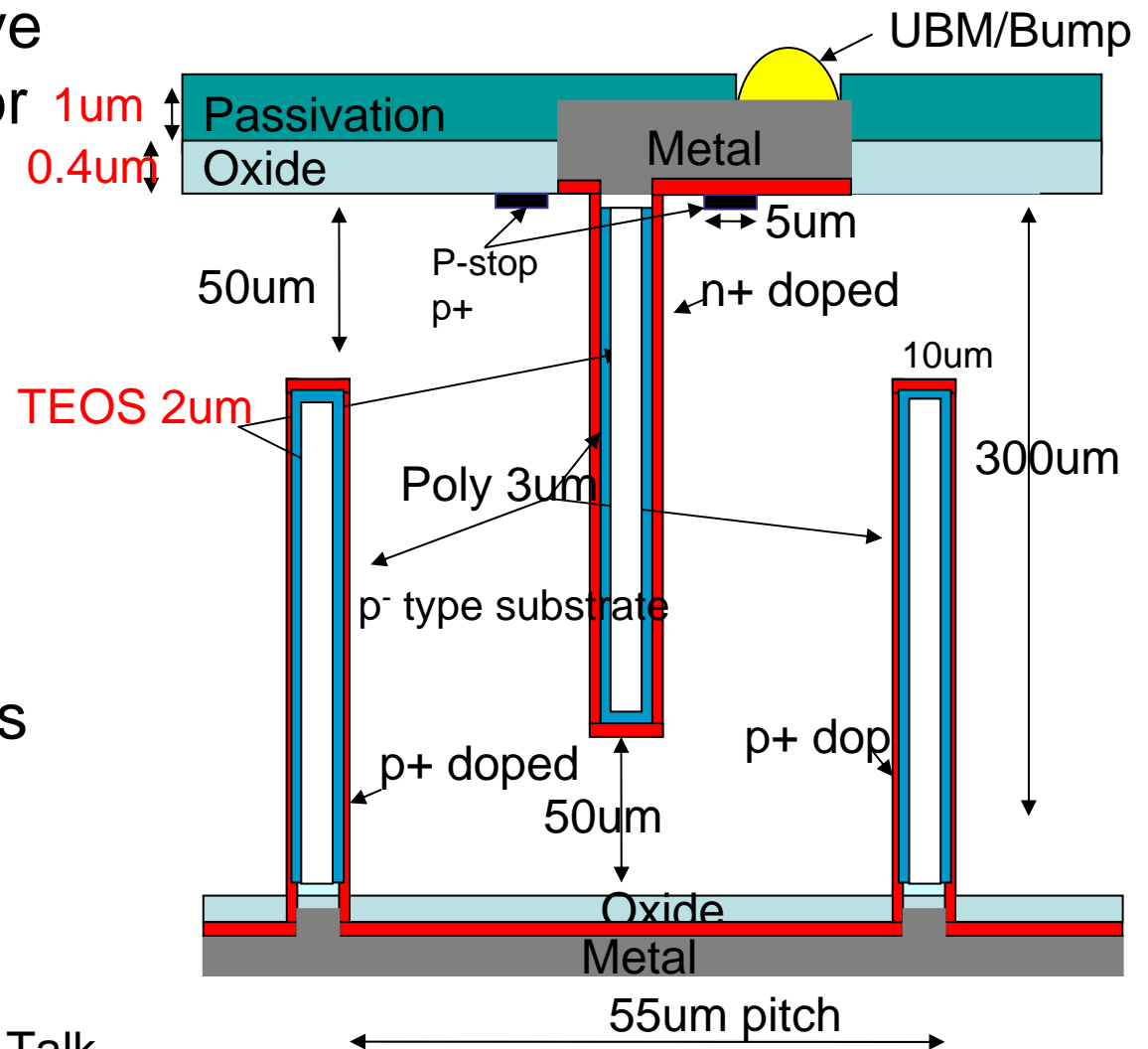
ICEMOS Tech

Bump bonding

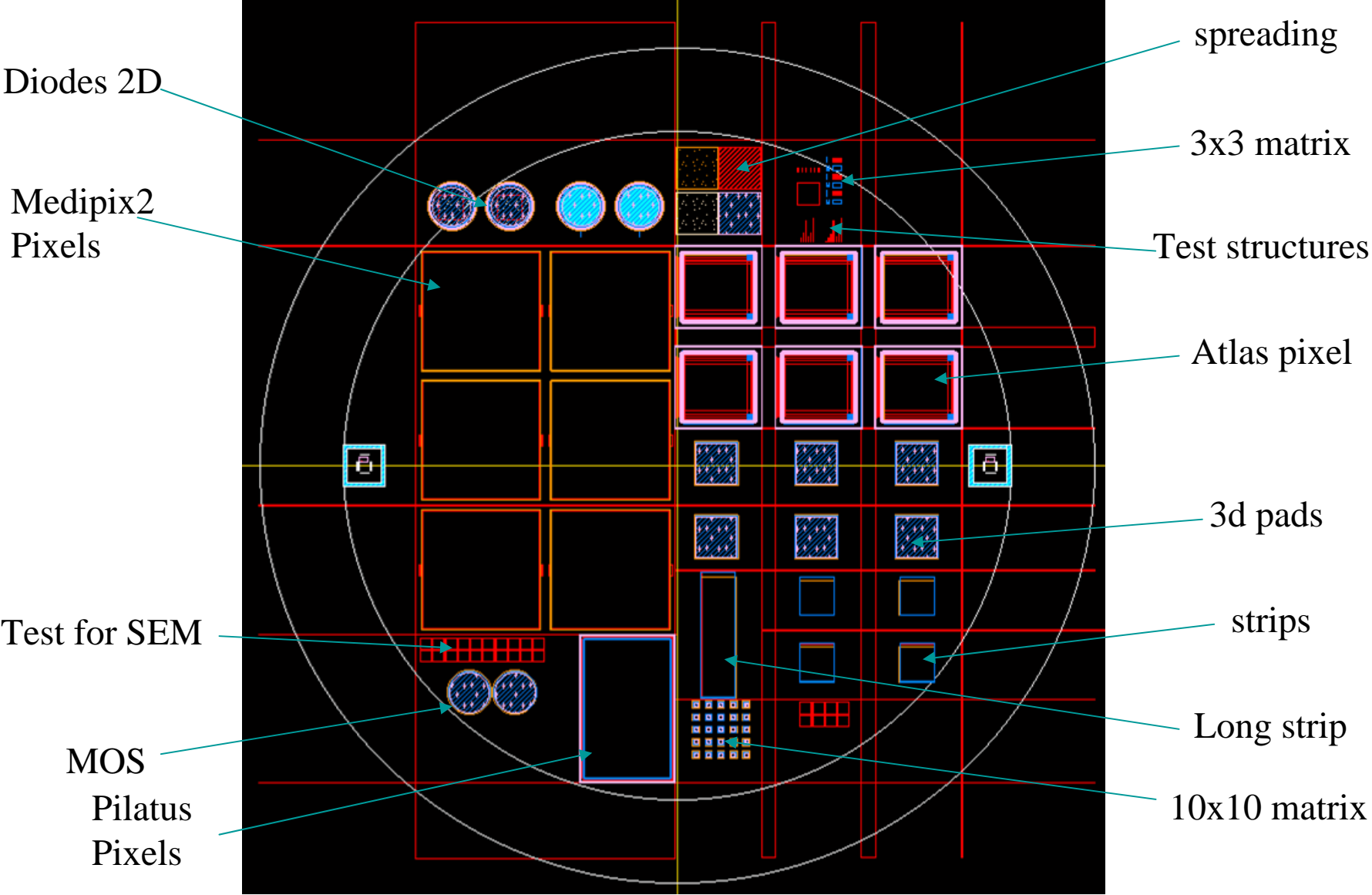
# Introduction

- CNM and Glasgow have designed a mask set for 3D detector fabrication
  - Mask ordered in past weeks
- Funded by RD50 Common fund
  - Request will arrive for 2kCHF from signatures
- Aim to fabricate devices at CNM with n- and p-type wafers

E-field and CCE simulated at Glasgow – Next Talk



# Mask design

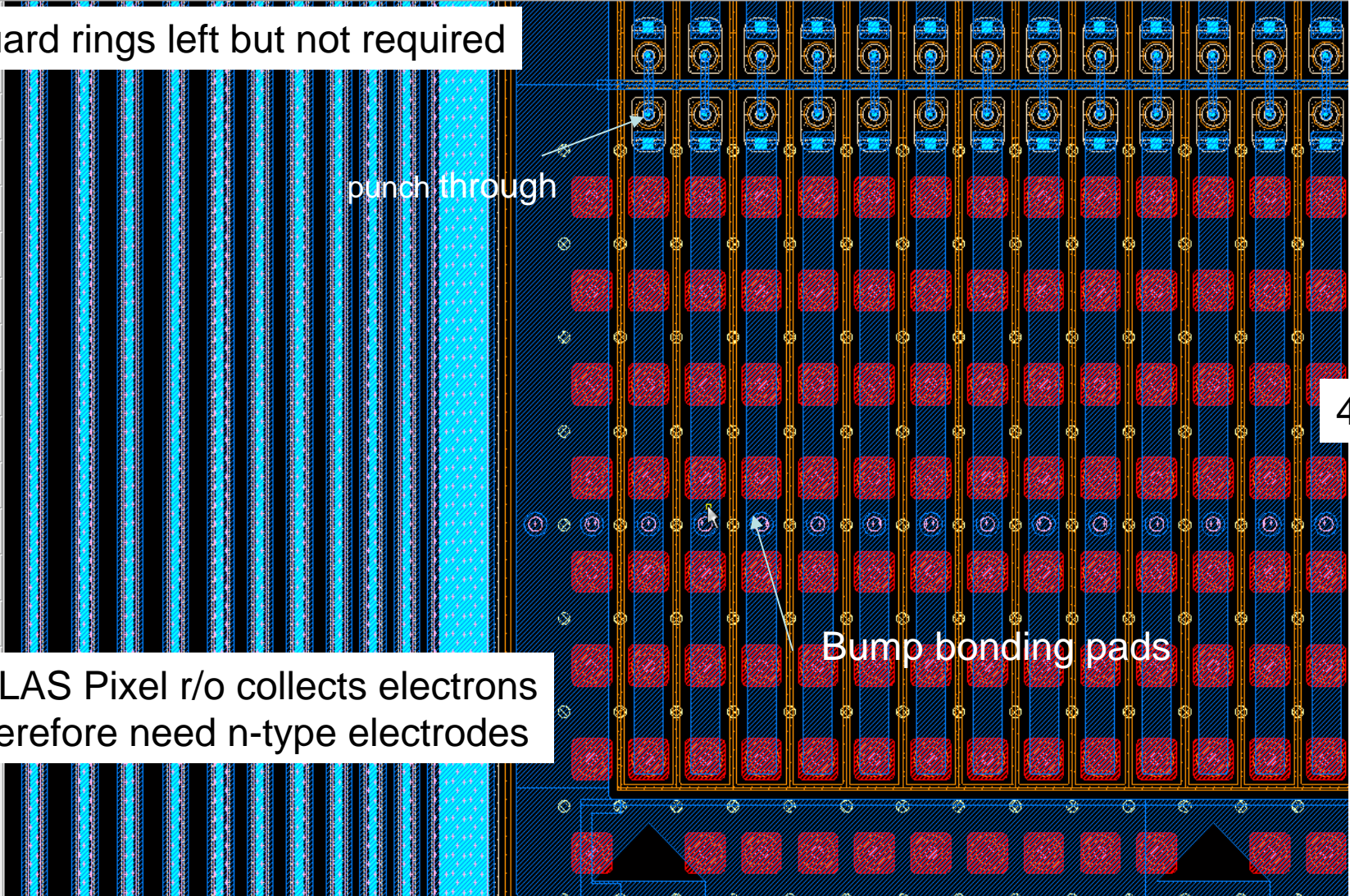


# Device summary

- 6 Medipix2 pixels Pitch 55um, 256x256
- 6 ATLAS pixels Pitch 50x400um, 164x18
- 1 Pilatus pixel Pitch 172um, 97x60
- 4 short strip Pitch 80um, 50x50
- 1 long strip Pitch 80um, 180x50
- 6 pads Pitch 55um, 90x90
- 25 10x10 pads Pitch 55um, 10x10
- 25 3x3 pads Pitch 55um, 3x3
- 2 standard pads, diffusion Diameter: 5000um
- 2 standard pads, poly Diameter: 5000um
- 2 MOS structure Diameter: 5000um
- Different test structure
- Structure for holes alignment

# Atlas pixels

Guard rings left but not required



punch through

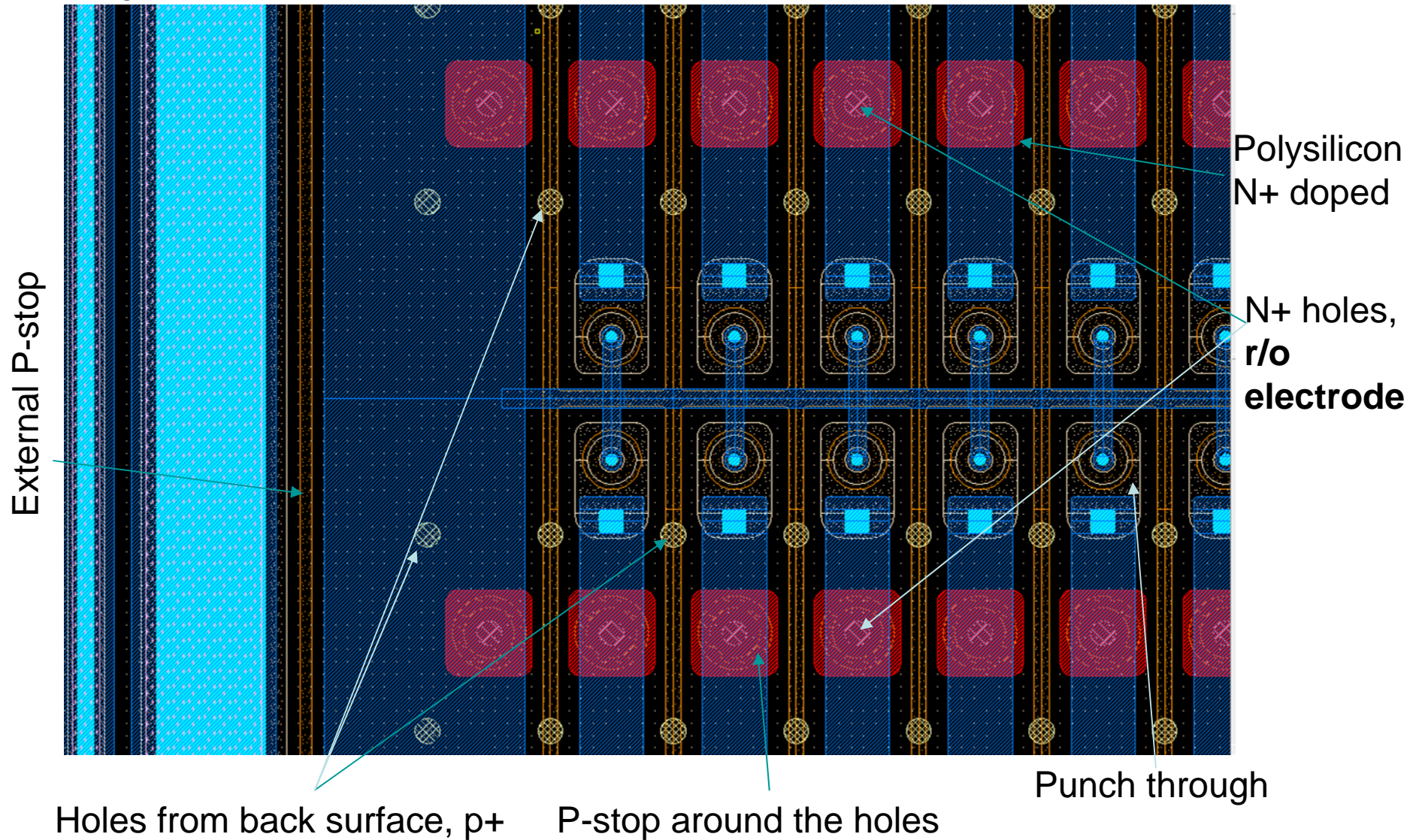
400um

Bump bonding pads

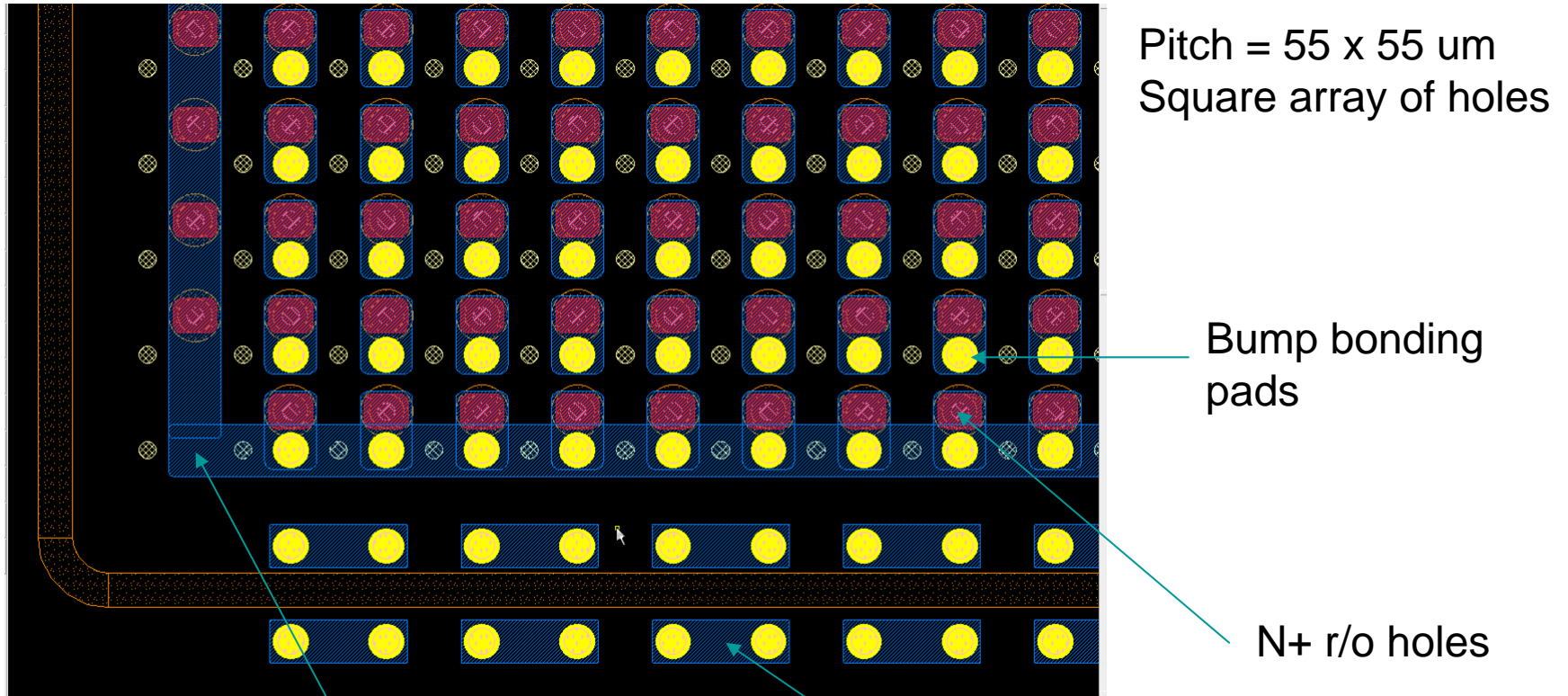
ATLAS Pixel r/o collects electrons  
Therefore need n-type electrodes

# Atlas pixels

Design based on real ATLAS device



# Medipix2 detector



**Medipix2 collects  
electrons and holes**

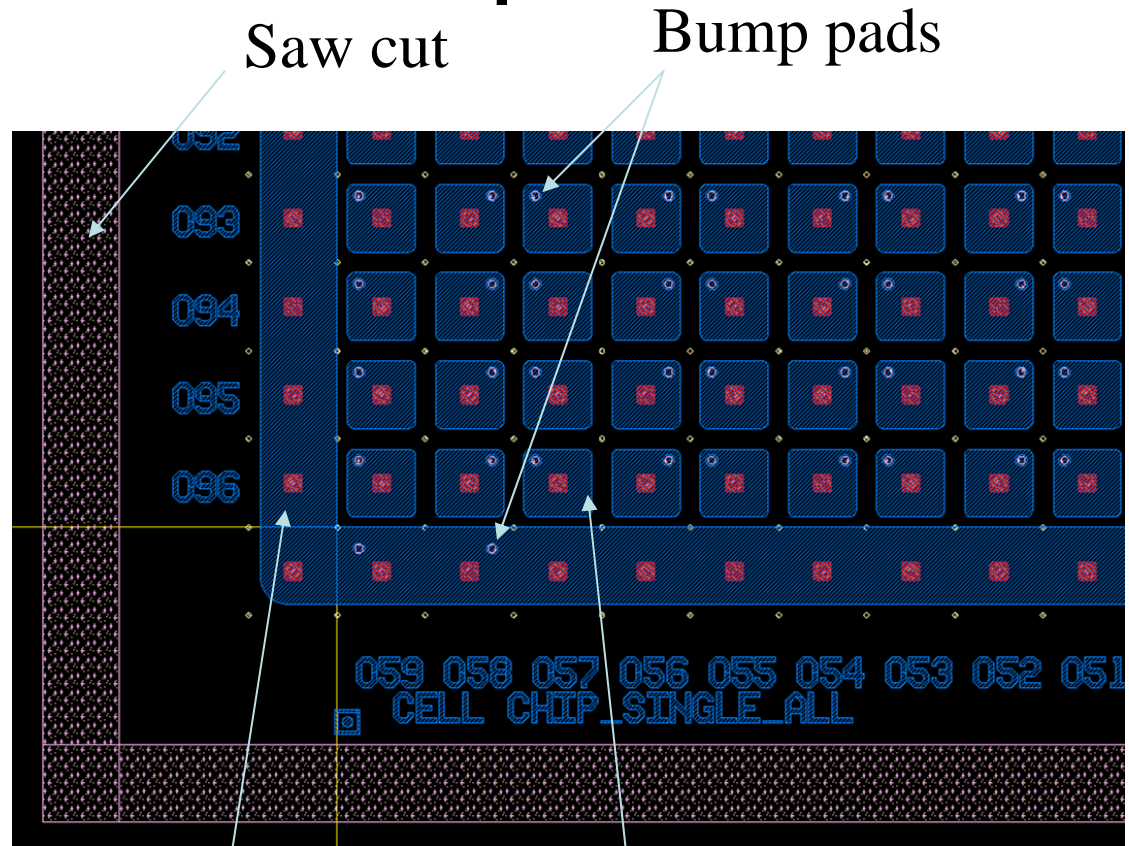
3D Guard ring

Snake - tests bumping

# Pilatus chip

Pitch = 172 x 172 um  
Square array of holes

**Pilatus r/o collects holes**  
**p-on-n type device required**



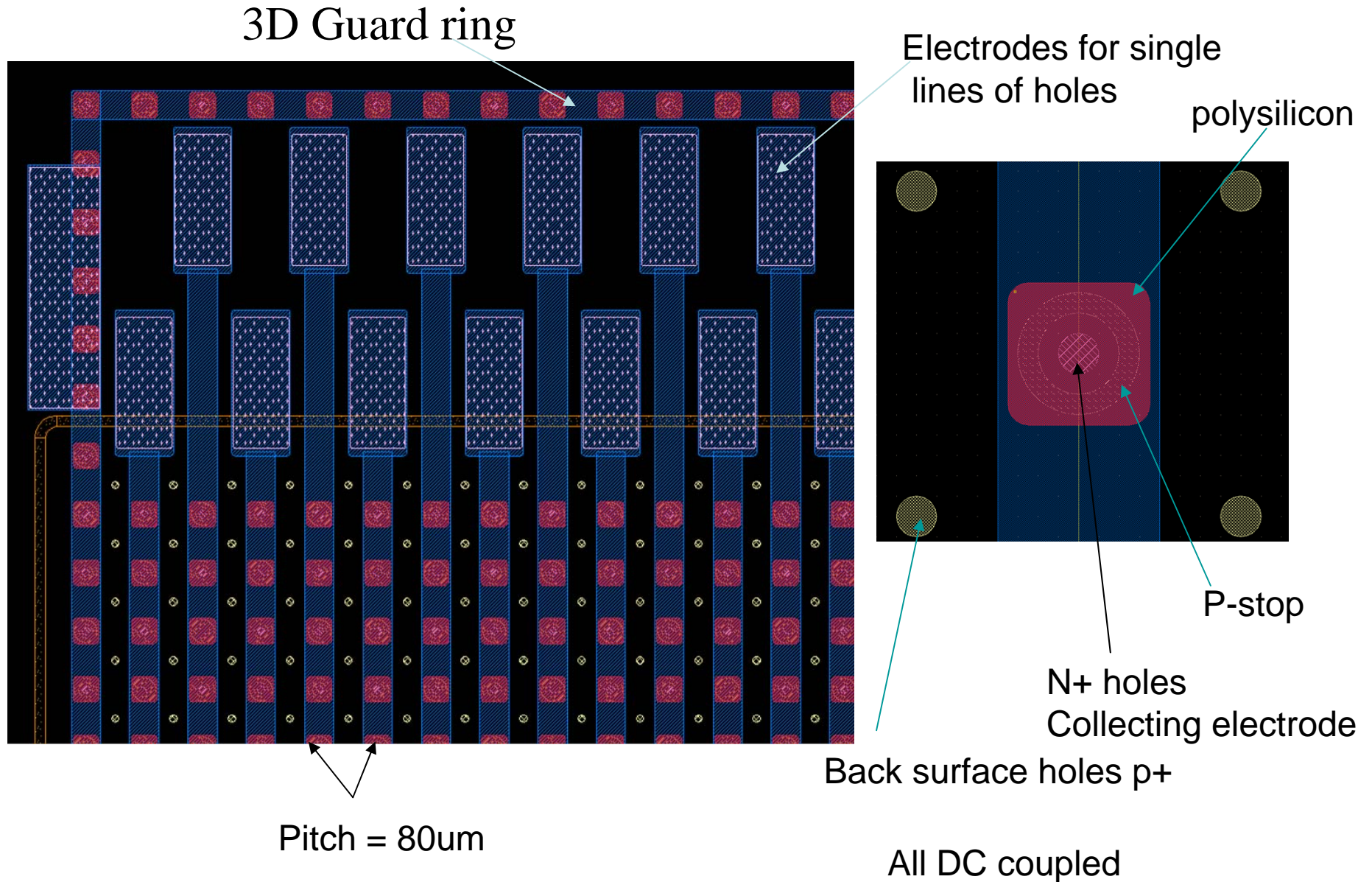
3D Guard ring

pixels

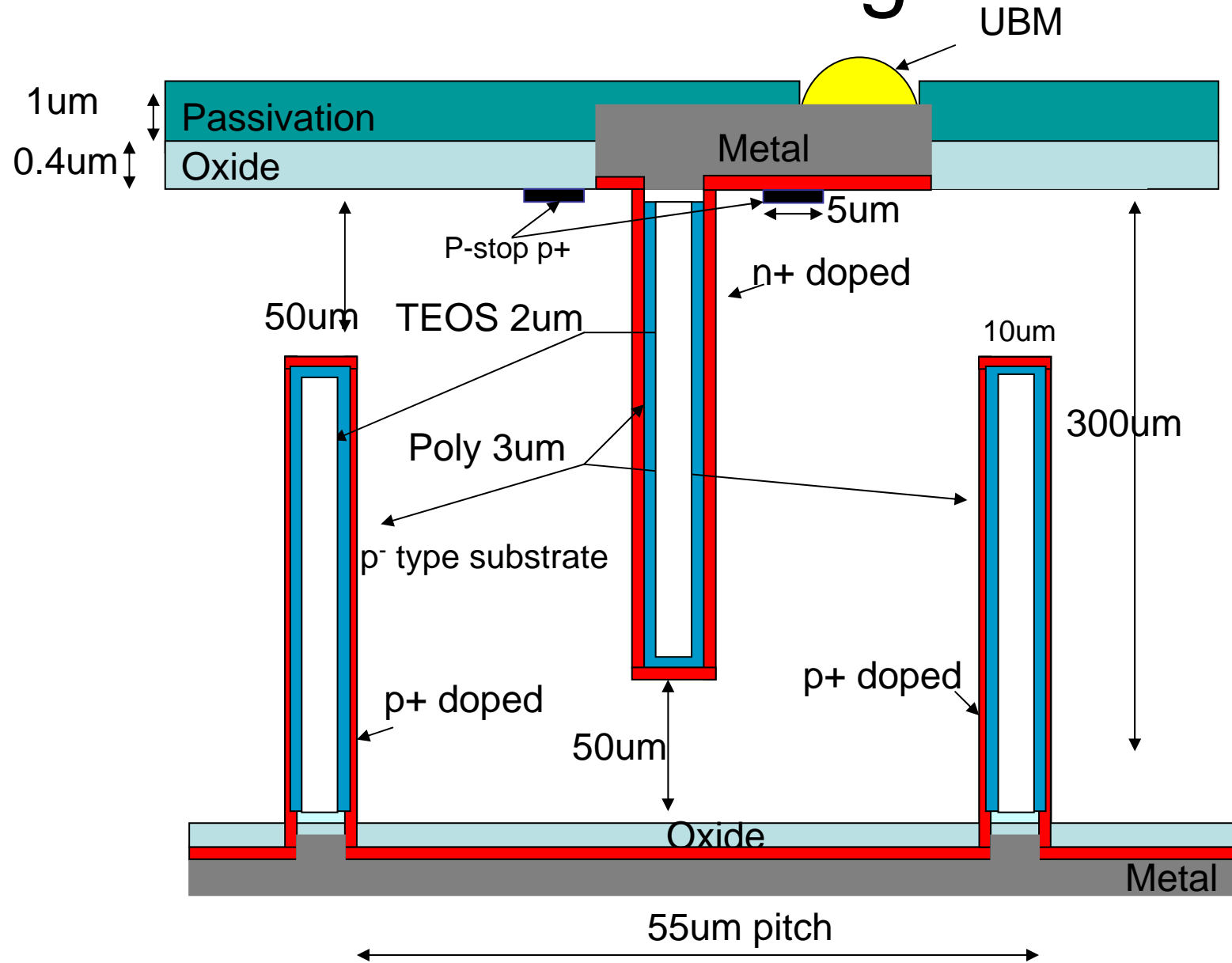
PSI R/O for Synchrotron sources



# Strip detectors



# Processing



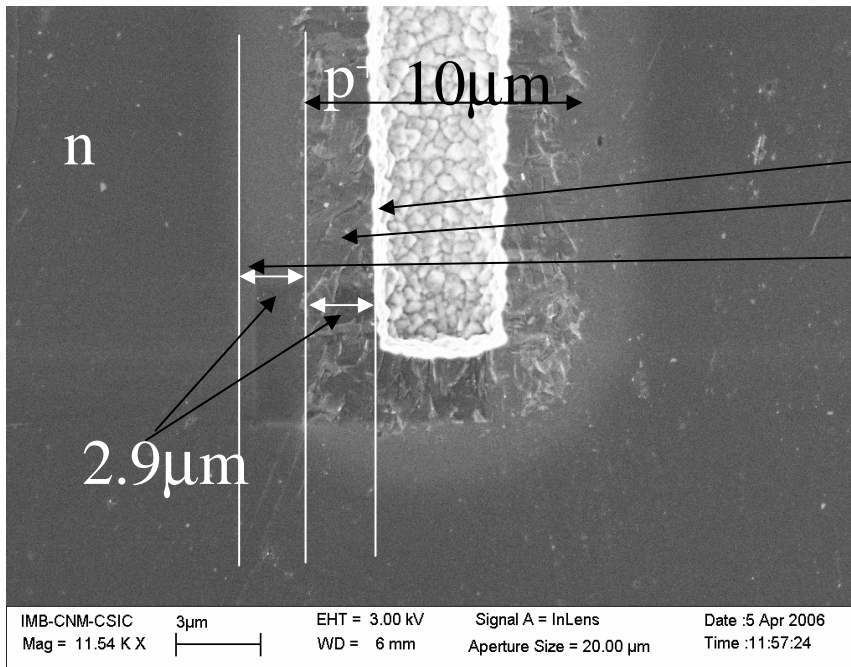
# Process developed and checked

## Process flow:

Etch  $\Rightarrow$  Fill with Poly  $\Rightarrow$  P doping  $\Rightarrow$  TEOS  $\Rightarrow$  Etch  $\Rightarrow$  Poly  $\Rightarrow$  B doping  $\Rightarrow$  TEOS

- Hole etching working well
  - Aspect ratio 24:1
  - Better with Al mask

- Doping down the hole works
  - Smooth profile at corners, not square
  - [B] same at top and bottom
- Study of P & B doping performed to obtain junction in crystal Si down hole
- Poly uniform down the hole
- TEOS enters the hole



# Processing plan

- 1<sup>st</sup> : p readout columns in an n-type bulk
- 2<sup>nd</sup> : n readout columns in a p-type bulk
- 9 wafers:
  - 1 wafer single sided for planar devices
  - 4 wafers with no bumps
  - 2 wafers for Medipix2 Sn/Ag bumps with Ni UBM left on strip pads
  - 2 with UBM for Indium – Pilatus and ATLAS
    - Ratios may change due to bumping developments

# IceMOS Technology Ltd

- Small N.I. Based silicon MEMS company
- Have all required equipment and skills for 3D
- 3 stage development plan negotiated
  - Dense high aspect ratio hole array development
  - Hole doping optimisation
  - Device fabrication
- We will supply new sets of masks
- Time scale to full devices order 6 months!

# Bump bonding

- Critical aspect for pixel devices
  - More effort required in this area with in RD50
- ATLAS r/o pixels in Glasgow with Indium bumps
- Pilatus Indium bumped at PSI
  - Diamond/RAL are building up a resource to work with PSI on bonding
- Medipix2 Solder bumps at CNM
- Freiburg to work on bumping 3D devices
- CNM produced Bump test device to check yield

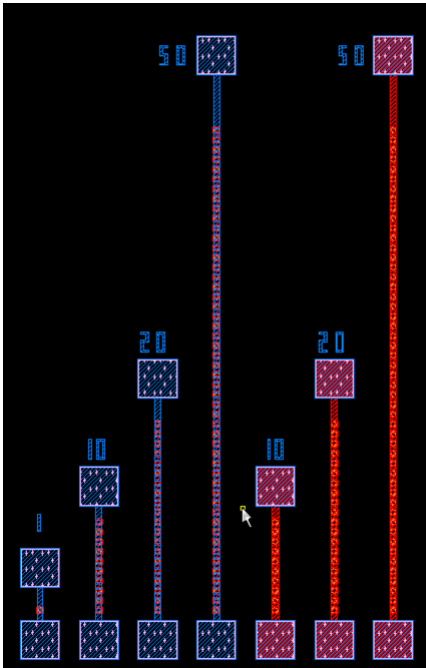
# Summary

- Multi-project pixel 3D Mask designed
- Fabrication process understood
- 1<sup>st</sup>: p-in-n 3D detectors + single sided
- 2<sup>nd</sup>: n-in-p detectors
- End of 1st process foreseen for the end of October
  - if we get the mask before summer.
  - CNM clean room closed in August.
- Bump bonding unsolved issue
- Commercial 3D vendor being pursued

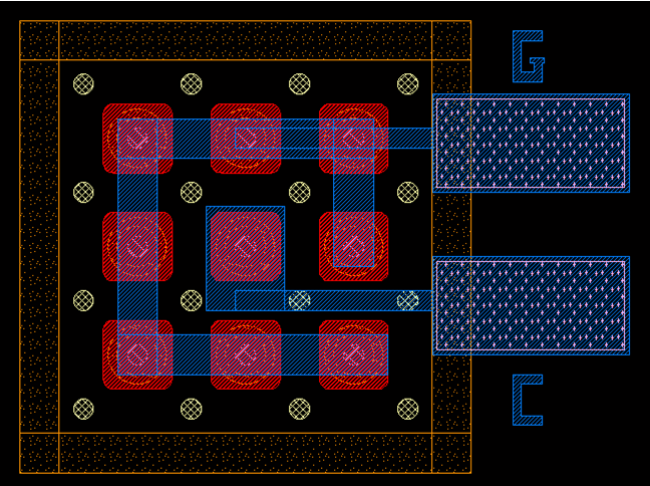
# Extra Slides



# Test structures

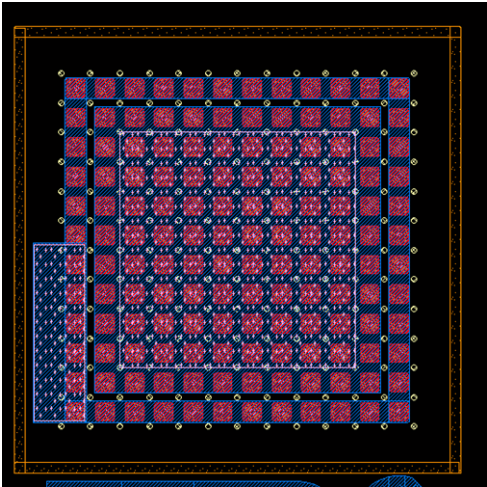


Test structure to measure the connection between the holes.

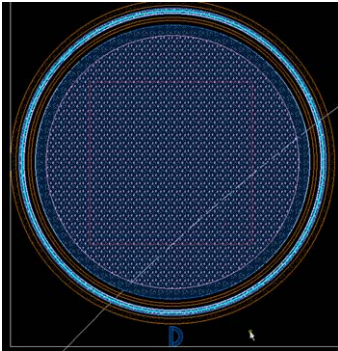


3x3 matrix

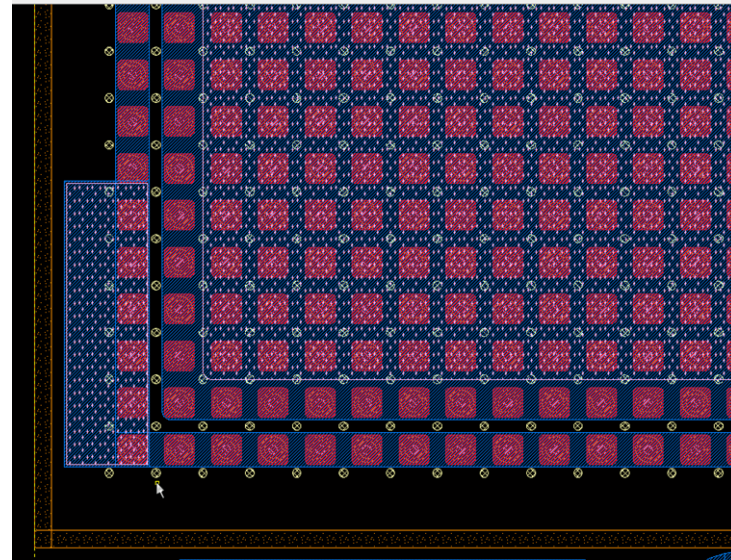
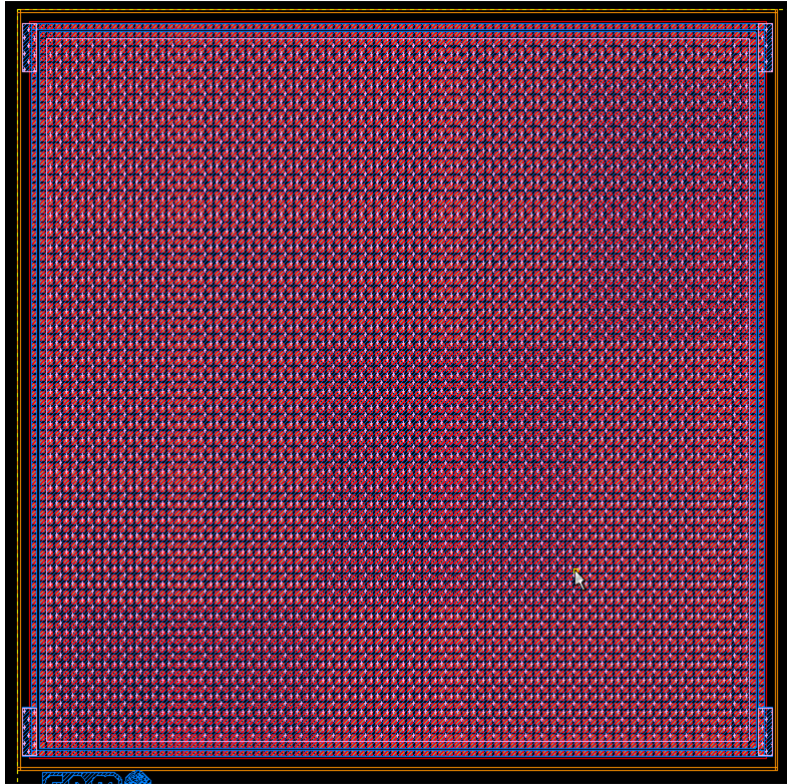
Standard Diode



10x10 matrix

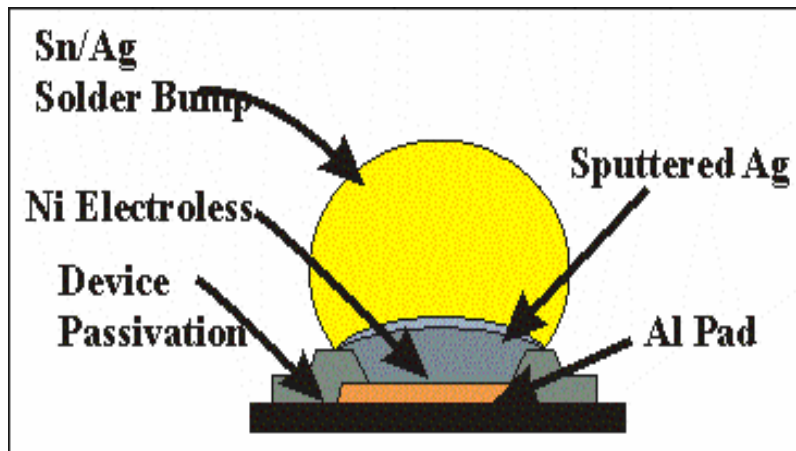
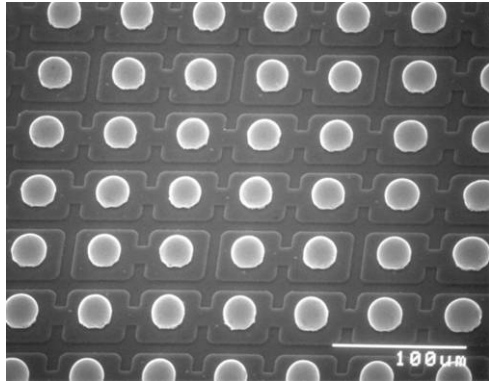


# 3D pad detectors



All holes connected by the metal layer

# Bump bonding



- Minimum pitch: 40μm
- Lead free technique
- Low cost process
- Fabrication steps:
  - 1. Under Bump Metalisation (UBM)
  - 2. Bump formation by electroplating
  - 3. Reflow

