Characterization of irradiated MOS-C with X-rays using CV-measurements and gated diode techniques

Q. Wei, L. Andricek, H-G. Moser, R. H. Richter,

Max-Planck-Institute for Physics Semiconductor Laboratory

Outline

- Motivation
- Experimental conditions
- Study of the radiation damage by CV-measurements and gated diode technique, annealing behavior at RT, comparison of extracted N_{ox}, N_{it} values
- Discussion of the results

Motivation

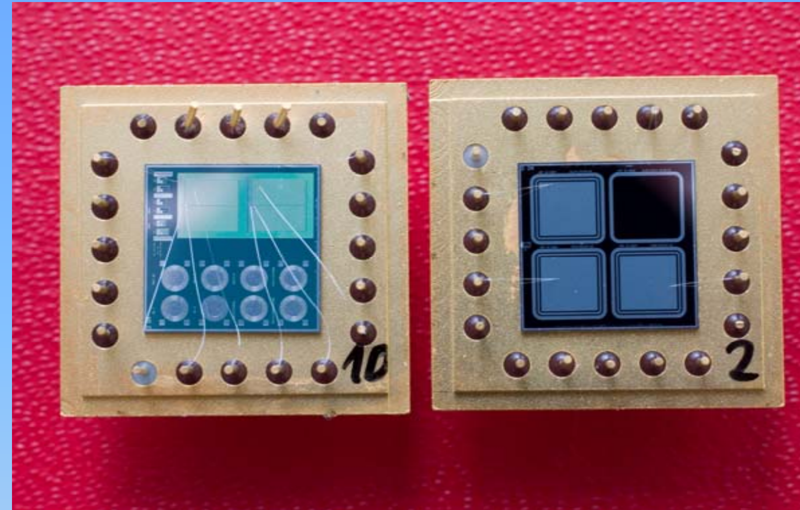
- Radiation damage of semiconductor devices (e.g. DEPFET)
- Study on the radiation damage with MOS-C using CaliFa teststand at MPI HLL Munich
- Comparison of results from two different measurement methods (MOS-C and gated diode)

Comparison between different semiconductor devices

(Only for the 1-D defects)

	MOS-C	Gated diode	DEPFET
N_{ox} (method)	ΔV_{FB} (CV-Measurement)	ΔV_{FB} & ΔV_g (CV-Measurement & gated diode technique)	ΔV_t (IV-Measurement)
N_{it} (method)	Stretchout (High-low frequency based on the CV)	Full width at 2/3 maximal of current (gated diode technique)	Subthreshold slope (Subthreshold technique)
Other parameters		S_0, $\sigma_{n/p}$ & τ_0 (gated diode technique)	g_m (IV-Measurement)

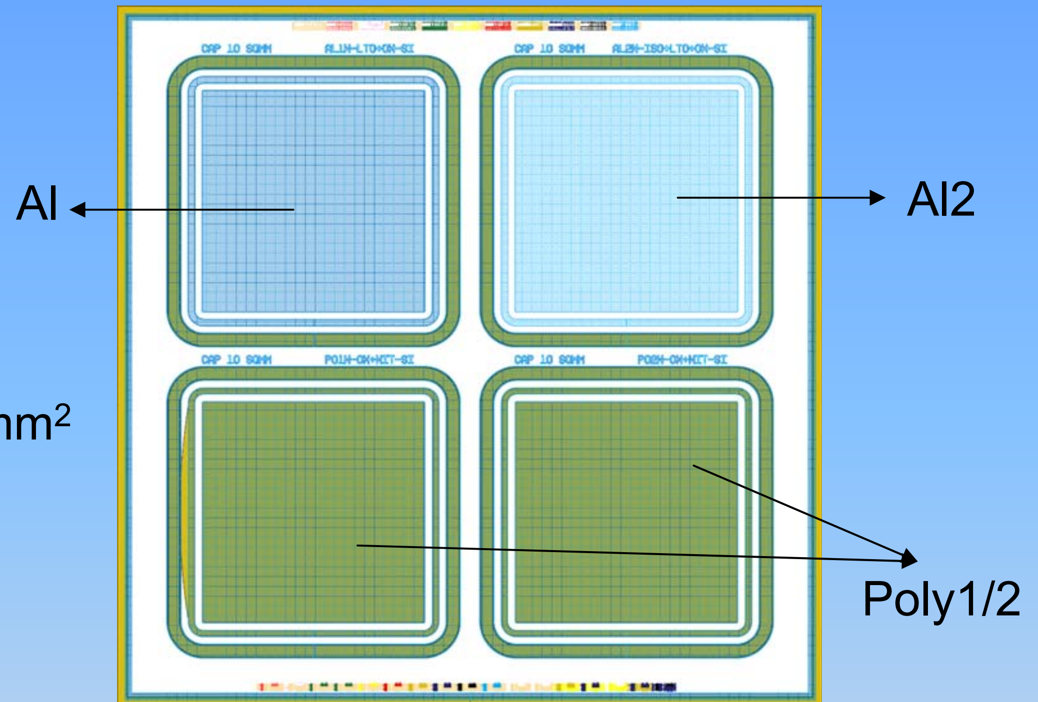
Experimental Conditions

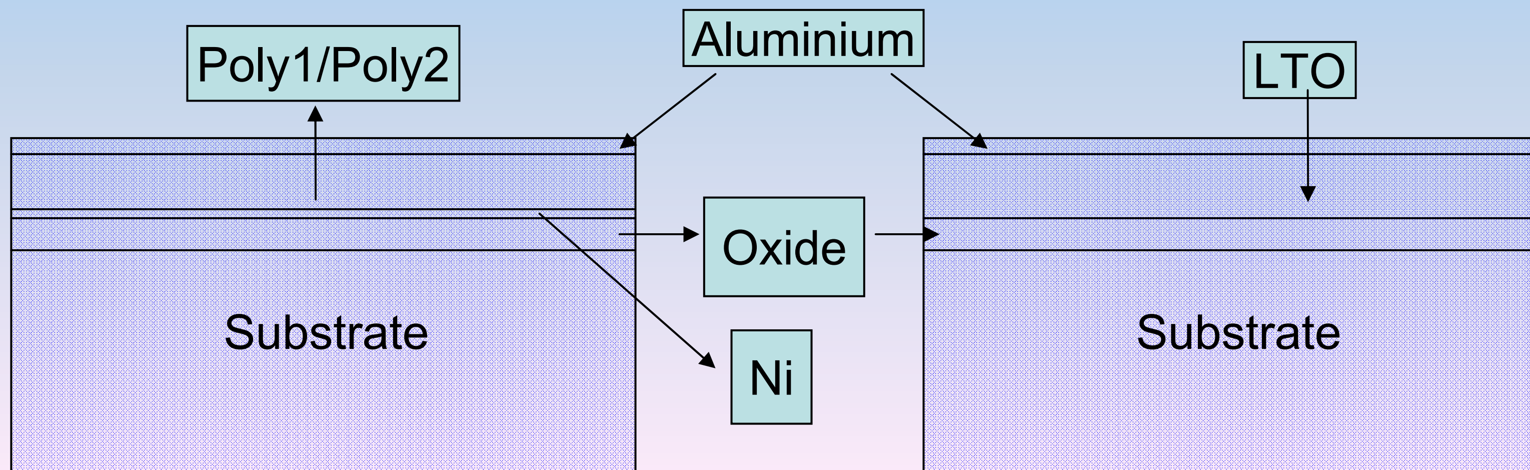


- Irradiation: X-Ray tube with Mo target at 30kV and 30mA (17,44keV & Bremsstrahlung)
  dose: 1 week of irradiation up to 1M rad, dose rate: 2.5rad/s (1rad=0.01J/kg)
- Samples:
  - Based on n-type high resistance silicon(450μm) wafer: doping concentraion ~ 10^{12} cm^{-3}
- Bias conditions: +5V,0V,-5V for MOS-C; 0V for gated diode
- Measurements:
  - CV: HF (10kHz); LF (20Hz)
    all values in series mode (C_s, R_s)
  - Gated diode: V_{Al}: 10V, V_{edge}: 0.25V, $V_{Al/Poly}$: from positive to negative values
  - Annealing: at RT for about 5 days on MOS-C and 10 days on Gated Diode

Cross section and layout of MOS-C

- MOS-C:
  - the upper left – Al1
  - the upper right – Al2
  - the lower left –Poly1
  - the lower right –Poly2
  - each contact area is about 10 mm^2



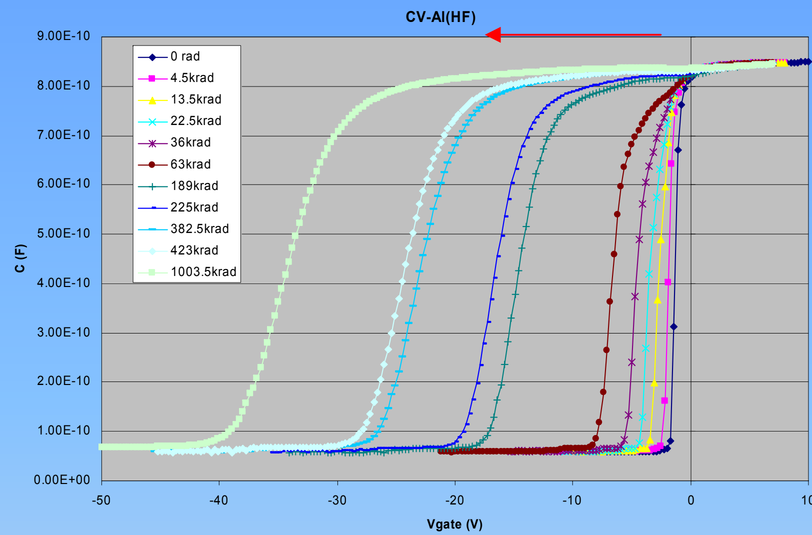


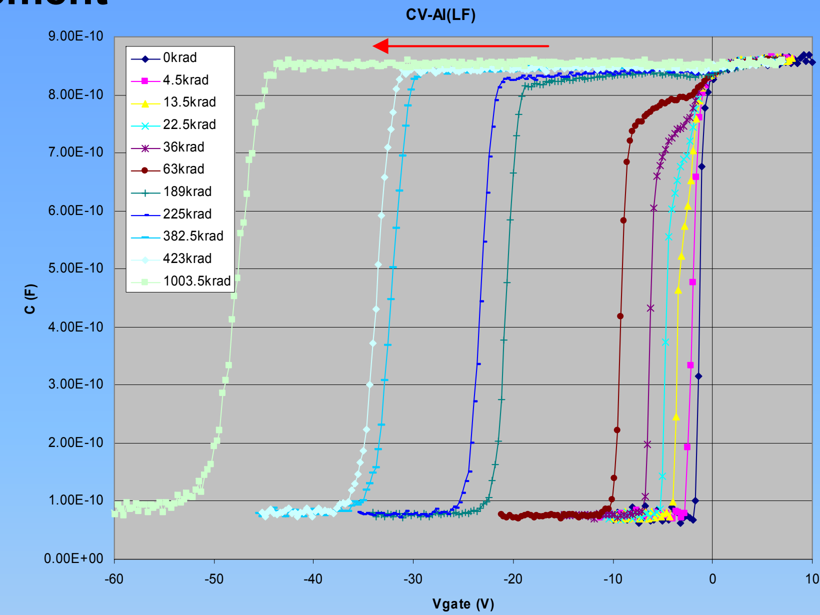
extracted results for MOS-C & Gated Diode

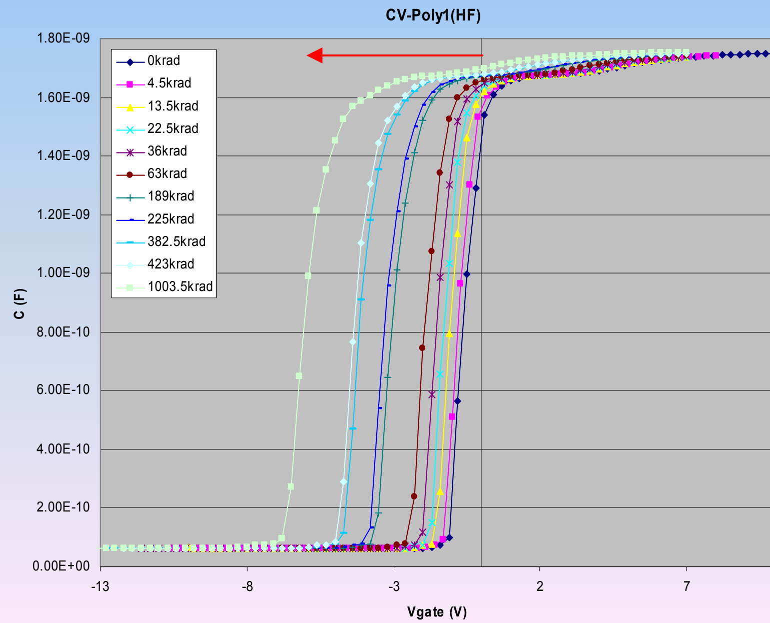
For MOS-C

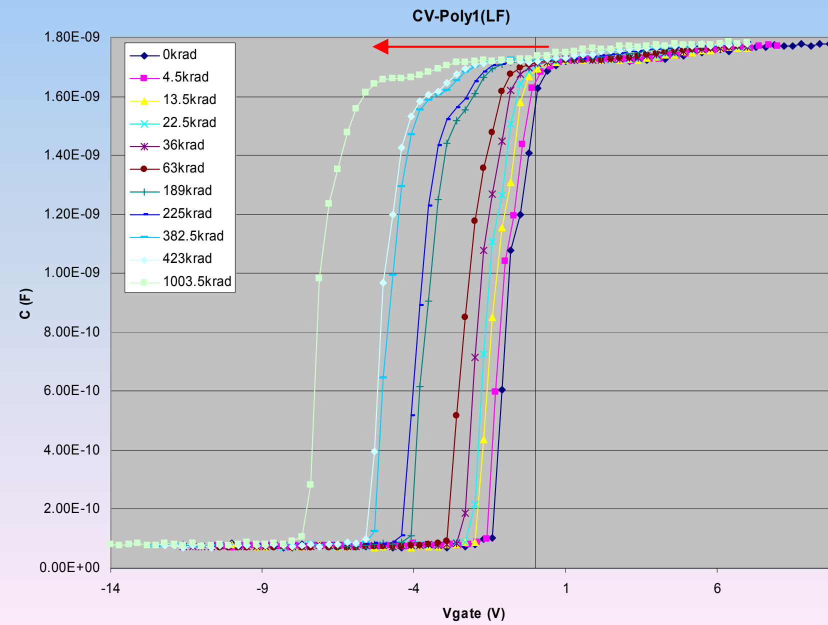
CV-Measurement

Gate Bias conditions: 0V





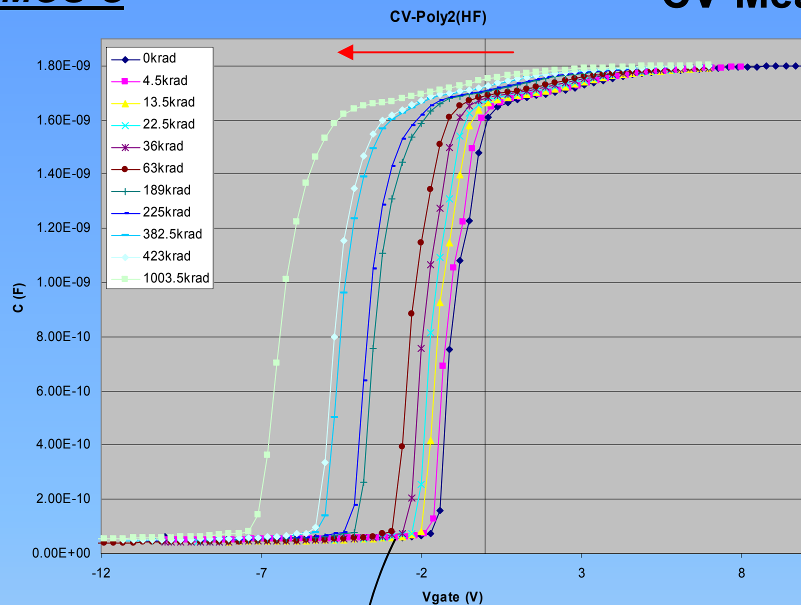


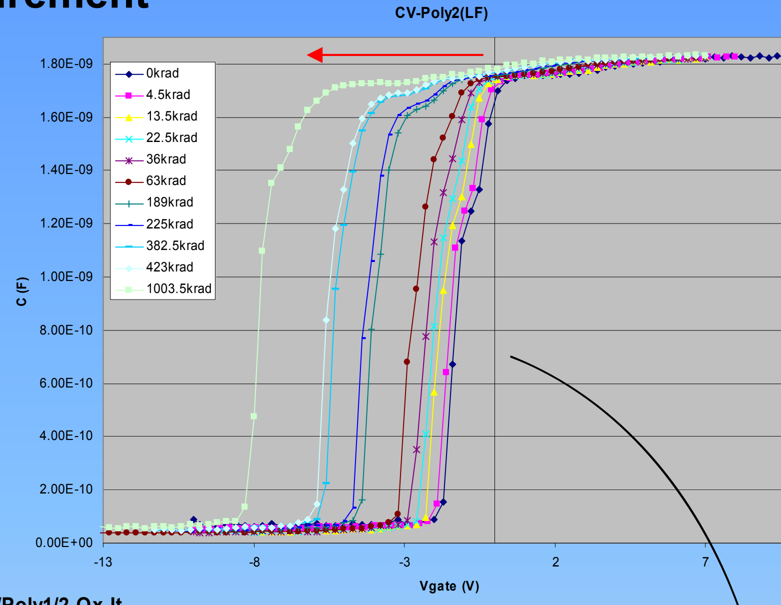


For MOS-C

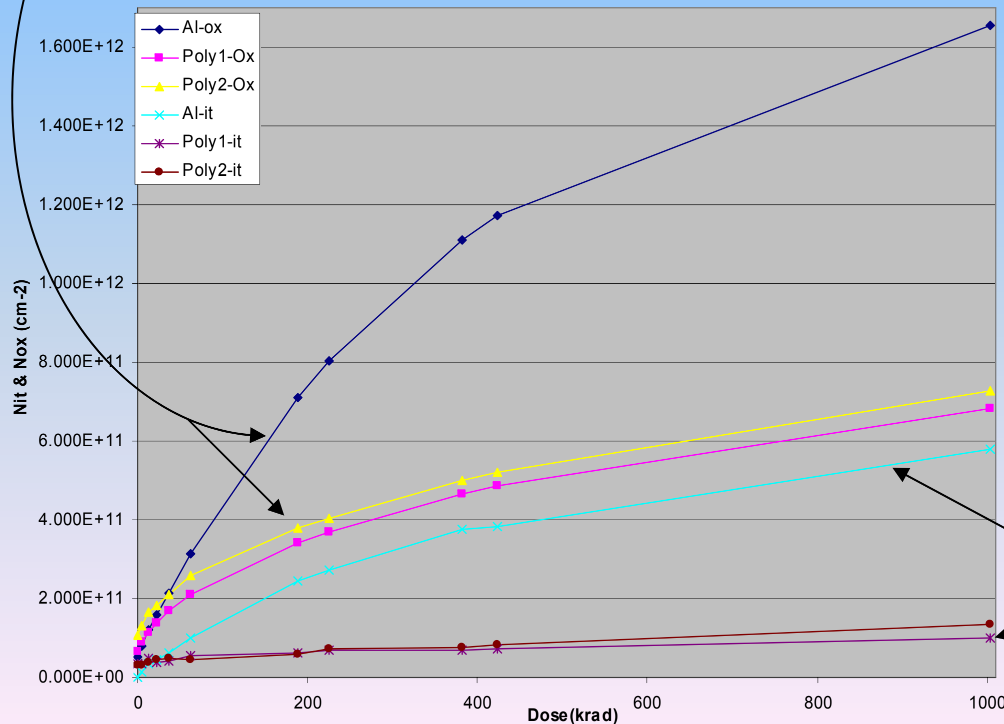
CV-Measurement

Gate Bias conditions: 0V





Flat band voltage Shift → N_{ox}

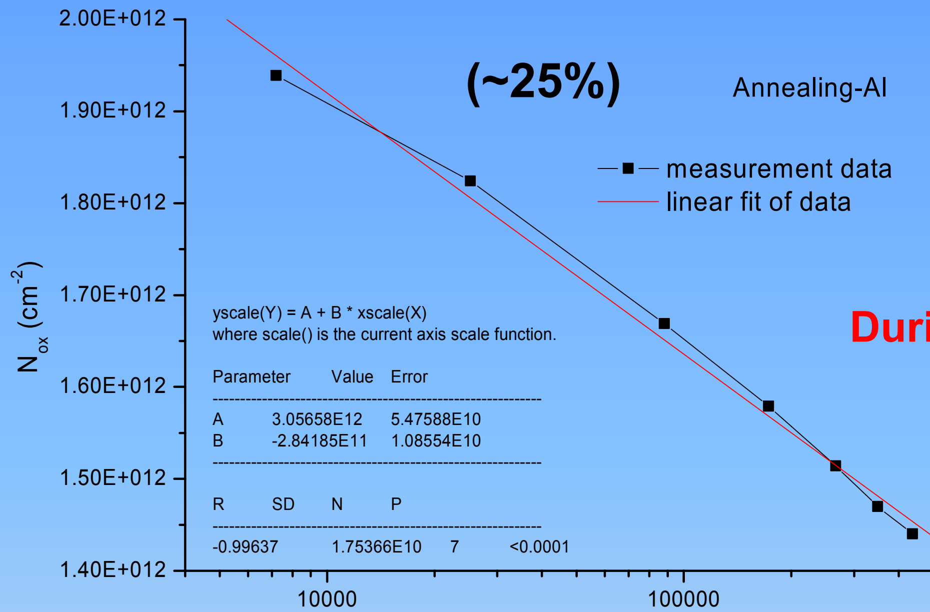


high-low frequency CV → N_{it}

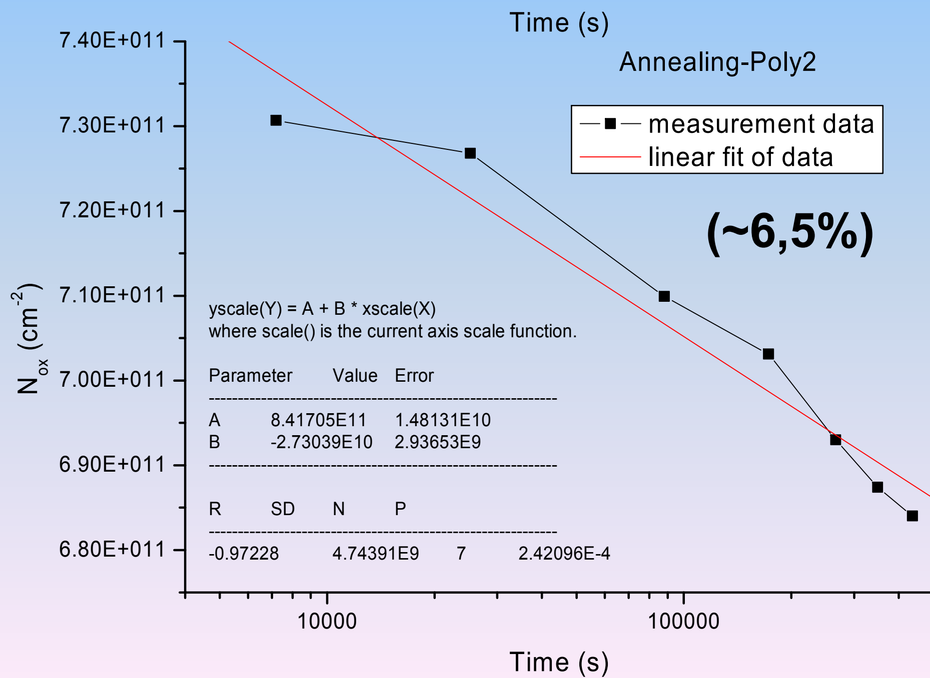
Annealing for MOS-C

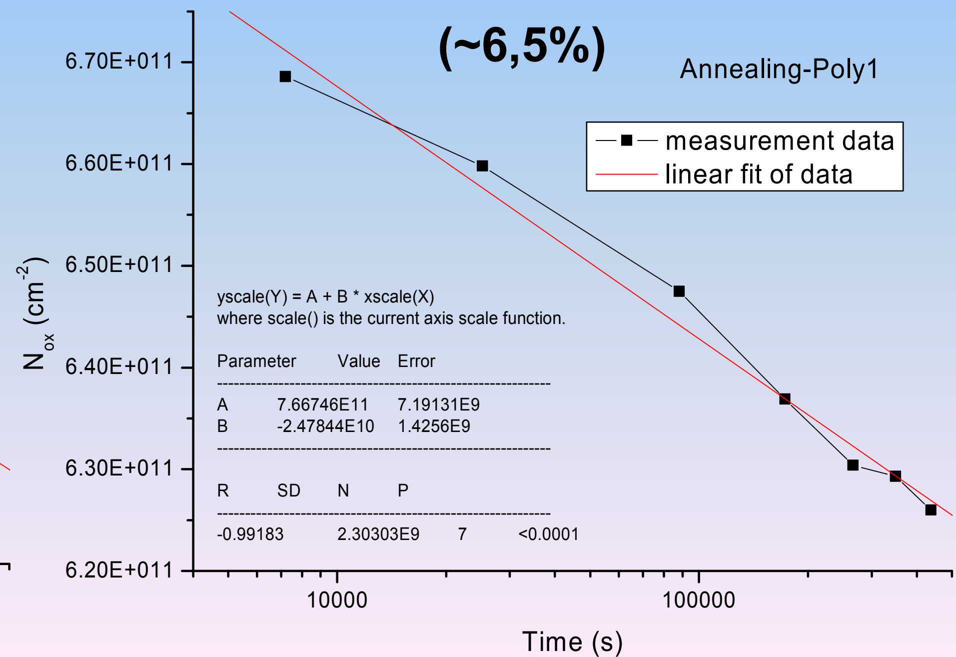
Weak annealing

Gate bias conditions: 0V



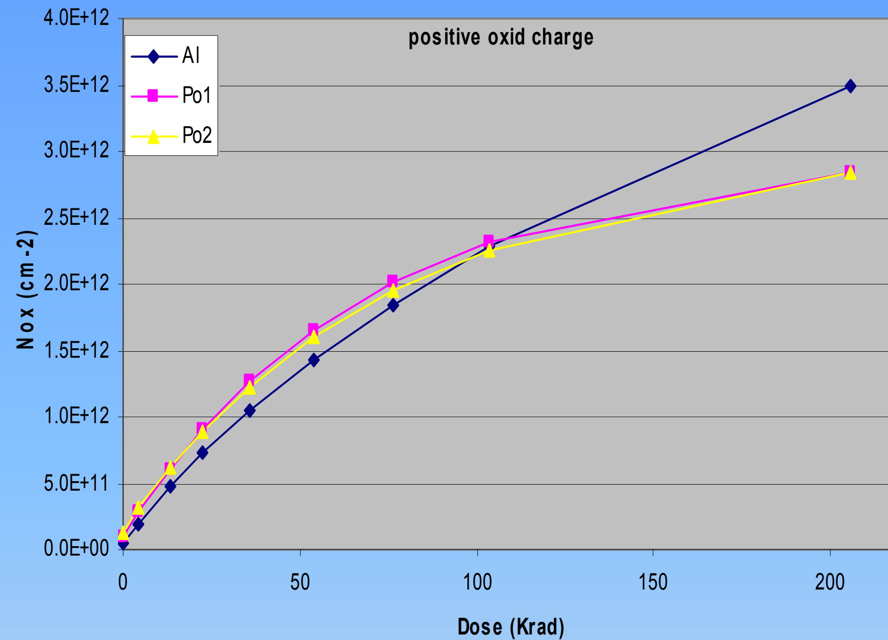
During annealing N_{ox} decreases linearly with ln(t)





For MOS-C

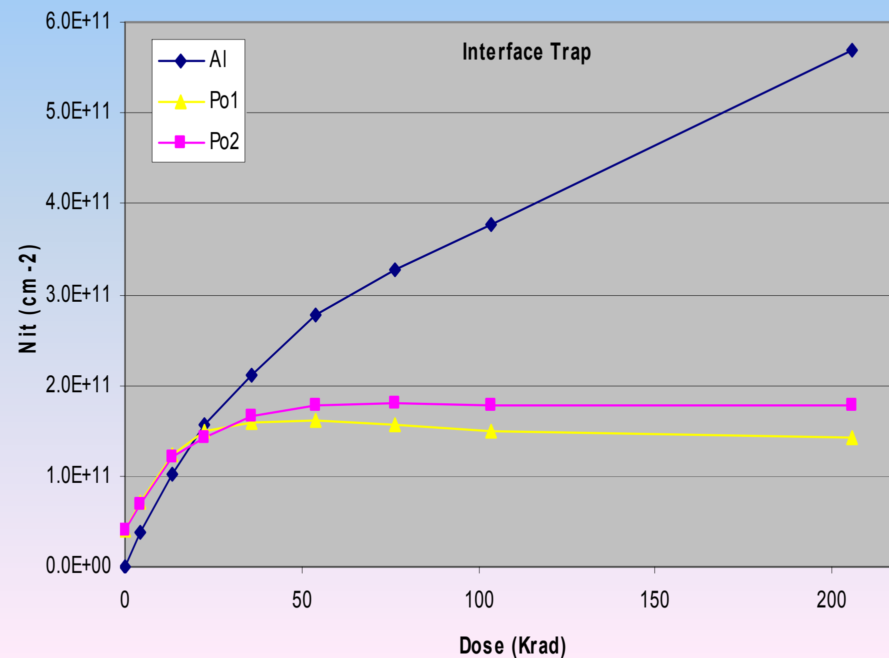
Gate bias conditions: +5V



Due to too large leakage current

at dose 200krad

CV-Measurement does not work



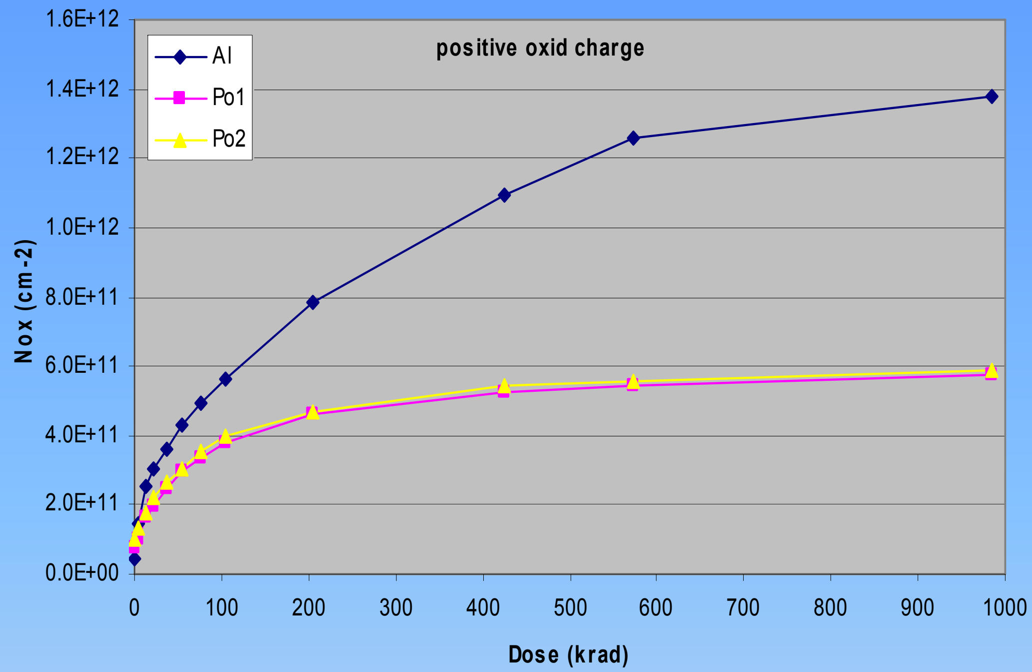
literatur:

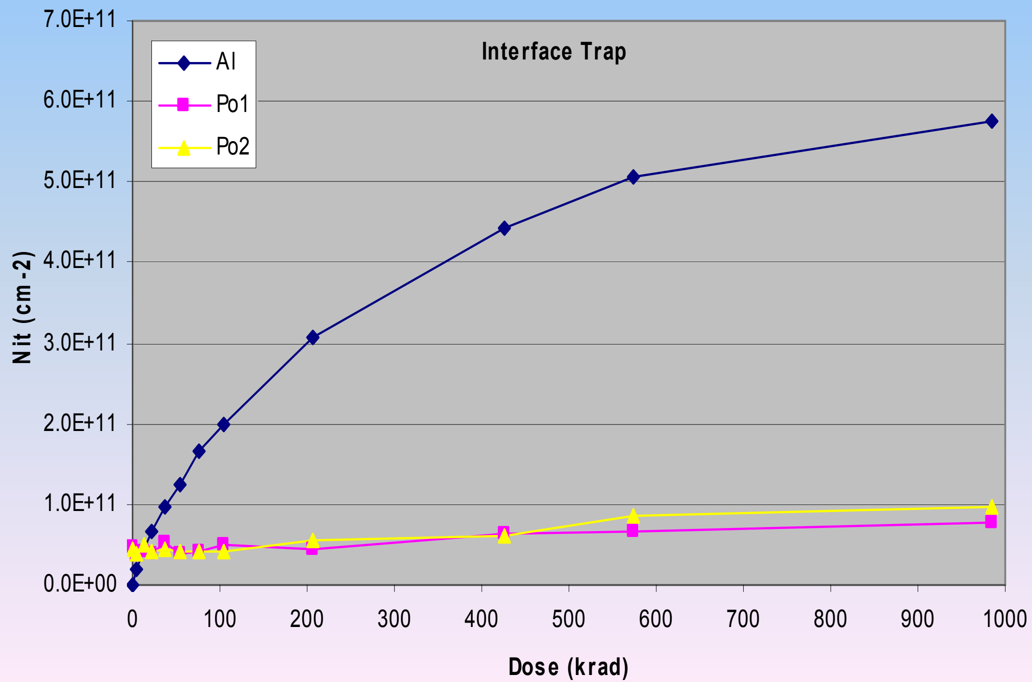
Interface trap will not saturate

at dose of 1Mrad!

For MOS-C

Gate bias conditions: -5V





For MOS-C

V_G at +5V Vs. V_G at 0V

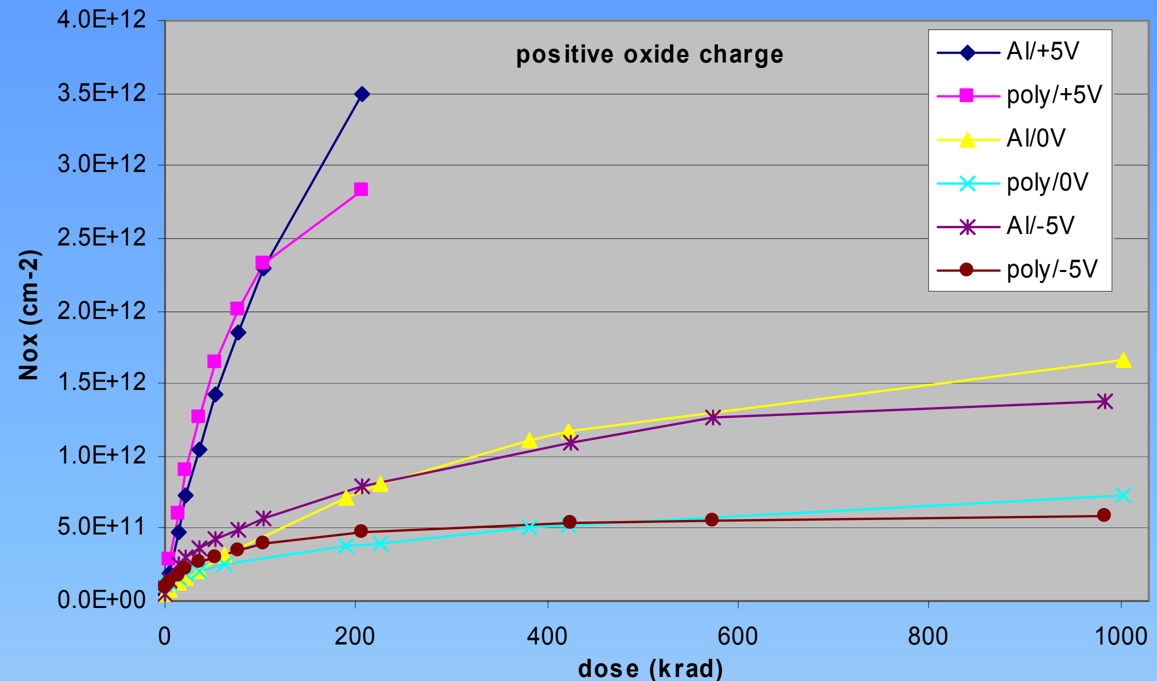
Much more defects (N_{ox},N_{it}) for positive gate than for 0V bias both poly-gate and Al-gate structure

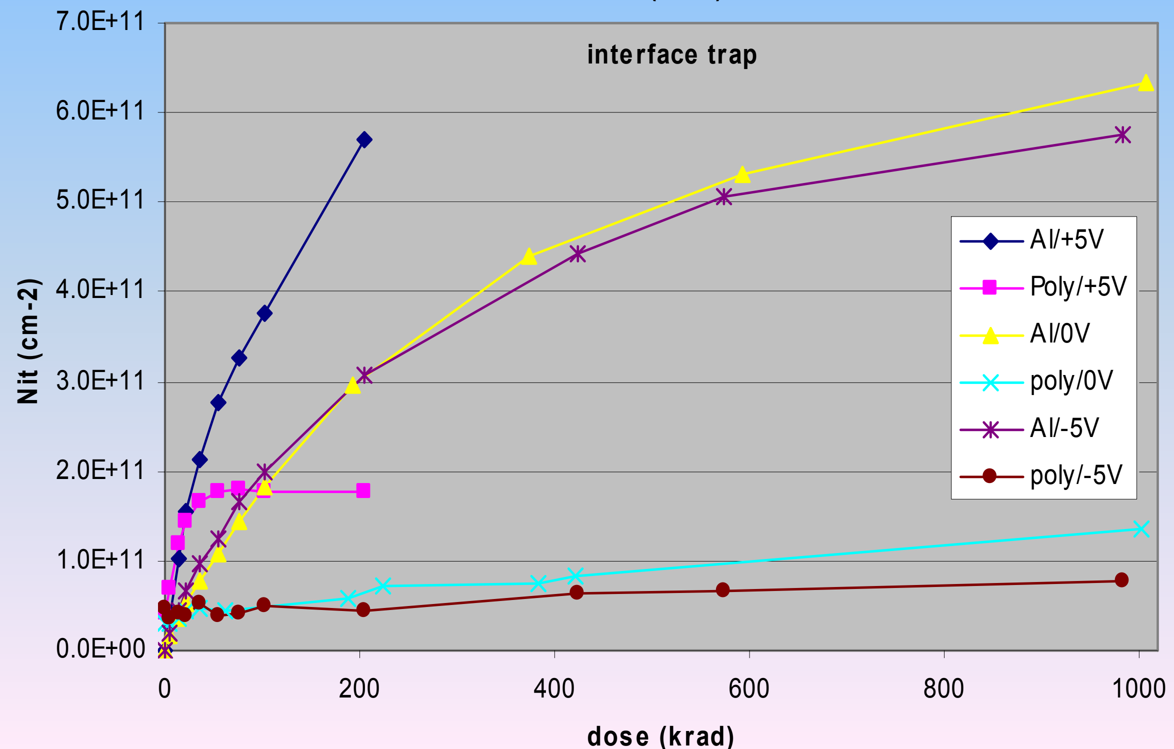
V_G at -5V Vs. V_G at 0V

Almost the same amount of defects (N_{ox},N_{it}) for negative gate bias as for 0V both poly-gate and Al-gate structure

For any given V_G

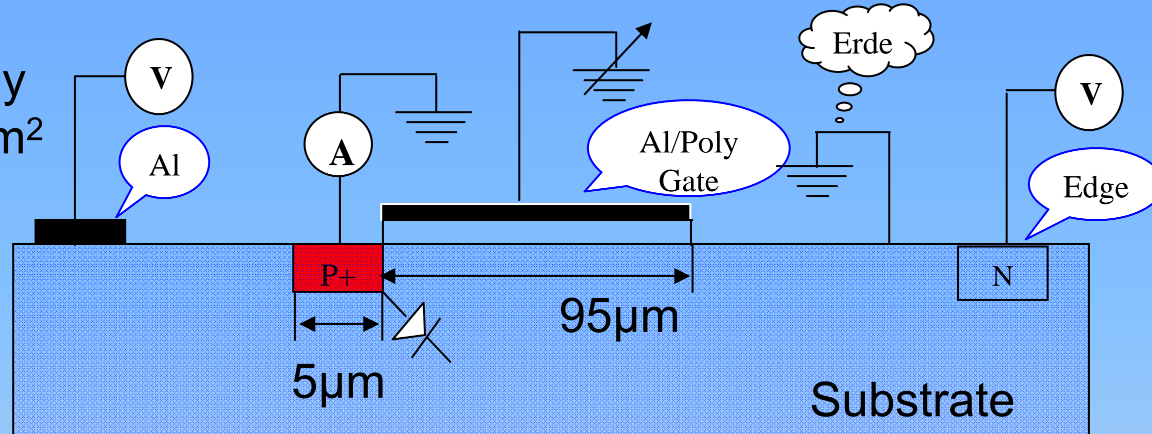
More defects for Al-gate than poly-gate

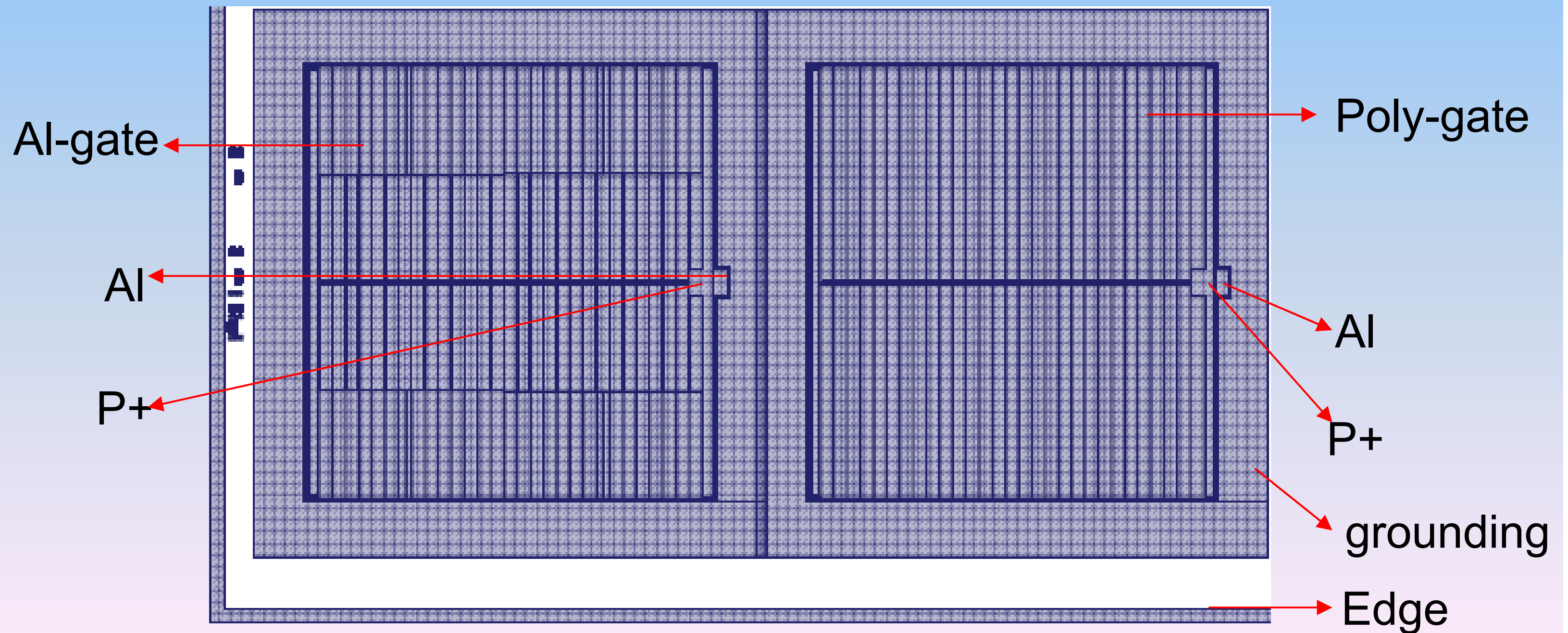




Cross section structure and layout for gated diode

- gated diode wafer
  - the left one – Al
  - the right one –poly
  - each area is 9 mm^2

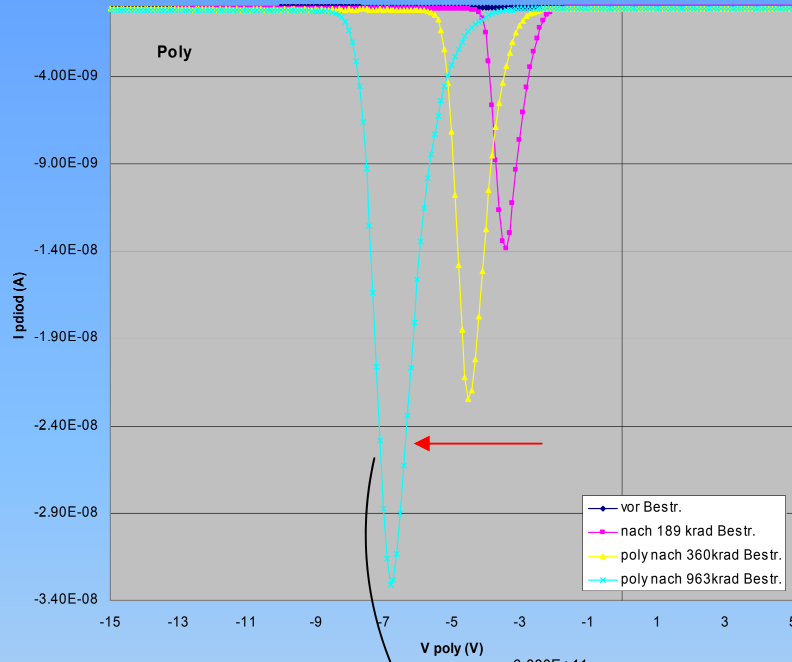


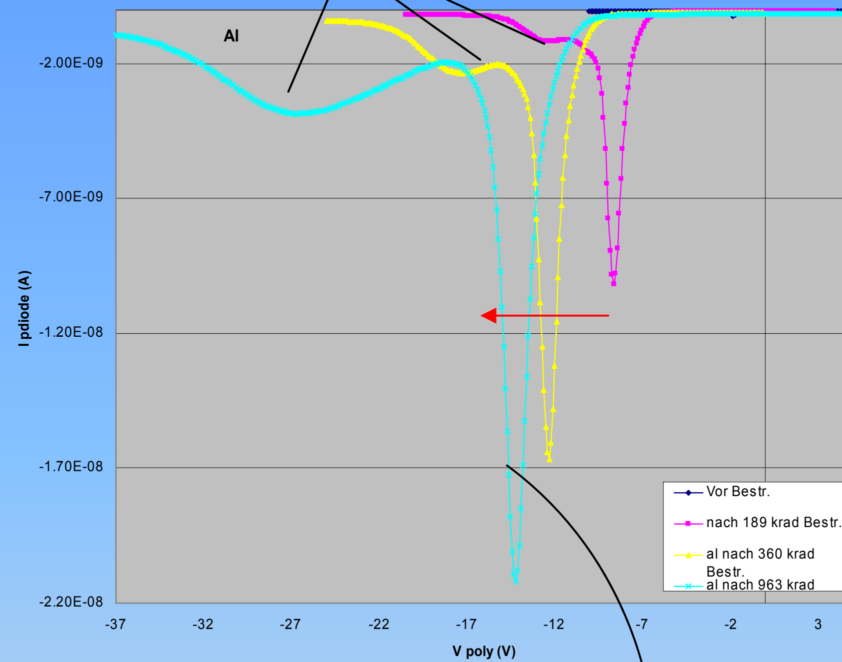


For gated Diode

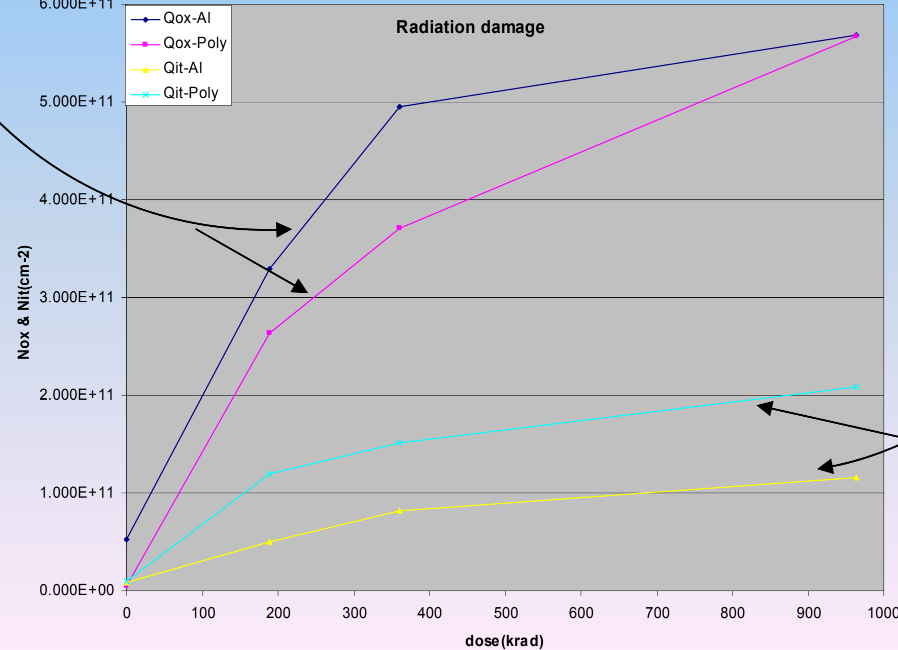
By using gated diode technique

Gate bias conditions: 0V





peak shift → N_{ox}

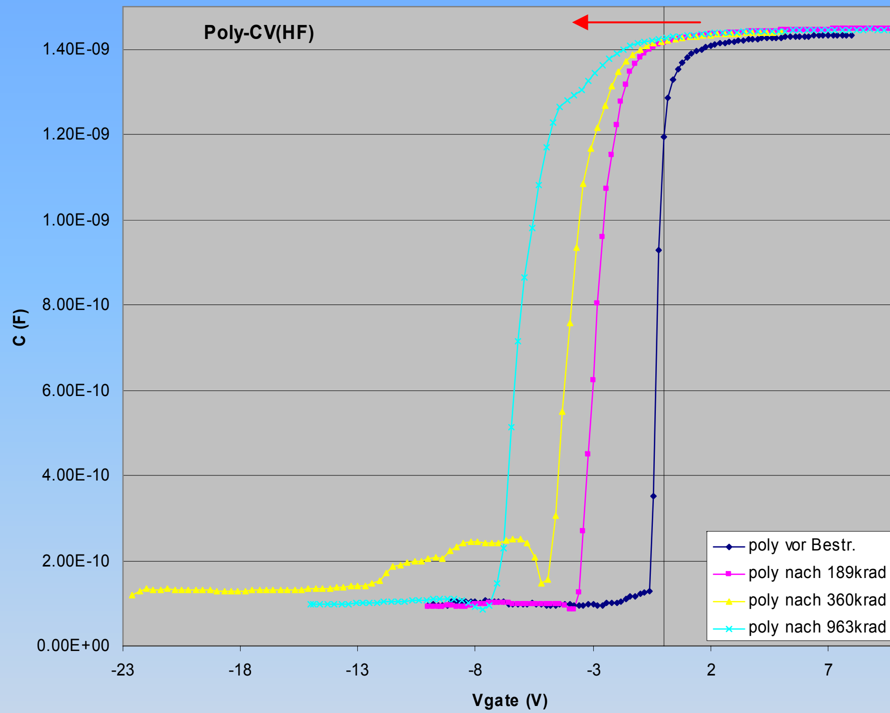


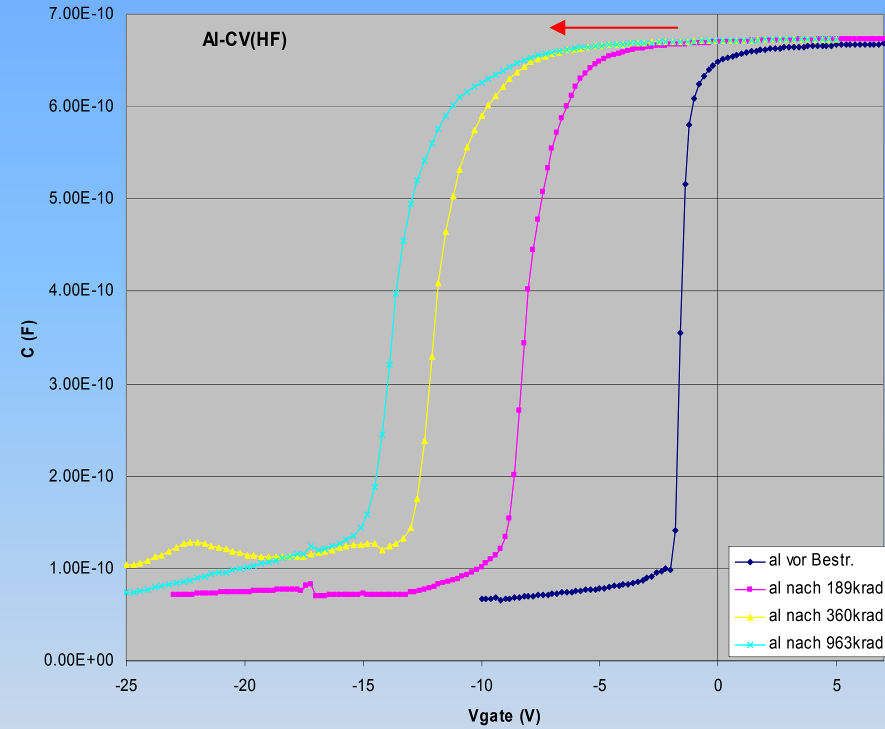
Full width at 2/3 I_{max} → N_{it}

For gated Diode

Gate bias conditions: 0V

Using CV-method (HF)



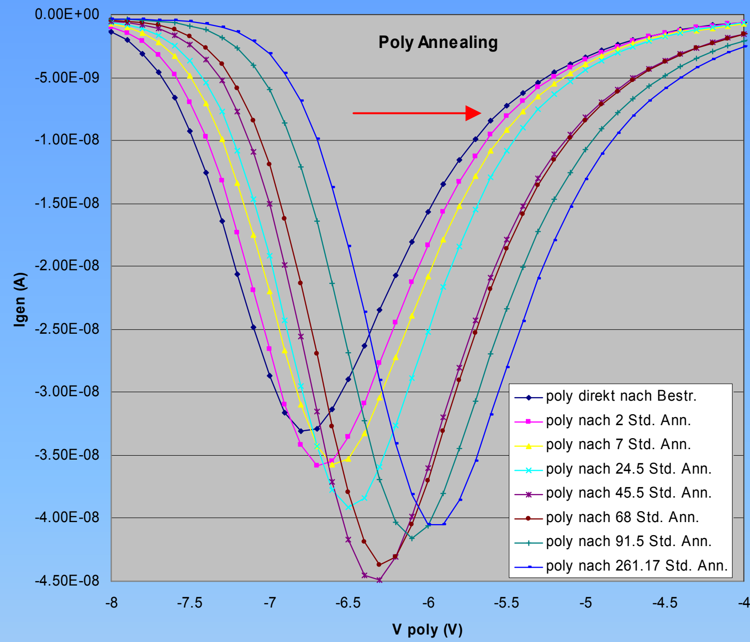


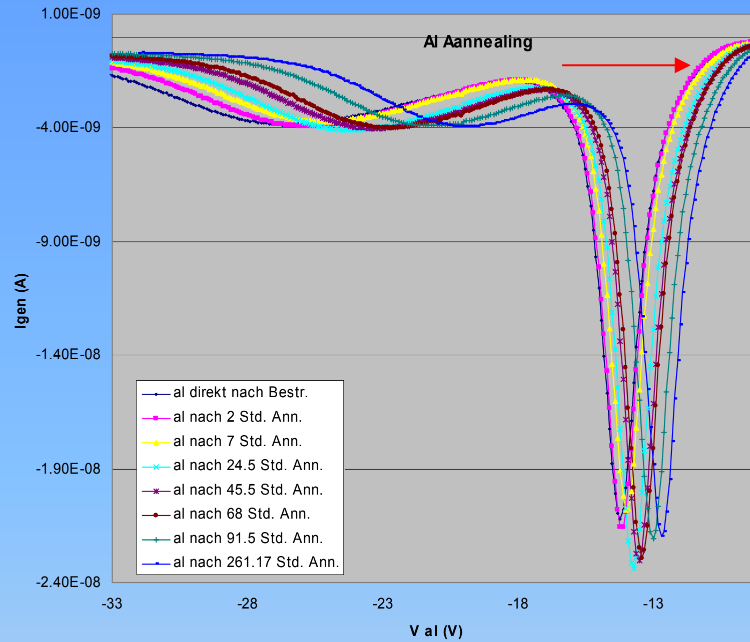
A good agreement for determination of N_{ox} by ΔV_{FB}(CV) and ΔV_G(gated diode technique)

Using gate controlled diode technique

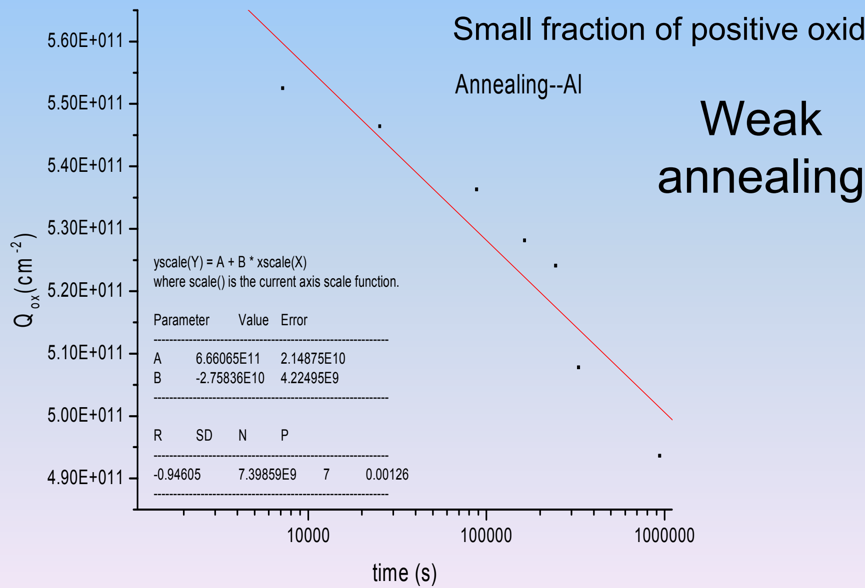
Annealing for Gated Diode

Gate bias conditions: 0V

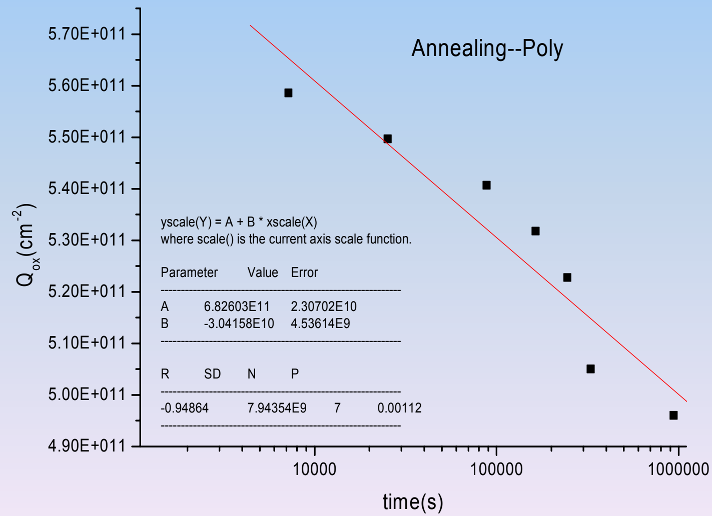




Small fraction of positive oxide charges (~11%) are recoverd!



Weak annealing

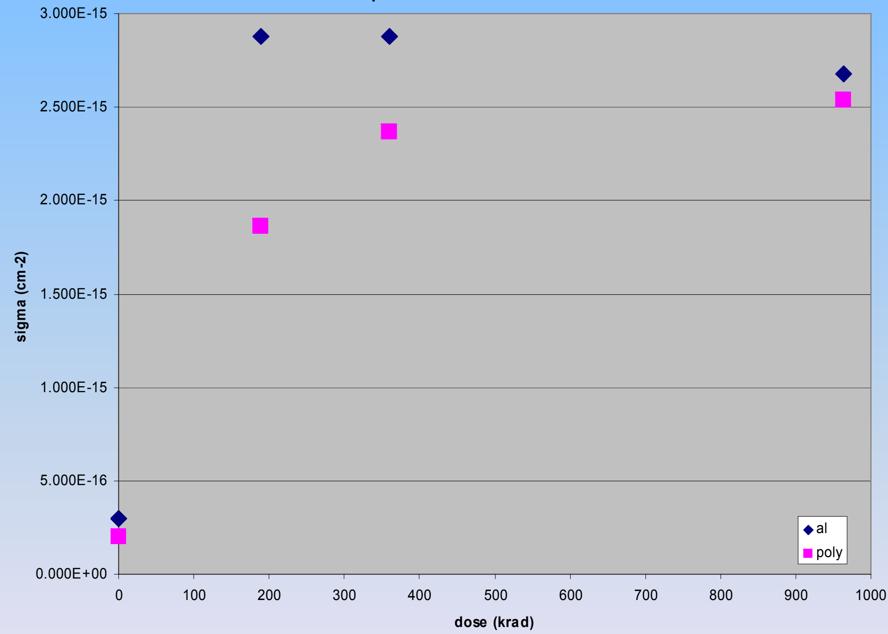


During annealing N_{ox} decreases linearly with ln(t)

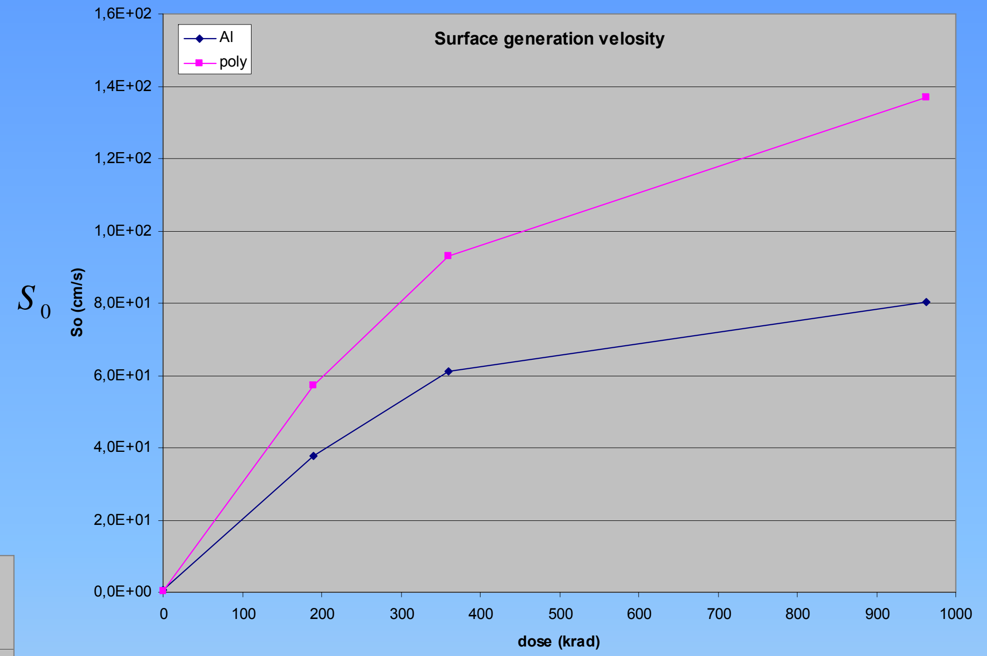
for Gated Diode

Gate bias conditions: 0V

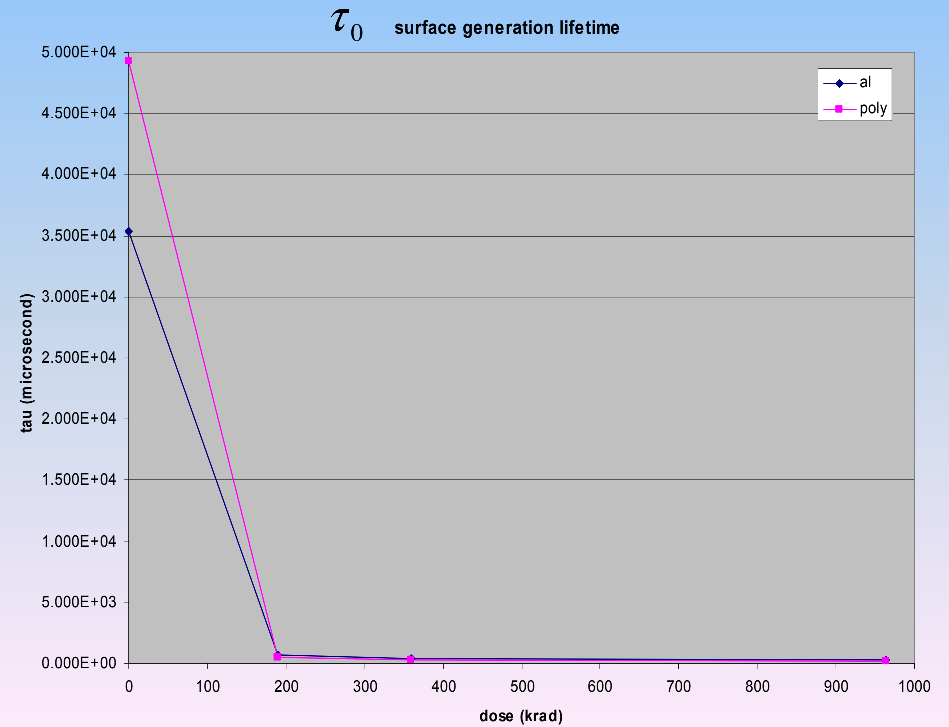
σ_n (due to another traps)



S_0



τ_0



Results for DEPFET

Bias during irradiaton:

1: empty int. gate, in „off" state, V_{GS}= 5V, V_{Drain}=-5V → $E_{ox} \approx 0$

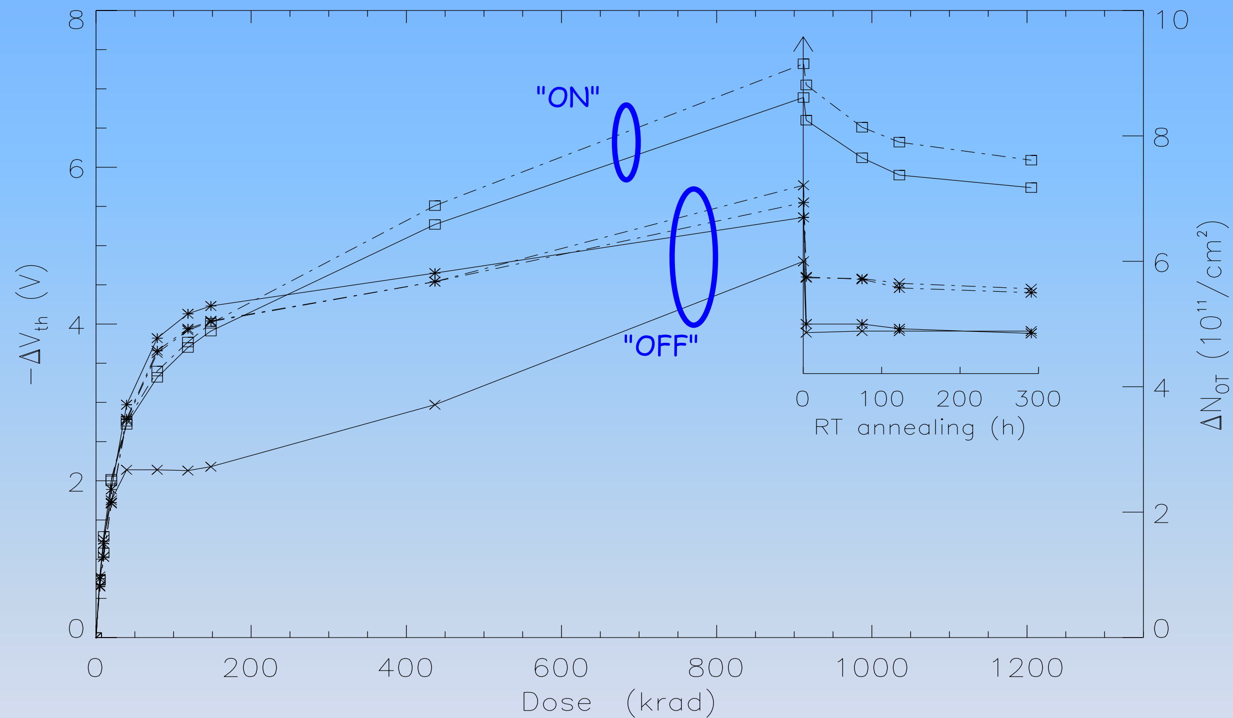
2: empty int. gate, in „on" state, V_{GS}=-5V, V_{Drain}=-5V → $E_{ox} \approx$ -250kV/cm

3: all terminals at 0V

GSF – National Research Center for Environment and Health, Munich

^{60}Co (1.17 MeV and 1.33 MeV)

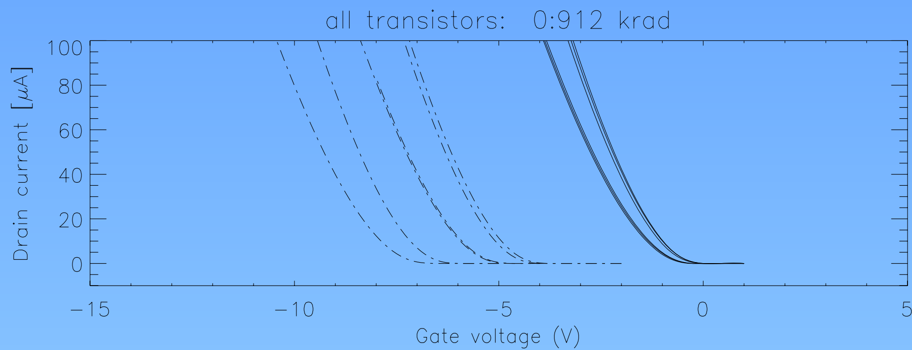
No annealing during irradiation
→ ~ 3 days irradiation

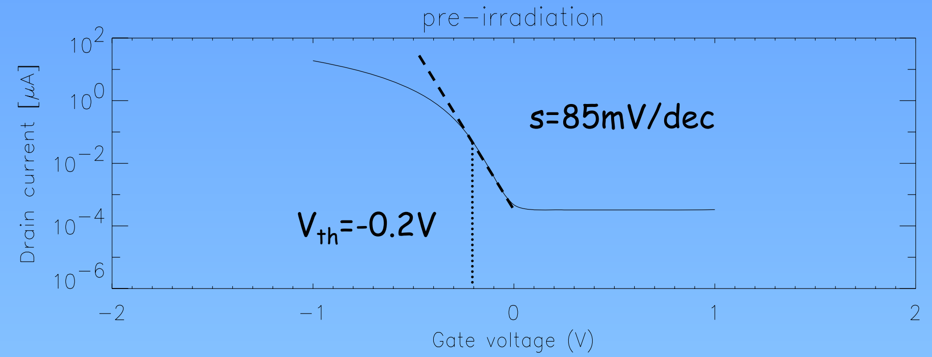


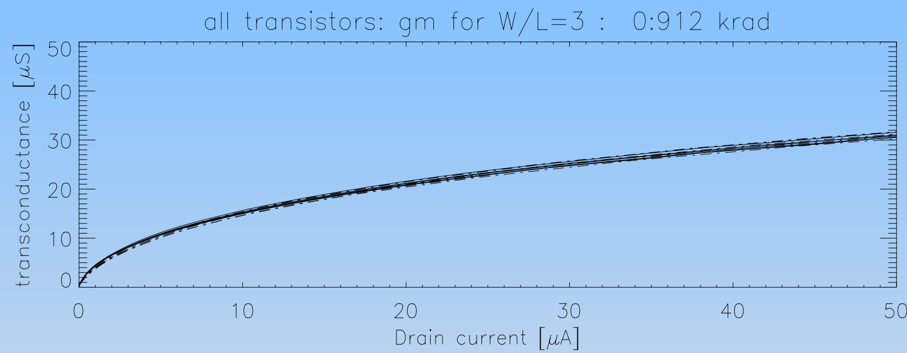
Radiation Effects (ionizing radiation)

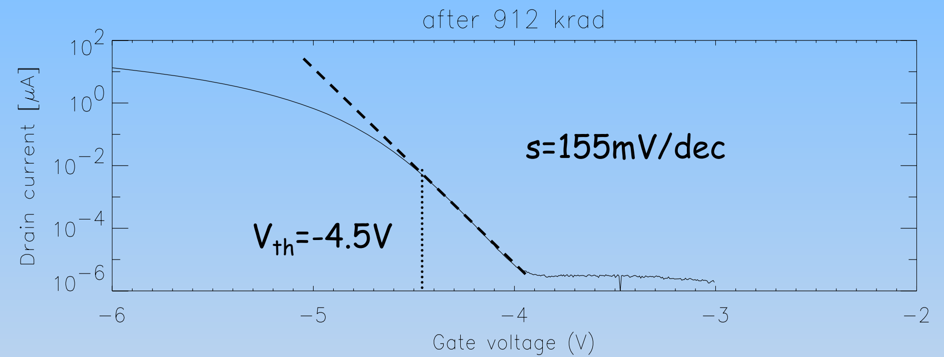
1. postive oxide charge: negative shift of the theshold voltage ($\sim t_{ox}^2$)
2. interface traps: higher 1/f noise and reduced mobility (g_m)

Transconductance and subtreshold slope









$$N_{it} = \left[C_{ox} / kT \ \ln(10) \right] (S_{D2} - S_{D1})$$

No change in the transconductance g_m

300 krad → $N_{it} \approx 2 \cdot 10^{11}$ cm^{-2}
912 krad → $N_{it} \approx 7 \cdot 10^{11}$ cm^{-2}

Literature:
After 1Mrad 200 nm (SiO_2):
$N_{it} \approx 10^{13}$ cm^{-2}

Discussion of the results

Comparison of N_{ox} and N_{it} between MOS-C and gated diode

for Al- and poly-gate structure at dose of 189krad and 1Mrad

dose	N_{ox}	MOS-C		Gated diode	dose	N_{it}	MOS-C		Gated diode
189krad	Al	8,3e11	>	3,3e11	189krad	Al	2,8e11	>	5,1e10
		V		≈			V		Λ
189krad	Poly	3,3e11	≈	2,6e11	189krad	Poly	6e10	<	1,2e11
dose	**N_{ox}**	**MOS-C**		**Gated diode**	**dose**	**N_{it}**	**MOS-C**		**Gated diode**
1Mrad	Al	1,9e12	>	5,7e11	1Mrad	Al	6,8e11	>	1,2e11
		V		=			V		Λ
1Mrad	Poly	6,7e11	≈	5,7e11	1Mrad	Poly	1,1e11	<	2,1e11

For poly-gate structure: more N_{it} on Gated diode than on MOS-C

For Al-gate structure: more N_{it} and N_{ox} on MOS-C than on Gated diode

For N_{ox}: the same for both Al-gate and poly-gate structure (Gated diode)

For N_{ox}: More N_{it} for poly-gate than Al-gate structure (Gated diode)

More N_{it} and N_{ox} for Al-gate than poly-gate structure (MOS-C)

For N_{ox}: a good agreement for poly-gate structure (MOS-C & gated diode)

(Poly-gate structure for three devices)

dose	DEPFET	N_{ox}	N_{it}
912krad	Poly	6~7e11	7e11

→

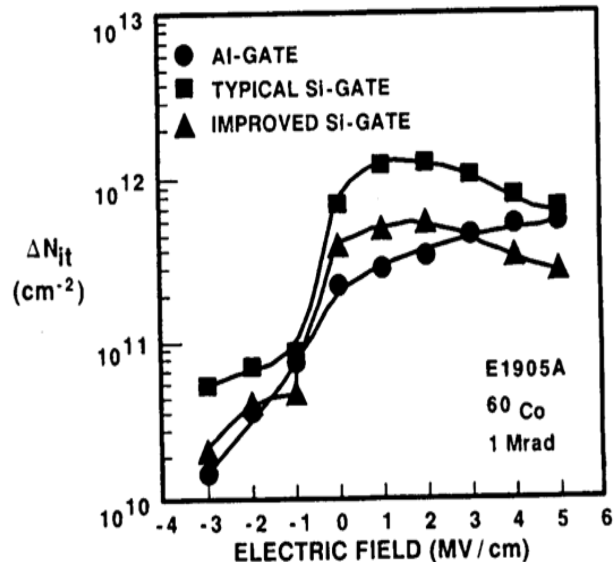
For N_{ox}: DEPFET=Gated diode≈ MOS-C √

For N_{it}: DEPFET>Gated diode>MOS-C ?

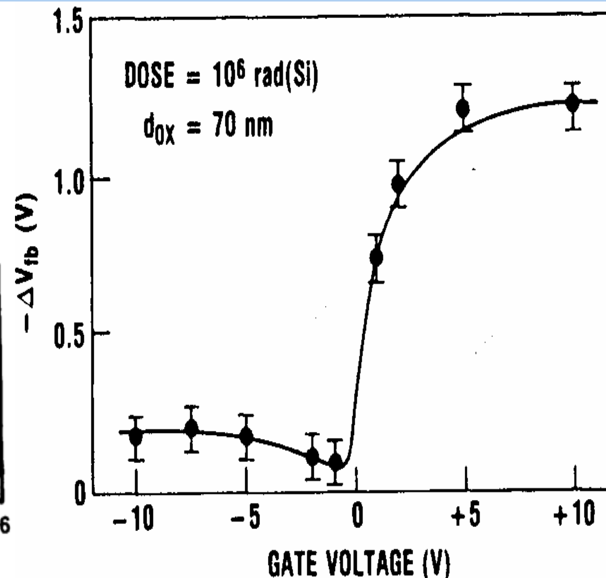
Comparison between literature and our experiment

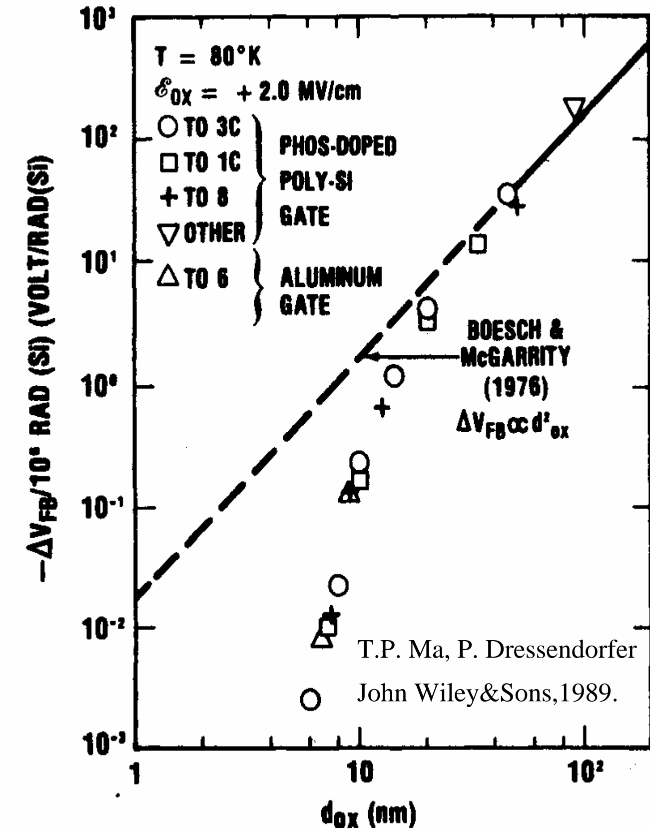
- Differences for the saturation effect of interface trap on MOS-C
- Differences for the generation of defects on MOS-C (poly-gate for DEPFET)
- Differences for defect generation at negative gate bias on MOS-C

Winokur, 1985.



Derbenwick, Gregory, 1975





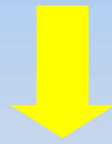
T.P. Ma, P. Dressendorfer

John Wiley&Sons,1989.

Backup slides

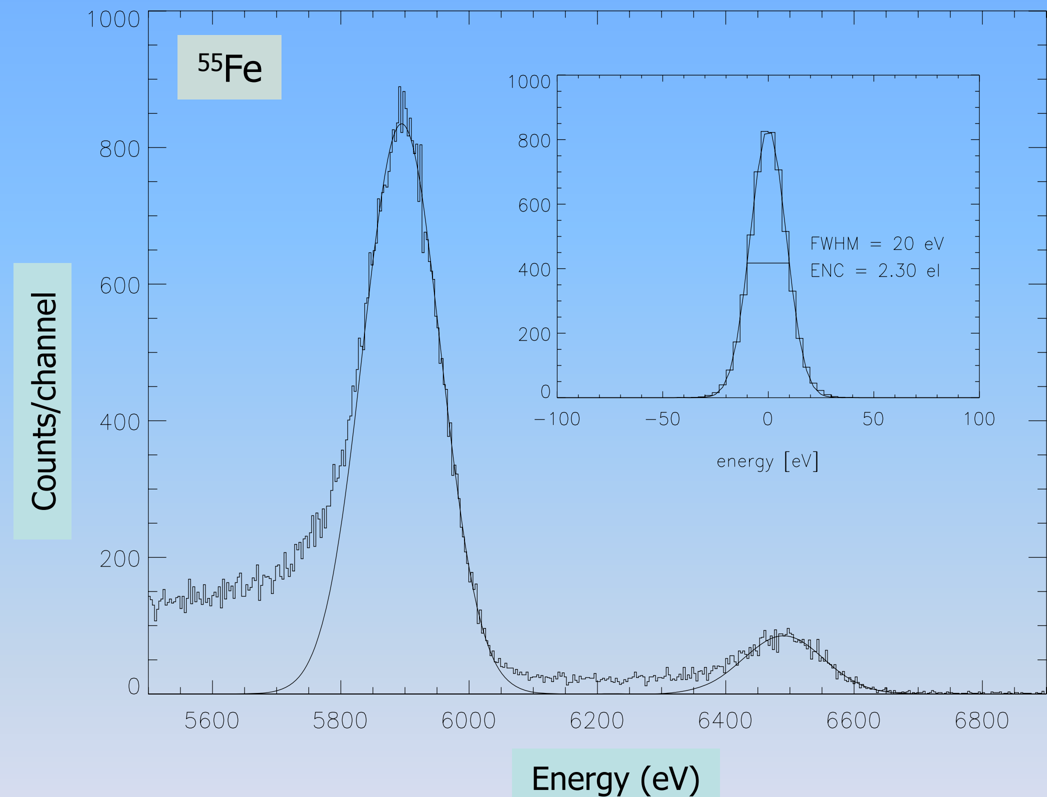
Performance before irradiation

- non-irrad. double pixel DEPFET
  - L=7µm, W=25 µm
- V_{thresh}≈-0.2V, V_{gate}=-1V
- I_{drain}=41 µA
- Drain current read out
- time cont. shaping τ=6 µs



Noise ENC=2.3 e^- (rms)

at T>23 degC

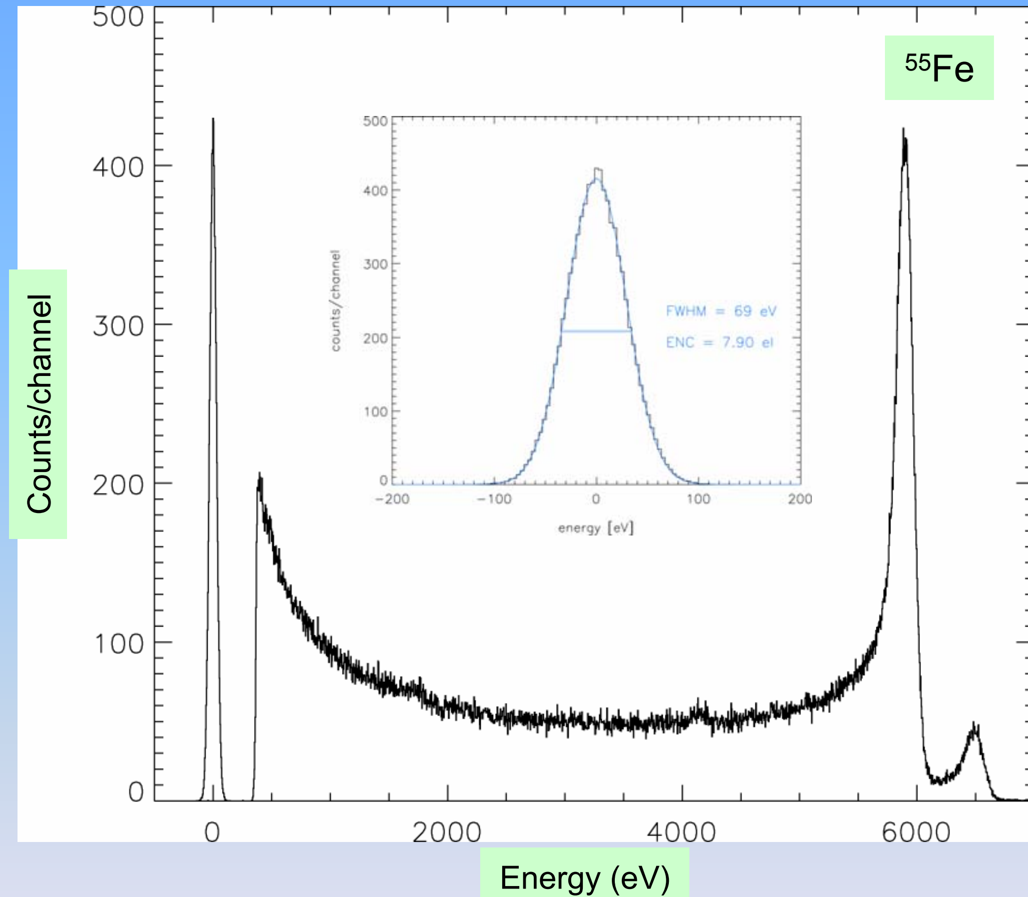


Performance after irradiation for DEPFET

- Irradiated double pixel DEPFET
  - L=7μm, W=25 μm
  - after 913 krad, ^{60}Co
- V_{thresh}≈-4V, V_{gate}=-5.3V
- I_{drain}=21 μA
- Drain current read out
- time cont. shaping τ=6 μs

Noise ENC=7.9 e^- (rms)

at T>23 degC



Non-irradiated:
Noise ENC=2.3 e^- (rms)