The bPOL12V story

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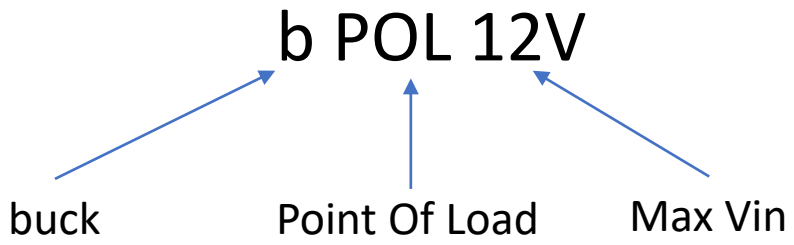
Introduction: what is a DCDC converter?

DC-DC converters are electronic circuits that convert a DC voltage level to another DC voltage level.

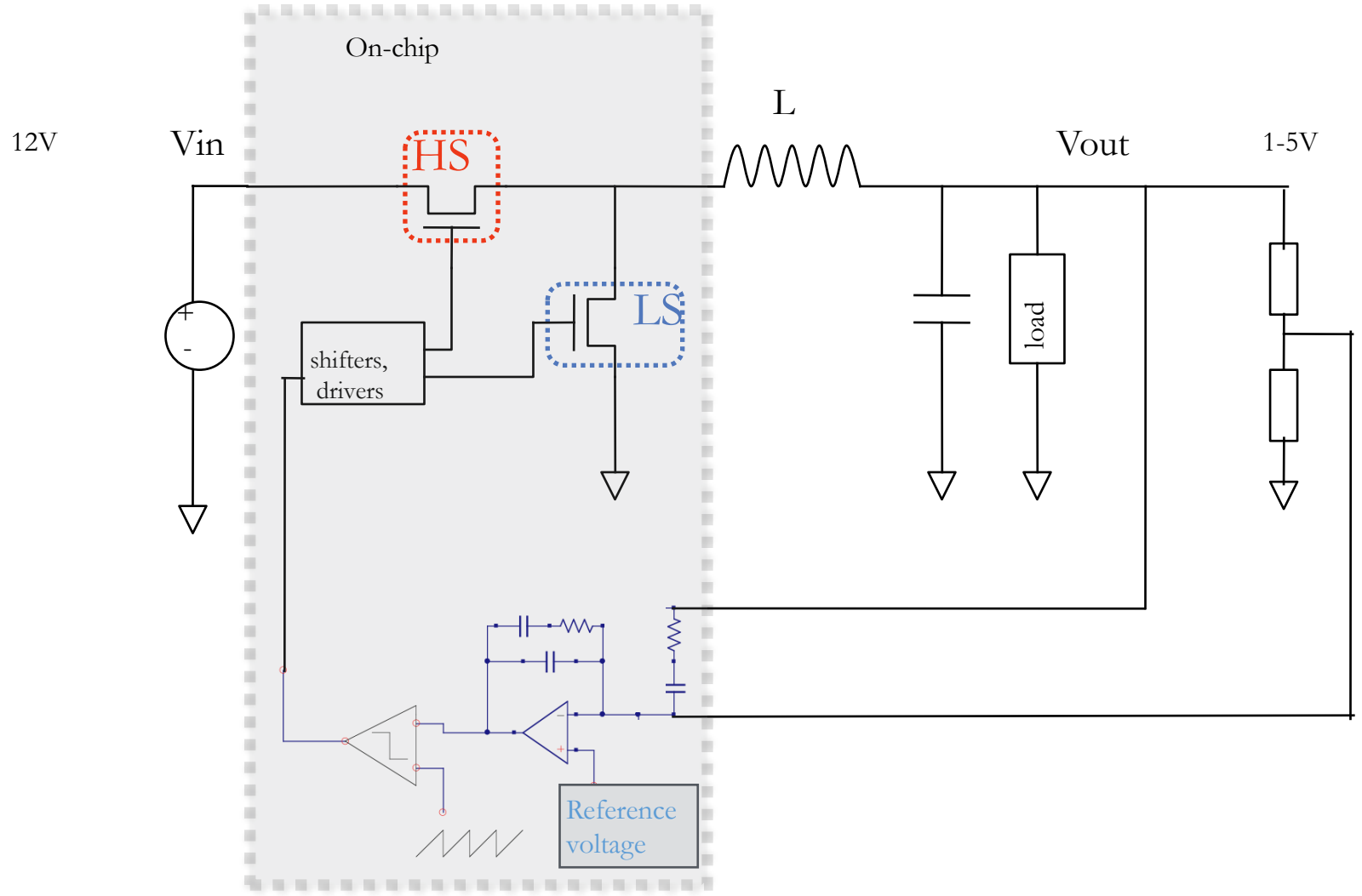
They are widely used in various applications, such as power supplies, battery chargers, and electric vehicles.

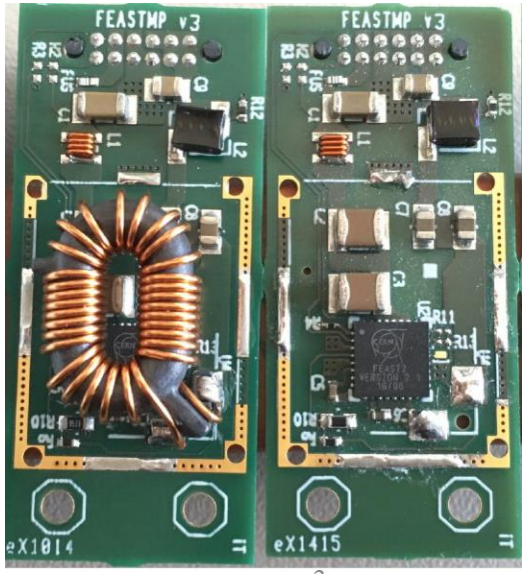
The two main types of DC-DC converters are buck converters (step down) and boost converters (step up).

In this presentation, we will focus on a buck converter, called bPOL12V, designed at CERN for meeting radiation and high magnetic field tolerance for HEP experiment

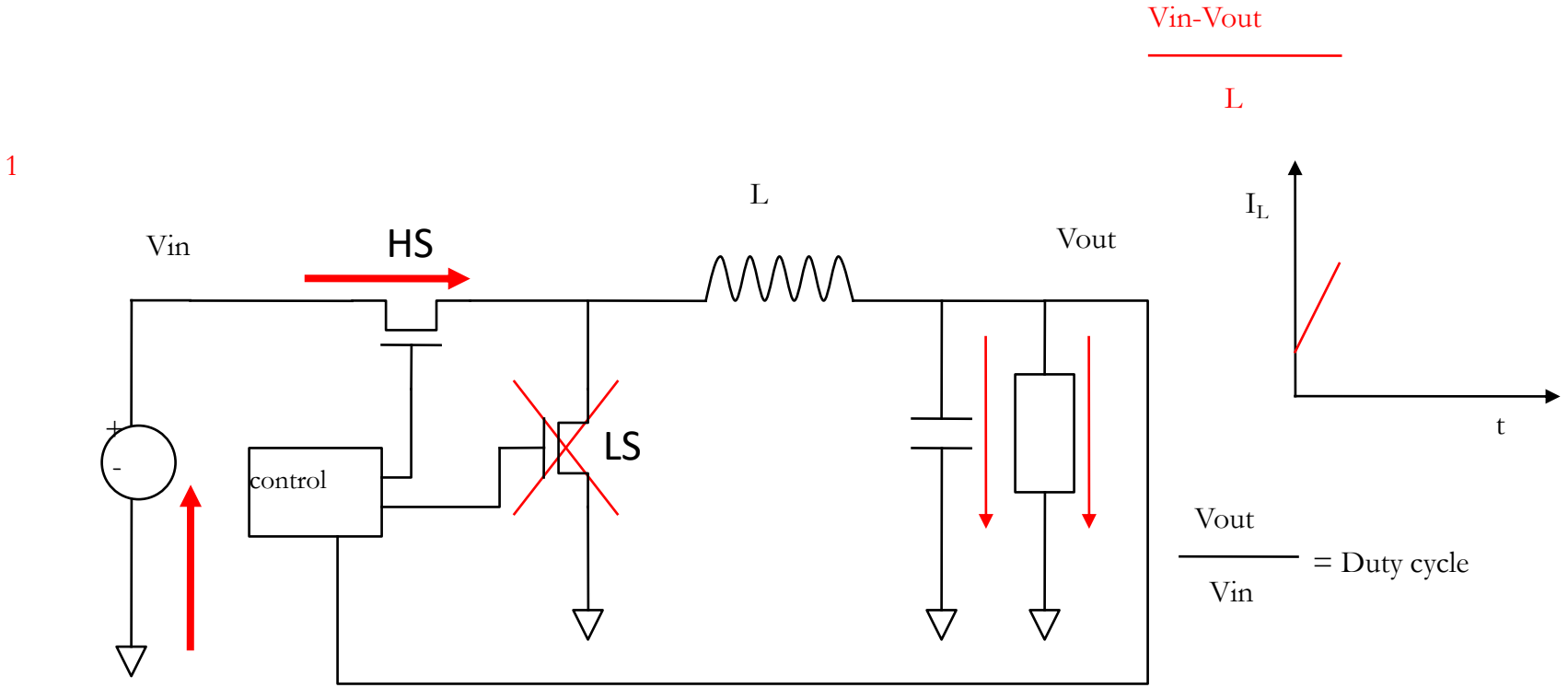


A buck DCDC converter in a nutshell



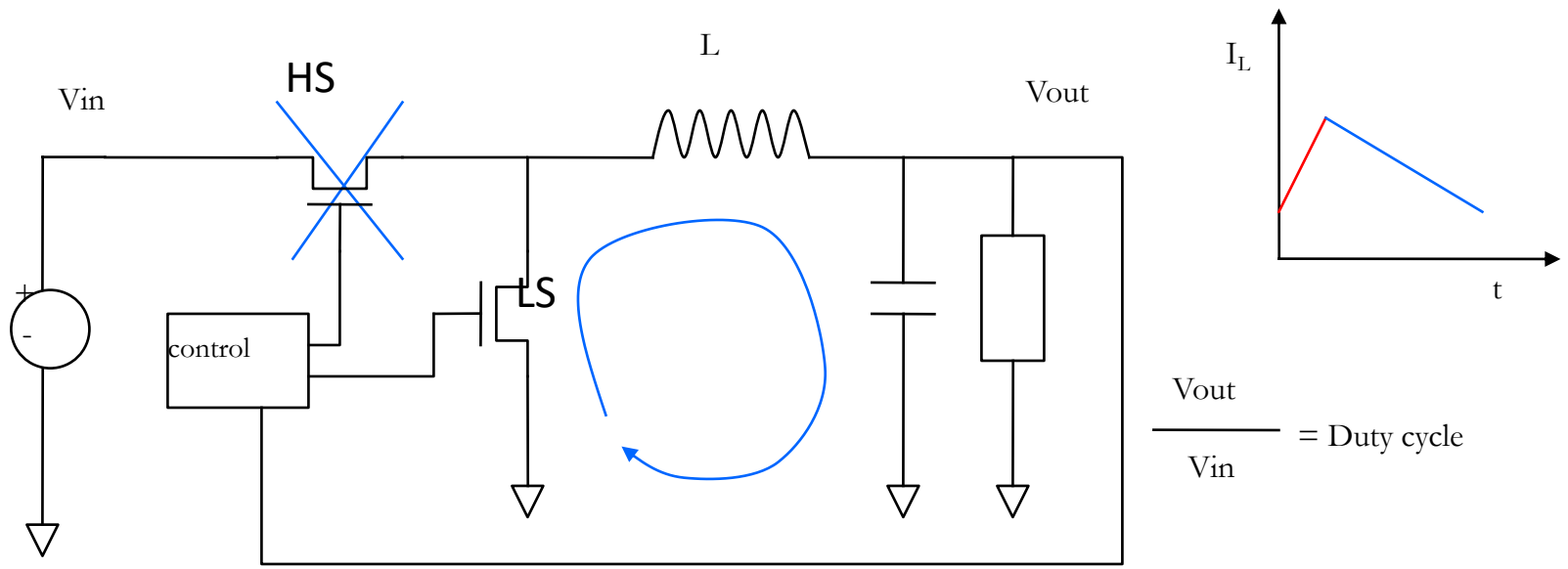


Operation of a switching converter HS-ON

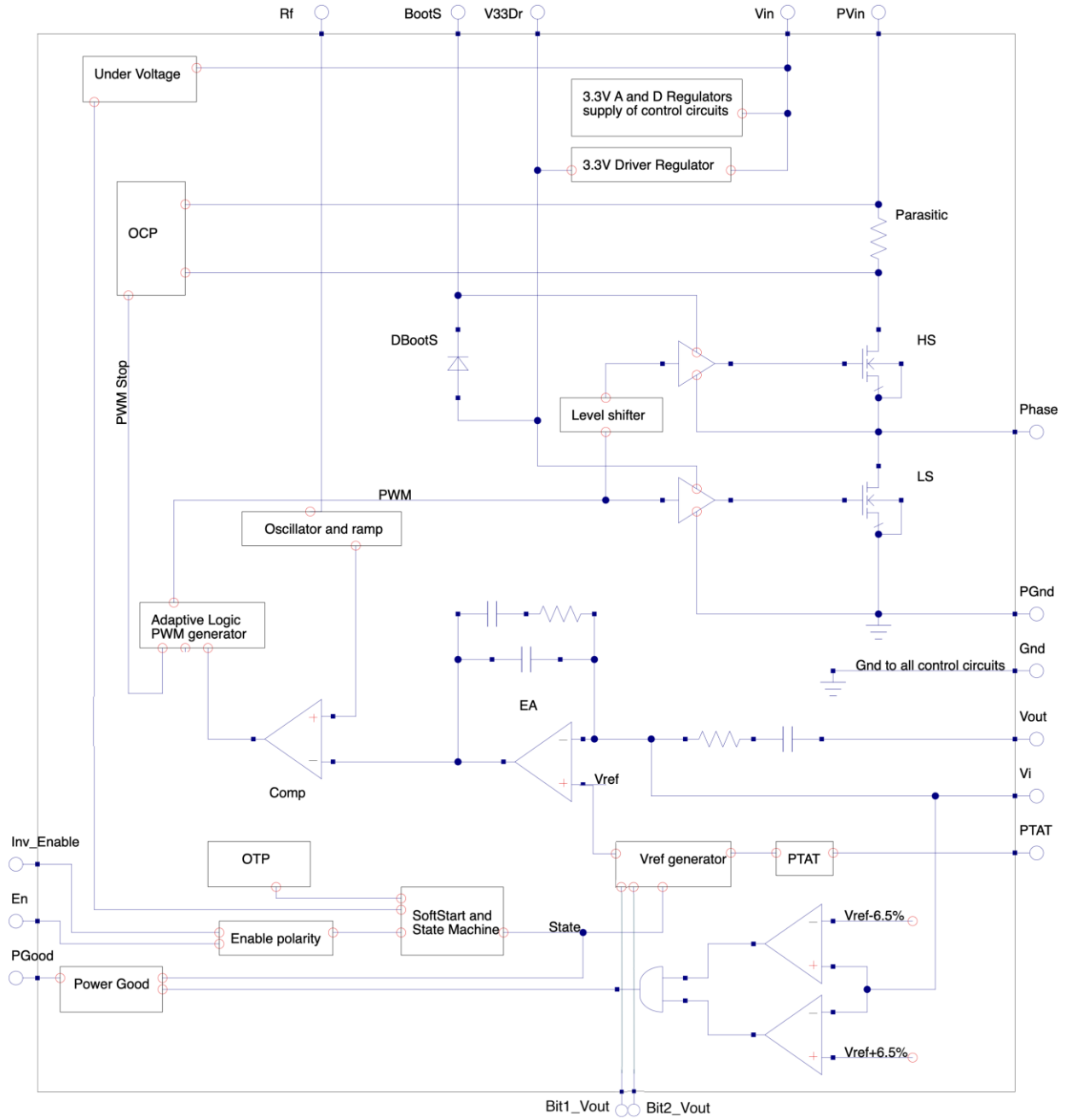


Operation of a switching converter LS-ON

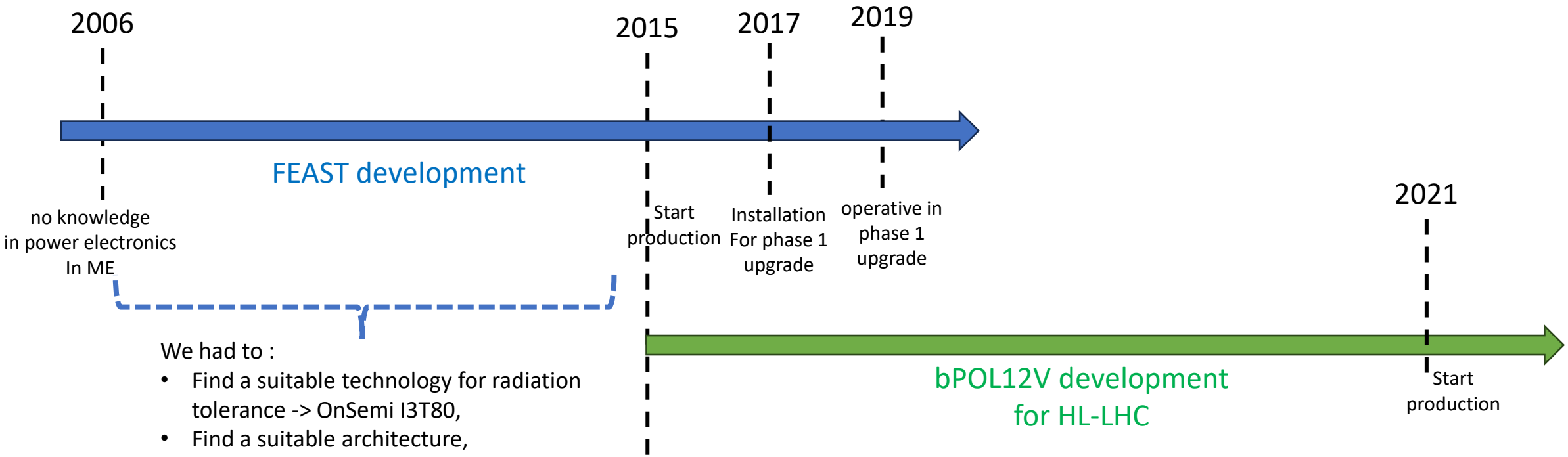
2



bPOL12V internal scheme



A bit of history: DCDC converter at CERN



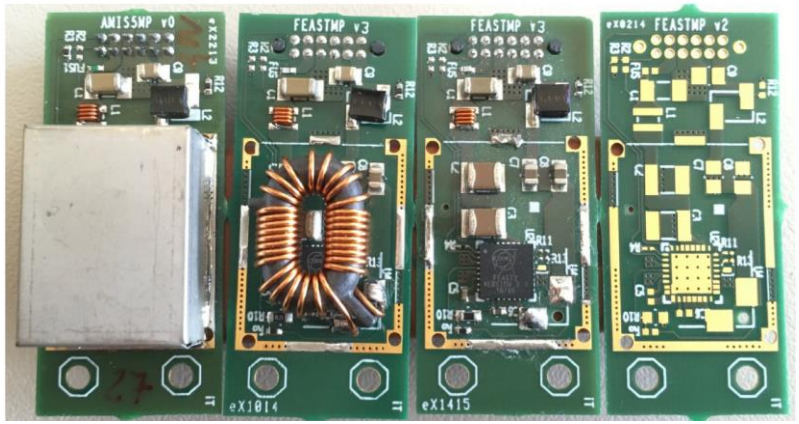
We had to :

- Find a suitable technology for radiation tolerance -> OnSemi I3T80,
- Find a suitable architecture, (collaboration with Univ. of Padova, prof. Spiazzi and Buso)
- Design the full converter (collaboration with Univ. of Udine, prof Saggini)
- Develop the module
- Prove that it is low noise and can be used in the system

Legacy converter:
FEAST, designed for Phase 1 upgrade (2019)

After 7 iterations on silicon in the years around 2013 we had a working DCDC converter + modules called FEASTMP that complied with the radiation levels for Phase 1 experiment upgrades.

Radiation levels
TID=150Mrad
DD= 5e14 n/cm^2
SEE “immune”



Next challenge: HL-LHC radiation level requirements

	Quantity	CMS environment (PS modules)	ATLAS environment (endcap strips)
TID	Energy deposited via ionisation	56 Mrad	51 Mrad
SEEs	Integrated flux of all hadrons above 10-20MeV		
Displacement Damage	Integrated flux in 1MeV-equivalent neutrons (scaled with NIEL)	9e14 n/cm^2	1.2e15 n/cm^2

REMINDER:
FEAST Radiation levels
TID=150Mrad
DD= 5e14 n/cm^2
SEE "immune"

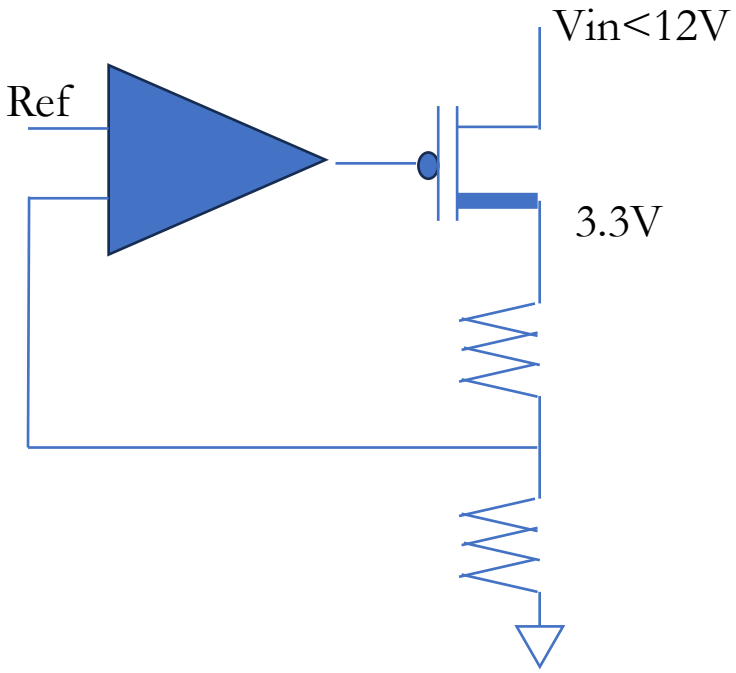
FEAST is not usable for HL-LHC application.
In 2013We have been charged to develop a new converter able to withstand a DD=2e15n/cm2

What's the limit of FEAST?

FEAST is limited by the Displacement Damage (DD) in the internal linear regulators

The linear regulators are needed to provide the 3.3V needed by the control circuitry from Vin (up to 12V).

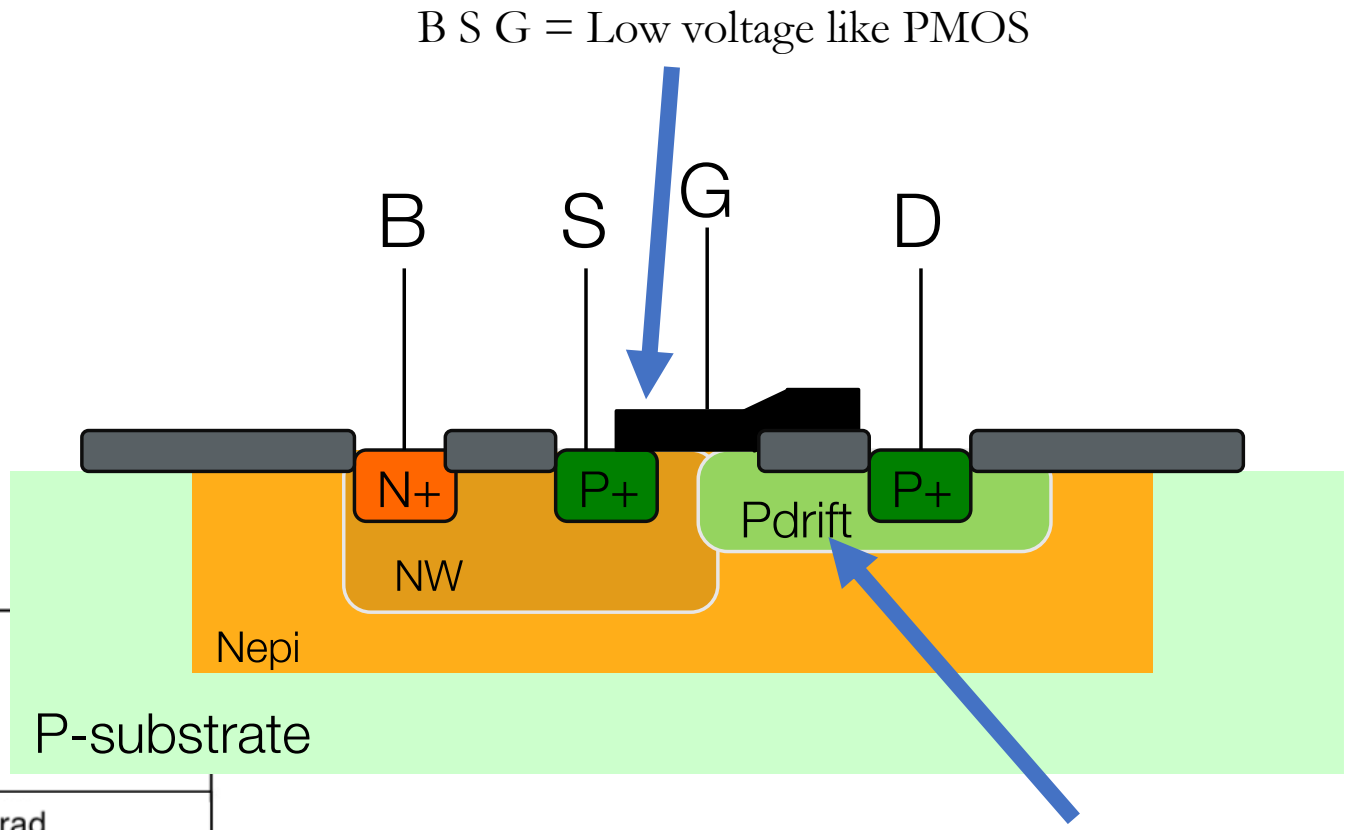
The pass transistor is HV LDPMOS rated 80V

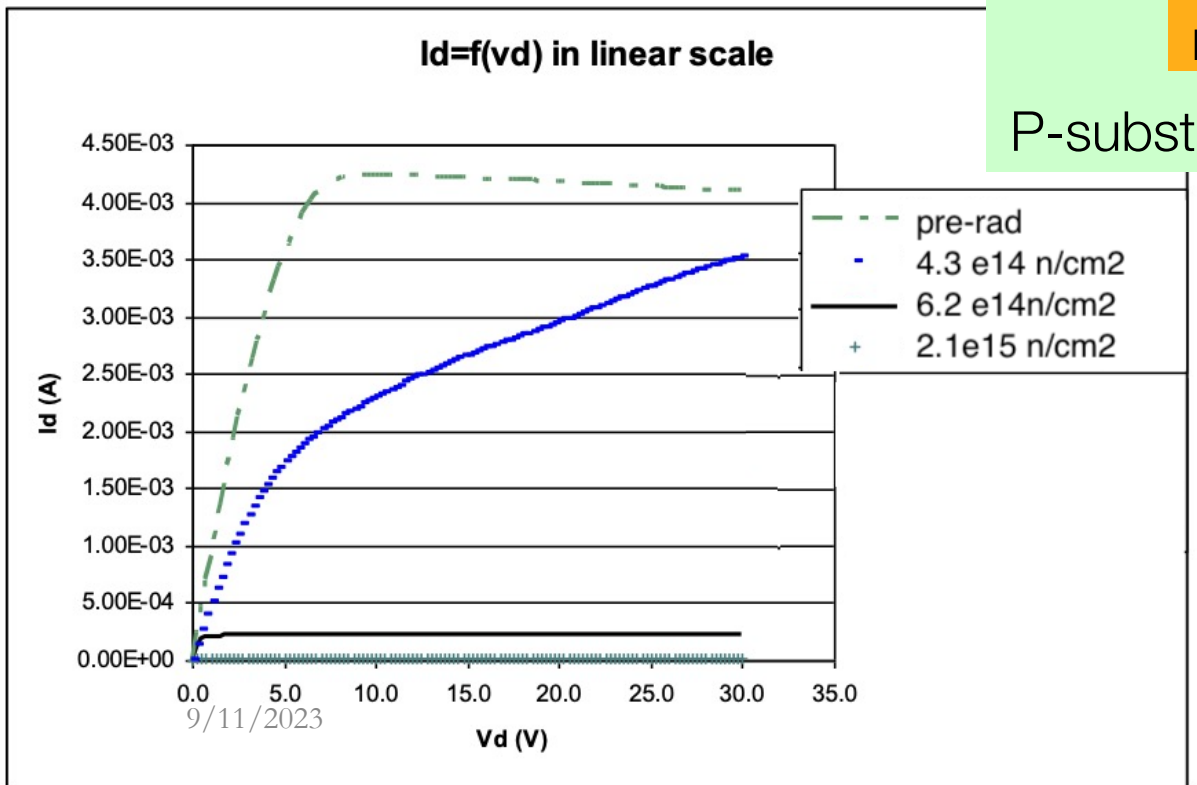


HV LDPMOS in this technology is a transistor that can stand Vds up to 80V, with Vgs=3.3V.

DD affects the on-resistance

HV LDPMOS



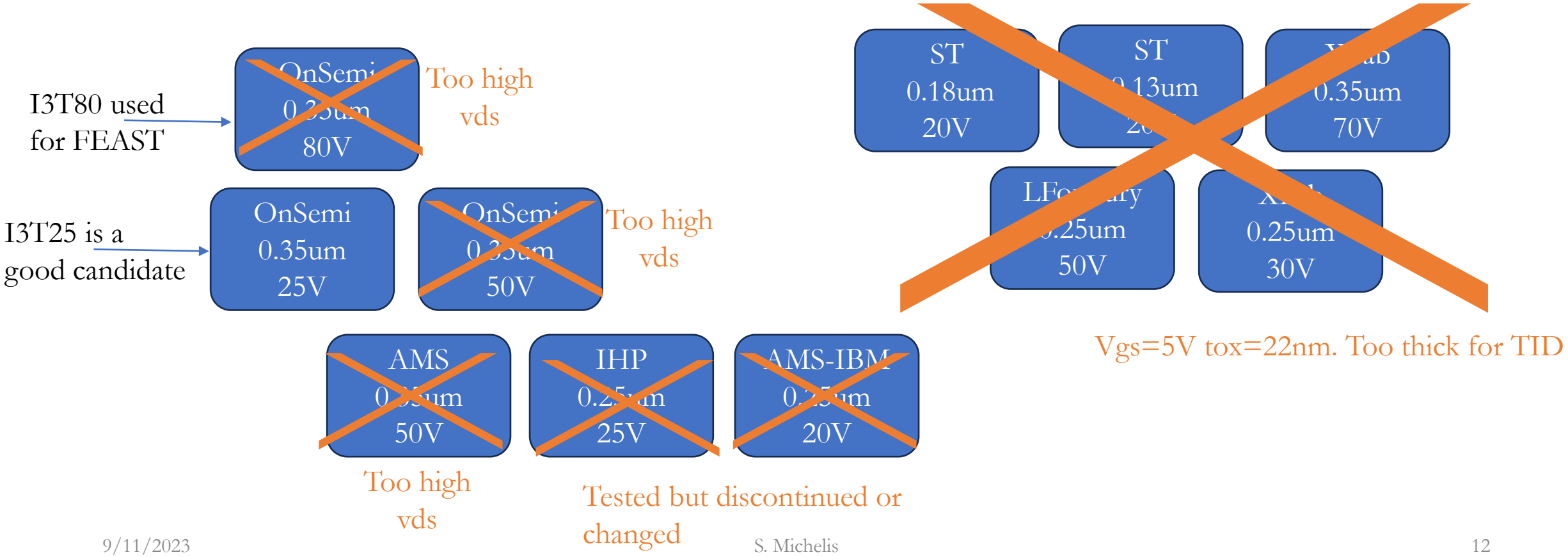


Low doped region to withstand the high VDS voltage

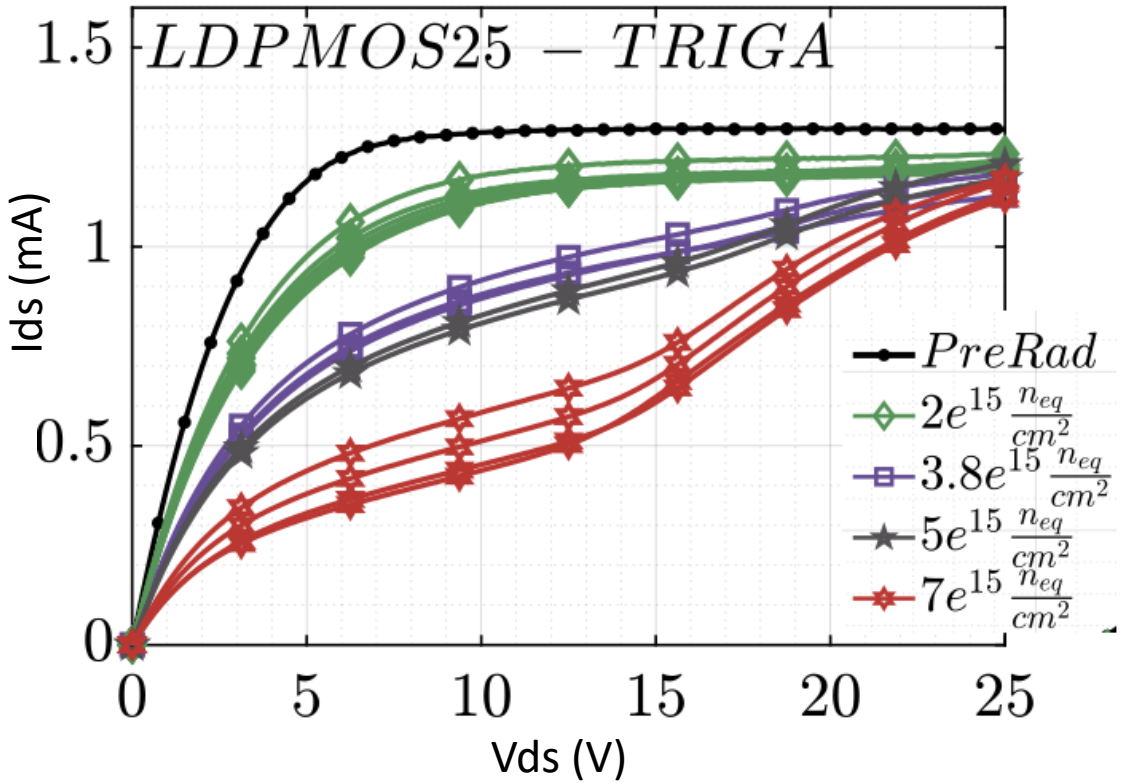
Limiting factor is the drift region, which is large and low doped for withstanding 80V

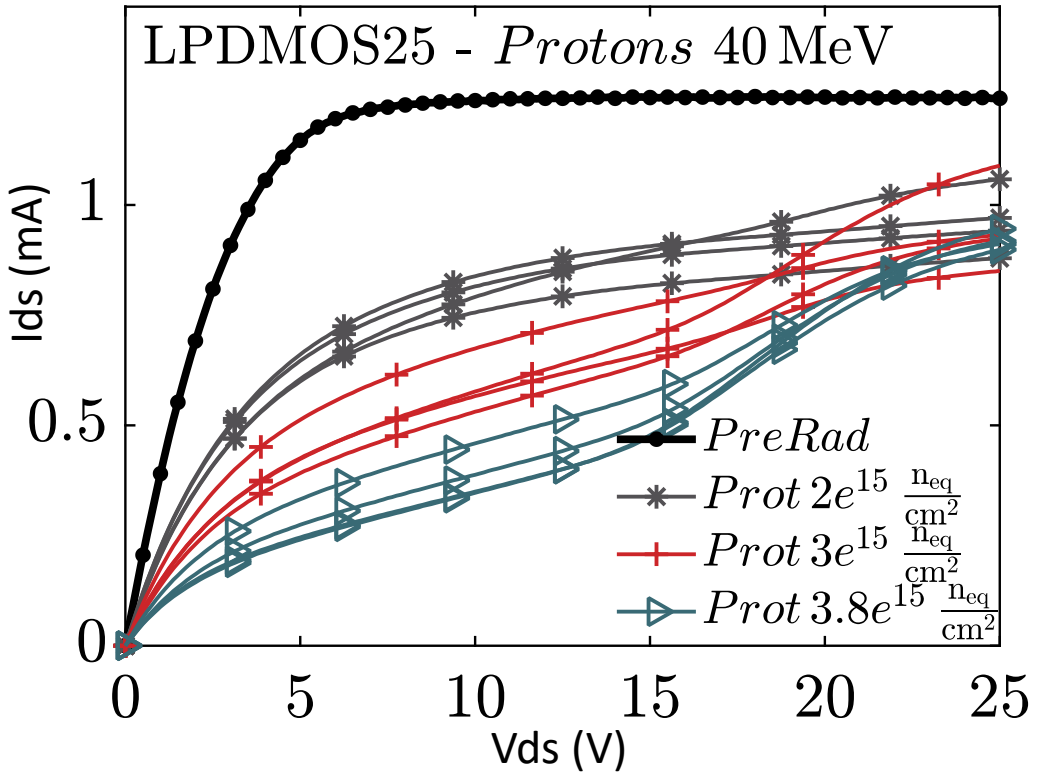
What can we improve DD resistance?

Only way is to change technology, but which one? Must be lower Vds voltage (smaller/higher doped drift region) but also Tox max=7nm



I3T25 response to DD





I3T25 is definitely a good candidate for reaching the 2e15n/cm2 necessary for HL-LHC experiment upgrades

Moving from FEAST to bPOL12V

We had to move all the design from I3T80 (FEAST) to I3T25 (bPOL12V) both from OnSemi

It is a sister technology, a lot of layers are similar.

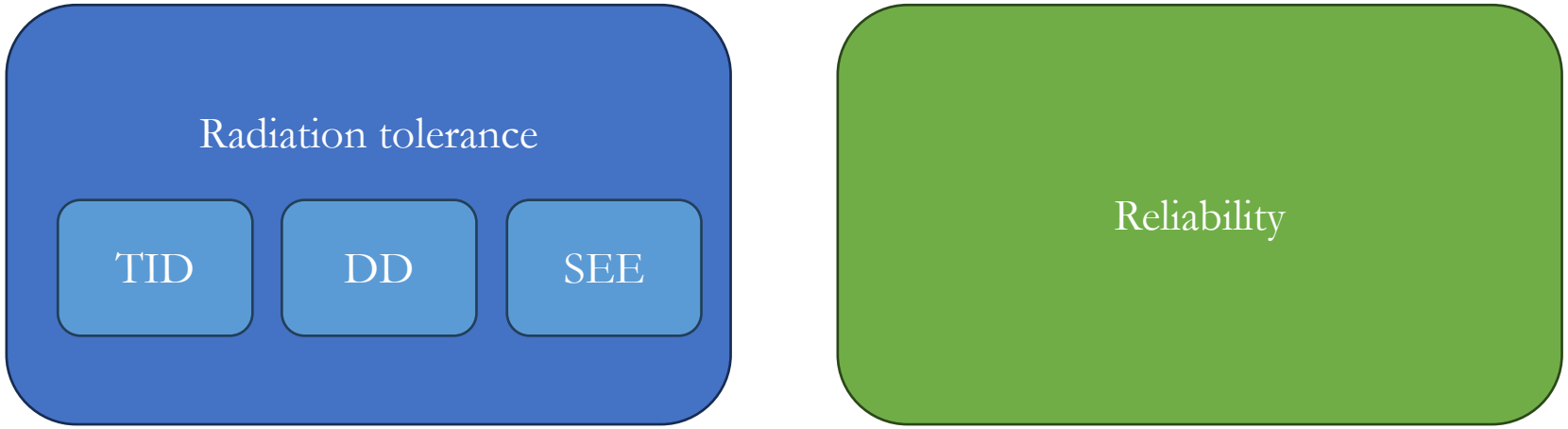
We had to re-do all substrate/well contacts and triple well design, change all high voltage circuits (HV bandgap, linear regulators)

We thought that it would be rather easy change.. But….

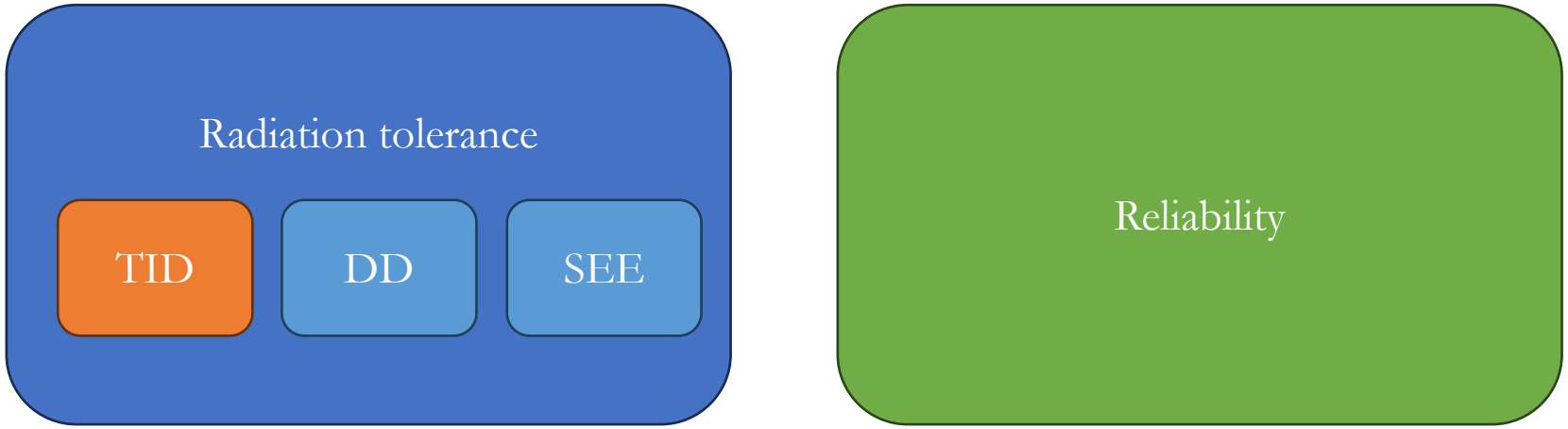
We ended up re-submitting the design 6 times!!!!!!!

Why?

Issues found during bPOL12V development



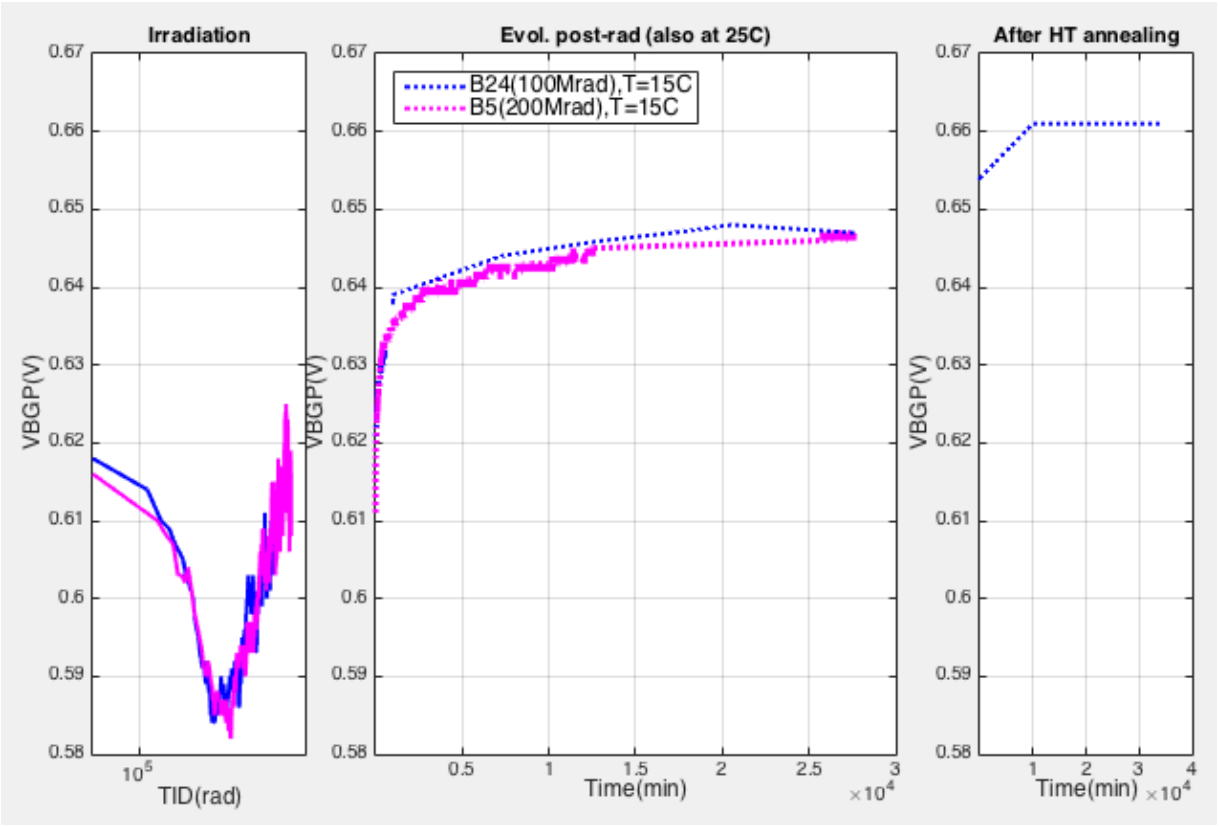
Issues found during bPOL12V development



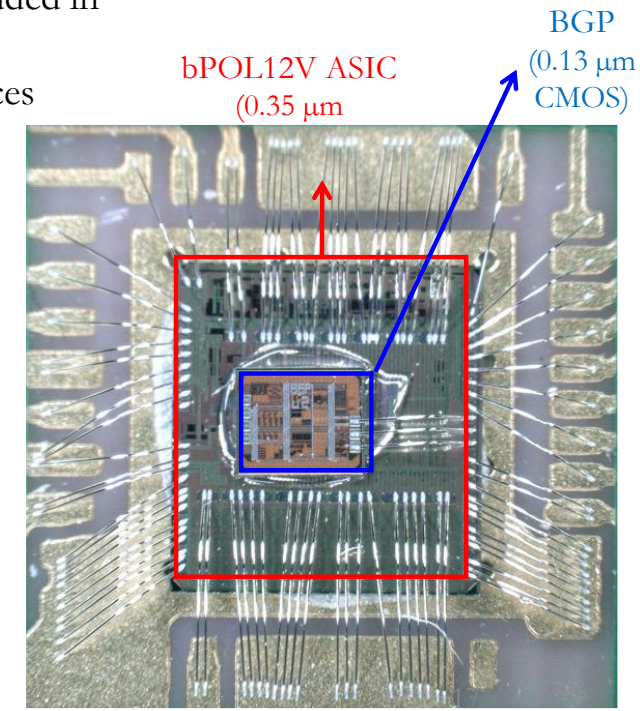
The on-chip reference voltage generator has two problems

(this is the best design we could make in the technology used)

1. The reference voltage can not be adjusted in this CMOS technology because there is no One-Time Programmable device offered. Production samples will therefore have a relatively large variability in their output voltage
2. TID irradiation shifts the reference voltage considerably, with a large post-irradiation annealing effect

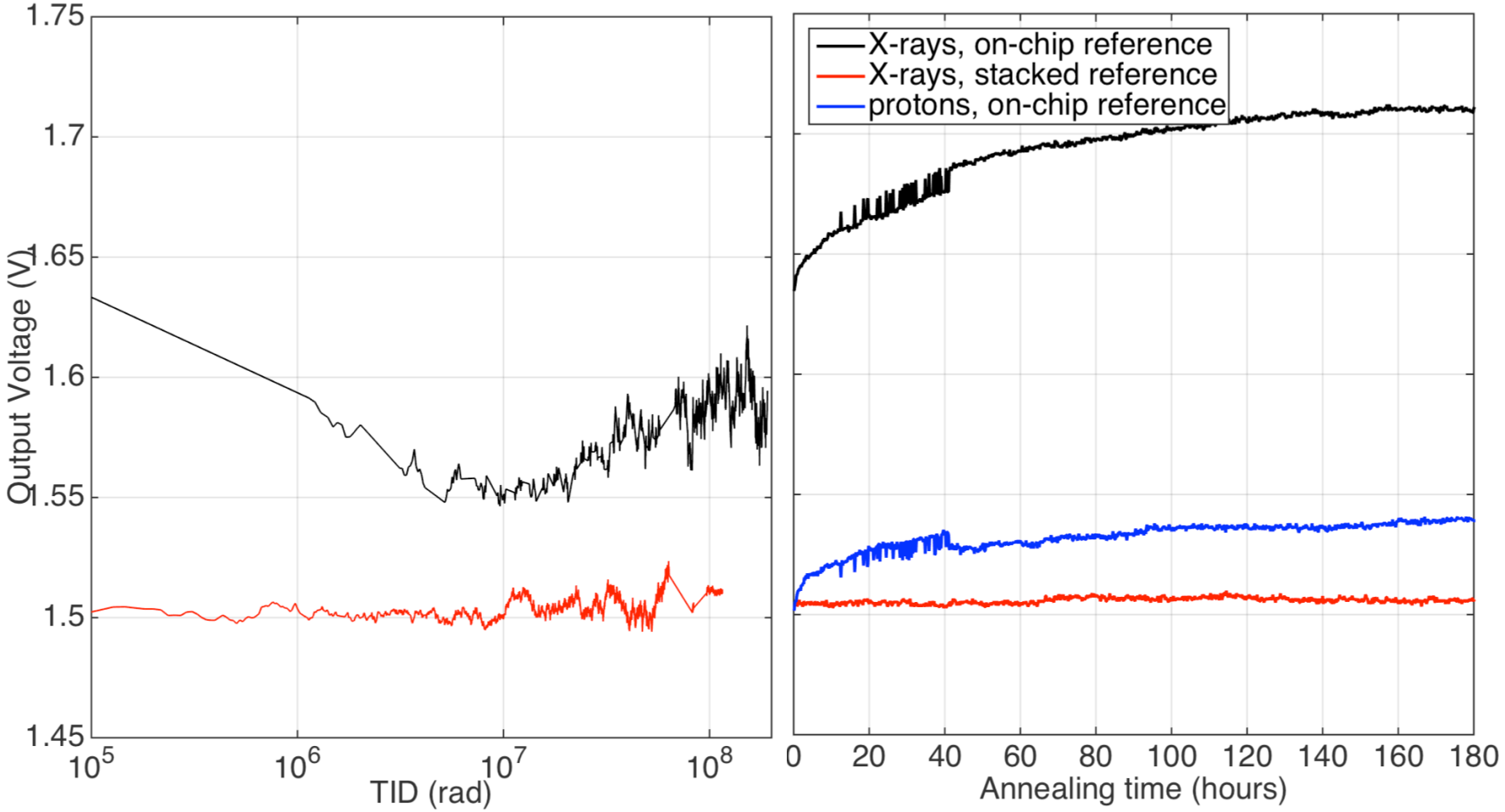


The on-chip reference is replaced by an external reference from a small 130nm chip embedded in the same QFN32 package.
This reference is adjustable via OTP devices available in the technology (e-fuses).



Co-packaging in QFN32

The TID effects on BGP (internal and external)

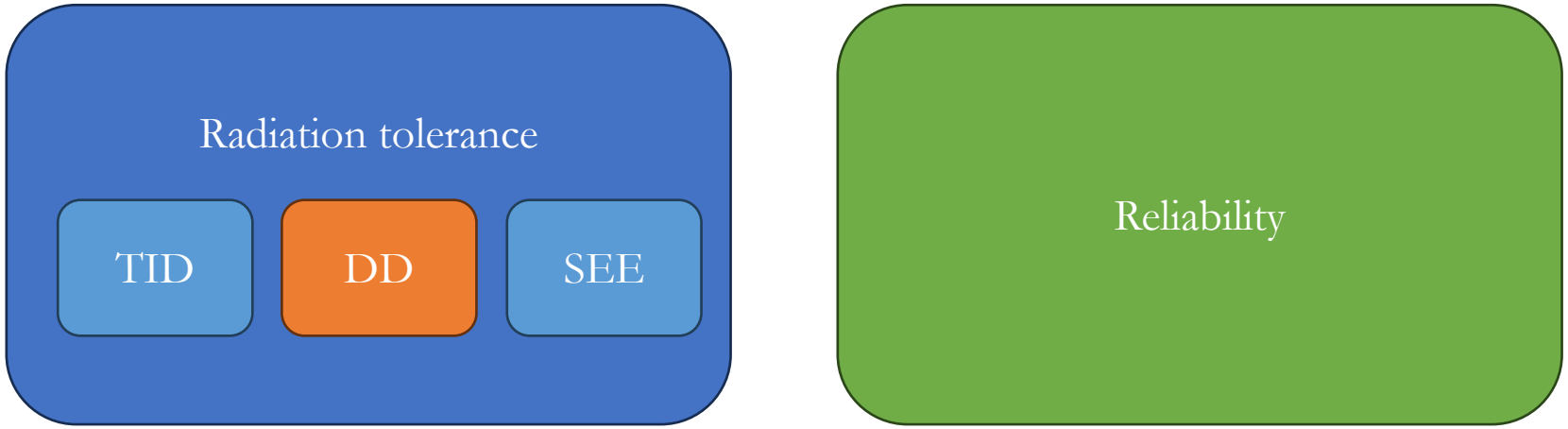


INTERNAL BGP
Irradiated up to 190Mrad @ -30C under bias
Annealed under bias (10V, 3A, about 60C)

INTERNAL BGP
Irradiated up to 4e14 p/cm^2 without bias
Annealed under bias (10V, 3A, about 60C)

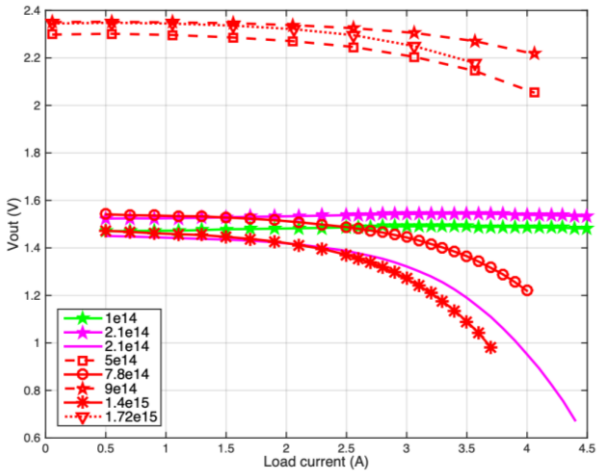
EXTERNAL BGP
Irradiated up to 114Mrad @ 25C under bias
Annealed under bias (10V, 3A, about 60C)

Issues found during bPOL12V development



DD effects discovered during the development

Poor regulation at large loads, starting at integrated fluxes of about 4.4e14 n/cm^2 (2e14 p/cm^2) (MC40 data)



On-chip 3.3V regulators (IRRAD data and Triga):

OK at 2.4e15 n/cm^2 (4.7e15 p/cm^2)
OK at 7e15 n/cm^2

Fail at 2.9e15 n/cm^2 (5e15 p/cm^2)

Big difference between P and N irradiation (as expected from single device test). NIEL not working for this technology

Large (>2x) change of switching frequency with load

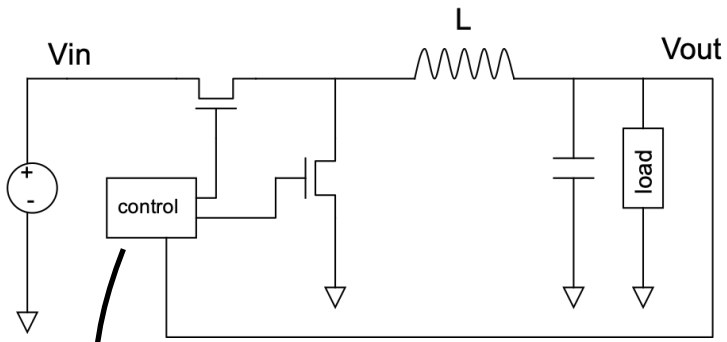
Change of OTP

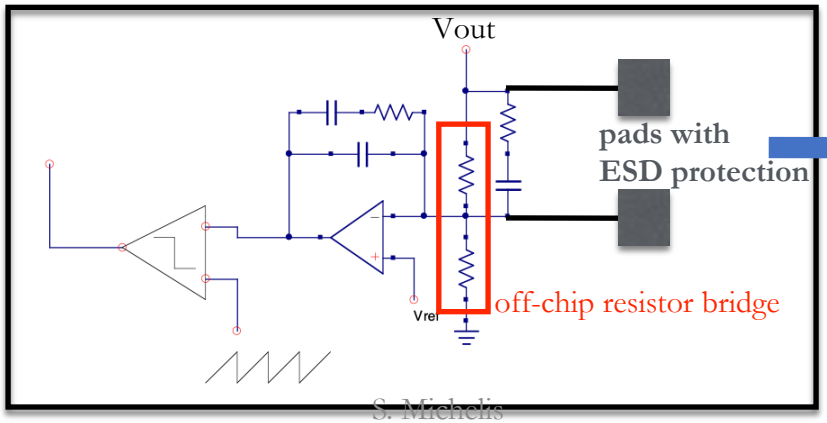
IRRAD facility at the CERN PS: 23GeV protons
Ratio of NIEL cross-section to 1MeV-equivalent neutrons: ~0.6
Many thanks to the IRRAD team (F.Ravotti, G.Pezzullo, …)

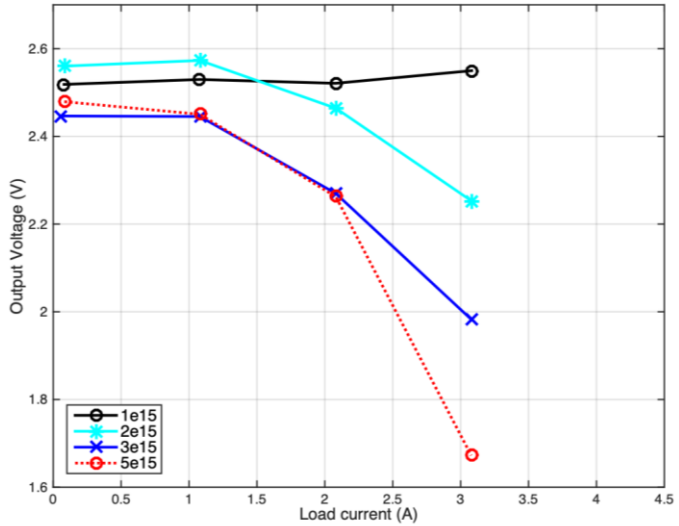
Cyclotron at the University of Birmingham (MC40): 25MeV protons
Ratio of NIEL cross-section to 1MeV-equivalent neutrons: ~2.2
Many thanks to the Birmingham team (L.Gonella and A.Hunter)

DD effects on bPOL12V – poor regulation

at large neutron integrated fluxes one of the bPOL12V versions showed unsatisfactory regulation at large loads.
This was wrongly interpreted at the beginning as switching noise from the substrate picked up by large wells in the feedback loop passive network.





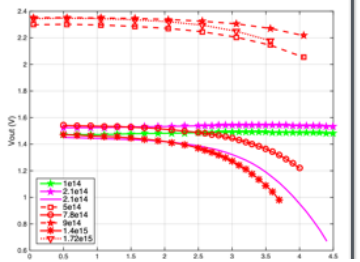


Sample exposed to 1-5e15 n/cm^2
(1MeV equivalent)

ESD elements and diodes protecting from plasma damage changed in V3 and V4

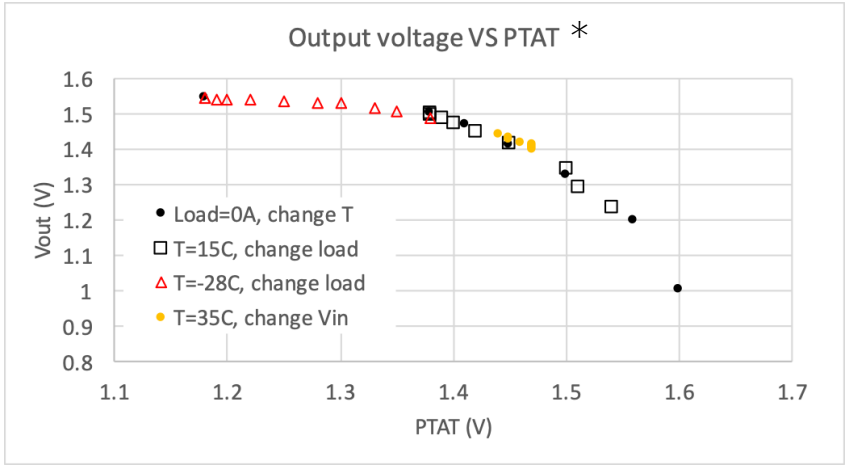
DD effects on bPOL12V – poor regulation

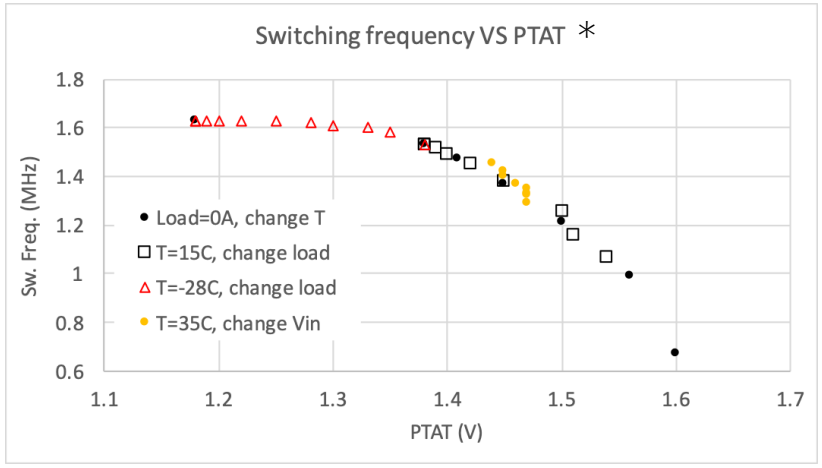
Poor regulation at large loads, starting at integrated fluxes of about 4.4e14 n/cm^2 (2e14 p/cm^2) (MC40 data)



Large (>2x) change of switching frequency with load

Real dependence from T, not from the load!



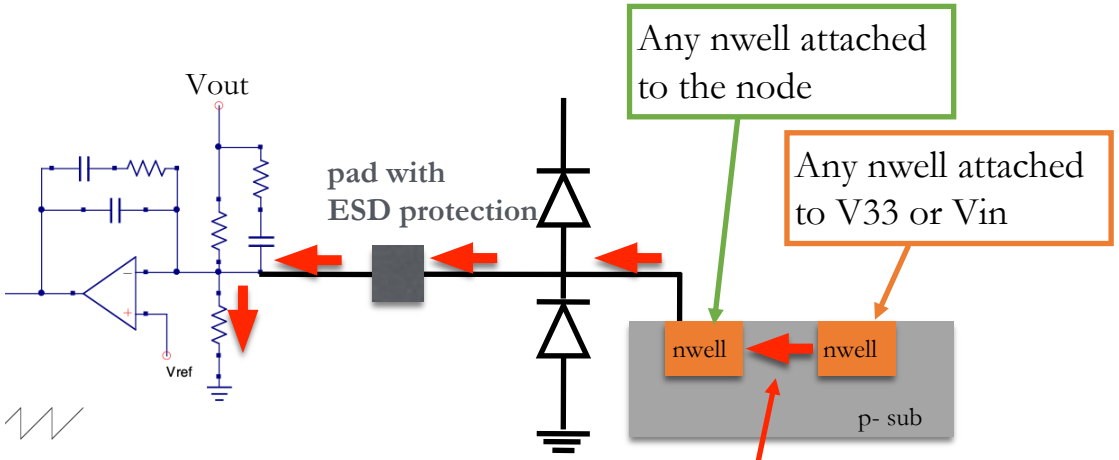


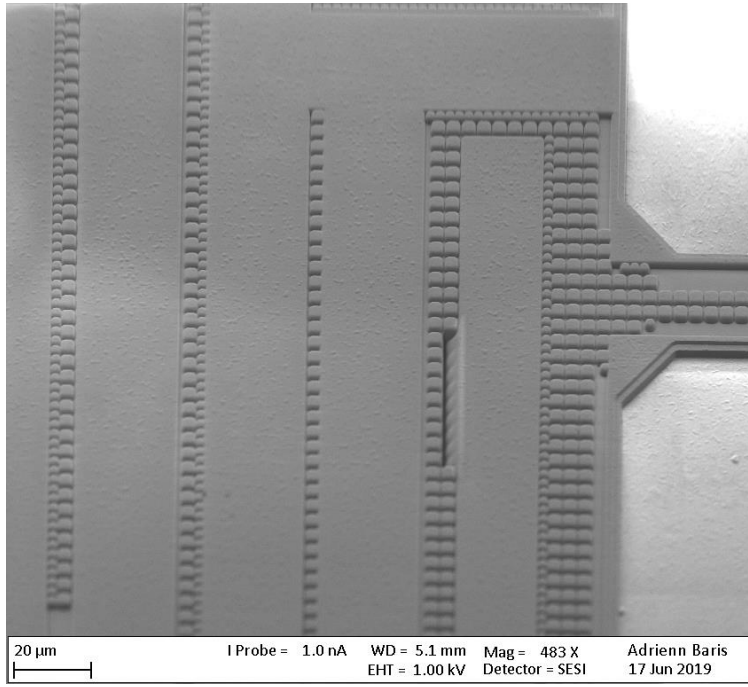
* The PTAT is the voltage output from an on-chip thermometer

Exactly same behaviour on Sw freq

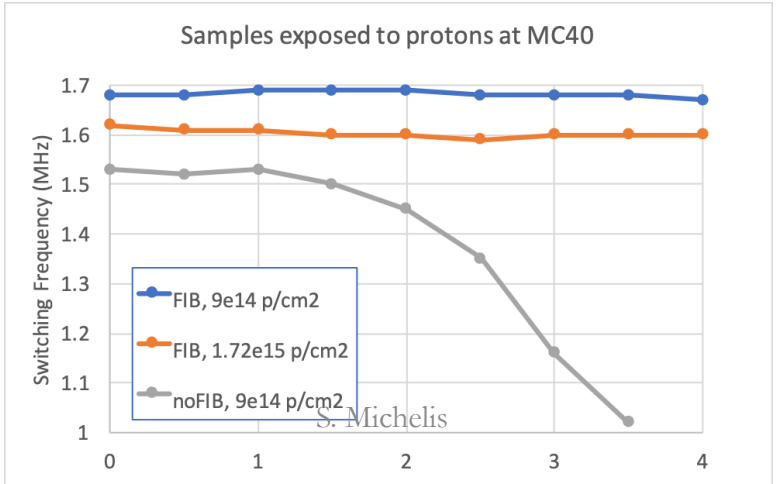
DD effects on bPOL12V – poor regulation

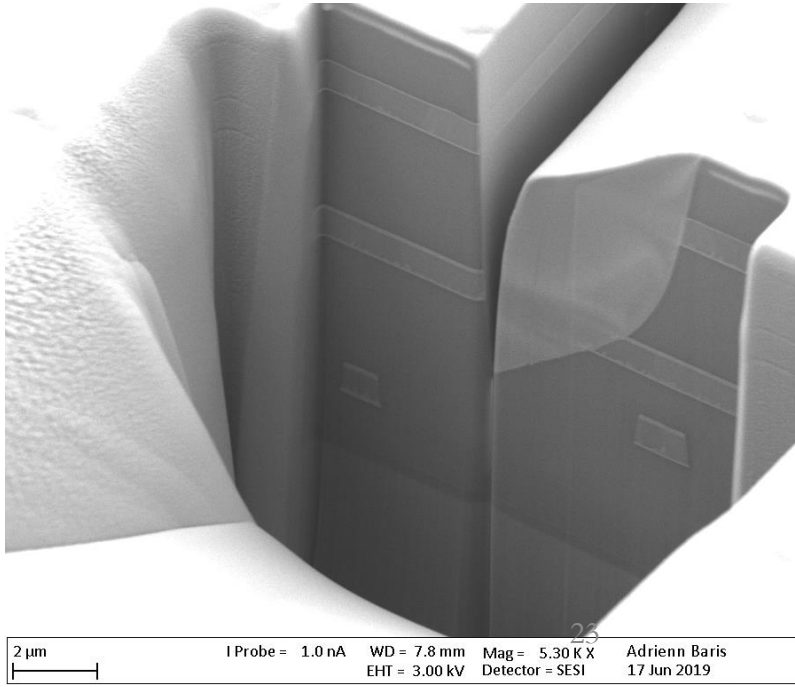
T-dependent currents flowing in the substrate seem to explain the observations





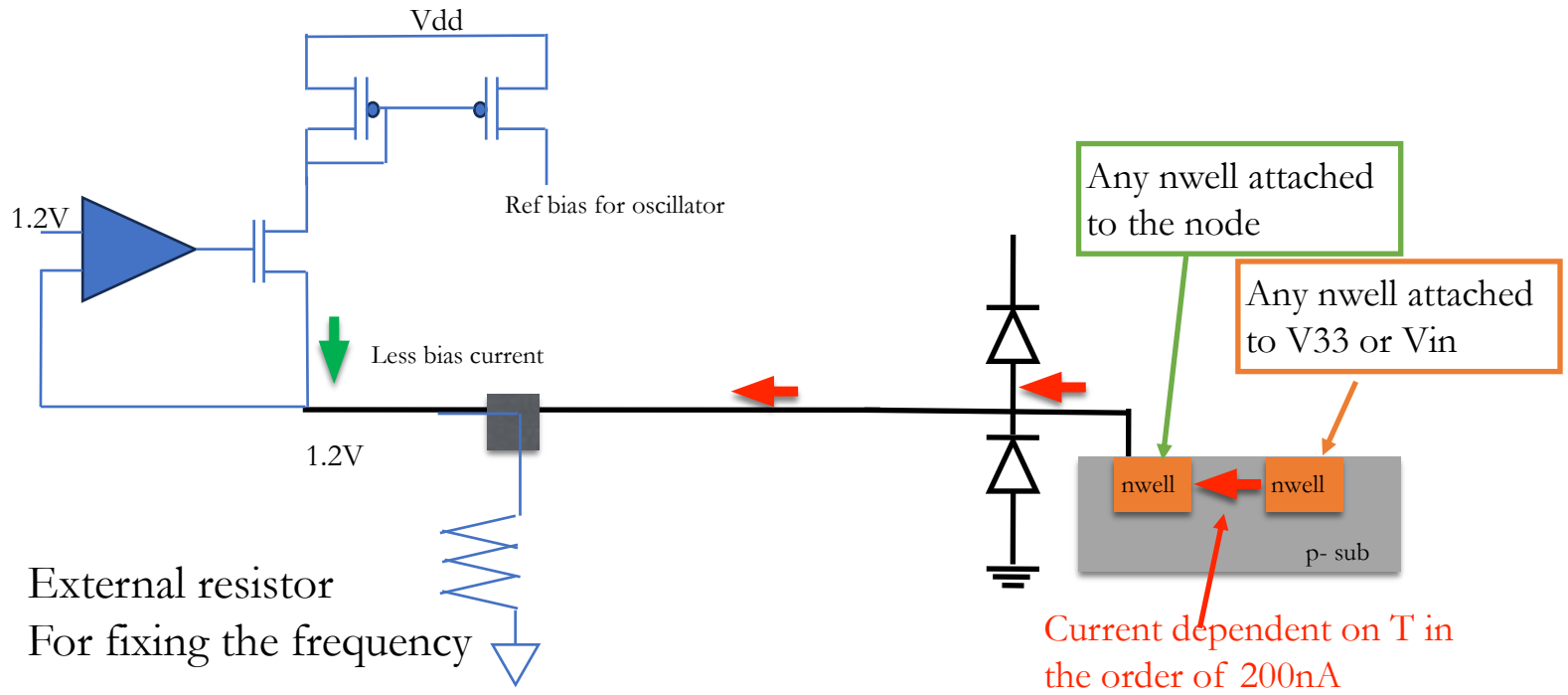
Removing with FIB the metal connection of the nodes to the nwell eliminates the symptoms!





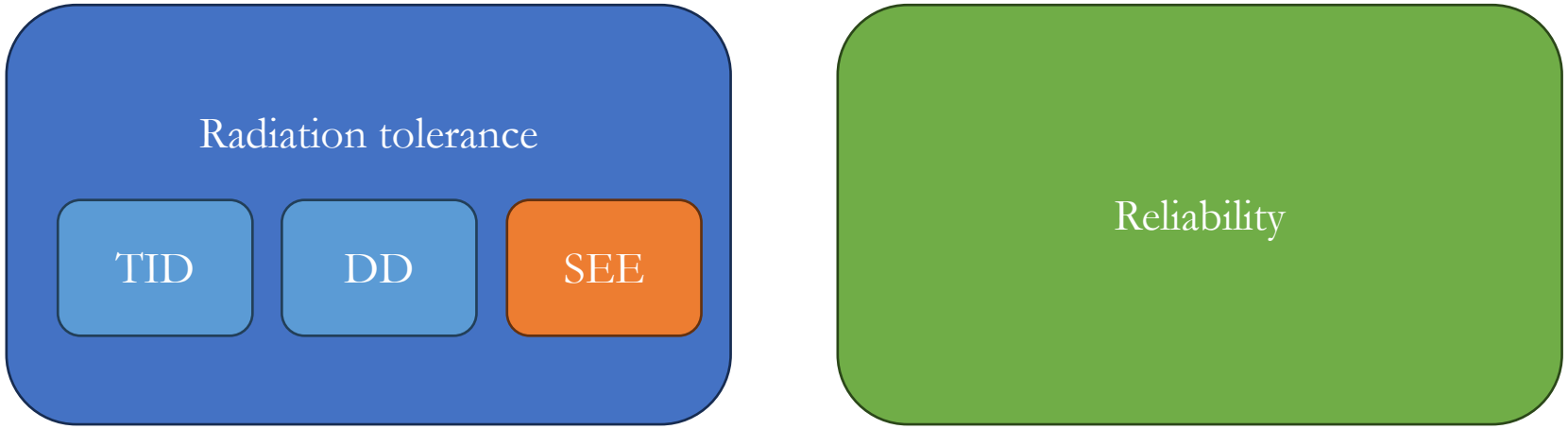
DD effects on bPOL12V – switching frequency change

Same isuue related to current coming from the substrate



Issue fixed decreasing the value of the resistor (factor 10) so the impact of the current injected is less important

Issues found during bPOL12V development

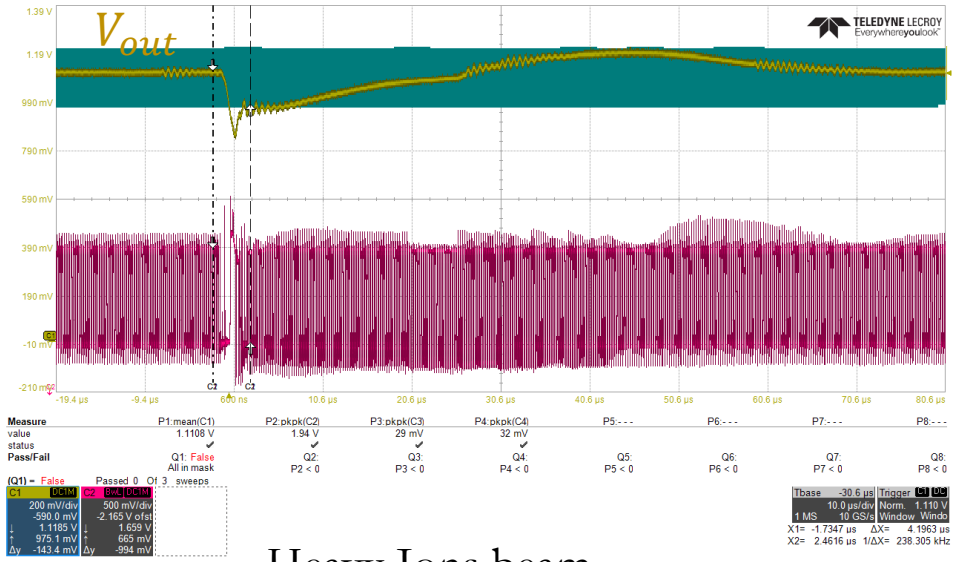


SEE in bPOL12V

The power ASIC suffered of little Single Event Effects (SEE) because we integrated the design techniques that we learnt from FEAST

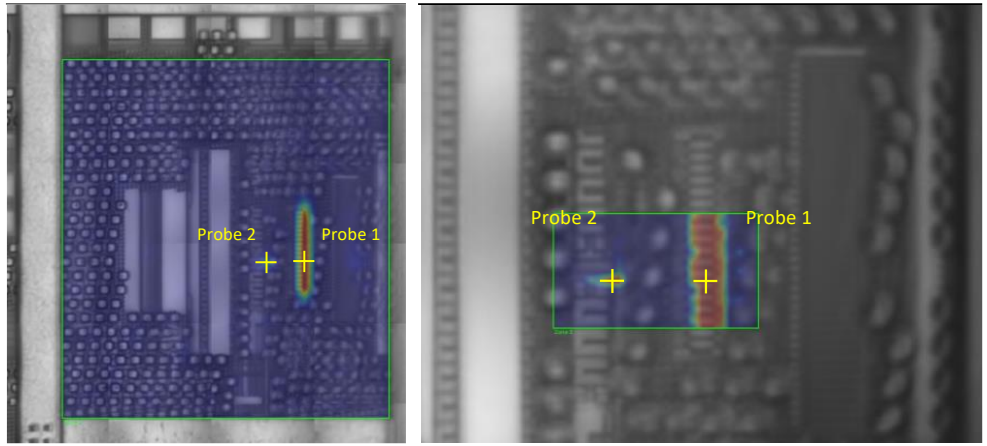
We found SEE issues on the BGP chip designed in 130nm (new chip)

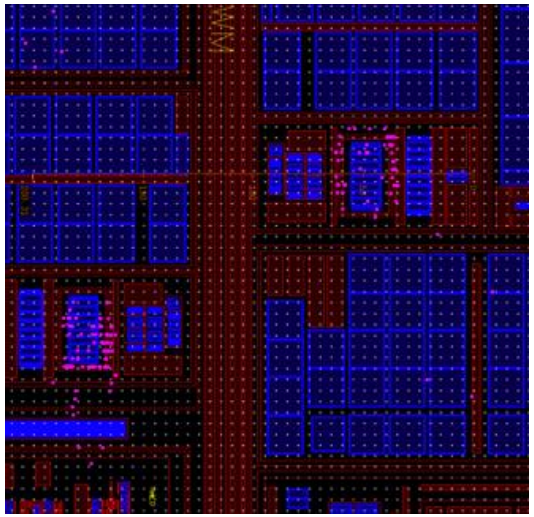
SEE issue on the BGP in 130nm



Heavy Ions beam
CRC Louvain la Neuve

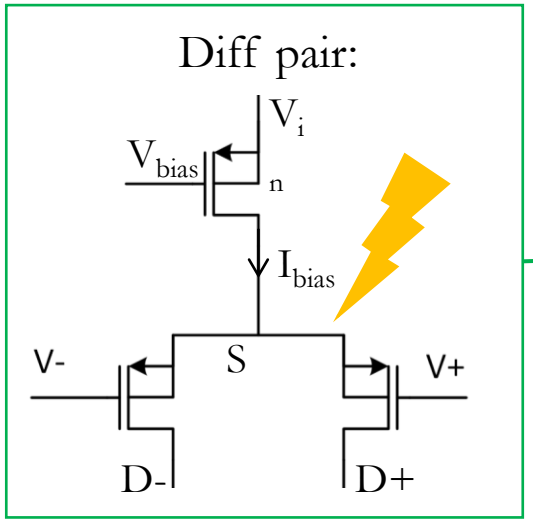
Laser beam in Pulscan

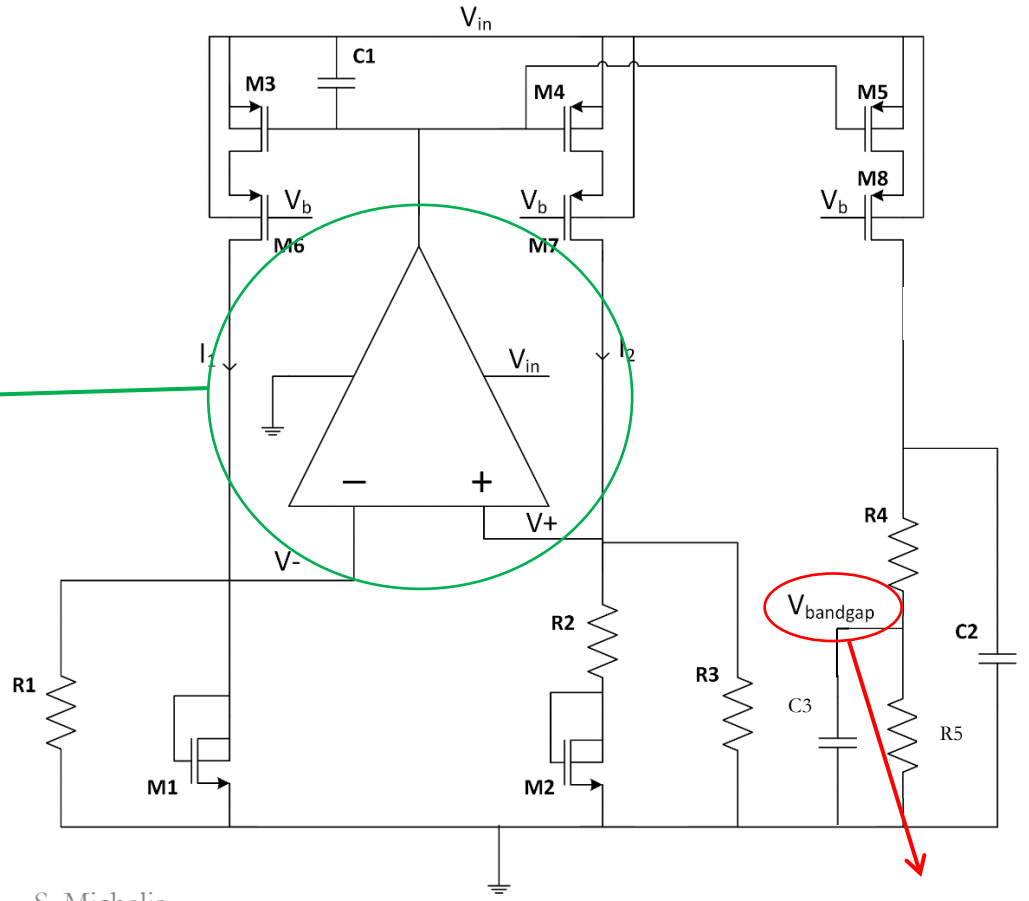


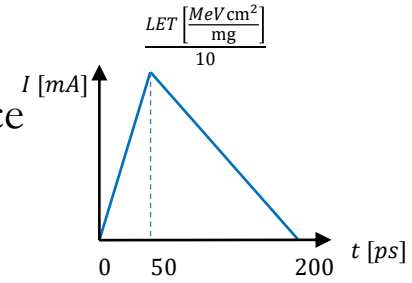


Focused Heavy Ions beam
GSI

SEE sensitive cell identified

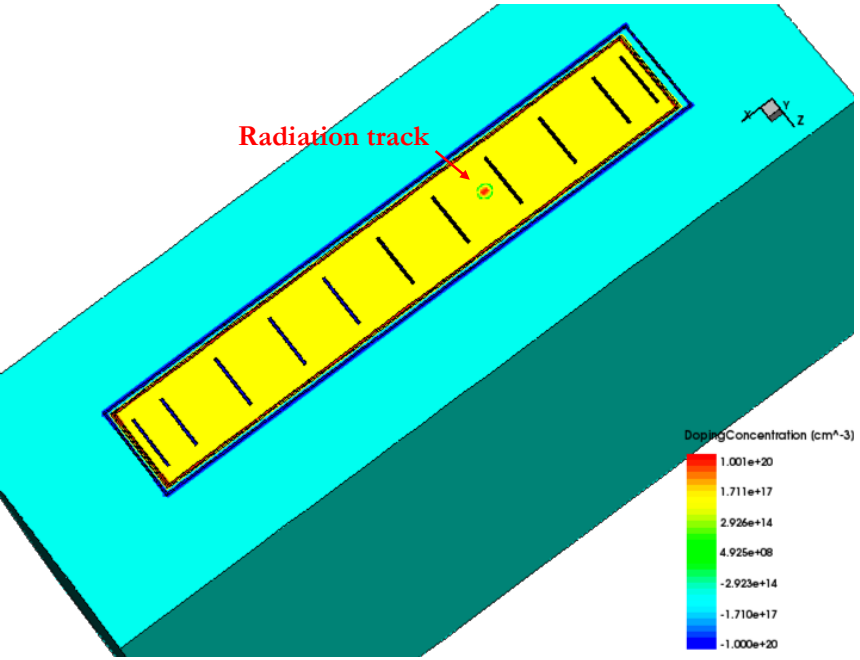


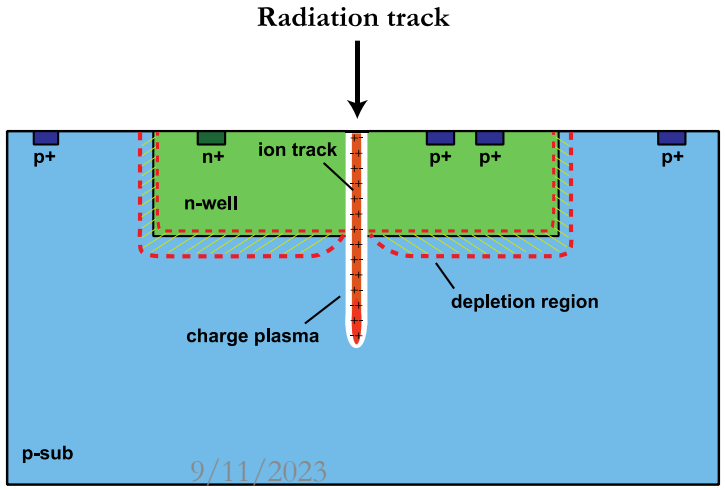


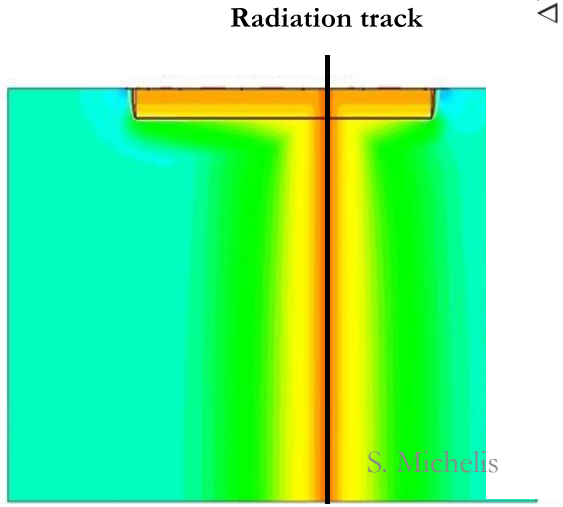


"usual" simulation does not reproduce what we see during testing

SEE simulation with TCAD

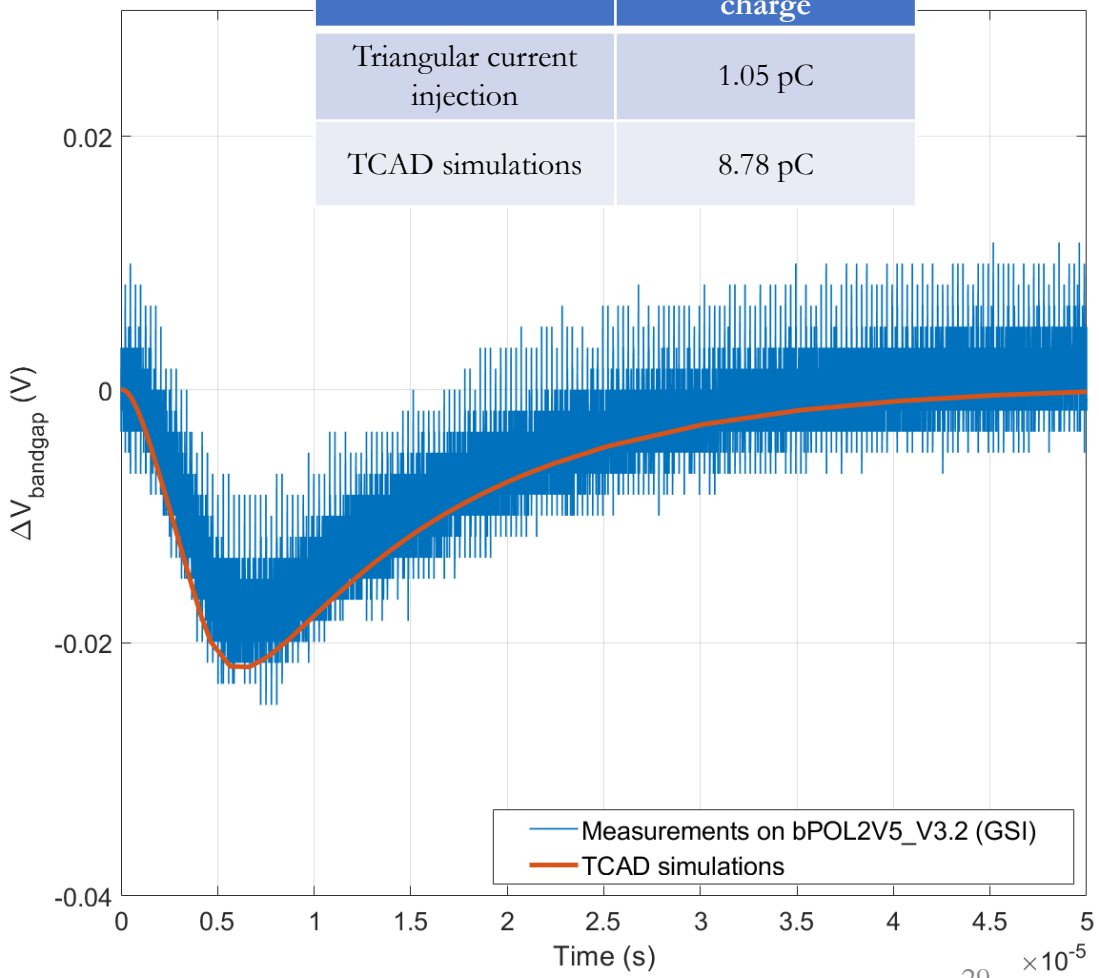






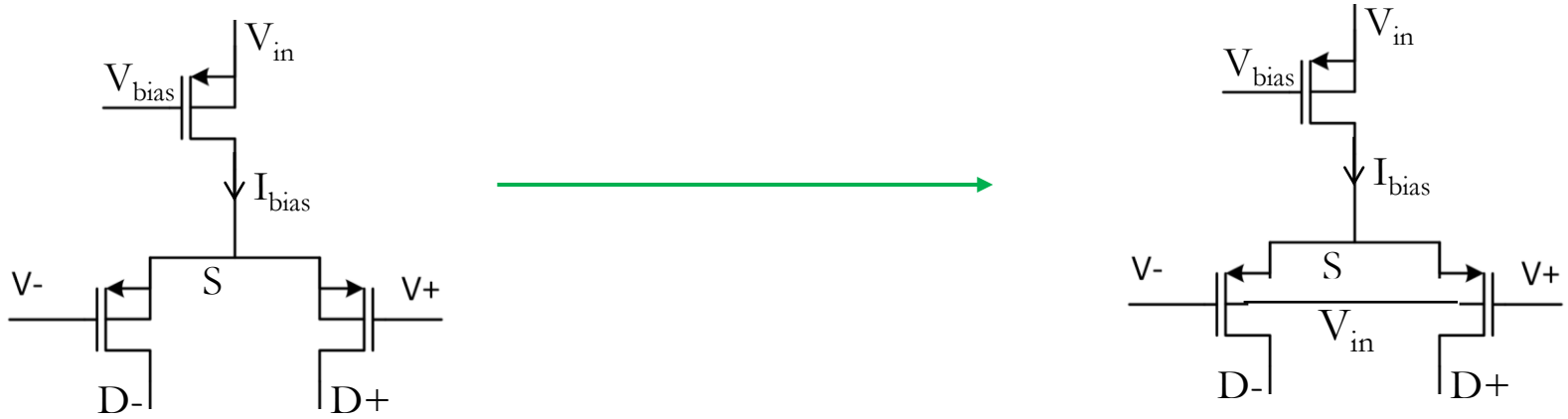
The injected charge is much higher than the usual simulated charge.

	Total collected charge
Triangular current injection	1.05 pC
TCAD simulations	8.78 pC



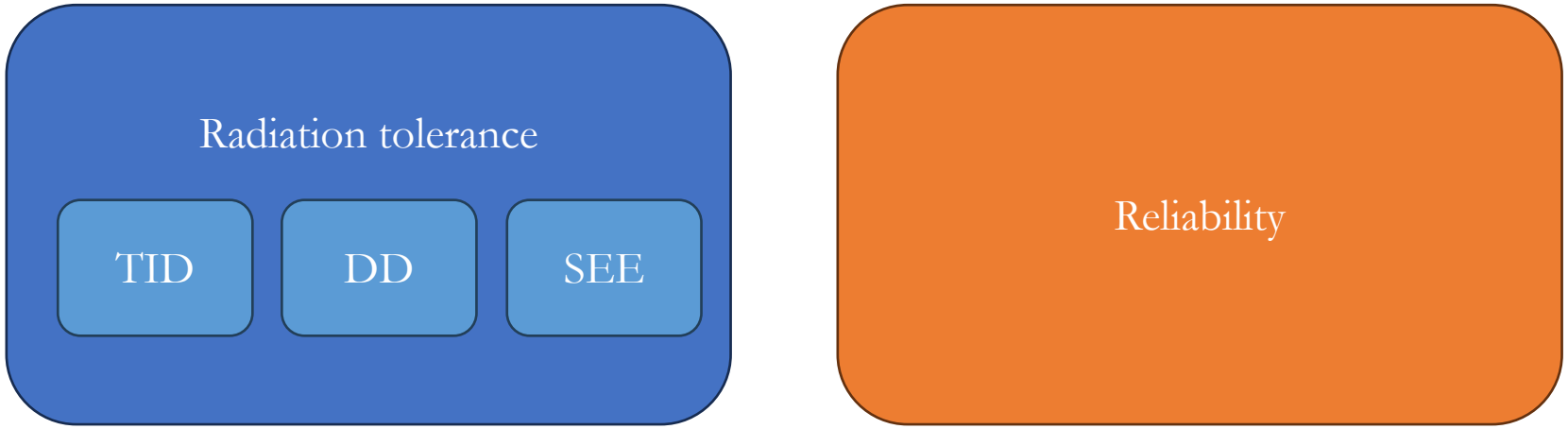
SEE issue on the BGP in 130nm: solutions

All BGP+voltage followers differential pairs



And add an RC the output to mitigate noise and possible additional transient. Better to be prudent!!!

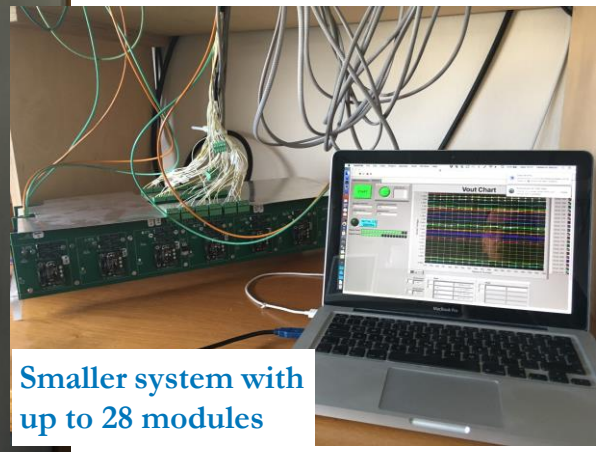
Issues found during bPOL12V development



Extensive reliability tests have been performed on bPOL12V over years

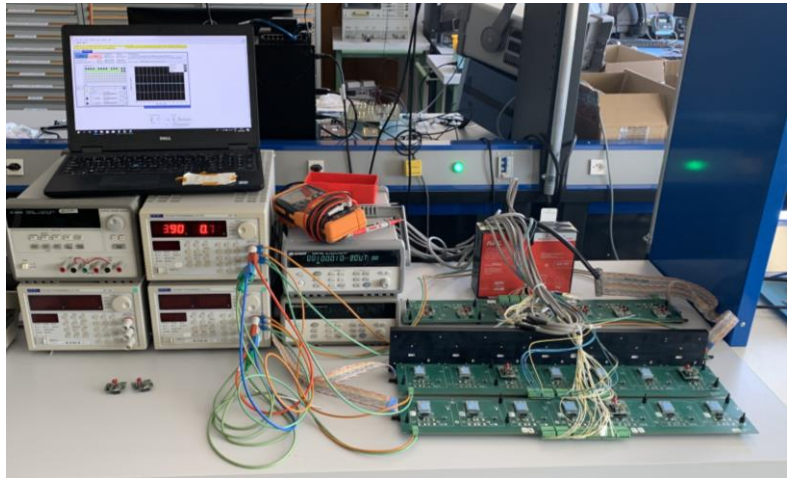
Long-term stress tests: samples kept in or beyond operating conditions for months (the longest run has lasted for ~ 2 year)

2 “Crate96” systems, each hosting up to 96 modules



Smaller system with up to 28 modules

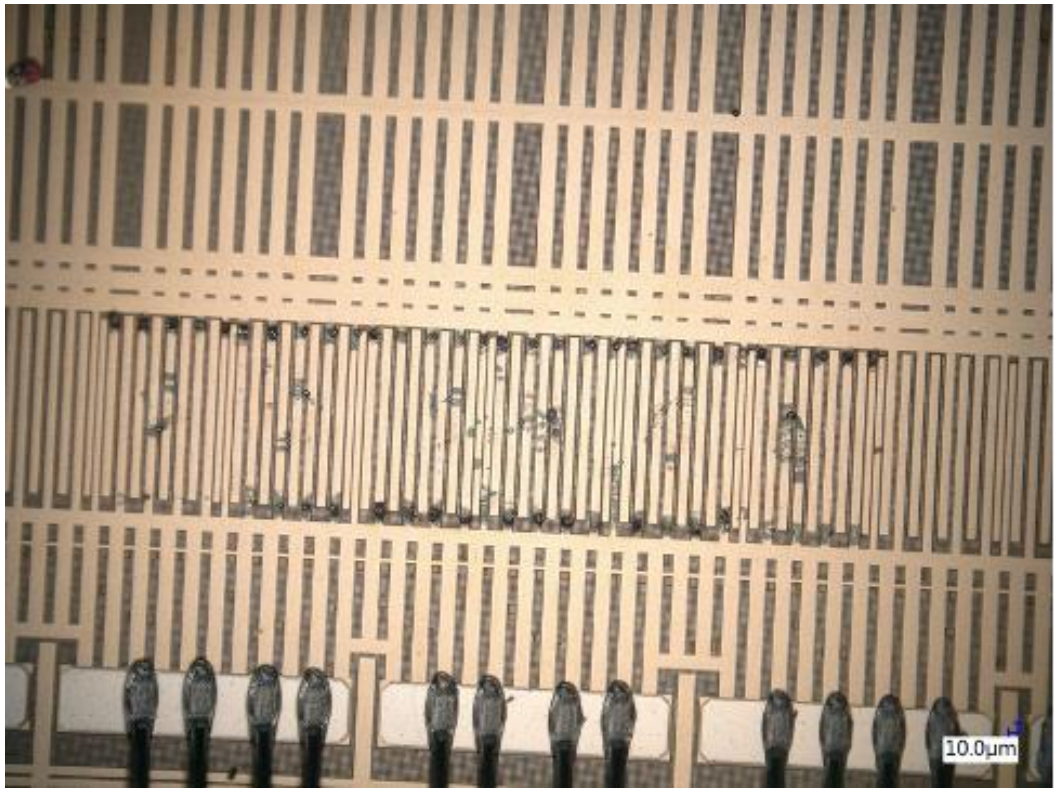
Accelerated stress tests: up to 28 samples stressed at high voltage



Reliability tests at low temperatures with 24 modules

Setup hosting up to 8 modules for additional reliability tests

Very bad results on V5



How do you tackle a problem like this?

We have been working over almost 1 year to have the problem fixed, using:

- hundreds of converters,
- Two racks
- Climate chambers
- Very sophisticated failure analysis tools (EMMI + Obirch= Photon Emission Microscopy)

First of all: you really want to kill them to find a pattern

Different reliability test runs records

Different :

Vout
Sw. frew
load
Inductor

Temp

Current pk-pk

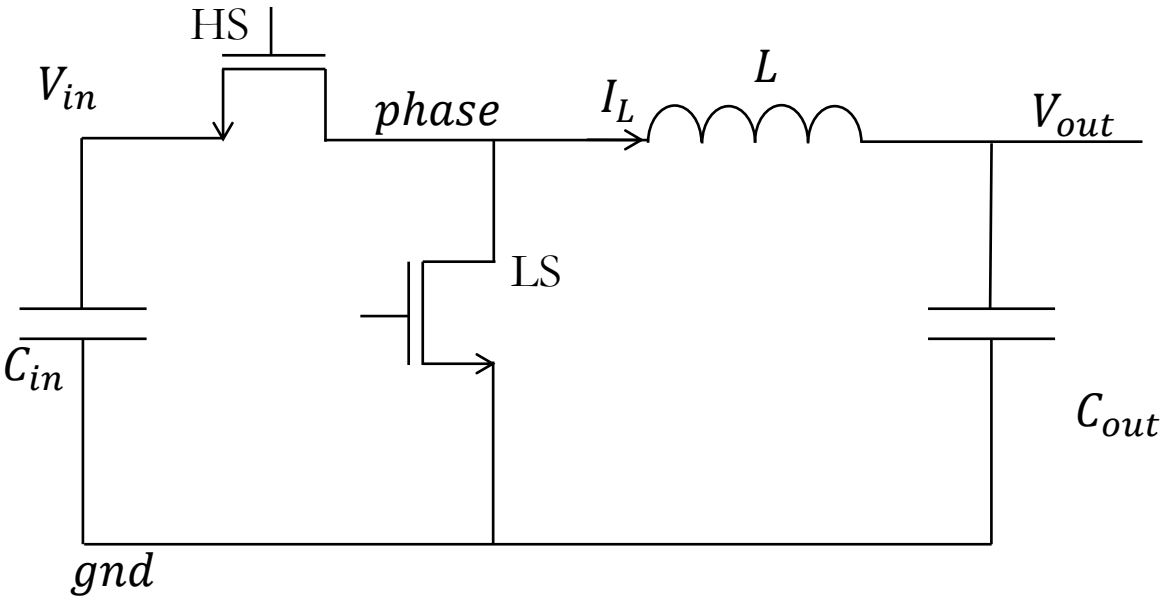
	Run in racks							Run at 3rd flloor		Runs in climatic chamber											
	1st run				2nd run			1st run		1st run		2nd run				3rd + 4th run					
	C2.5V_3.75A	C1.5V_3.75A	C2.5V_0A	C1.5V_0A	C2.5V_2A	C1.5V_2A	C2.5V_2A_HR	C2.5V_3.75A	C1.5V_3.75A	C2.5V_3.75A	C1.5V_3.75A	C2.5V_3.75A Rboot	C1.5V_3.75A Rboot	C2.5V_3A_HR	C2.5V_3A_LR	C2.5V_3.75A Rboot	C1.5V_3.75A Rboot	C2.5V_3A_HR	C2.5V_3.75A_LR	C2.5V_3A_HR Rboot	C2.5V_3.75A_LR Rboot
Vout (V)	2.5	1.5	2.5	1.5	2.5	1.5	2.5							2.5	2.5				2.5		
Fsw (MHz)	2.50	1.80	2.50	1.80	2.50	1.80	1.80							1.80	3				3		
Iout (A)	3.75	3.75	100m	100m	2	1.95	2							3	3				3.75		
L (nH)	220	460	220	460	220	460	220							220	1380				1380		
# conv	24	24	24	24	32	32	32	4	4	4	4	2	2	2	2	4	4	4	4	4	4
T	5-25days 85-90 C		5-25days 60 C		11d 42 C 8d 80 C 12d 90-115 C			1d 7V 90C 6d 7V 100C 6d 8V 100C 7d 9V 100C 6d 10V 100C		4days 40C 11V		~10 days 25C				5+5days 25C					
Delta I (A)	3.51	1.56	3.51	1.56	3.51	1.56	4.88							4.88	0.47				0.47		
Ipk (A)	5.5	4.53	1.85	0.88	3.76	2.78	4.44							5.44	3.23				3.98		
Ivalley (A)	2	2.96	-1.65	-0.68	0.24	1.21	-0.43							0.63	2.76				3.51		
Failure #	22 11 hard fails HS 11 soft fails HS		0		0			1 soft fail HS, 8V in first 20min		3 hard fails HS 2x1.5V, 1x2.5V		0 dead, only OCP change in High Ripple				3 hard fails HS in LR without Rboot only OCP change in High Ripple without Rboot					

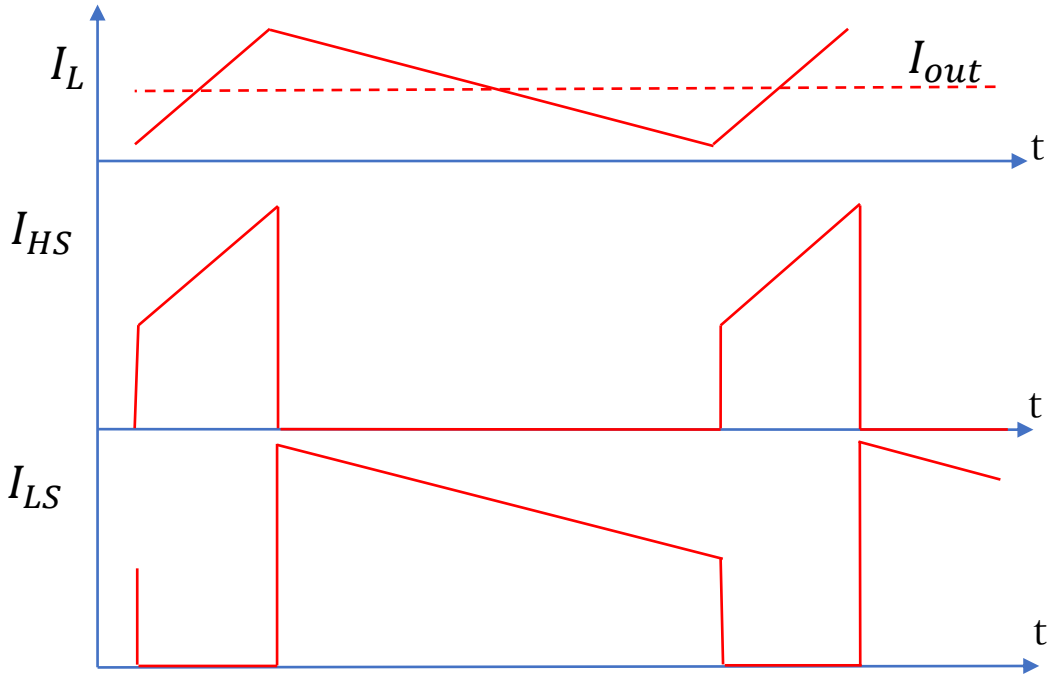
Surprise surprise: 2 damages

We discovered not only one issue, but two types of failure/damage:

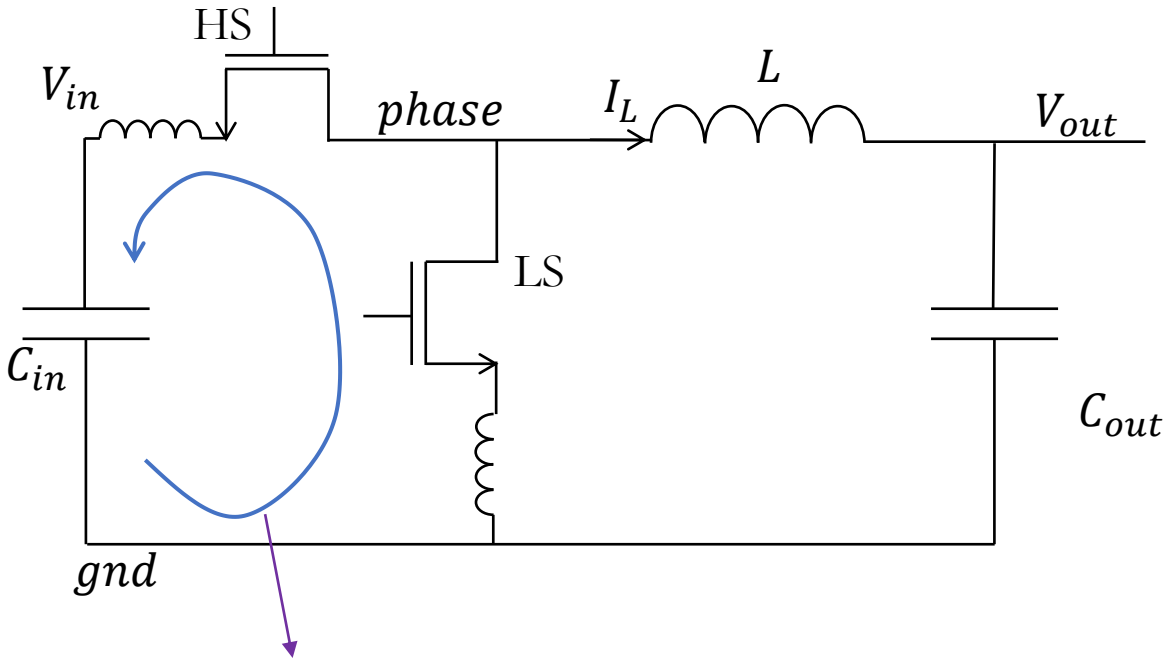
- hard failure with the bPOL12V_V5 stop working (often with visible bubbles on the High Side transistor)
- soft failure with the converter still running but with an increased input current. This current was increasing during time, as an evolving damage.

Buck Converter operation

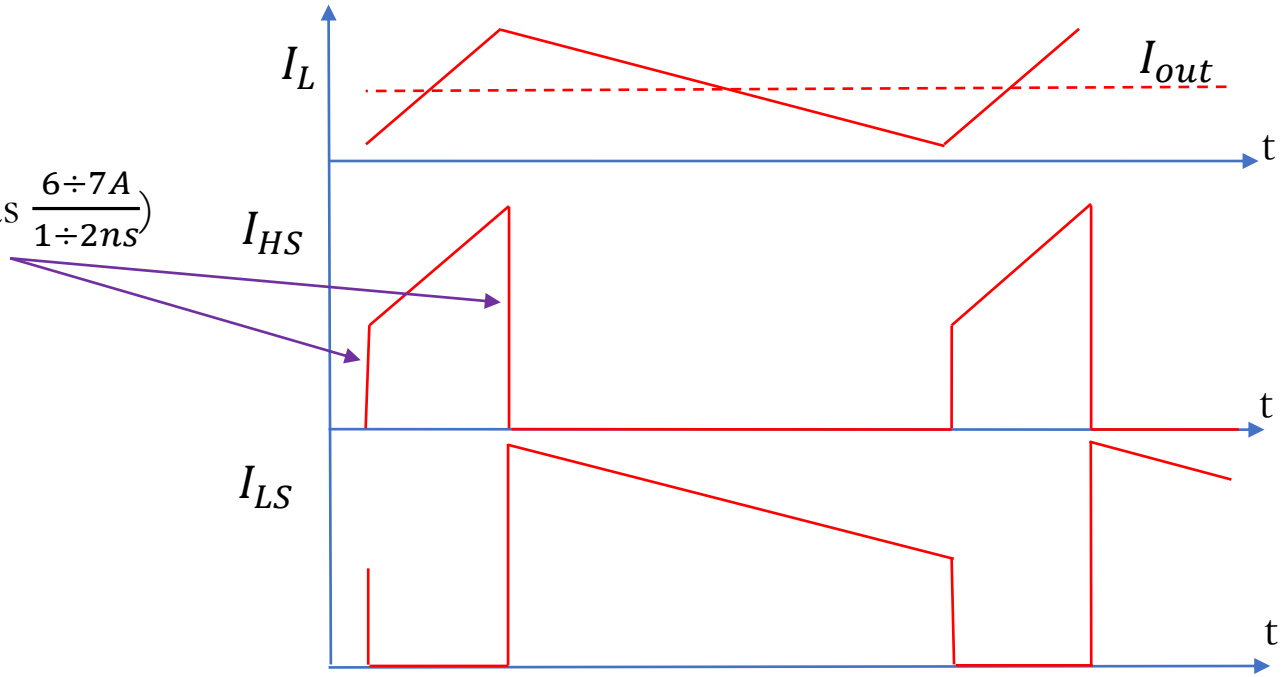




Buck Converter operation



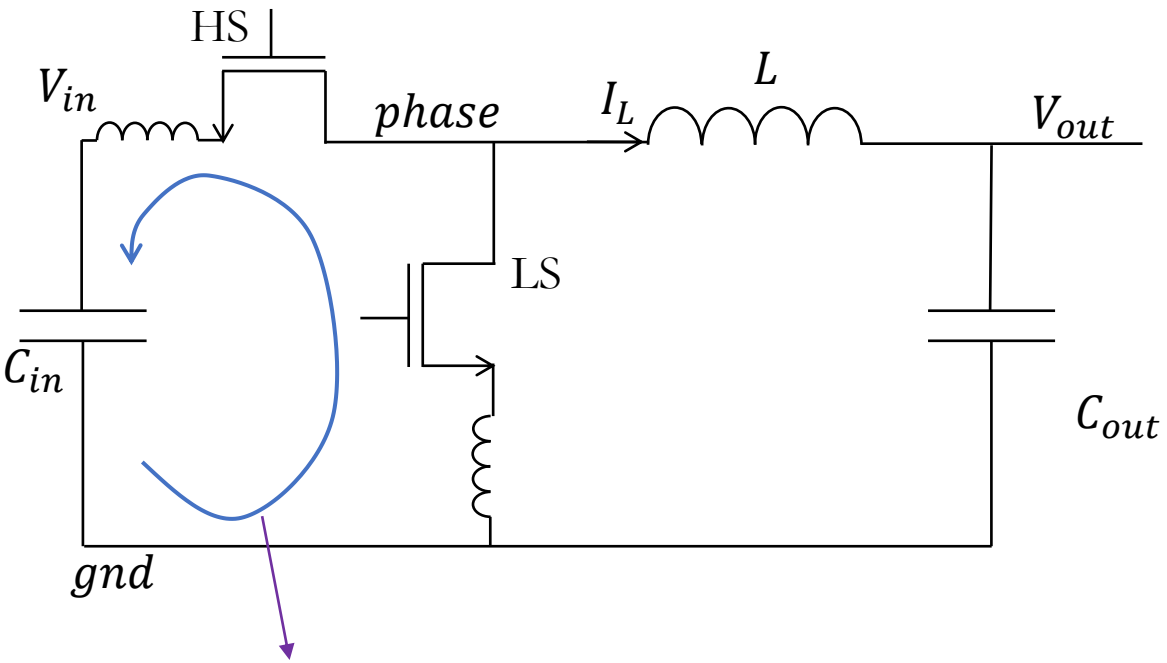
Large $\frac{dI}{dt}$
(as high as $\frac{6 \div 7A}{1 \div 2ns}$)



The current is exchanged between HS and LS through this loop. The loop series parasitic inductance L_{par} leads to overvoltages ($V_{ds,max} \approx V_{in} + L_{par} \cdot dI/dt$).
Contributions to L_{par}:

- Bonding
- PCB
- Input capacitor ESL

Buck Converter operation



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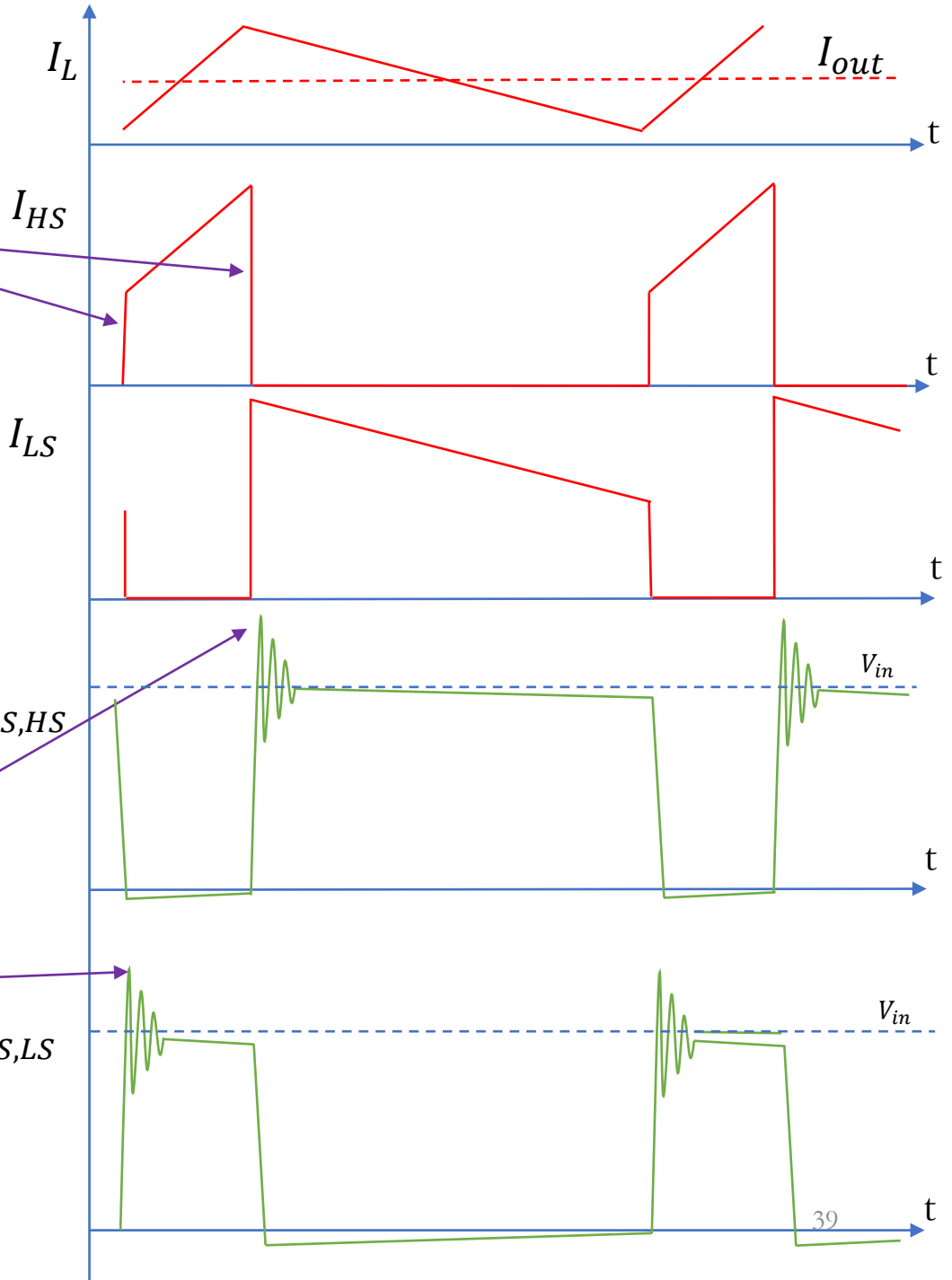

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- Bonding
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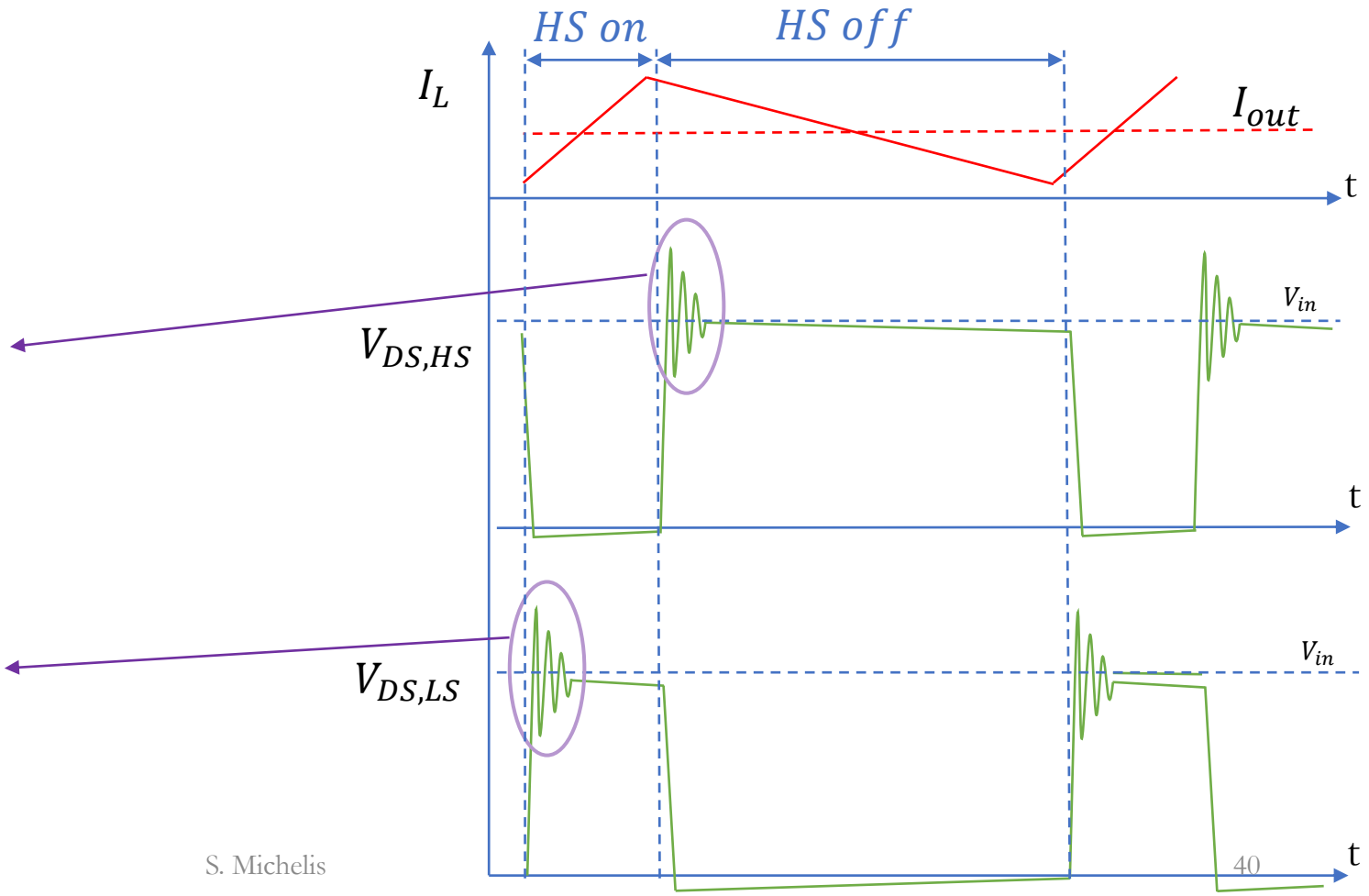
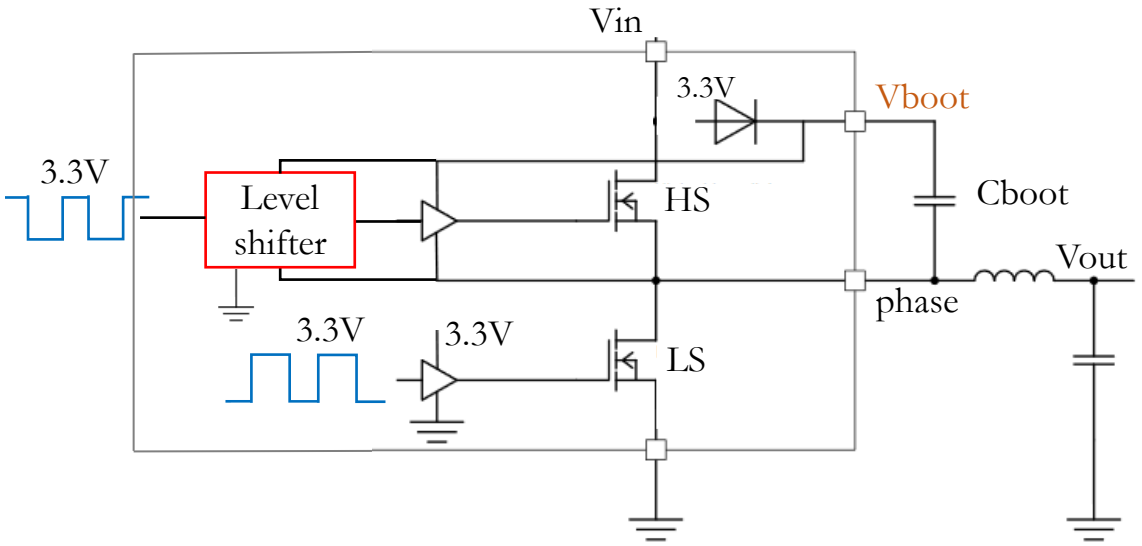
Causing:

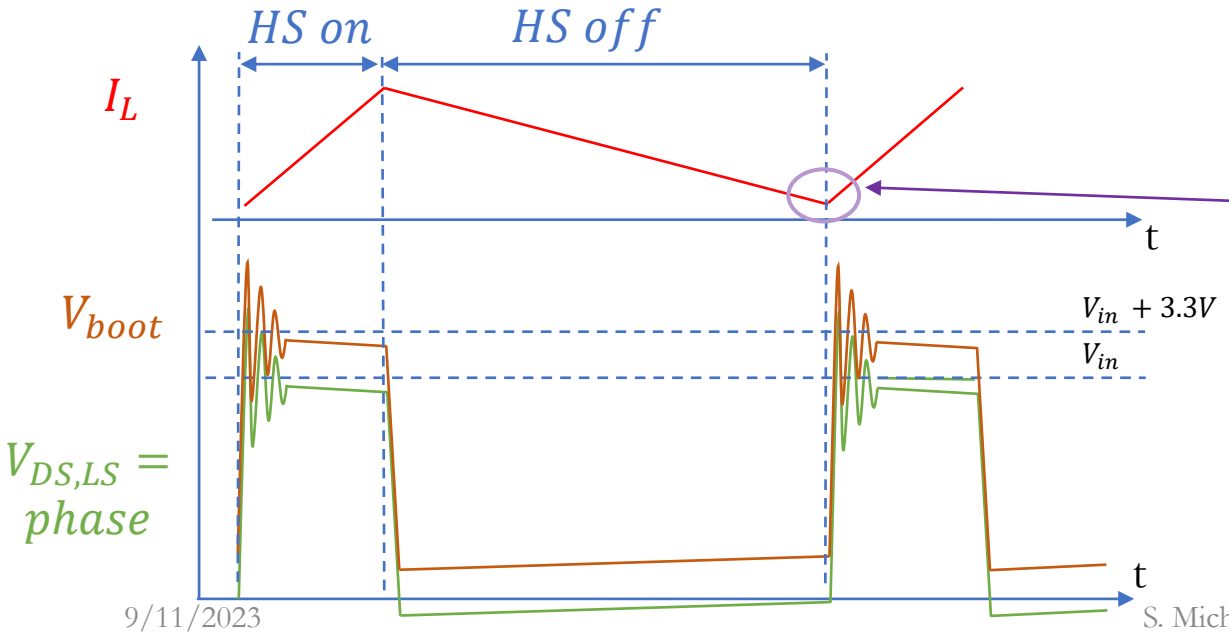
HARD FAILURE

SOFT FAILURE



Hard failure: Level shifter failure (1/4)



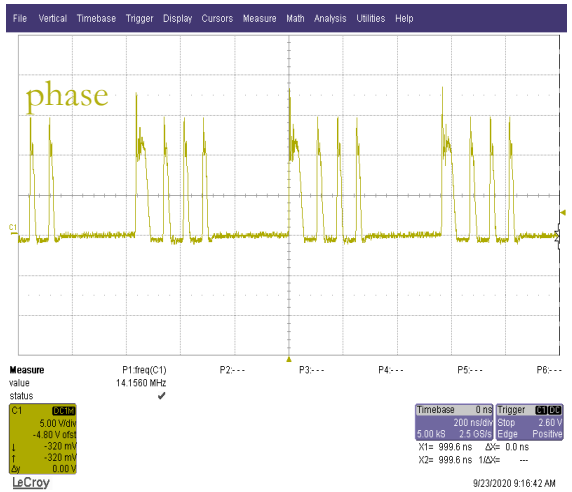


It has been found that two transistors in the level shifter experience a maximum V_{ds} of $V_{boot} \approx phase + 3.3V$.

When turning on HS, V_{boot} can exceed the breakdown voltage ($\sim 16\ V$), leading to the failure of the level shifter.

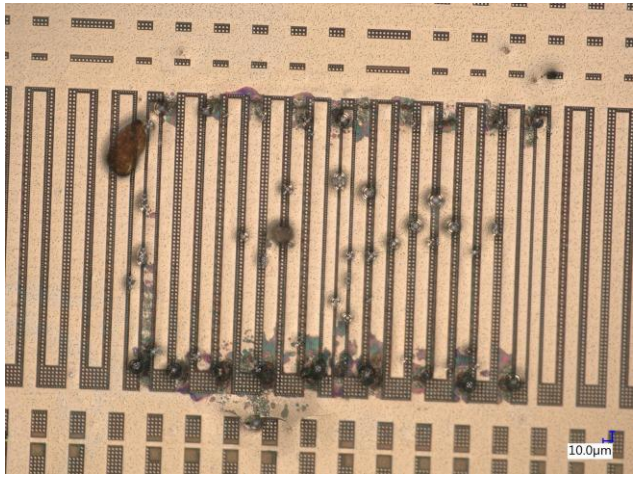
This damage occurs faster for higher V_{in} and higher valleys of I_L.

Level shifter failure (2/4): symptoms



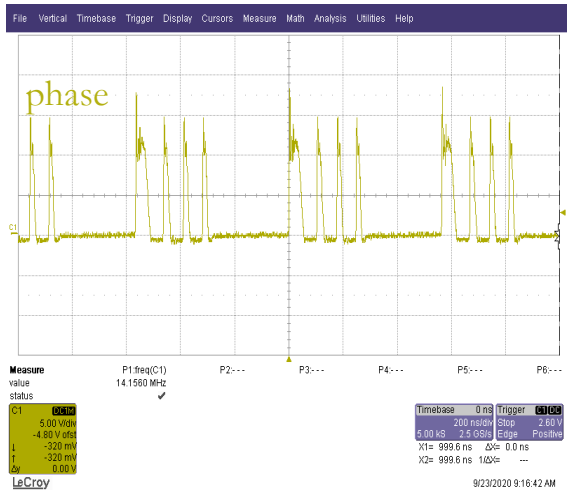
First symptom: anomalous switching behavior

If left on, it can evolve into…



Hard failure (visible damage on HS, the converter stops switching)

Level shifter failure (2/4): symptoms



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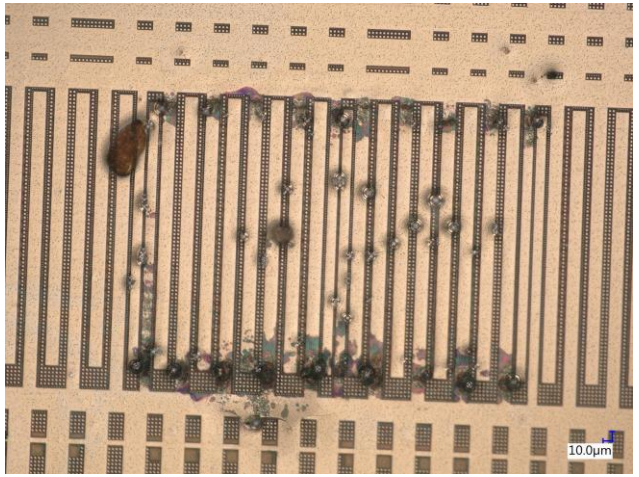
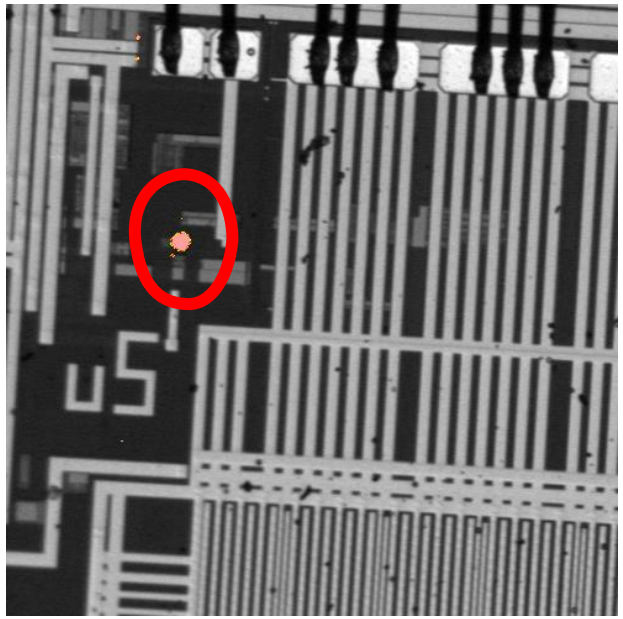


Hard failure (visible damage on HS, the converter stops switching)

Level shifter



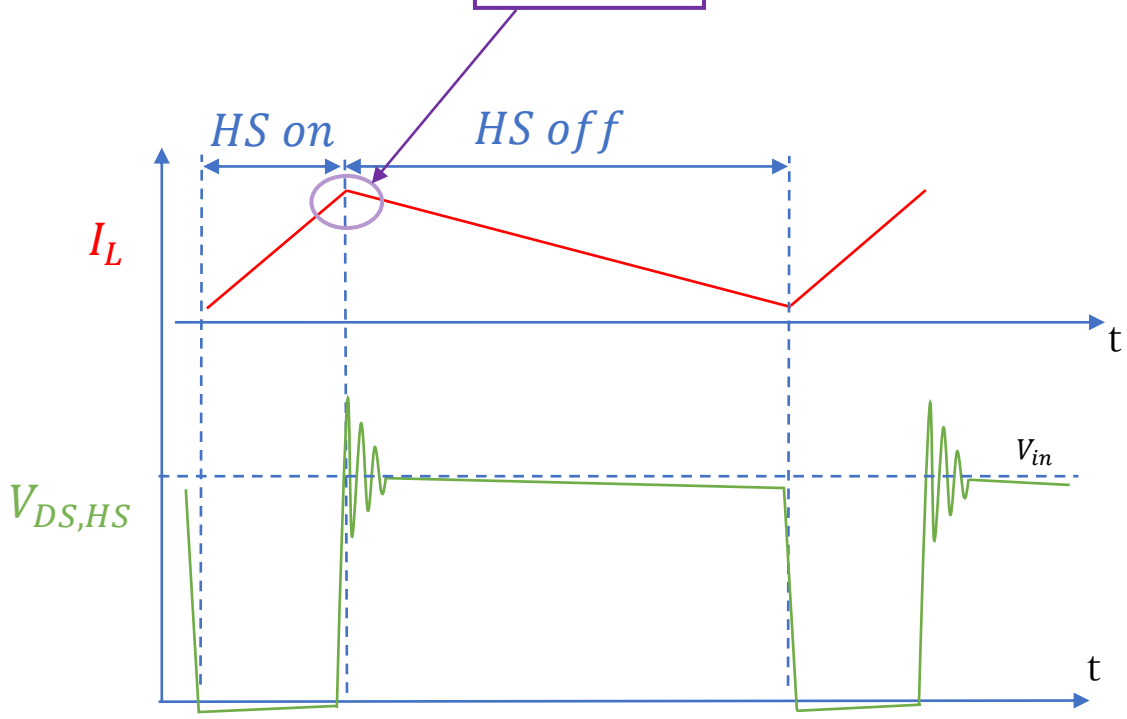
Emission Microscopy (EMMI) failure analysis (performed at Advanced Silicon, Lausanne) confirmed that the damage is localized in the level shifter

HS soft failure (1/2)

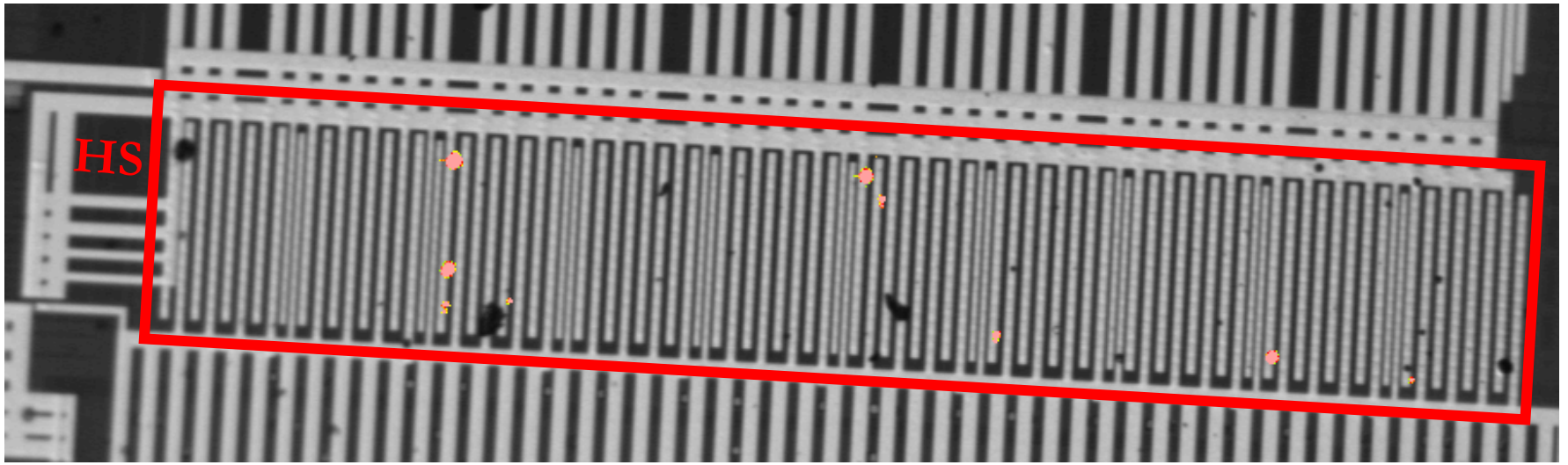
When the HS switch is turned OFF, the overvoltage on $V_{DS,HS}$ can damage the device.

The resulting damage is what we call an *HS soft failure*: the converter is still functional, but the leakage current of HS is increased by a few mA.

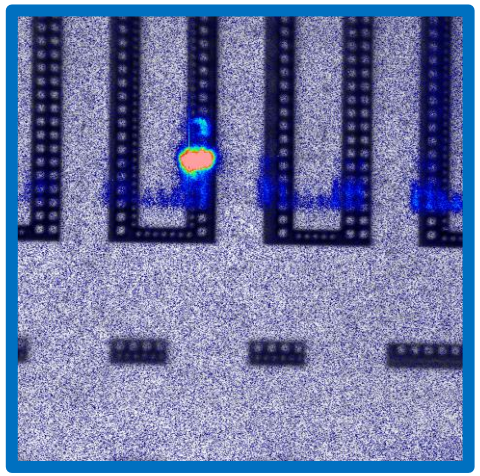
The damage occurs faster for higher V_{in} and higher peaks of I_L.



HS soft failure (2/2)



Magnified view



EMMI failure analysis confirmed that the damage is localized in the HS switch.

Implemented solution (ASIC):

The turning OFF of the HS switch has been slowed down, in order to decrease the overvoltage (lower dI/dt)

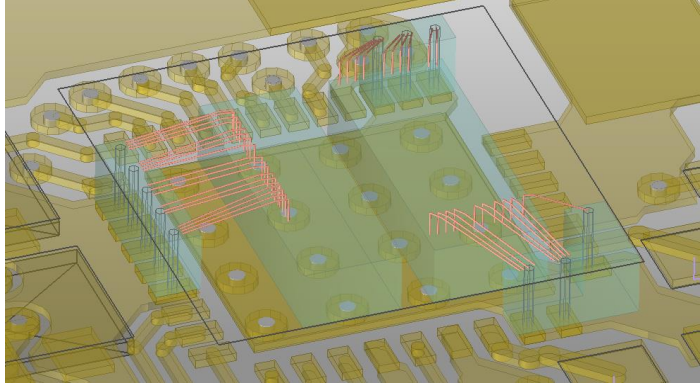
Reliability conclusions

Failure type	Conclusion from the testing campaign	Actions (ASIC)	Actions (PCB)
Hard fail	Overvoltages occurring HS turning ON (level shifter damage)	1. The level shifter has been redesigned 2. Slower turn-on to reduce dI/dt	To further reduce the voltage stress, PCB layout strategies have been devised to reduce the value of the input parasitic inductance L_{par}. We must ensure that the value of L_{par} is well controlled in all the modules that use bPOL12V.
Soft fail	Overvoltages occurring HS turning OFF (HS damage)	Slower turn-off to reduce dI/dt	

All implemented in V6

A reliable operation of bPOL12V requires a well-controlled input parasitic inductance L_{par}.

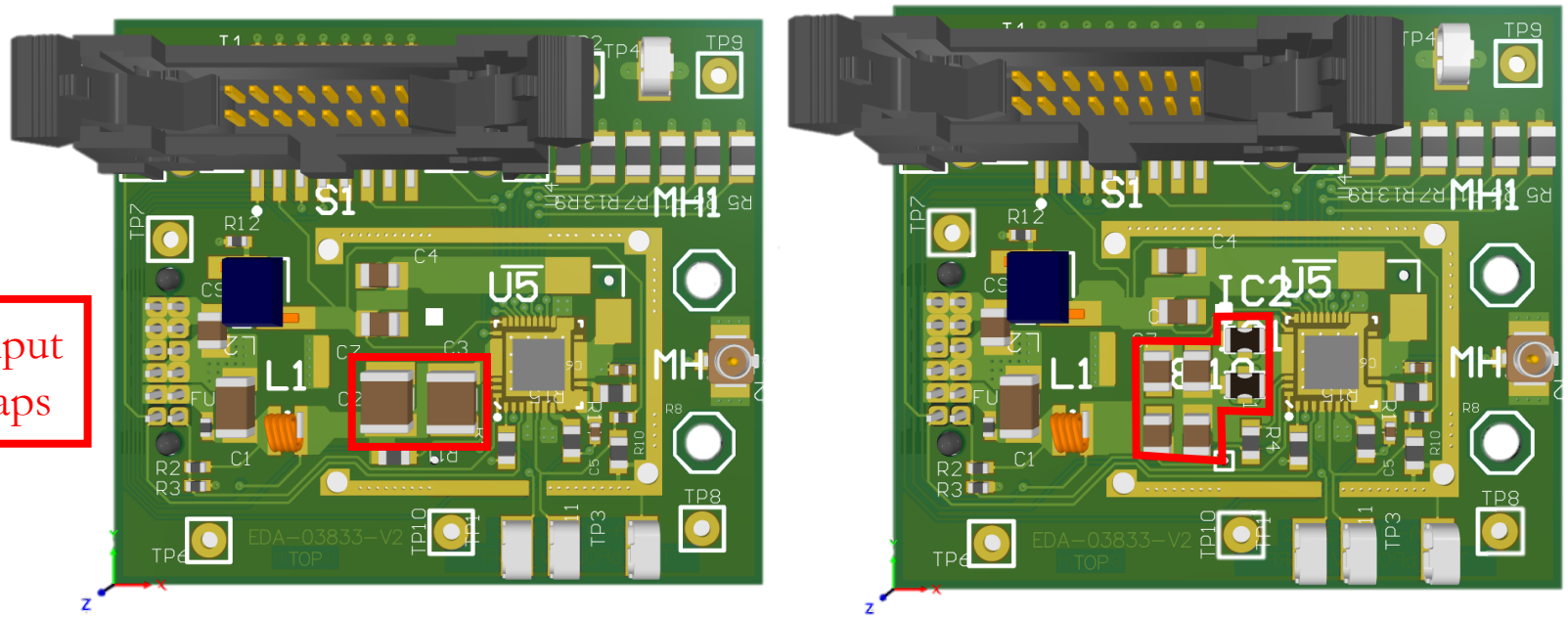
L_{par} has been extracted using SIWave (considering PCB, bond wires and input capacitors), and strategies have been devised to minimize it.



Original test PCB

Optimized PCB

Input caps



Extracted L_{par}	Original dielectric thickness ($300\mu m$)	$50\mu m$ dielectric
Original input caps	$1.22nH$	$0.72nH$
Improved input caps (low-ESL)	$0.70nH$	$0.44nH$

From prototyping to final production

Prototyping has been a long journey with plenty of issues

FEAST (legacy converter)

July2015

V1: change of technology,
re-design of all HV part with 25V LDPMOS

Substrate noise

Feb2016

V2: larger noise from substrate in V1, higher than FEAST. Increase of distance control-power
improve PSRR- and PSRR+ of BGP, BGPHV + lin reg. Increase of OTP and OCP th for TID
Power good comparators changed

March2017

V3: change of oscillator (picking-up noise from substrate)
change of BGP to DTNMOS
startup change in HV BGP

BGP TID Issues

Dec2018

V4: added change of Vout config bit for Atlas, added compatibility with external BGP
Increase OCP for DD, Increase UVLO limit for CMS
Change of HS drivers (slower), Added testmode for production testing

DD+SEE Issues

Jan2020

V5: Change ESD protections for Vout and Rf for DD Back fast drivers,
Change pull-down resistor Enable pin, Increase clamp on phase

Reliability Issues

Jan2021

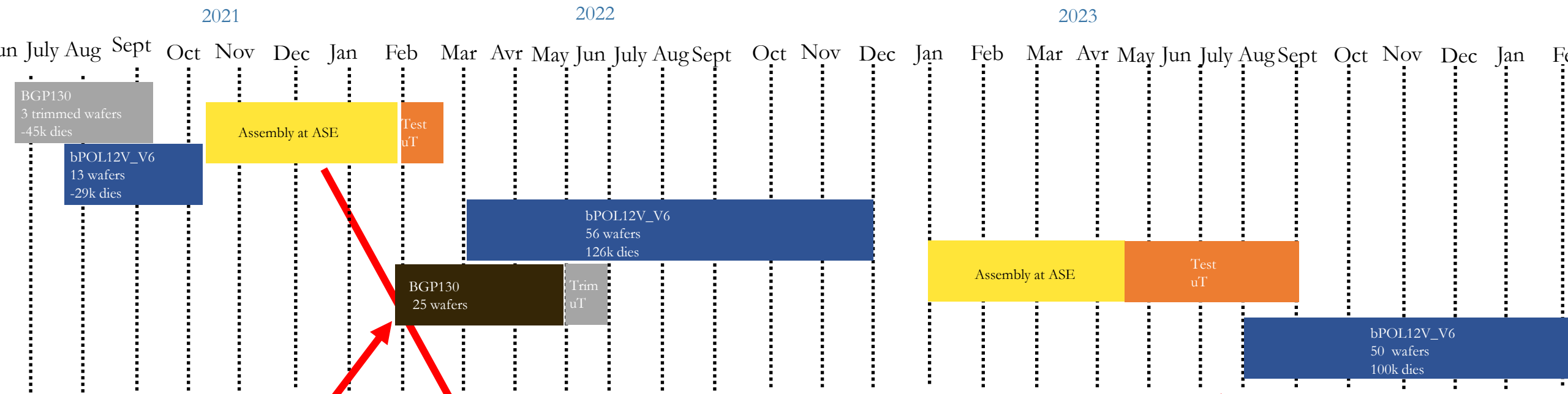
V6: Change of drivers, change of level-shifter

Production

6 years

6 prototypes!!!!

But…. Production has been painful as well!!!!!



ISSUE WITH TSMC

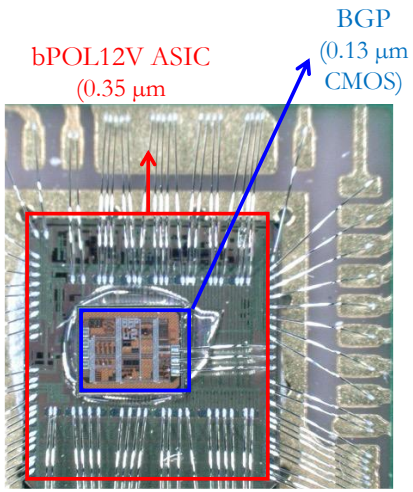
Order placed for 10 BGP wafers, TSMC refused to produce. Thanks to P. Malisse and Kostas after 7 months of negotiations, TSMC accepted to produce 25 wafers

ISSUE WITH ASSEMBLY

First assembly had very poor yield (80%)
ASE wrongly put an electrical conducting glue between bPOL12V and BGP chip

ISSUE WITH OnSemi

OnSemi sold the I3T25 Fab to LA semiconductor, impossible to produce more wafers.
Thanks to P. Malisse and Kostas after 6 months of negotiations, OnSemi proposed a 10x higher price
After 9 months the price reduce to 3x, 50 wafers ordered



Some numbers

Produced bPOL12V

1st run (2021)	2nd run (2023)	3rd run (2024)	total
22k	140k	100k	260k

needed bPOL12V

ATLAS (LS3)	CMS (LS3)	LHCb+Alice (LS4)	LHC	total
44k	130k	25k	21k	220k

We will have a contingency of around 40k samples, only stock remaining because the Fab closed, no more production is possible

Conclusions and take-home messages

bPOL12V is able to withstand the radiation tolerance requirements for HL-LHC

Design with HV technology and DD is complicated

An "easy" on-paper move from FEAST to bPOL12V has been very long (6 years and 6 prototypes)

Reliability is very complicated to achieve working close to the maximum device voltage rating

Production has been also plenty of hard walls, both foundries refused to produce more and long negotiations have been necessary.

Accurate testing with neutrons and protons must be done before sending new prototypes in production

Too many prototypes, too fast cycles, pushed to get the product but too short time for full testing (particularly DD and reliability)

Reliability must be tackled since first prototype

Don't be shy to order since the beginning the needed wafers, market evolves quickly and big companies do not care about CERN needs. We have been lucky to have IMEC support