

Third MODE Workshop on Differentiable Programming for Experiment Design



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Smart pixels with data reduction at source

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Highly granular pixel detectors allow for increasingly precise measurements of charged particle tracks, both in space and time. A reduction in pixel size by a factor of four in next-generation detectors will lead to unprecedented data rates, exceeding those foreseen at the High Luminosity Large Hadron Collider. Despite this increase in data volume, smart data reduction within the pixelated region of the detector will enable physics information to be extracted from the pixel detector with high efficiency and low latency, and has the potential to provide precise vertex information at the LHC bunch crossing frequency of 40 MHz (Level-1 trigger) for the first time. Using the shape of charge clusters deposited in arrays of small pixels, the physical properties of the traversing particle can be extracted by locally customized neural networks. Data from the sensor will be processed with a custom readout integrated circuit designed on 28 nm CMOS technology capable of operating at 40MHz and in extreme radiation environments. This talk will present a promising co-design strategy for on-chip data reduction that links the development of pixel sensors, ASICs, and algorithms in a fundamental way.

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