

SRS scalable readout system

-readout of triggerless VMM frontends-

This is a hardware and system -oriented document of SRS for triggerless VMM frontends. Similar documents for SRS with APV, Timepix, SAMPA, SiPMs frontends may follow in time. <u>VMM</u> is the acronym for a 64 –channel, self triggerable ASIC, which was adopted by the <u>RD51 collaboration</u> on a detector-pluggable hybrid card for readout by the SRS backend and its DAQ system.

For more information on VMM installations for applications, examples, firmware, software and operations refer to <u>Lucian's VMM User page</u> and <u>tutorial video</u>

Rev. 27022023



Pros and Cons of triggerless readout

<u>Pro</u>

- 1. No external trigger HW
- 2. high readout efficiency
- 3. full angular coverage
- 4. high trigger rates*
- 5. Pattern injection (event, time)**

*paper: 'Rate-capability of the VMM3a Front End in the RD51 Scalable Readout System' NIMA 1031 (2022) 166548 <u>https://arxiv.org/abs/2109.10287</u>

**MPGD22 Israel, L.Scharenberg

"Performance of he new RD51 VMM3/SRS beam telescope page 14

<u>Con</u>

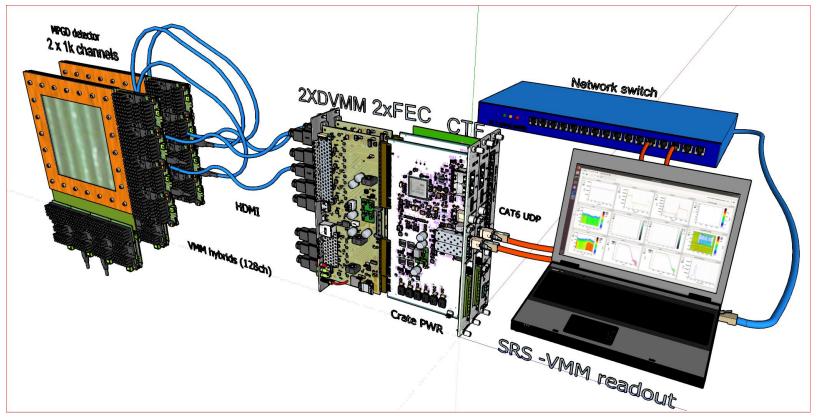
- 1. Higher threshold levels needed
- 2. Higher accidental events
- 3. Noisy channel mask mandatory
- 4. More SW overhead for eventbuilding
- 5. Runtime limit*= timestamp overflow

2023 news on triggered RO option SRS/VMM> Firmware,project to implement triggered mode In VMM in collaboration NA64 / GDD / NMX / Focal

* VMM run duration > 1 day after to insertion of markers

SRS 2022: SRS: from detector to Online

The Scalable Readout System SRS with VMM frontend, so far implemented as a triggerless, multichannel readout system for gas and photon detectors. Triggered readout planned for 2023.

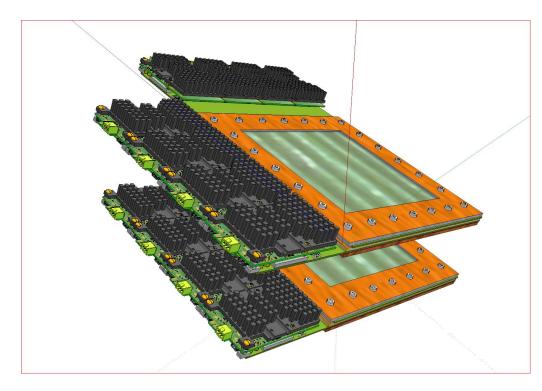


1 FEC for 8 VMM hybrids / 1024 detector channels connected via HMDI AD cables to DVMM. 2 FEC's with CTF (common clock) for 16 hybrids, 2048 ch. DVMM cards with octal HDMI connector including 70 W power for 16 VMM hybrids. Power / housing for 2 FECs and CTF via 1 Minicrate (not shown). 1 GB Ethernet /UDP uplink from FEC to Network via SFP+ jack, fiber or optical 1 GBE for network with Jumbo packet support. ESS DAQ Software with Vmm Controls installed under Linux.



Detectors with VMM hybrids

Since 2019, MPGD detectors are fabricated with 0.5mm pitch, <u>140 pin HRS connectors</u>* mating with <u>5mm stackheight</u> the HRS connectors of VMM hybrids.



10 x 10 GEM detector 4x VMM hybrid in x (512 ch) 4x VMM hybrid in y (512 ch) total 1024 channels/ detetctor 140 pin HRS connectors* on detector weight 8 VMM hybrids ~ 800 g heat dissipation 8 VMM hybrids~ 30W

Note 1: ventilation recommended Note 2: low-impedance GND connection from VMM hybrid Digital GND to Earth/ SRS crate required.

* On detector: FX10A-140S14-SV On hybrid: FX10A-140P14-SV1



SRS Minicrate

Minicrate for FEC and DVMM cards with <u>CTF card</u> slot and 2x 65W power for up to 16 VMMhybrids. 3U x 84TE rack-mountable crate 500W AC input, 3 horizontal slots : 2 slot FEC/DVMM, 1 slot CTF card (required for 2 FECs) HDMI links ports on the rear-side DVMMs. AC power inlet 110-240V AC. Octal frontpanel LED status display of ATX adapter voltages. Slide switch for remote on/off via coax cable 50 Ω terminator, power panel for direct access +12V,+5V,+3.3V for user service electronics. Rear M8 wing-screws for GND braid attachment to VMM hybrid digital GND. Top cover detachable for access to trimmers and SATA Power cables. <u>PMX powerbox</u> recommended for HDMI cables > 2m.



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SRS Eurocrate

Eurocrate for FEC and DVMM cards with <u>CTF card</u> slot and 8x 62W power for up to 64 VMM hybrids. 6U x 80TE rackmountable crate 2x 500W AC input, 9 vertical slots : 8 slots FEC/DVMM, 1 slot CTF card (required for >1 FECs). HDMI links ports on the rear-side DVMMs. Two AC power inlets 110-240V AC for FECs 1-4 and 5-8. Rear-panel with LED status displays two ATX adapter voltages and 2 slide switches for remote on/off via coax cable 50Ω terminator. Rear power panel for direct access +12V,+5V,+3.3V for user service electronics. Rear M8 wing-screws for GND braid attachment to VMM hybrids, 1 per DVMM. Two frontside powerbuses for FEC1-4 and CTF card, FEC 5-8. 5 x SATA cables each with 3 SATA connectors for DVMM card power. With 500 W ATX supply up to 64W @12 V per SATA cable to DVMM (-> 8 VMM hybrids), <u>PMX powerbox recommended for HDMI cables > 2m</u>.



Eurocrate User manual

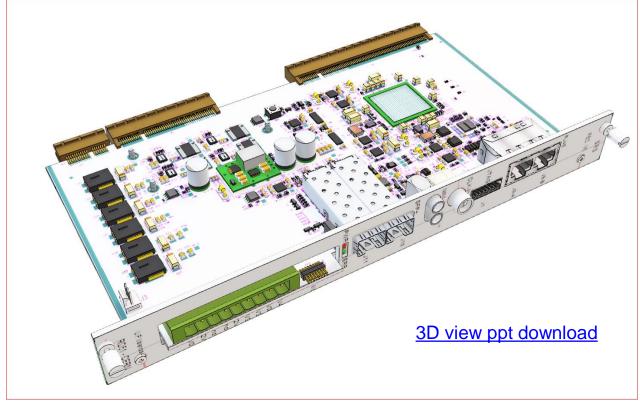
Note 1: Slot 1 for CTF card only Note 2: ventilation from the bottom is mandatory for >2 FECs (any commercial 1U rack-mountable ventilator) 1U air exhaust volume on top of crate Note 3: SATA cable routing to DVMMs required Note 4: bf default, slide switches on backpanel must be in "ON" position

3D view download ppt



FEC V6 card

The FEC V6 is a <u>FPGA firmware operated</u> frontend concentrator with an SFP port for Gigabit ethernet uplink to Online. Straddle-mounted frontend adapter like the DVMM card interface up to 8 HDMI links to its Virtex-6 FPGA*. Single FEC cards can therefore read out up to 8x128 channels from a detector equipped with 8 VMM hybrids. Up to 2 FEC cards can be housed and powered in a 3U Minicrate with a 9-way cable bus powering the FEC via the frontpanel. The FEC has a default a 40 MHz system clock transmitted to the frontend. Several FEC cards require a common, external CTF clock, connected via an RG45 cable to an octal CTF fanout card in the same crate.



The FEC V6 frontpanel has a rich set of connectors and 2 status LEDs. Several configuration jumpers are on the FEC PCB

Default <u>FEC firmware</u> for the ESS DAQ system for VMM frontend can be <u>updated via</u> <u>a frontpanel JTAG connector</u>**

Further I/O options require dedicated Firmware: <u>NIM input, NIM</u> <u>output</u>, external LVDS Clock input, <u>16 pin programmable User I/O</u>, RG45 and a second SFP.

A <u>DDR3 memory plugin</u> can be inserted on the backside of the FEC.

Recommended:

FEC firmware optimization 2018 student report, by Yan Huang, CCNU Wuhan

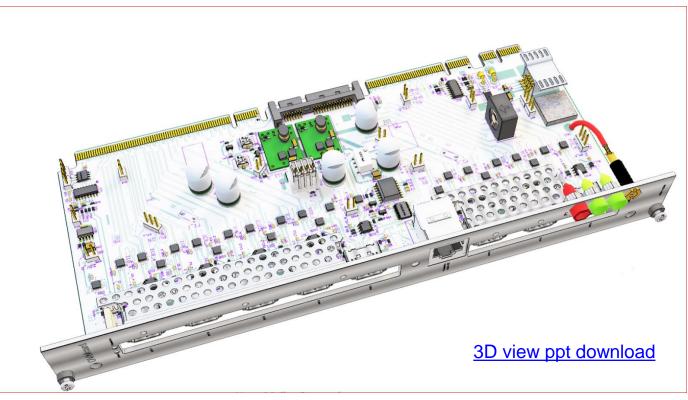
* XC6VLX130T-1FFG784C

** the correct Flash Chip and Size needs to be determined, several versions were mounted over time.



DVMM adapter card

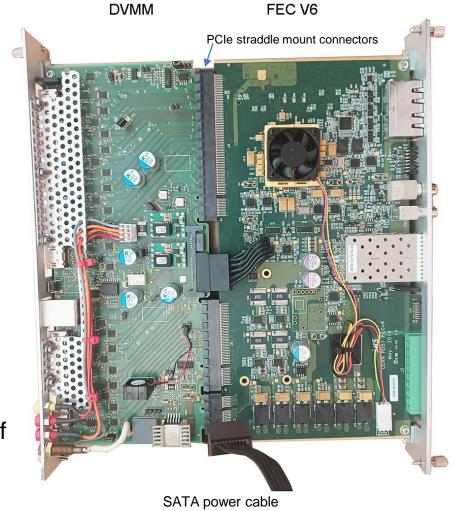
The <u>DVMM adapter gets</u> inserted into the PCIe connectors of the FEC V6 from the rear side of the Crate. It provides 8 HDMI ports to VMM hybrids via HDMI A-D cables. DVMM cards take power from the SATA cables of the Crate in order to distribute two voltages P1 and P2 to all connected VMM hybrids in the frontend. In the direct mode, P1,P2 power is brought over the HDMI cables, in the indirect mode, a PMX power multiplexer card, connected over a power cable to the DVMM Frontend Banana outlets, distributes P1 and P2 via short jumper cables to the individual VMM hybrids. The direct mode is only recommended for short HDMI cables since the voltage drop increases with length. A low impedance GND connection between all VMM hybrids and DVMM is required to avoid GND lifts and bit errors over the LVDS transmission links.



Two DCDC bucks generate each up to 10A of the two P2 supply lines for up to 8 VMM hybrids. Due to voltage drop over HDMI the Voltages on the DVMM need to be adjusted higher than required at the VMM hybrid AUX power connectors (on VMM: P2=1.8V, P1 =3.2V) On DVMM before 2022 the P1 Voltages was only crudely settable via Jumpers, as from 2022 DVMM cards also have a fine adjustment trimmer for the P1 voltage. Due to the high supply currents the DVMM mode "Power over HDMI" is not recommended for HDMI cables longer than 2m. In any case it is mandatory to connect the DVMM or SRS crate to all VMM hybrid digital GND, best via low -ohm copper braids attached to the crates.The PMX-1 powerbox is a solution for power from DVMM frontpanel to the VMM hybrids. The PMX-2 powerbox is a new power solution for long HDMI cables, allowing the use of external power supplies (5-33V) incl. USB-C.



FEC-DVMM Combo



FEC and DVMM link adapter are tightly plugged together via their 3 PCIe connectors to form a card combo that fits into SRS crates.

The FEC and DVM logic are powered via the FEC front panel connector.

The extra SATA power cable is required to be plugged on the DVMM card if the VMM frontend is to be powered from the SRS Crate.

FEC on frontside of crate

DVMM on rear side of crate



VMM hybrid

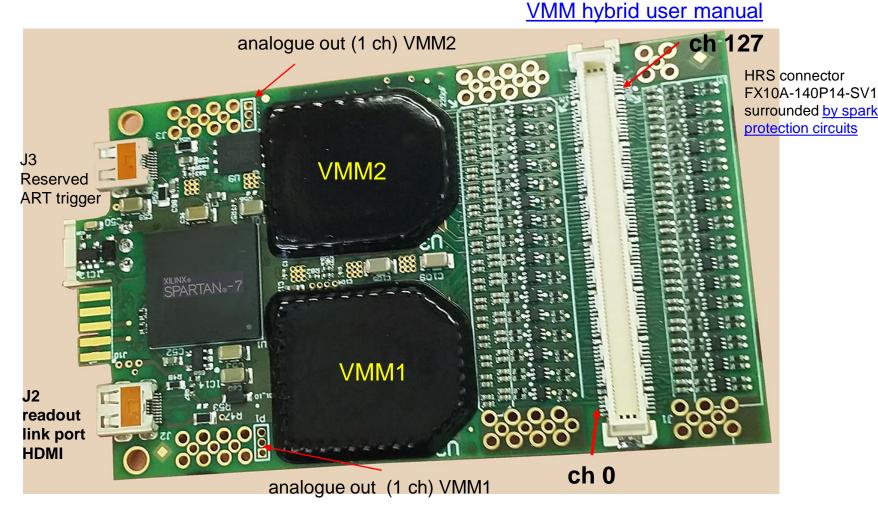


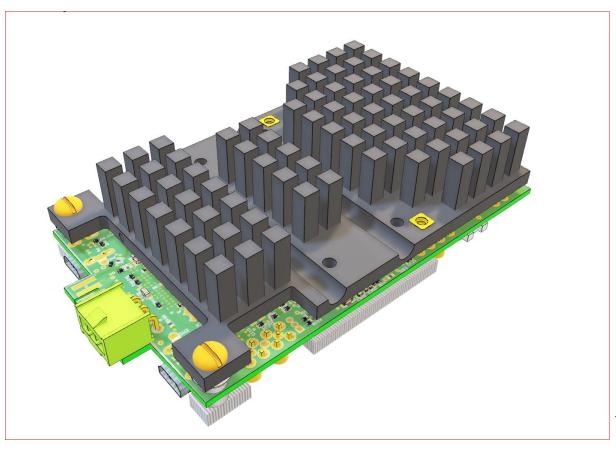
Photo VMM hybrid V5 (2022+) bottom side (cooler plate removed)

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VMM hybrid with convection cooler

<u>VMM hybrid for SRS</u>*, 128 channels, 2 VMM3a ASICs, 100g, 4Watt, plugs directly to a MPGD gas or photon detector with 140 pin <u>HRS connector</u>. <u>Multipurpose ALU cooler</u> (convection / water pipe) to keep die temperatures below 55 C for long lifetime and low noise. HDMI readout link to DVMM card via micro HDMI-AD cable. 3-Pin AUX <u>power connector</u> for P1 (+3.3V) and P2 (+1.8V). <u>PCB Edge connector for Jtag and I2C</u>. Two 3 pin connectors access to analogue Vmm signals (shaper , baseline etc)

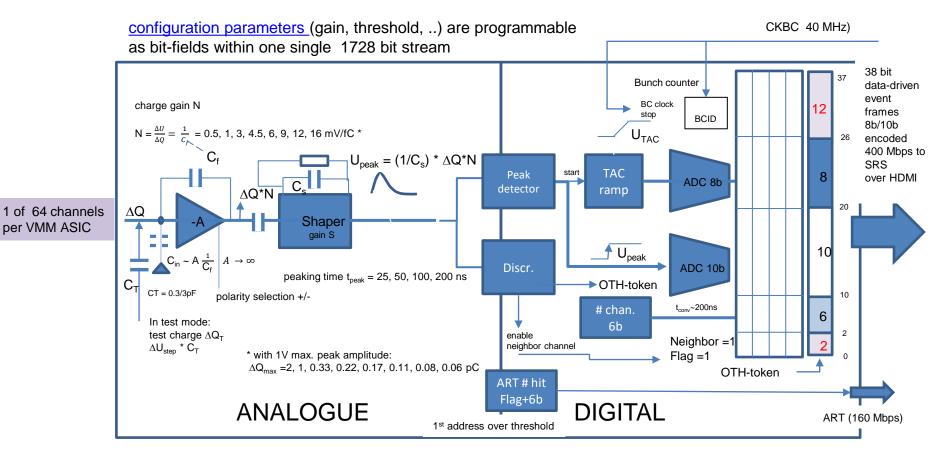


3D view ppt download

* latest revision V5, 2022+



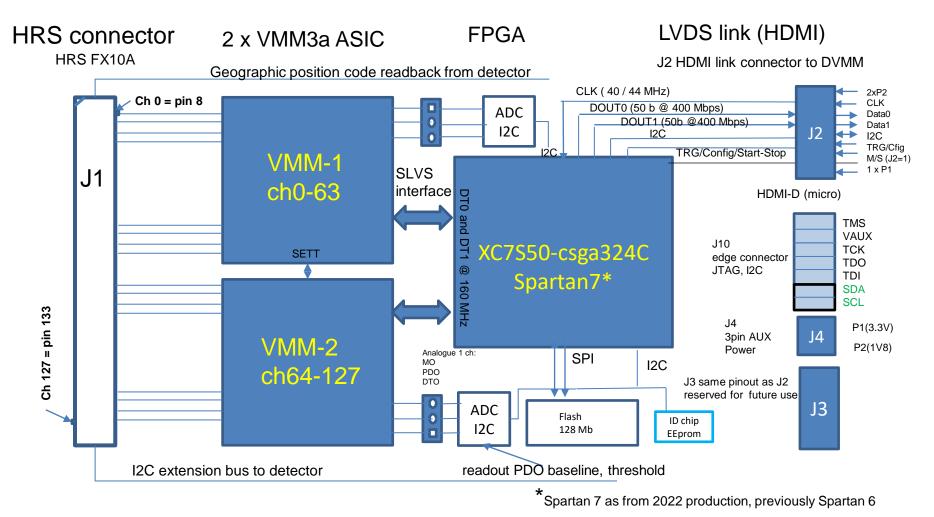
VMM3a in continuous readout mode*



ATLAS NSW specification VMM3a ASIC

*AKA self-triggered

VMM3a – hybrid block diagram



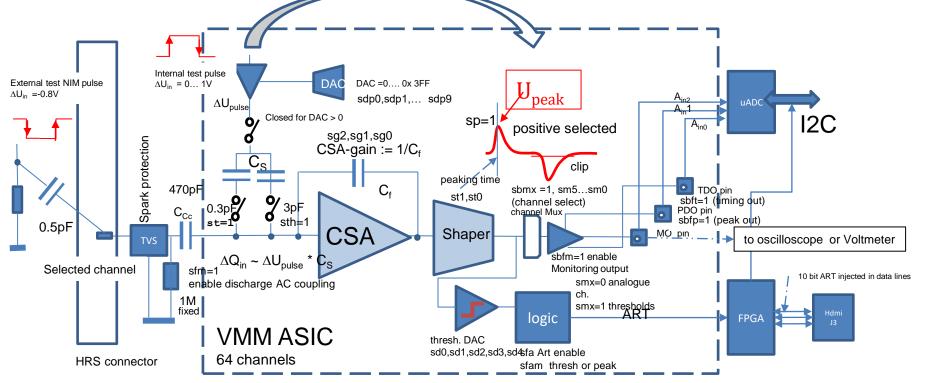
2/27/2023

scalable readout system



VMM-test pulse

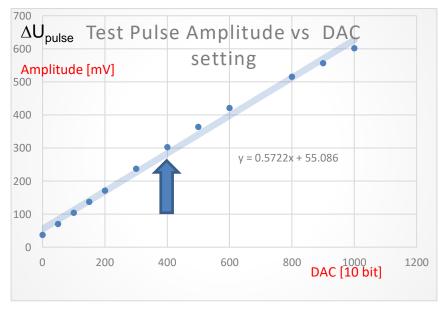
VMM channels can be pulsed either via its internal test pulser or via capacitive coupled charge from an external fast pulse transition. The internal pulser is coupled via a programmable capacitor of value 0.3 or 3 pF from a pulse amplitude that is programmable via a DAC between ~ 0 ..1 V. All 64 channels can be pulsed. Alternatively, an external NIM pulse of amplitude -0.8V, terminated over 50 OHM can be coupled via 0.5pF to selected VMM channels. The injected charge of the pulse edge corresponds to Q ~ U*C . Rectangular pulse shapes produce 2 charge pulses of opposite polarities on both edges, therefore pulse should be >> than the shaping time. By selecting the VMM threshold and polarity, one transition can be suppressed from generating a shaper peak. One programmable analogue shaper channel can be mux'ed to the Monitoring output pin for monitoring via an Oscilloscope.





Internal Test pulser

Amplitude vs. DAC setting



linear fit A[mV] = 0.5722* DAC + 55.086[mV]

Measure amplitude via Common monitor: scmx, sm5-sm0 [0 000001] pulser DAC. switch off sbmf to avoid a small DC Bias.

Selected Test pulse Amplitude 10 bit setting: sdp0,sdp1,... sdp9 => 0...1024

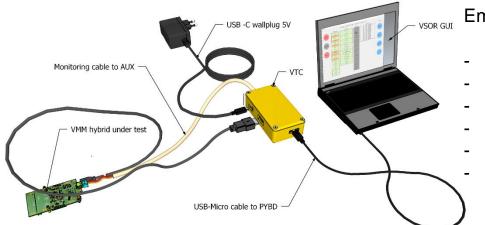
Test @ DAC = 400: (below saturation for high gain) measured: U = 302.5 mV (fit: 284 mV)

Charge injection Q = Cs*U Cs=0.3 pF : **90.75 fC** Cs= 3pF : **907.5 fC**

Note: this charge setting is global for all 64 channels of a VMM chips



VMM hybrid test via VTC

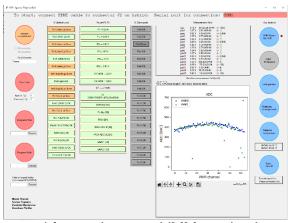


<u>Note</u>: since 2022 the VTC serves to the OXY team also as single SRS readout node of 1 VMM hybrid via an optical ethernet link with Muon trigger rates up to 2kHz, see Chapter "new SRS developments"

VTC documentation:

VTC box provides power to single VMM under test Embedded uPython subsystems test sequence:

- Connectivity and power
- I2C access all devices on VMM
- Readout of unique serial number
- Baseline all channels
- Test pulser ADC all channels Result storage in database

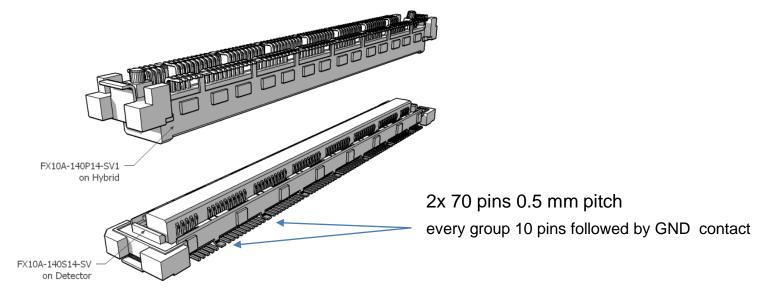


used for testing new VMM productions

Hirose FX10A-140P male on hybrid

RD51 decided in December 2016 to replace the legacy Panasonic 130 pin connectors by new 140 pin HRS FX10A connectors, starting with the VMM SRS hybrids and progressively implemented on the detector frames.

For a transition time, adapters between Panasonic and HRS are available.

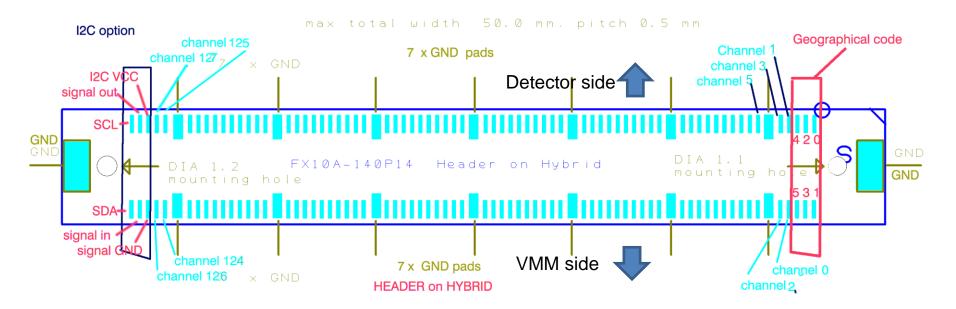




Pinout HRS connector on hybrid

I2C extension option and geographical code as from VMM hybrid V5 (2022+)

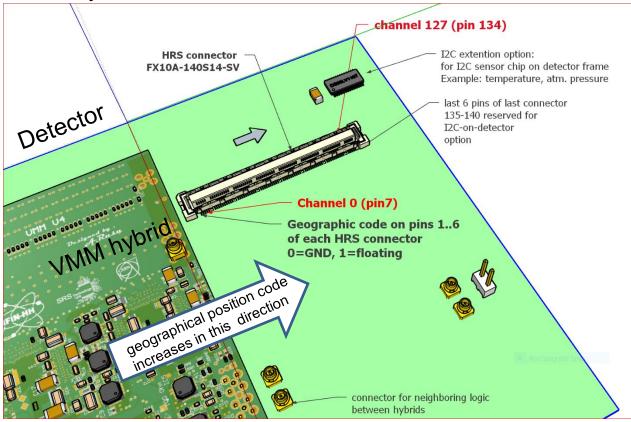
View onto the HRS connector on the bottom side of the hybrid





VMM channel mapping

VMM hybrid on detector frame

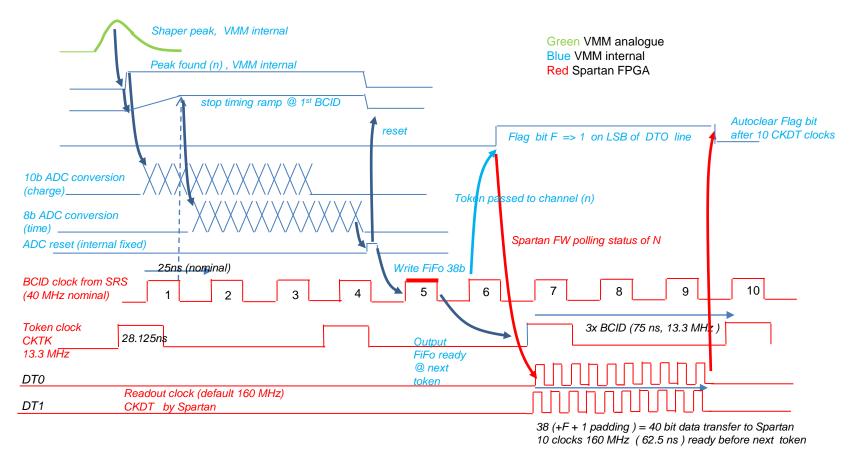


Ch0 is HRS pin 7 as shown Ch127 is HRS pin 134 as shown Ch1 is pin opposite to pin 7 Ch2 is right neighbor pin to pin 7 Equal channels = VMM hybrid side Un-equal channels = Detector side Neighboring logic requires that odd-even sides must not be inverted ch0-63 go with VMM1, ch64-127 with VMM2. Left side HRS pins 1-6 used for reading Geographic position code on detector frame Right side pins 135-140 for I2C extension to sensors or Bias Volt generators.



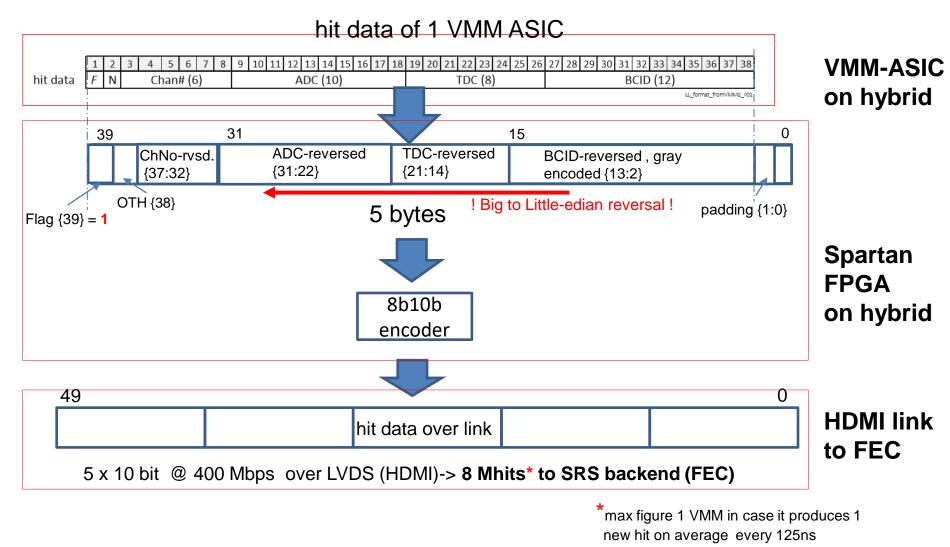
VMM3a – self-triggered readout

Analogue → Digital





38b-VMM hit to 50b over link



8b/10b control words

For info:

8b/10 bit encoding provides a DC-free average transmission balance and is widely used (Gbit-ethernet, PCI-e, Thunderbolt, Seral ATA, USB-3, etc)

8b/10b control symbols are 10b symbols do not have a corresponding 8b data correspondence and can therefore be used as data type delimitors

					$v_1v_1v_1 < -> \Gamma \subseteq \bigcup Synchion_2ation$
			RD-	RD+	
K28.0	1	000 11100	001111 0100	110000 1011	── K28.d0 → Link FEC to VMM
K28.1	1	001 11100	001111 1001	110000 0110	→ K28.d1 → IDLE VMM to FEC
K28.2	1	010 11100	001111 0101	110000 1010	── K28.d2 → VMM DATA header
K28.3	1	011 11100	001111 0011	110000 1100	── K28.d3 → FEC ACQ mode
K28.4	1	100 11100	001111 0010	110000 1101	── K28.d4 → FEC Config header
K28.5	1	101 11100	001111 1010	110000 0101	K28.d5 VMM ART header
K28.6	1	110 11100	001111 0110	110000 1001	
K28.7	1	111 11100	001111 1000	110000 0111	
K23.7	1	111 10111	111010 1000	000101 0111	
K27.7	1	111 11011	110110 1000	001001 0111	
K29.7	1	111 11101	101110 1000	010001 0111	
K30.7	ular S h ip	111 11110	011110 1000	100001 0111	

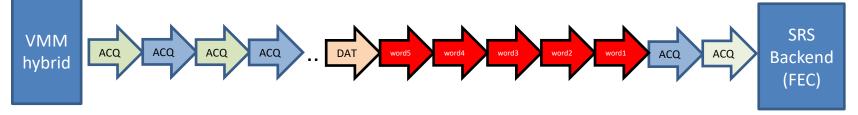
10b



 $VMM \sim FEC$ synchronization



8b/10 symbol sequence from VMM to backend



On physical link (HDMI), 10 bit encoded symbols (reversed)

11 0011 1100 (K28.d3 RD-) [ACQ], 00 1100 0011 (K28.d3 RD+) [ACQ], 11 0011 1100 (K28.d3 RD-) [ACQ], 00 1100 0011 (K28.d3 RD+) [ACQ], 00 1100 0011 (K28.d3 RD+) [ACQ], 11 0011 1100 (K28.d3 RD-) [ACQ], 1010111100 (K28.d2 RD-) [DAT], 5 x DATA 10 bit encoded, 00 1100 0011 (K28.d3 RD+) [ACQ], 11 0011 1100 (K28.d3 RD-) [ACQ], etc

In this example, the VMM sends 8b10 ACQ control symbols, inserts a DAT header symbol in front of 5 x 8b10b words (hit) and continues sending ACQ symbols until the next event

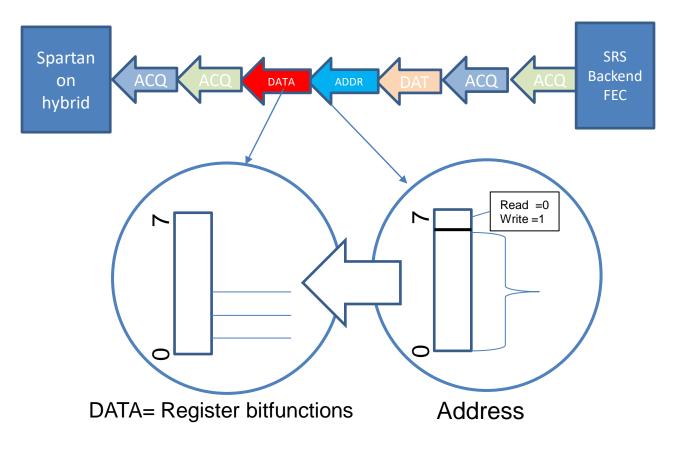
On the physical link, the symbols and data words are 10 bit, the VMM hardware (FPGA) sends

8+1=9 bit symbols and 8bit VMM data words to the 8b10b encoder which sends the encoded stream the physical link. The SRS backend (FEC) decodes

the 8b10b encoded symbols/data back into 8+1 Control symbols and 8 bit data words



Command from FEC to VMM Configuration registers in Spartan

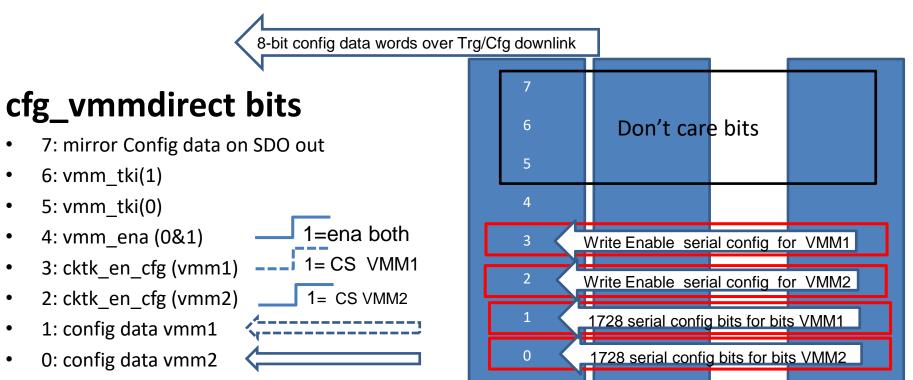




VMMdirect @ addr.3

Spartan Configuration Register

Detailed document on VMM Spartan firmware

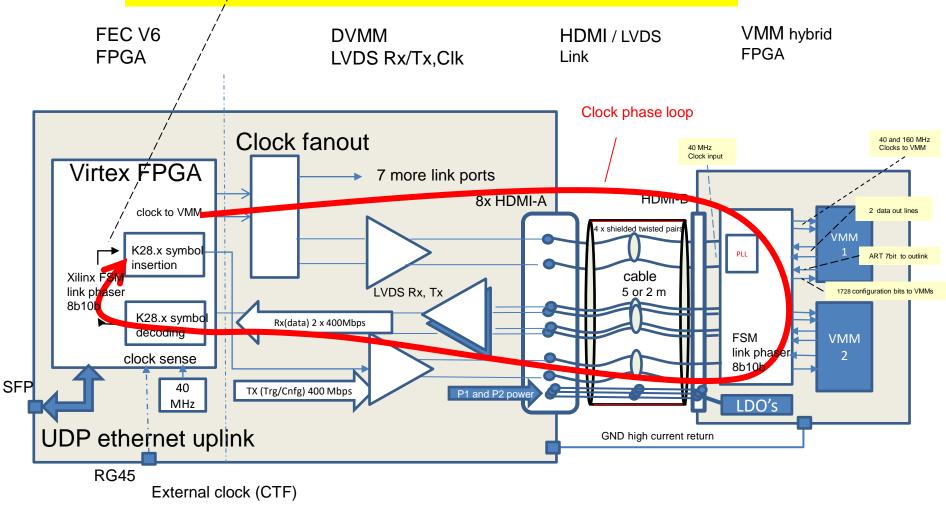


Config. data to buffer



synchronization frontend ⇔ backend

Link Status 1->2->3->4 required before DAQ can record VMM data reliably. Bad link status; check GND connection frontend/backend, bad cables, unstable CTF clock...





DAQ and Slow controls

Credits: Dorothea Pfeiffer / ESS Lund

	FEC 1					
Dpen Communication	General Advanced	HDMI 1	HDMI 2 HDMI 4 HDMI 5			
all alive	L0 settings		nomi 2 nomi 4 nomi 5			
Send		Hybrid	Hybrid 1			
	sL0enaV sL0ena		VMM	VMM 1 VMM 2		
	Boffset 0 0		V NOM			
Reset Warnings	offset 0 0		🖌 1 🚽 2	General Settings Adva	inced Settings	Channel Settings
c	rollover 0 0			Input charge polarity	negative	* SD SZ010b SZ08b SZ06b
	window 0 ¢		Position	Analog (Channel) Monitor	Pulser DAC	▼ SC SL ST STH SM 0 mV ▼ SMX 0 mV ▼ 0 ns ▼ 0 mV ▼
√ 1	truncate 0 0		Axis	Gain (sg)	3.0 mV/fC	• 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
2	nskip 0 🗢		Y •			
3	sLOcktest		Position	TAC Slop Adj (stc)	60 ns	▼ 2 0mV ▼ . 0mV ▼ 0ns ▼ 0mV ▼
4			65535 🗘	Peak time (st)	200 ns	▼ 3 0mV ▼ . 0mV ▼ 0ns ▼ 0mV ▼
5	Deprecated		120	ReadADC	ADC res.	4
	Frame Cnt 👻			SRAT Mode	Timing At Peak	▼ 5 0 0 mV ▼ 0 mV ▼ 0 mV ▼
6	HINFO+Dataler +		Geographical Position			6 0 0 0 0 0 V V 0 0 0 V V 0 0 V V 0 0 V V 0 0 V V 0 0 V V 0 0 V V 0 0 V V 0 0 V V 0 0 V V 0 0 V V 0 0 V V 0 0 V V 0 0 V V 0 0 V V 0 V V 0 V V 0 V V 0 V V 0 V V 0 V V 0 V
7						7 0mV • 0mV
8	✓ High Res.		Read I2C	Neighbor Trigger (sng)	Disable At Peak	
	Triggered Mode			Analog tristates	Sub Hysterisis	
Q	Enabled		S6	Analog Instates	Sub Hystensis	11
	Time offset (ns)		CKTK			12 0 mV v 0 mV v 0 ns v 0 mV v
Global ACQ	1024000		0 ns	ADC		13
	Time window (ns)	✓ 1	CKBC	ADCs	8-bit Conv. Mode	
Pulser	102350			10b ADC 200ns -	8b ADC 100ns	
External	Trigger Delay (ns)		40MHz • 18.72		1007000 100113	16 0 mV + 0 mV + 0 mV + 0 mV + 17 0 mV + 0 mV + 0 mV + 0 mV +
External	0		CKDT	6b ADC Low -		
ACQ On			80 MHz	Dual Clock		
			CKBC skew			20 0 0 0 0 0 V V 0 0 V V 0 0 V V
ACQ Off	WarmInit FEC		0 ns			21 0 0 0 mV + 0 mV + 0 mV + 0 mV +
	Reboot FEC		TK Pulses	Dual Clock ART Dual C	lock Data Dual Clock 6-	bit 22
ifg file			2			23
ng ne	Link Status		Set all Hybrids			24 0 mV • 0 mV • 0 mV • 0 mV •
			Test Pulse			25
MeasurementConfig	Read System Parameters					26 0 mV + 0 mV + 0 mV + 0 mV + 27 0 mV + 0 m
	Parameters		Skew	Threshold DAC 270	\$ 241.45 mV	
-	FEC Response		Ons 👻	Test Pulse DAC 500	\$ 428.62 mV	
	Clear		Width			30 0 mV + 0 mV + 0 mV +
Load	Data 3:0		128x25ns *			31
	Data, 4: 0		Polarity	Apply t	all VMMs	32 0 0 mV + 0 mV + 0 ns + 0 mV +
Save	Data, 5: 20055055		Positive 👻	Han	l Reset	
0846						

ESS DAQ : <u>https://github.com/ess-dmsc/essdaq</u>

Analysis tool for ESS DAQ data : https://github.com/ess-dmsc/vmm-hdf5-to-root

VMM3a slow control user manual on gitlab

Slow Controls GUI for SRS run control with VMM3 frontend connected via DVMcard



Slow control configuration

Credits: Dorothea Pfeiffer / ESS Lund

0.0		VMM 0
General Settings Advanced Settings		General Settings Advanced Settings
		Advanced VMM settings
lonitoring and hybrid external ADC		Leakage Current (slg)
Analog monitor (sm)	iture •	Double Leakage (ufm)
Read ADC		feedbeck currents factor 10x (s/h)
		mid tail concellation (stic)
/MM main settings		auto-reset at end ramp (stor)
Input charge polarity (sp)	negative 👻	Timing control to fix liming at threshold (sea
Gain (sg)	3.0 mV//C *	
Peak time (st)	200 ns 👻	atti emabled stpp.atci[01]: To T
TAC Slop Adj (stc)	60 ns *	timing outputs control 2
Timing choice (srat)	Peak *	(stpp)
Sub hysteresis (ssh)	Bipolar shape (sbip)	SLVS 100 Ohm termination
Neigbor trigger (sng)	DDR CKDT (sdcks)	te to
MM ADC settings		
ADCs on/off (s10b)	8-bit conv. mode (s8b)	art Bi
10b ADC (Ampl) (sc010b) 2	00 ns *	Level 0 settings (not implemented)
Bh ADC (Time)	00 ns *	sl.0era sl.0ckinv sl
(,	fast reset at 6-b completion (sfrst)	nskipm sLDenaV
	(3=31)	truncala_i 💿 🗢
nalog Monitor		window_1 0 0
sbfm sbft	sbfp sbmx	Liloffset_i 0
		ART mode
		ART (sfs) Of
(sdt) 300 265 mV		Timing mode (sfam) The

neral Settings Advance	d Settings			
ced VMM settings				
Leakage Current (slg)			At Peak (p)	
Double Leakage (sfm)		extreme	tion (stgc)	
feedbeck currents factor 10x (sh)		feedback	k currents I0x (sixh)	
mild tail concellation		skip d	18-47	
(stic) auto-reset at			32) very from	
end ramp (stor)		high cha	rge (srec)	
ng control to fix timing at th	reshold (sra	(=1)		
II enabled		direct ou	tput legic	
tpp,stot(01): ToT		(6	81)	
timing outputs control (lifpp)	2	timing outputs control 1 (stat)		
S 100 Ohm termination				
bc to		tk	d	
art Bd		ena	63	
0 settings (not implemen	ied)			
sL0era sL0ck	inv s	LOdokinv	sL0ckt	set
nskipm sl.Den				
truncate_i	\$	nakip_i		0
Litoffset_1 0	0	offset		-
mode				
RT (sfø)	оп			٠
ming mode (sfam)	The	eshold		*
Charles and the second second second		200		

The Slow controls which is integrated in the GUI of the ESS DAQ system gives access to all required control bits of the VMM.

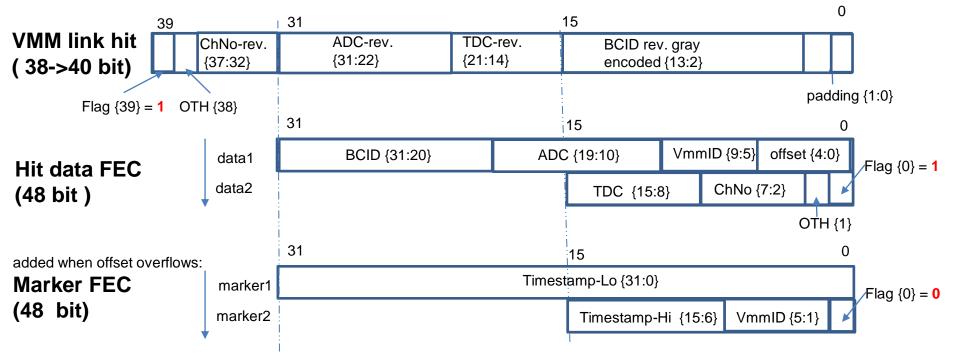
The standard settings (left) are for standard applications The advanced settings (right) for more advanced users.

An Excel sheet summarizes the VMM configuration bits and functions used by the slow Controls

advanced settings general settings



Data format VMM hits on FEC V6



Offset: every 12 bit BCID overflow, offset is incremented by 1

BCID overflows every 4096 BC clock periods (102 / 92.16 µs for CKBC = 40.0 / 44.4 MHz) Bunch crossing clock CKBC: 2.5 MHz, 5 MHz, 10 MHz, 20 MHz, 40 MHz, 80 MHz and 160 MHz transmitted from FECs / CTFs to all VMMs

Flag: 1 for data, 0 for timestamp

OTH: hit over threshold =1; can be 0 if neighboring logic is enabled

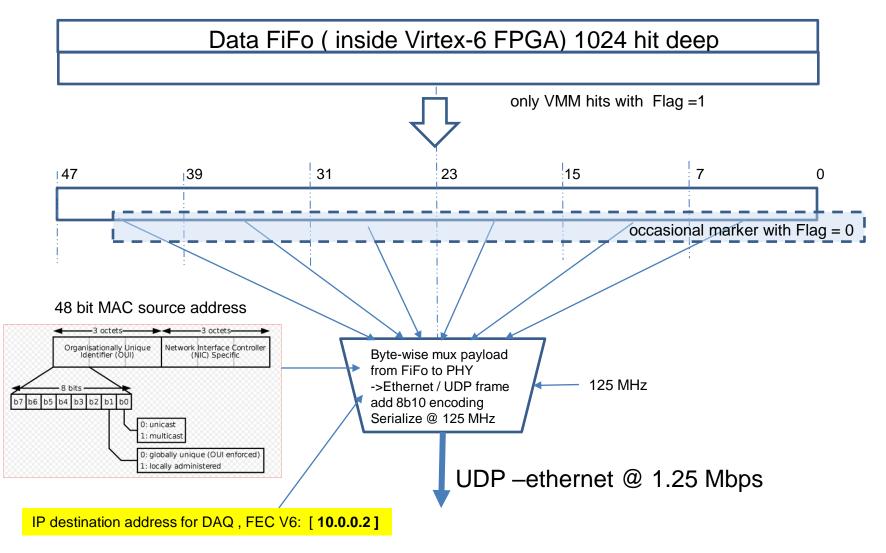
VmmID : 5 bits for 32 VMMs or 16 VMM hybrids. So far only max 8 hybrids can be connected to one FEC

ChNo: VMM channel Number 0-63, VmmID even: channels 0..63 on hybrid VmmID odd: channels 64 ..127 on hybrid ADC: 10 bit ADC value of the VMM peakfinder

TDC: 8 bit time relative to VMM peak found ramp (several start /slope options, cleared at next CKBC down-edge Marker: 42 bit timestamp added if offset goes from 15 to 0, overflows every 1.2 days



Hit data to UDP





Data payload in Ethernet frame

The FEC builds ethernet frames for Jumbo packets with an MTU 9000 hence requires that the network support 9kB Jumbo frames. Online networks without Jumbo frame support may split the FEC generated packets back into smaller 1500 bytes however this is inefficient and may lead to more UDP collision loss.

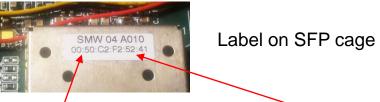
Preamble	SFD	MAC Destination address	MAC Source address	Length / Type	Data payload	FCS		
7byte	1byte	6byte	6byte	2byte	461500 / 8960 bytes*	4byte		
				Payload 1460 byte for default 1500 bytes MTU size (last 2 bytes can be padding) Jumbo Frames*: Payload 8960 byte, 9000 bytes MTU* size				
Preamble + SI 8 byte Sync se to identify start SFD = last byte	quence of fram		er1010101 <mark>1</mark>	Length/Type 2 byte payload length and Ethernet Type FCS: 4 byte CRC frame check sequence				
				*Note: SRS uses Jumbo frames for higher network efficiency MTU denotes maximum size of an IP packet that can be transmitted without fragmentation over a given medium.				



MAC addresses on FEC V6

The FEC-V6 Source and Destination Mac addresses are stored in an EEPROM (IC9,AT24C01BN) and read out via I2C by the FPGA for association with the PHY transmitter output to ethernet.

EEprom address: AOF10078 = 8b firmware version <u>Source address</u> AOF2007A = upper 14b MAC base address Samway (0050C2) AOF2007D = lower 14b MAC addr = FEC serial Nr <u>Destination address</u> AOF30000 = 16b hex. IP address for of the FEC [**10.0.0.2**] (for pinging the FEC) Local IP address, DAQ PC [10.0.0.3]



MAC address label on FEC cards: 00.50.C2= SAMWAY, F2.52.41= FEC serial Nr

For reprogramming the PROM, see <u>Samway F-47 FEC module test procedure document</u> and <u>FEC Firmware</u> <u>upgrade tutorial</u>

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VMM Flash Configuration

- Version 3 and 4 VMM hybrids produced up to 2020 are mastered by a Spartan-6 FPGA (XC6SLX4-3CSG225C) with 16 Mbit Flash AT45DB161E**. Version 5 hybrids produced as from 2022 are equipped with a Spartan-7 (XC7S50-csga324C) with 128 Mbit Flash S25FL128LAGNFA010. The Flash can be updated via a JTAG dongle connected via a <u>VMM specific connector</u> adapter.
- The default FPGA configuration bitstream is loaded at power-up of the 3.3V P1 voltage from the Flash chip. Using a JTAG master Dongle, the Spartan can also be directly configured with a different configuration than contained in the Flash. This direct configuration is volatile and needs to be repeated after each power cycle.
- V4.1 hybrids produced as from 2019 also contain an ID/ Flash chip AT24CS02 containing a unique 128 bit ID string and 2kbit of eEprom connected via the I2C bus of the Spartan which is also available on the Dongle connector. The Eeprom can be used (VTC test, ADC readout via I2C) for reloading alternative VMM configuration files.
- The FPGA is the essential interface between the two VMM ASICs (SLVS) and the SRS readout links (LVDS) over HDMI, hence the VMM Flash firmware is critical to proper functioning of the VMM features. User should make sure to have a validated, latest version* in the Flash.
- The FPGA configures in master serial mode in which the FPGA masters the readout clock to the Flash chip. On Auto Detection of power-up (P1), the Spartan FPGA generates "CS low" level on pin 4 and sends the "SCK" clock at 2MHz to pin 2 of 16 or 16 Mbit** Flash (U9) via R40. The Flash chip sends back the configuration bitstream on SO (pin 8). At successful completion (16 Mbit/2MHz ~ 8 s), the Spartan releases the "DONE signal" (pullup resistor R88 goes high)
- The FPGA configuration includes a default 1728 bit VMM configuration file which, at powerup is copied to the two VMMs chips (~ 50 us each)

<u>* https://gitlab.cern.ch/SRS_firmware/bit_mcs_files/-/blob/latest</u>



FEC firmware update

For full info on the FEC firmware please consult the Readme on gitlab

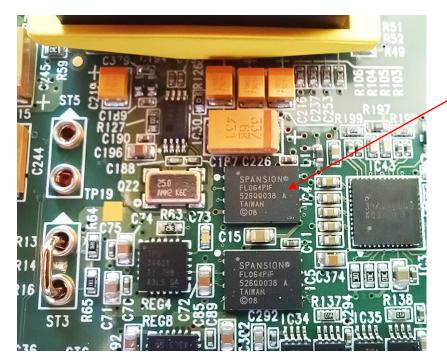


Photo Flash chip on FEC V6 card (production 6 / 2018)

Identify the Flash Chip and Size Following these instructions

Flash IC4 contains the safe boot and IC5 the normal boot configuration, selection via Jumper ST5. S<u>everal Flash versions</u> exist. The latest (2019+ production) requires these Flash parameters for the programming: N25Q128 1.8/3.3 V

Note that the system clock can be 40 or 44 MHz depending on a Compilation choice for the bitfile For more information go here https://vmm-srs.docs.cern.ch/firmware/ https://vmm-srs.docs.cern.ch/versions/



Network Links for SRS

The network link FEC –> Online DAQ can be either copper or fiber. The upper SFP slot (J11) must be used with the following SFP plugins:

Copper: (CAT5e, 6, 6a network cables for BER 10⁻¹² over 100m)

Type 1000BASE-T 1.25 GBd 3.3V with RG45 jack Plugins like Broadcom/Avago ABCU-5730RZ , ABCU-5730RZ or similar Cisco GLC-T compatible. EXCEPT ! SGMII versions <u>New:</u> GSFP-2.5-T 2.5 Gbps copper SFPs (Factor 2 ! FEC BW with upgraded 100-Base-T IP core on Virtex, being investigated by Doro)

Fibre: (G50/125 multimode optical fibre Cord fitted with LC/LC connectors)

Type 1000Base-SX Multi-Mode for 850nm for up to 550meter with 50/125µm OM2 multimode fibre at 1.25Gbps Plugins like FS –Europe SFP1G-SX85 (550m)

<u>Network switches:</u> Jumbo frame support and large DRAM buffers recommended for connection of multiple FEC cards.

Example copper RG45 only: Netgear 110MX , unmanaged 10 GBE switch with 8 ports RG45. Example: 1 copper and Fiber: FS- Europe, S3950-4T12S 10 Gbps 12x 10Gb, 0.5Gbyte Buffer, SFP+, 4x Gigabit RJ45

Example 2: Netgear GS110MX 10 GBPs not managed, 8 x Gigabit RJ45









UDP User Datagram Protocol

SRS uses UDP over IPV4 for realtime data transfer.

UDP is a transport layer protocol providing end-to-end communication for applications. UDP provides integrity verification via checksum of the header and payload, it provides however **no guarantees of message delivery** and the UDP layer retains no state of UDP messages once sent.

Lacking reliability, UDP applications may encounter some packet loss, reordering, errors or duplication. Applications should provide some handshaking as real-time confirmation that the message has been received.

The UDP datagram header consists of 4 fields, each of which is 2 bytes:

Source port	Destination port		
Lenght	Checksum		

Source port: 0 if unused. 0-1023, otherwise a "<u>port number</u>" Destination port*: required , 0-1023 "<u>port number</u>" of the destination Length: Nr. bytes of UDP header + UDP data, min 8, max 65,507 Checksum: header and data. Optional for IPV4 and must be zero if not used

UDP over IPV4 with pseudo IPV4 header

Source IPV4 address					
Destination IPV4 address					
00	protocol	UDP lenght			
Sourc	e port	Destination port			
Len	ight	Checksum			
Data					

Source and Destination IPV4 only for checksum Protocol for UDP = 0x11 (17) Checksum: header and data. Optional for IPV4, must be zero if not used

SRS/ VMM : UDP destination port for is 6006 netmask is 255.255.255.0



SRS network monitoring

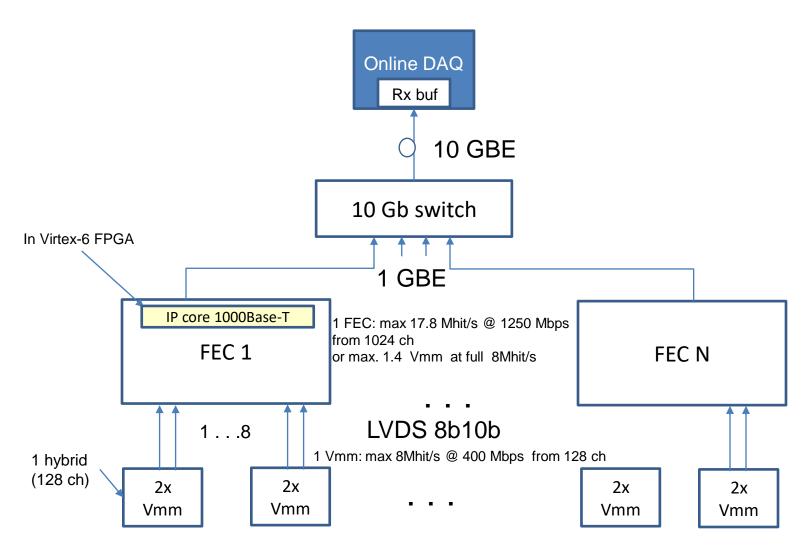
The use of Wireshark as network protocol analyzer is very common for SRS DAQ systems and highly recommended.

Please refer to document "<u>VMM3a/SRS</u> <u>Network package structure</u>" by Lucian Scharenberg for full details how to use Wireshark for analyzing SRS network traffic for VMM readout.

	y a display filter								
	Time	Source	Destination		Length Info				
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	5 0.249339	10.0.0.1	10.0.0.3	SRSVMM_			40, Markers		
	6 0.268166	10.0.0.4	10.0.0.3	SRSVMM_			0, Markers		
	7 0.330430	10.0.0.1	19.0.0.3	SRSVMM			28, Markers		
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	11 0.584970	10.0.0.1	10.0.0.3				54, Markers		
	12 0.633869	10.0.0.4	10.0.0.3				0, Markers		
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	16 0.830402	10.0.0.1	10.0.0.3	SRSVMM_			77, Markers		
	17 0.906921	10.0.0.1	10.0.0.3	SRSVMM			78, Markers		
	18 0.997253	10.0.0.1	10.0.0.3	SRSVMM			25, Markers		
	19 1.001044	10.0.0.4	10.0.0.3				0, Markers		
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	21 1.123674	10.0.0.1	10.0.0.3	SRSVMM_			00, Markers		
	22 1.183903	10.0.0.4	10.0.0.3	SRSVMM_			0, Markers		
	23 1,191735	18.0.0.1	10.0.0.3	SRSVMM_			38, Markers		
	24 1.258205 25 1.316808	10.0.0.1	10.0.0.3	SRSVMM_			62, Markers 43, Markers		
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Readout to Online





Bandwidth from VMM to Online

•	VMM-> FEC: 1 VMM hit 40 bit / 50 bit encoded	

- hit latency 50b@ 0.4 Gbps =125 ns
- max VMM hit rate 8 MHz
- FEC->1 GBE: Input: 1 VMM hit 48 bit raw / 58 bit
- encoded +20% framing overhead ~ 70 bit
- -> hit latency 70b@1,25 Gbps = 56 ns
- max hit rate 1/56ns = 17.8 MHz
- Output 1.25Gbps:
- Single FEC data payload max
- 17.8 MHz*48bit = 0.864 Gbps = ~0.1 Gbyte/s to Online
- 10GBE switch ->DAQ: FEC Output:
- max 1.25Gbps/ 0.864 Gbps => theor. max 1.4 hybrids full (-> count 1 hybrid)
- N x FECs: 1 full load VMM hybrid / FEC
- depending on switch, add UDP collision loss and Rx overflow :
- FEC output with **1.25 Gb SFPs**:
- 10 GBE switch **10 FECs: 10 x hybrids @ 8MHz/hybrid**
- FEC output with **2.5 Gb SFPs**:
- 10 GBE switch 10 FECs 20 x hybrids @ 8 MHz/hybrid

Coming eFEC strategy higher rates with avoidance of Rx buffer overflow:

- add flow control DAQ-> eFEC (trigger)
- add embedded realtime triggers
- alt. use of VMM triggered readout



New SRS developments for VMM frontends



SiPM adapter for VMM hybrids

256 ch SiPM Adapter prototype tested on Alice Focal Testbeam 2022 with 4 VMM hybrids and SRS DAQ

photo A.Rusu 53 VMM hybrid

64 ch adapter plugs on VMM hybrid. Next version with high/low gain for extended dynamic range will use all 128 VMM channels

64 differential channels to SiPM frontend



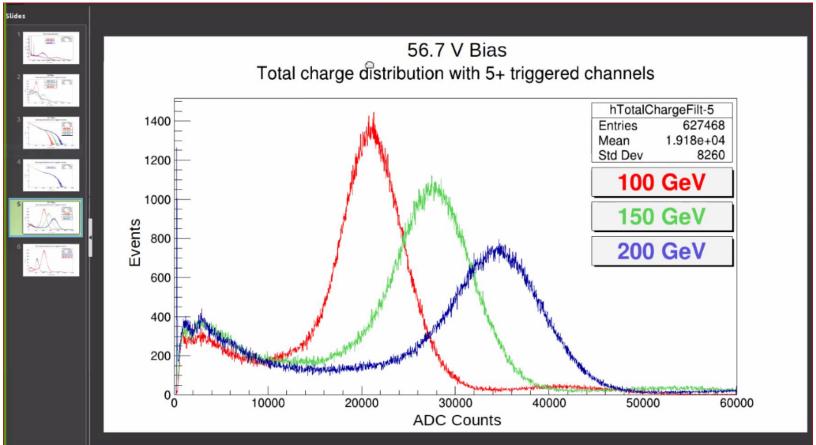
SiPM adapter, design A. Rusu

SiPM bias generator Ubr 10-80V included 41 & settable via Slow Controls

Testbeam 2022, SRS with VMM-SiPM adapter for readout of Focal SiPMs



Credits: Valentin Buchakchiev / Alice Focal



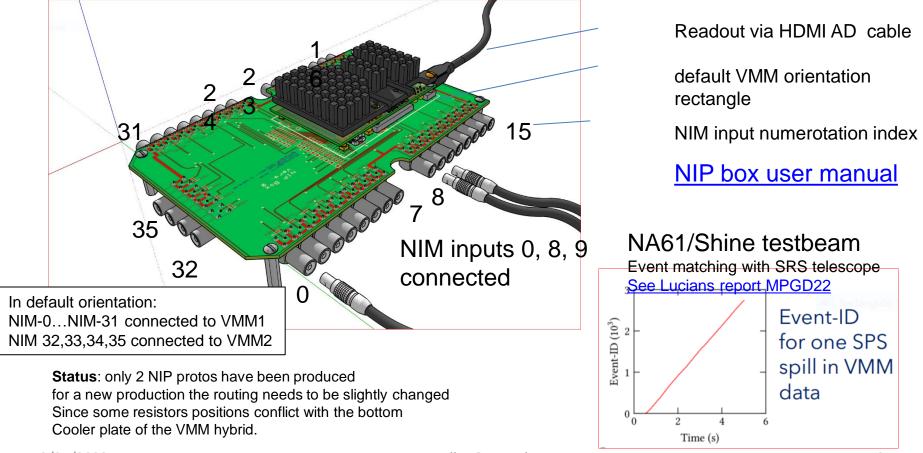
the detector was equipped with Hamamatsu MPPC series SiPMs and the Bias Voltage of the adapter was programmed via a VTC used as I2C master to 56.7V.

Hans.Muller@cern.ch



NIP – NIM pattern injector for VMM

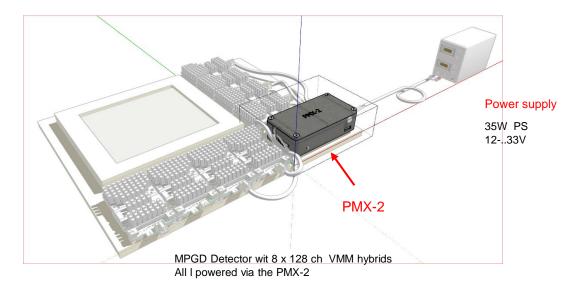
The 1st NIP prototype was successfully used in the <u>NA61 /SHINE testbeam</u> in 2022 to inject event-IDs into the VMM data stream to perform event matching with the VMM triggerless readout. For this purpose, a complete , <u>high rate GEM beam telescope</u> with SRS frontend and backend was borrowed to NA61 with a specially designed NIP pattern injection box



2023 preview

POWERBOX PMX-2

PMX-2 allows the use of floating power-supply to eliminates GND lifts between the frontend and the backend and to enable the use of long HMDI links between the VMM frontend and the crates.

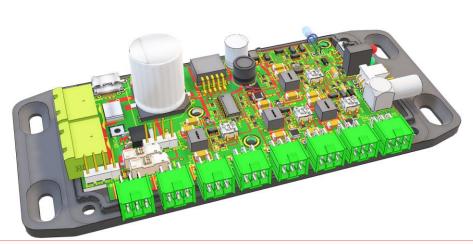


8x PMX-2 cards being assembled at CERN for this week

Hans.Muller@cern.ch



PMX-2 electronics on 1590BFL chassis plate



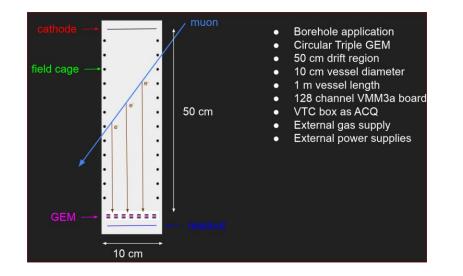
PMX-2 in 1690BFL box with ESP32 sensor option plugged

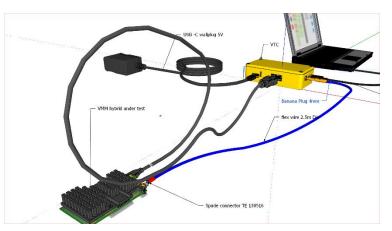


Manual and 3D powerpoint views



Low- rate, triple GEM readout* via the VTC at OXY Colleague



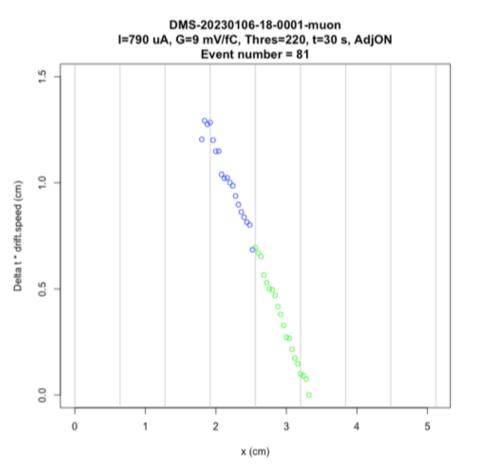


VTC-DAQ: program the SoC card in the VTC to read VMM hits via I2C at rates O(2 kHz). FW and SW credits: D. Pfeiffer ***Project:** "Low Noise Electronics Development at Occidental College for Dark Matter and Muon Research".

OXY 2023:



1st Muon tracks recorded with VTC



Feb 2023:

After optimizations (VMM firmware, SoC uPython SW, GND/noise), the OXY team recorded clean Muon track events with their VO detector.

OXY built 5 more VTCs for use in a deep (1/2 km) borehole with Ethernet over optical-fibre from the SoC.

A -VTC-like uSRS box is in advanced planning



eFEC , future backend of a scalable RO architecture

New features:

1 eFEC: max 64 FE- hybrids @ 128ch (8k ch) with 8 x FE uAssister cards and 8 powerboxes

FE links to uAssister fibre or copper

Backwards compatible with FEC with 8 HDMI link (legacy)

Horizontal + Vertical RO architectures

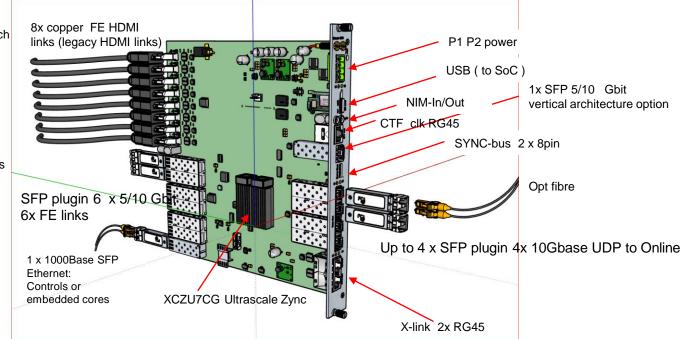
Sync and Xrosslink buses

SoC plugin for development and diagnostics

1 Single card to fit in SRS crates Minicrate : 2 x eFEC Eurocrate: 8 x eFEC Power: SATA only

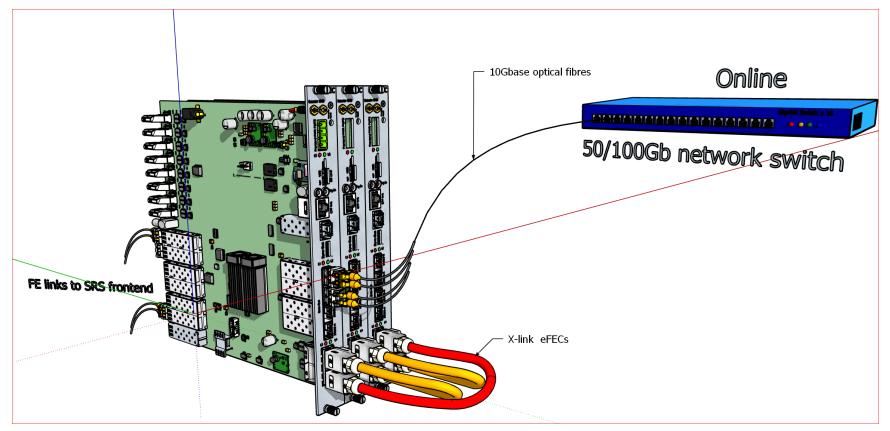
Output up 40 Gbps to network switch

realtime triggers over all channels (user defined firmware)





Scalable eFEC stack, large systems



SRS Eurocrate crate not shown



SRS VMM users

(... subset of user's we know of ...)

- GEMs with VMM frontend and SRS readout SW at the NMX Diffractometer ,Multiblade Detector with wire readout using VMM and SRS readout + other ESS instruments considering VMM frontend, ESS European Spallation Source, Lund Sweden
- <u>Gaseous Detectors for Preclinical Proton Beam Monitoring</u>, at Dep Physics Medical, LMU Munich
- SRS readout with cooled VMM's in a vessel for tracking system for the S800 spectrometer at (FRIB RIB Facility Michigan USA)
- New TPC for HYDRA at GSI/TU Darmstadt for measuring pions, SRS readout with VMM frontend @ GSI/TU Darmsatadt
- muon tomography for geological applications, SRS VMM readout, LSBB Rustrel, FR
- use of GEM telescope with SRS/VMM readout and NIP pattern injector, NA61/Shine CERN
- Triple GEM in borehole with VMM readout via VTC, OXY colleague LA ,USA
- Cygnus neg. ion TPC in pressure vessel for charge readout VMM/ SRS , Hawai Univ. Honululu
- Micromegas with VMM SRS readout for PANDA-FAIR phase 0 , MAINZ Univ. Physics DE
- GripiX TPC with Timepix 3 readout via SRS adapter, BONN Univ. Physics DE
- Qualification MM for Atlas NSW, LMU Physics Faculty Munich
- readout of Multiplexed MM with VMM SRS for NA64. Plans for addition of external VMM trigger, ETH Zurich, CH
- MPGDs for photon detection, VMM, INFN Trieste
- VMM trigger readout Controller ROC for ATLAS NSW, IFIN-HH- RO
- SRS ATCA readout system for NEXT TPC, UPV Valencia Sect. Gandia
- MPGD's for several national research project, SRS with VMM included, JLAB T.Jefferson Natl Accelerator USA
- cosmic telescope with VMM readout, Universidad de los Andes, Bogota
- GEM beam telescope with SRS VMM for testbeams and VMM qualification , GDD lab CERN
- XYU-GEM ambiguity-free readout with VMM /SRS (RD51 -Note -2022-09), GDD lab CERN
- TPC with SRS/VMM readout for search of X17 particle at a 5 MV accelerator , Melbourne Univ. AU
- don't find your experiment based on SRS ? Let us know