

PULPOKS 2023

**A stacked MOSFET-switch for distribution
of bunch trains at 4.5 MHz**

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Hamburg, 24.04.2023

Overview

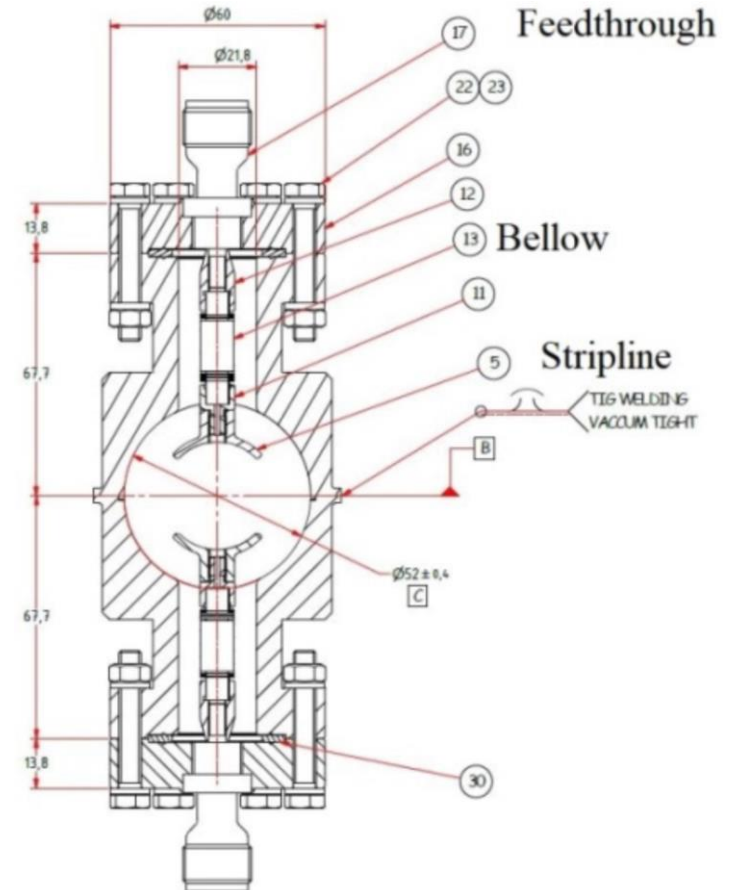
- Specifications
- Necessary Components
 - Mosfets
 - PCBs
 - Ferrite
 - MOSFET driver IXDD604
 - ...
- Prototype measurements with IsoVu probes
- Outlook

XFEL dump pulser specifications

Development of a 4.5MHz, 8kV, 50Ω dump kicker

Currently we use a 5kV pulser from FID

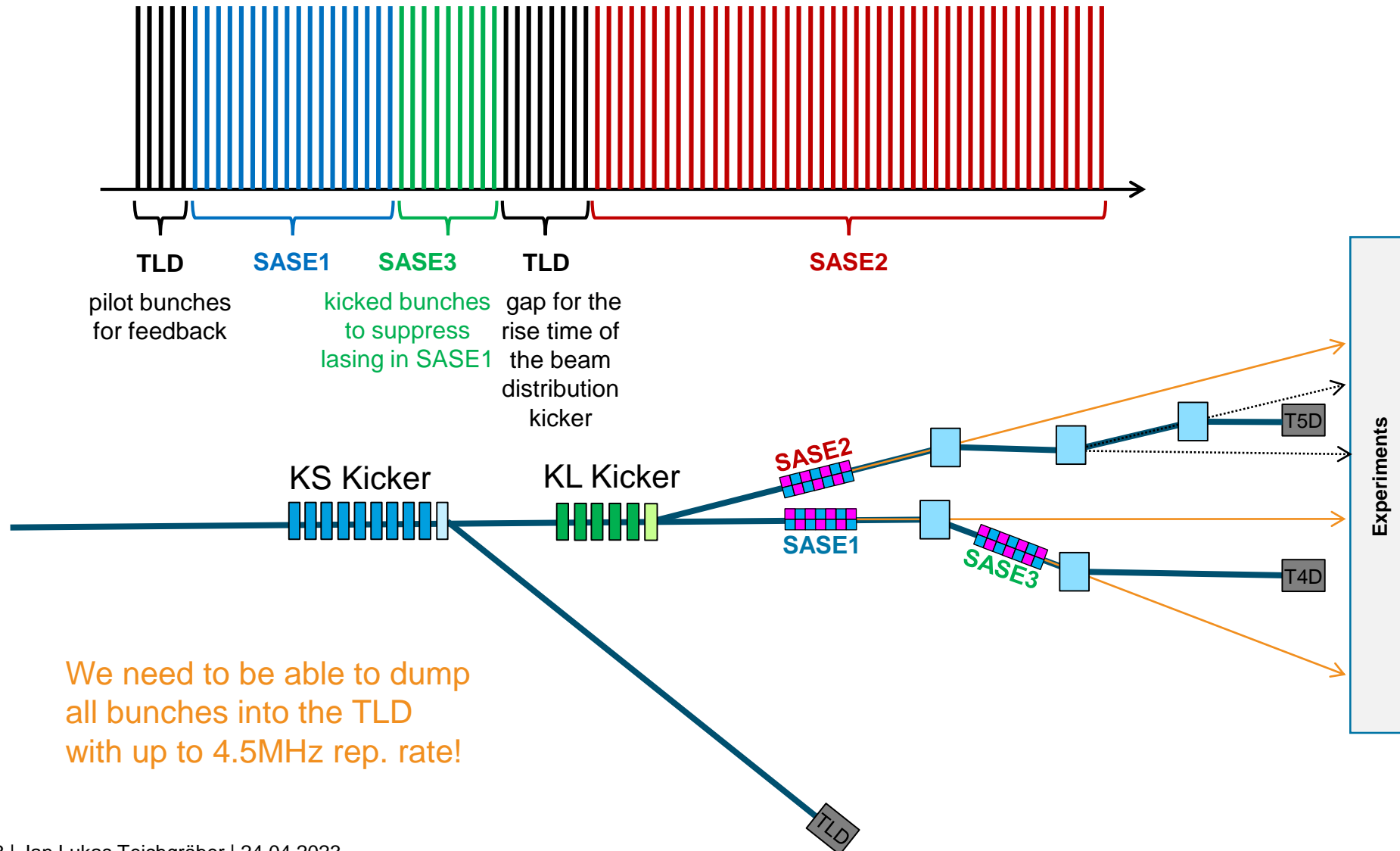
necessary kick angle	$\varphi = 0,5\text{mrad}$
beam energy max.	$E = 17,5\text{GeV}$
kicker length	$l = 2000\text{mm}$
kicker tube inner diameter	$d = 52\text{mm}$
kicker gap	$a = 30\text{mm}$
impedance	$Z = 50\Omega$
conductor width	$d_{in} = 30\text{mm}$
pulse width	$t_p = 30 - 100\text{ns}$
rise time	$t_r = 15\text{ns}$
fall time	$t_f = 15\text{ns}$
pulse shape	rectangle
max. current	$I = 160\text{A}$
max. voltage	$U = 8\text{kV}$
puls frequency	$f = 4,5\text{MHz}$
no. of pulses	2700 per train
rep. rate	10Hz



-> reduce the dependancy from single company

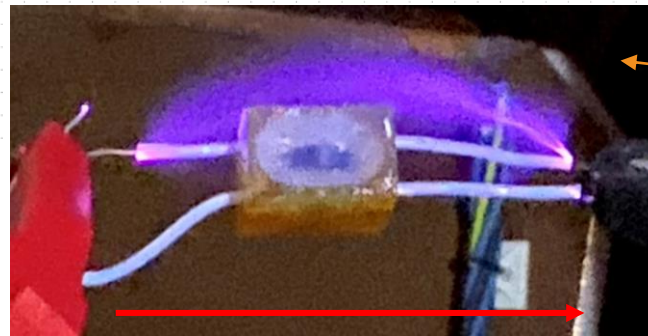
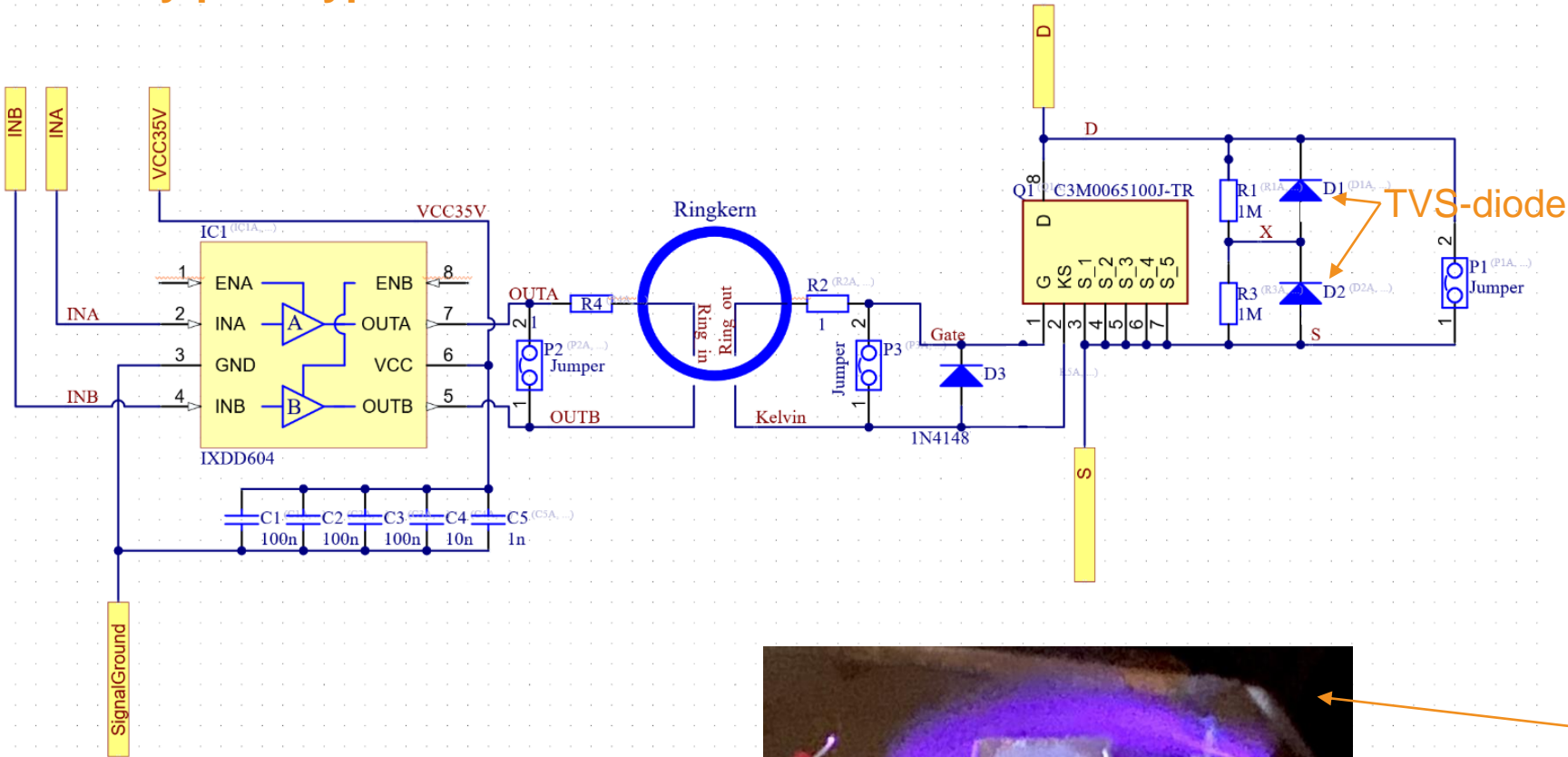
XFEL dump pulser

Driving SASE1, SASE2 and SASE3 simultaneously

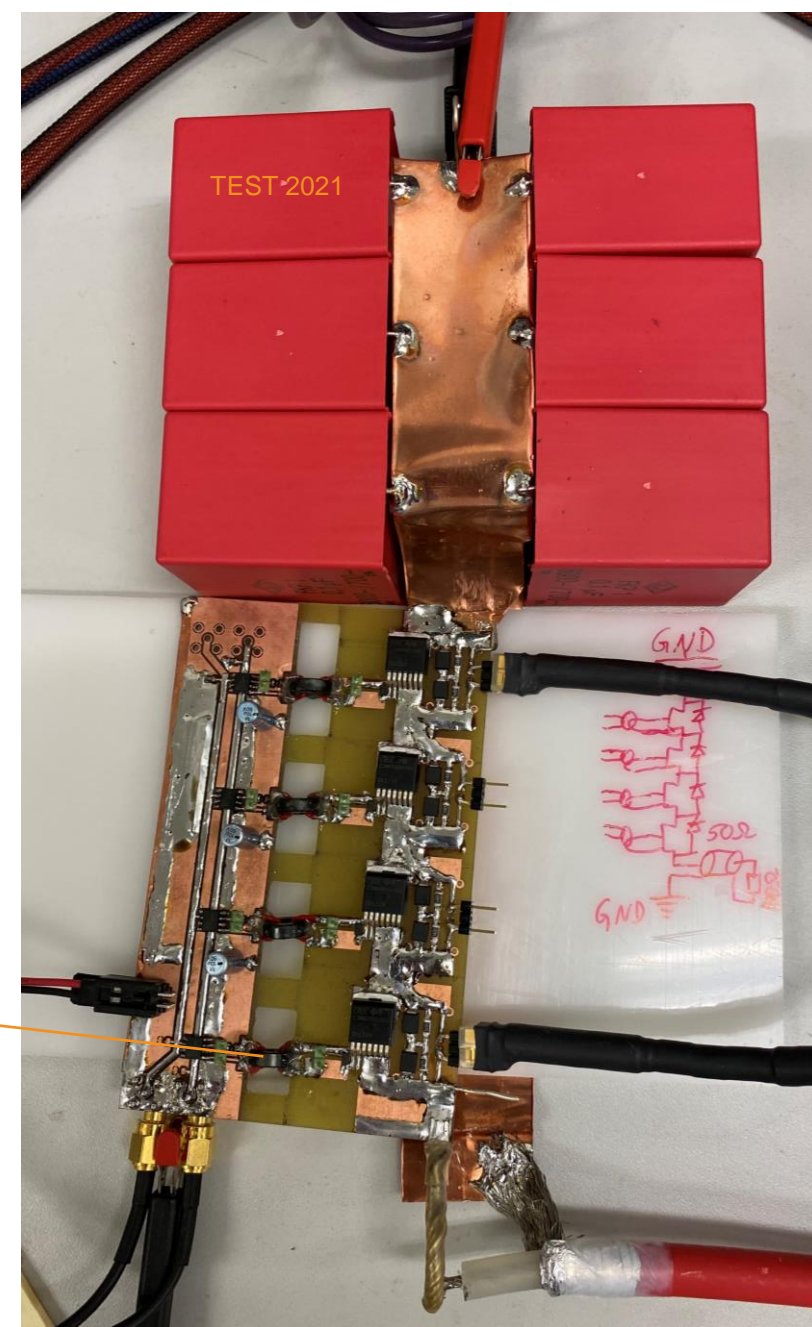


XFEL dump pulser

Early prototype with 4 MOSFETS



20kV
no problems at 10kV

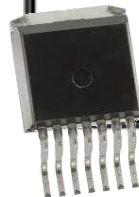
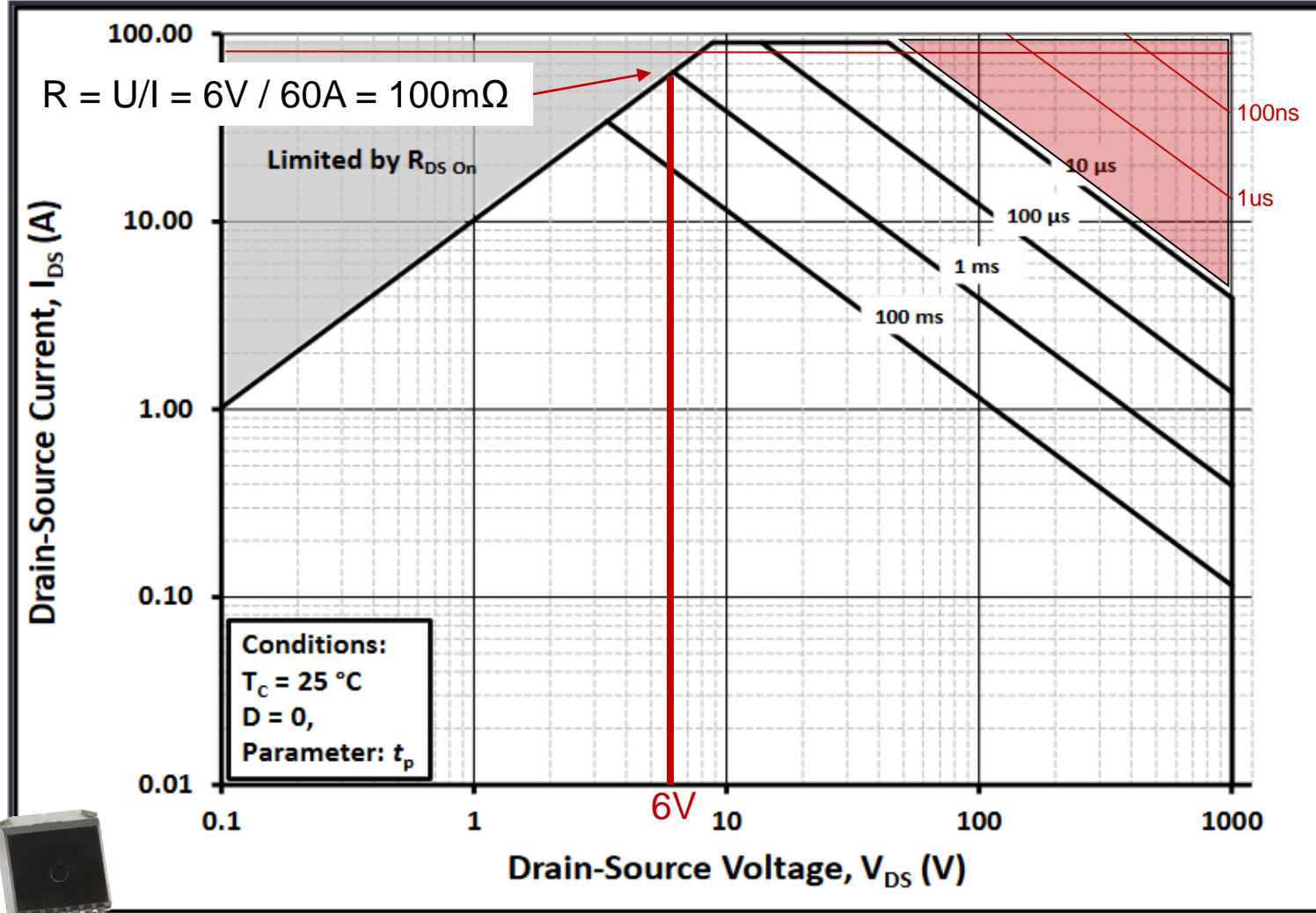


XFEL dump pulser specifications

Development of a 4.5MHz, 8kV, 50Ω dump kicker

- 16 MOSFETS in series -> **safety factor 2**
- 32 MOSFETS per pulser (2 in parallel)
 - expected losses up to 20W per MOSFET (mostly switching losses)
 - 640W have to leave the system while providing galvanic isolation
- possible solution:
 - cooling fins?
 - submerge in oil?
 - thermally conductive and isolating substrate?

$V_{max} = 1000V$



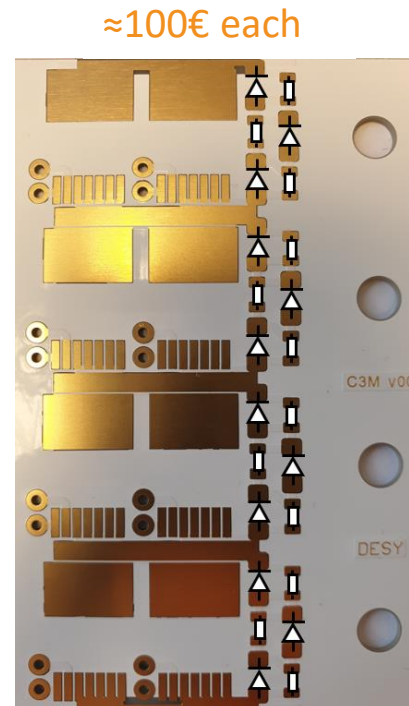
C3M0065100J

Figure 22. Safe Operating Area

XFEL dump pulser

Materials - PCBs

- PCBs made of Aluminium nitride
- thermal conductivity $\approx 170\text{W/mK}$ (copper 400W/mK)
- dielectric strength $> 17\text{ kV/mm}$
 - 2mm should be sufficient for 8kV
- dielectric constant (1MHz) $\approx 8\sim 10$
- PCBs can be bought e.g. from ceramic-pcb.com



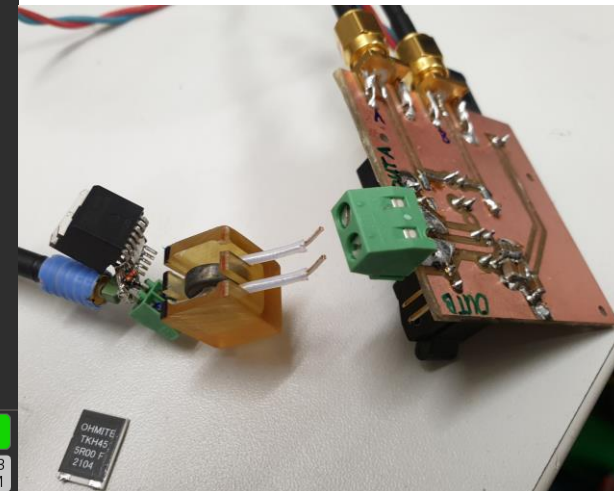
XFEL dump pulser

Materials - Ferrite



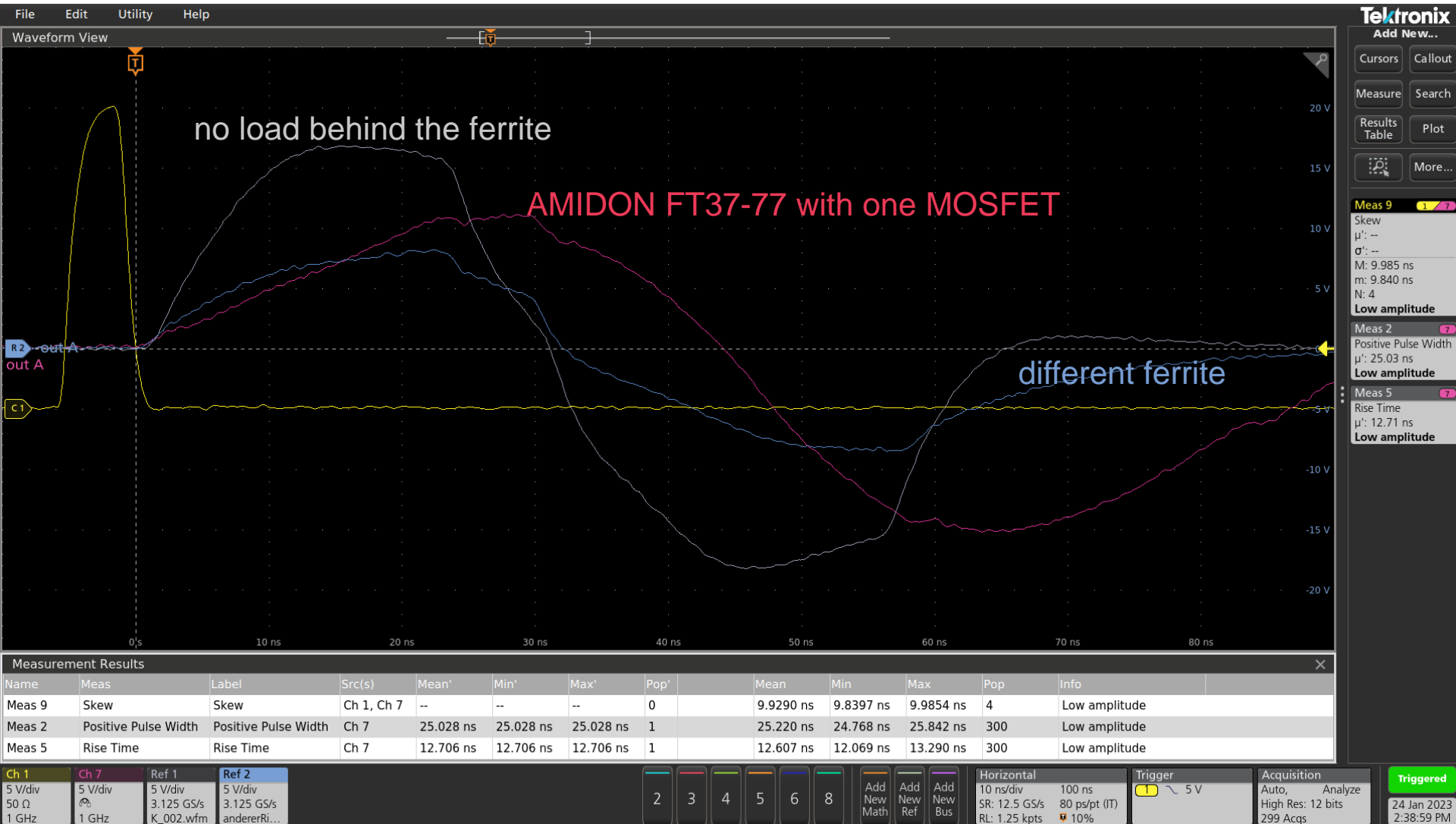
the MnZn ferrite core:
AMIDON FT37-77

there is approx. 500ps
delay between the different
cores.
too much to ignore



XFEL dump pulser

Ferrite test with 24V driver

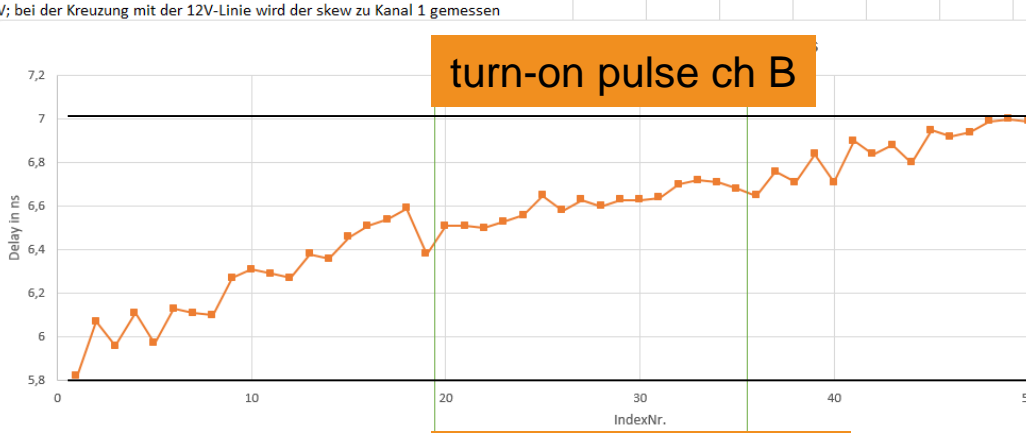


Paralleling more MOSFETS requires changes in the gate driving structure.

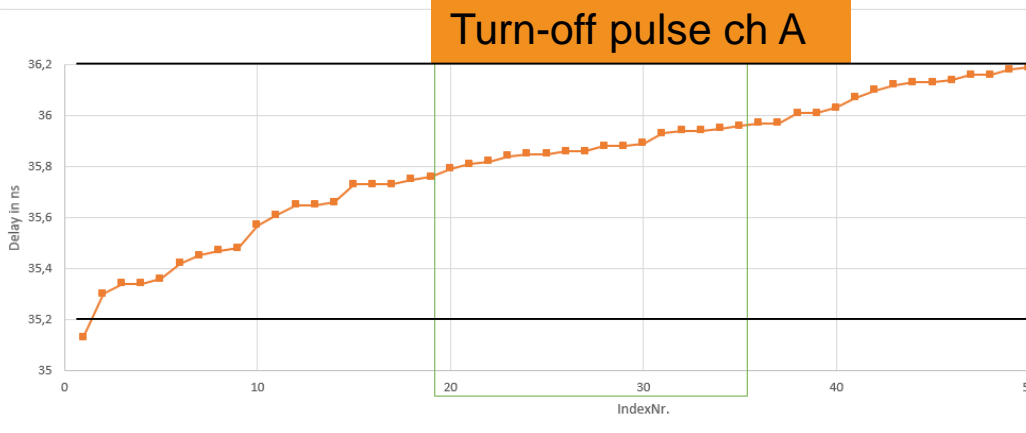
XFEL dump pulser

Materials – MOSFET driver IXDD604

IndexNr.	Treibernummer	CH B	CH A
01	46	5,82	35,13
02	44	6,07	35,3
03	12	5,96	35,34
04	21	6,11	35,34
05	43	5,97	35,36
06	48	6,13	35,42
07	20	6,11	35,45
08	15	6,1	35,47
09	08	6,27	35,48
10	50	6,31	35,57
11	30	6,29	35,61
12	18	6,27	35,65
13	47	6,38	35,65
14	22	6,36	35,66
15	19	6,46	35,73
16	24	6,51	35,73
17	27	6,54	35,73
18	02	6,59	35,75
19	49	6,38	35,76
20	28	6,51	35,79
21	23	6,51	35,81
22	25	6,5	35,82
23	03	6,53	35,84
24	29	6,56	35,85
25	32	6,65	35,85
26	16	6,58	35,86
27	14	6,63	35,86
28	06	6,6	35,88
29	26	6,63	35,88
30	09	6,63	35,89
31	05	6,64	35,93
32	17	6,7	35,94
33	10	6,72	35,94
34	04	6,71	35,95
35	07	6,68	35,96
36	01	6,65	35,97
37	13	6,76	35,97
38	11	6,71	36,01
39	33	6,84	36,01
40	38	6,71	36,03
41	34	6,9	36,07
42	31	6,84	36,1
43	36	6,88	36,12
44	37	6,8	36,13
45	39	6,95	36,13
46	41	6,92	36,14
47	35	6,94	36,16
48	45	6,99	36,16
49	42	7	36,18
50	40	6,99	36,19
Mittelwert:		6,405	35,66



$\Delta T = 1.2\text{ns}$



$\Delta T = 1\text{ns}$

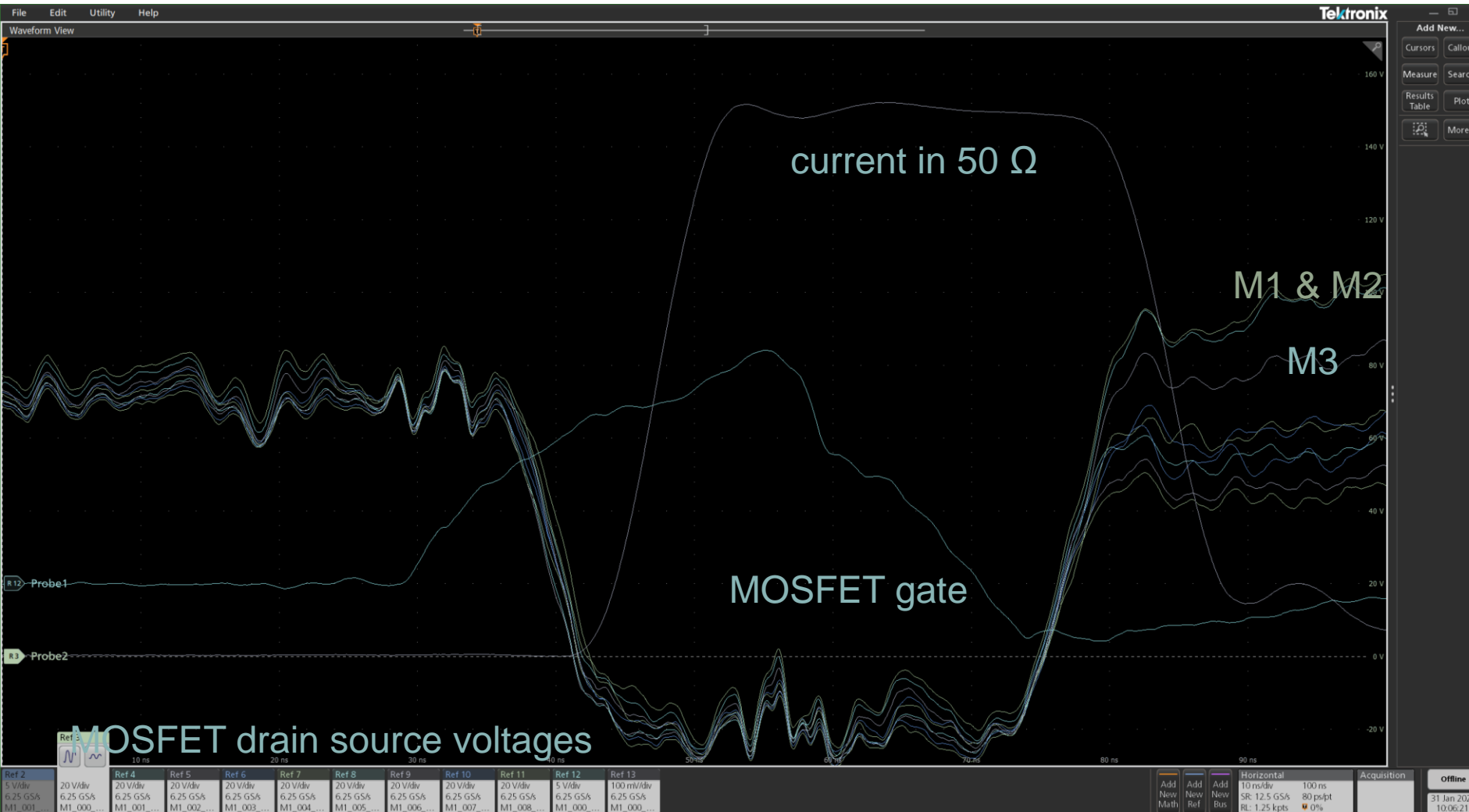
Die Kanäle A und B innerhalb der Treiber scheinen recht gut zueinander zu passen (maximal 250ps Differenz zwischen A und B).
Die Treiber sind nach dem Delay des Abschalttriggers CH A sortiert.
 Am sinnvollsten ist es wohl nach dem Ausschalttrigger zu sortieren, also Kanal A. Die Differenz ist hier aber so gering, dass es keine Rolle spielt.
 Für die erste Platine werden die Treiber Index20 bis Index35 verwendet.
 Das sind also die grün eingefärbten Treiber (28, 23, 25, 03, 29, 32, 16, 14, 06, 26, 09, 05, 17, 10, 04, 07)

different turn off time
 -> different turn off voltage
 -> 1ns delay in gate voltage is too much
 -> 500ps looks good enough

we haven't found an easy way to reliably change the pulse length and delay for each individual channel

XFEL dump pulser

Measurements – 800V with 8 MOSFETS in series and 2 parallel

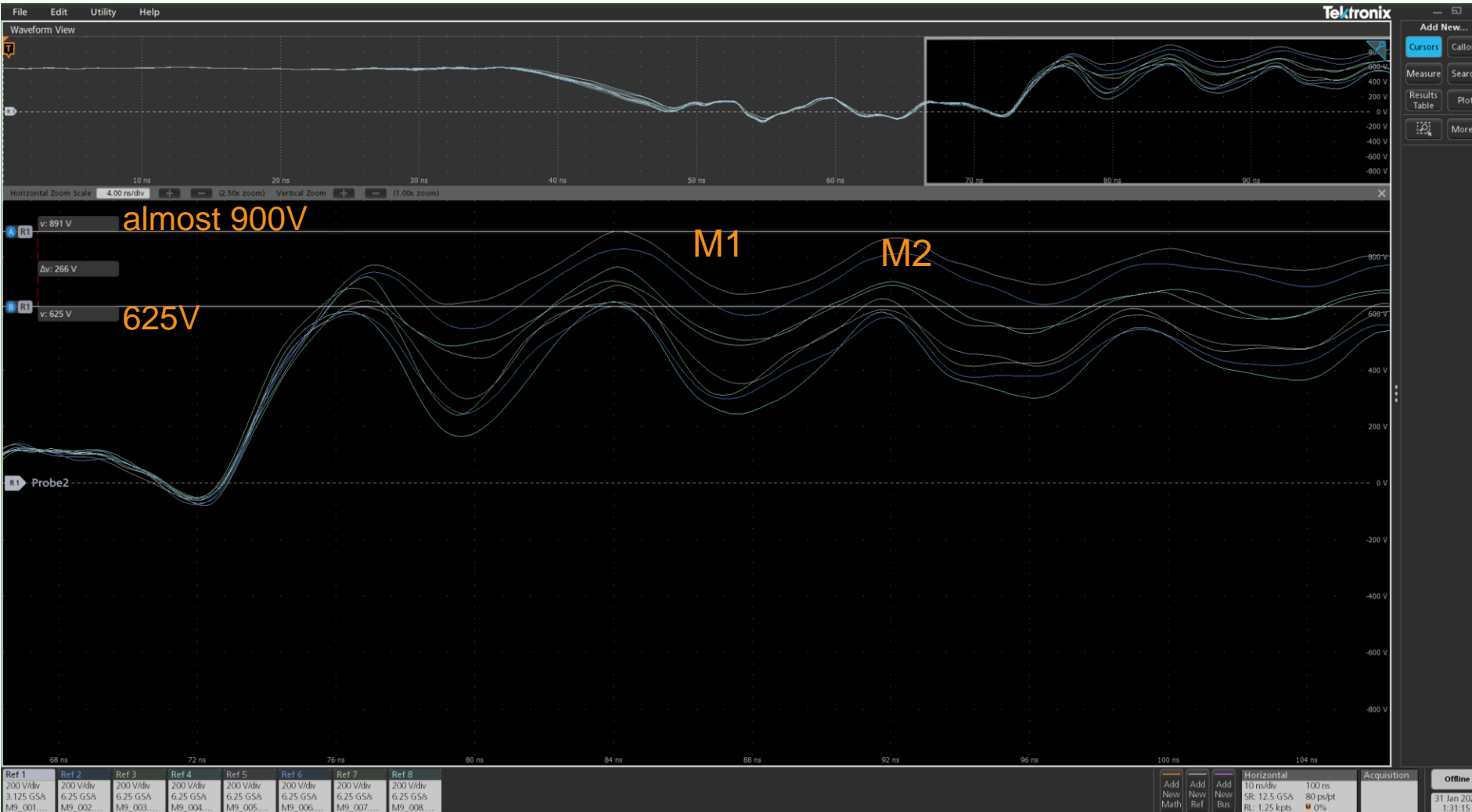


the turn off voltage over the 8 MOSFETs is not the same

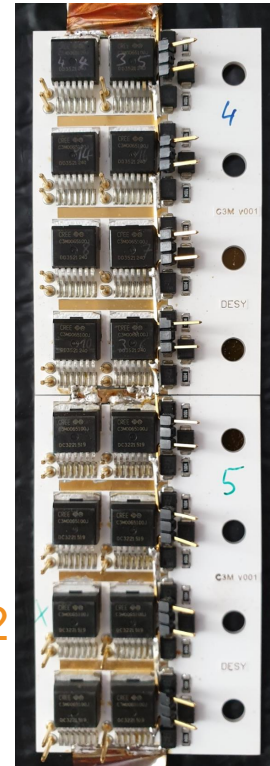


XFEL dump pulser

Measurements – 5000V with 8 MOSFETS in series and 2 parallel



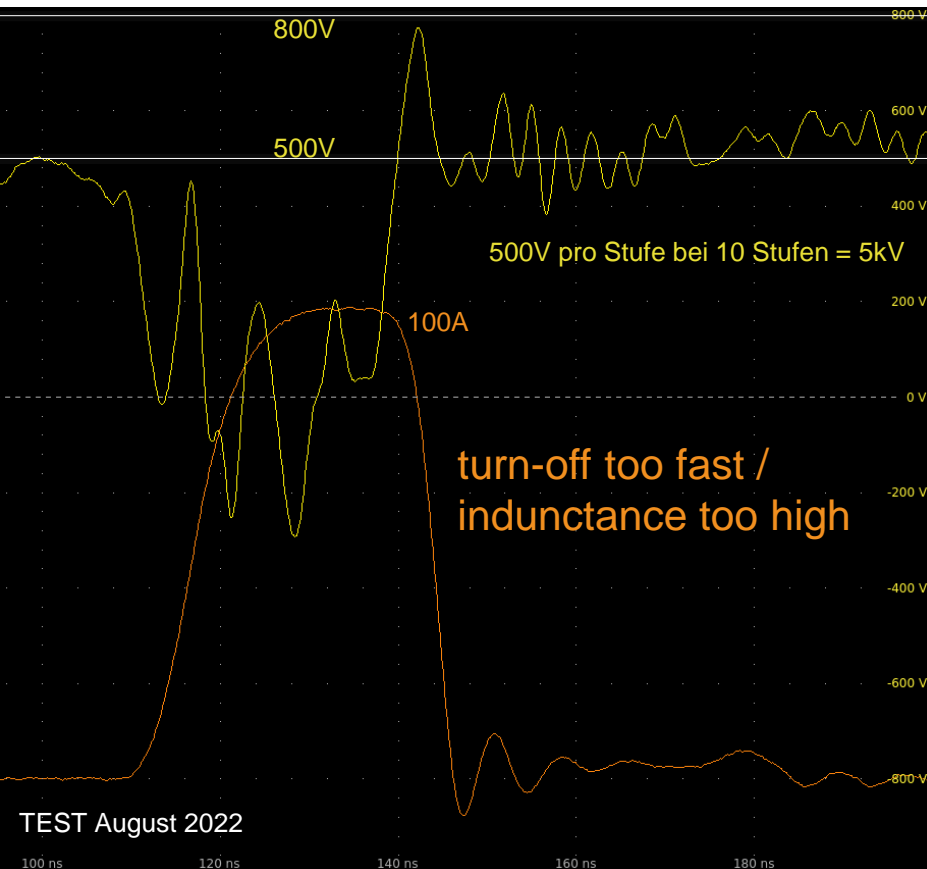
the turn off voltage over the 8 MOSFETs is not the same



XFEL dump pulser

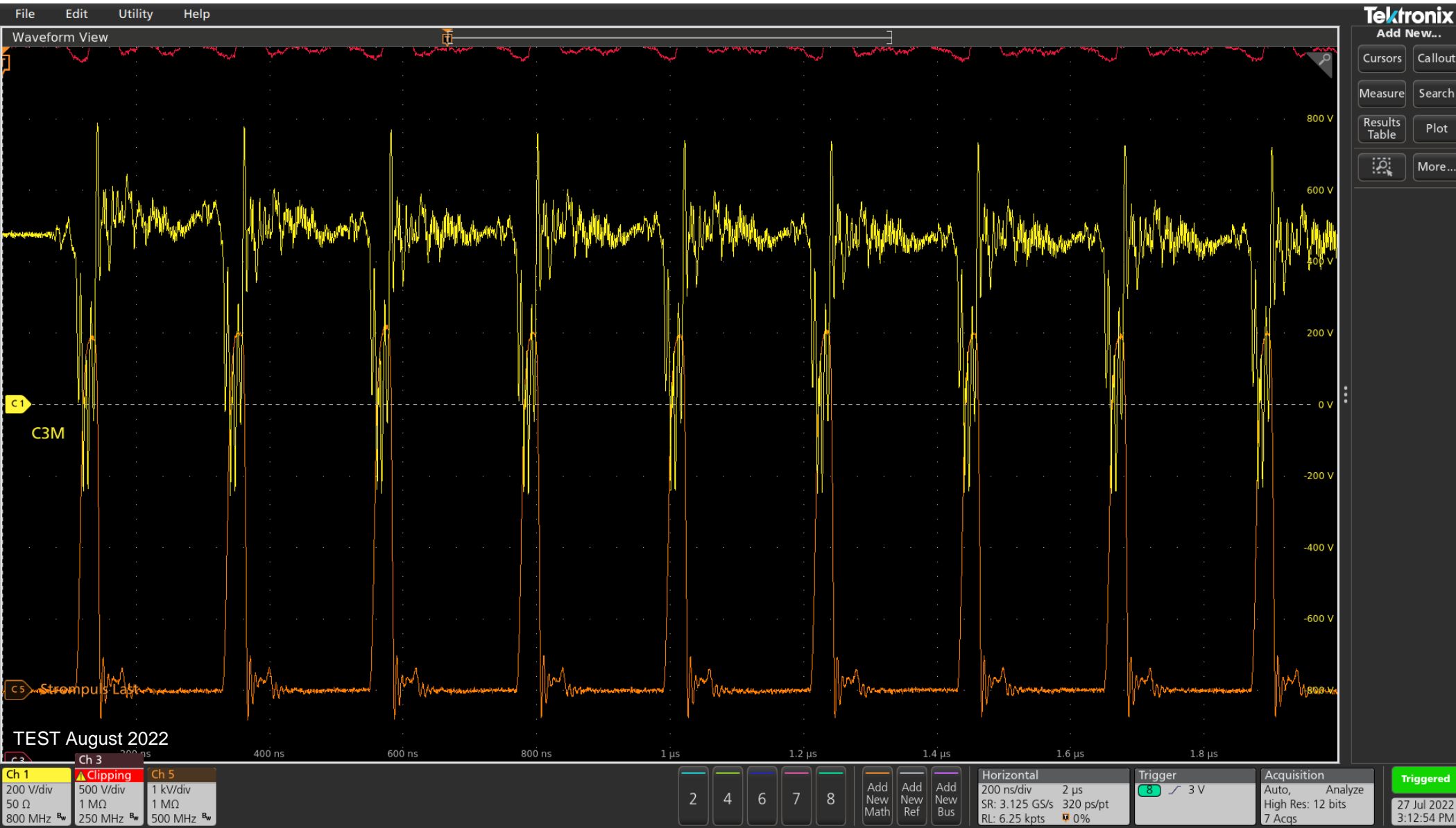
Measurements – 5000V with 8 MOSFETS in series

cooling is difficult without parallel MOSFETs



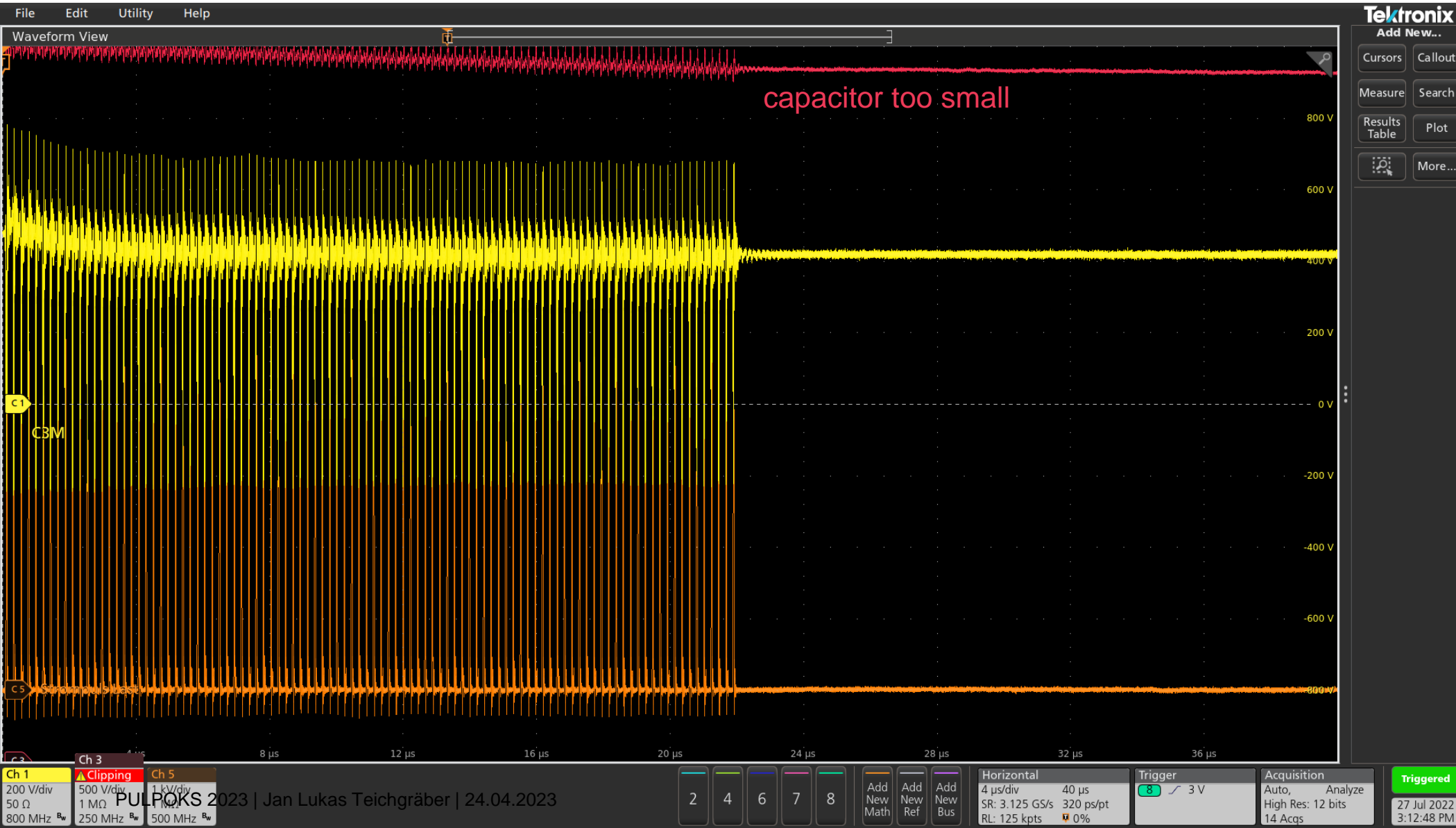
XFEL dump pulser

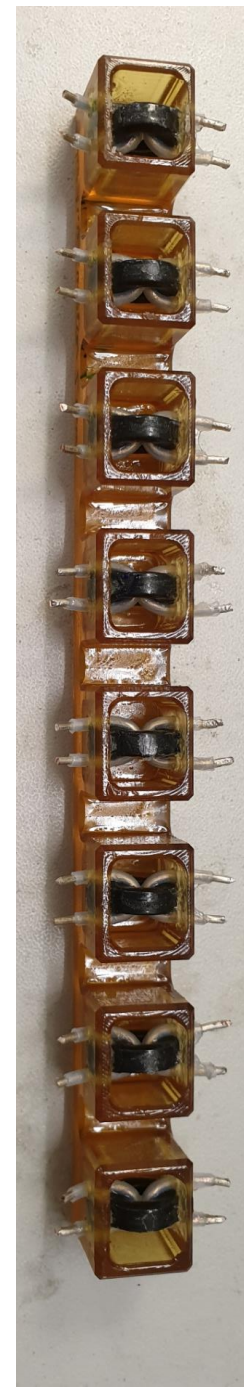
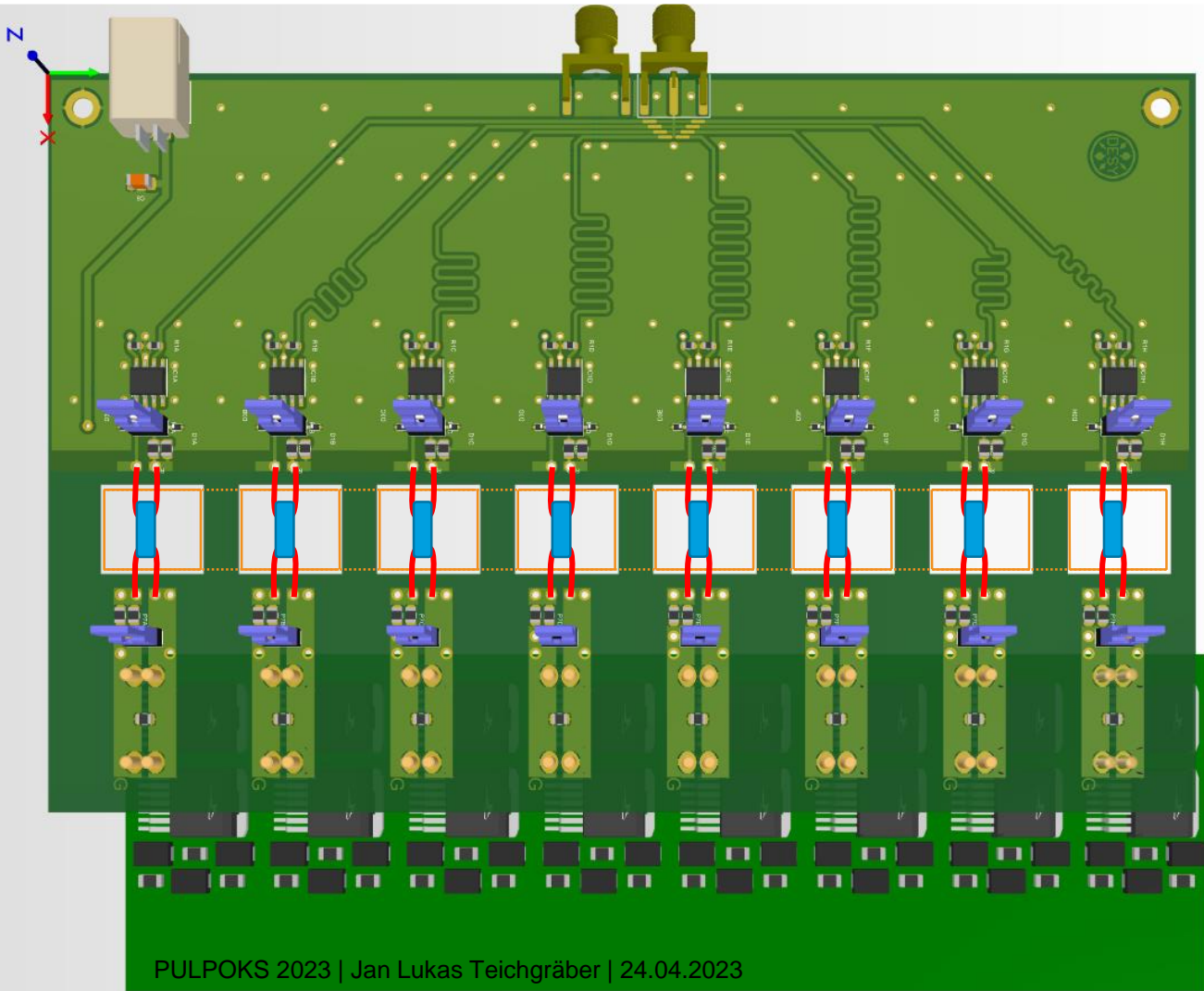
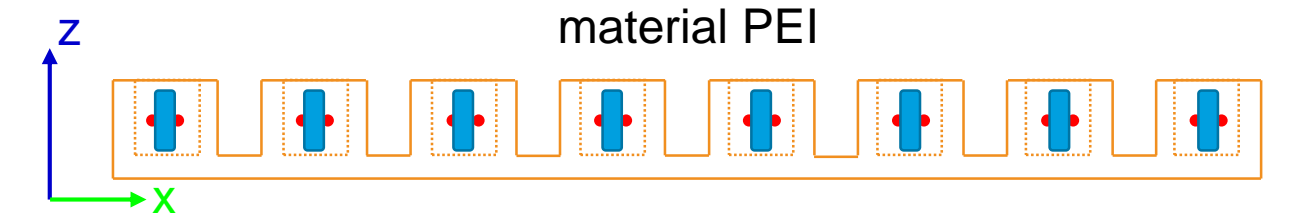
Measurements – 5000V with 8 MOSFETS in series



XFEL dump pulser

Measurements – 5000V with 8 MOSFETS in series



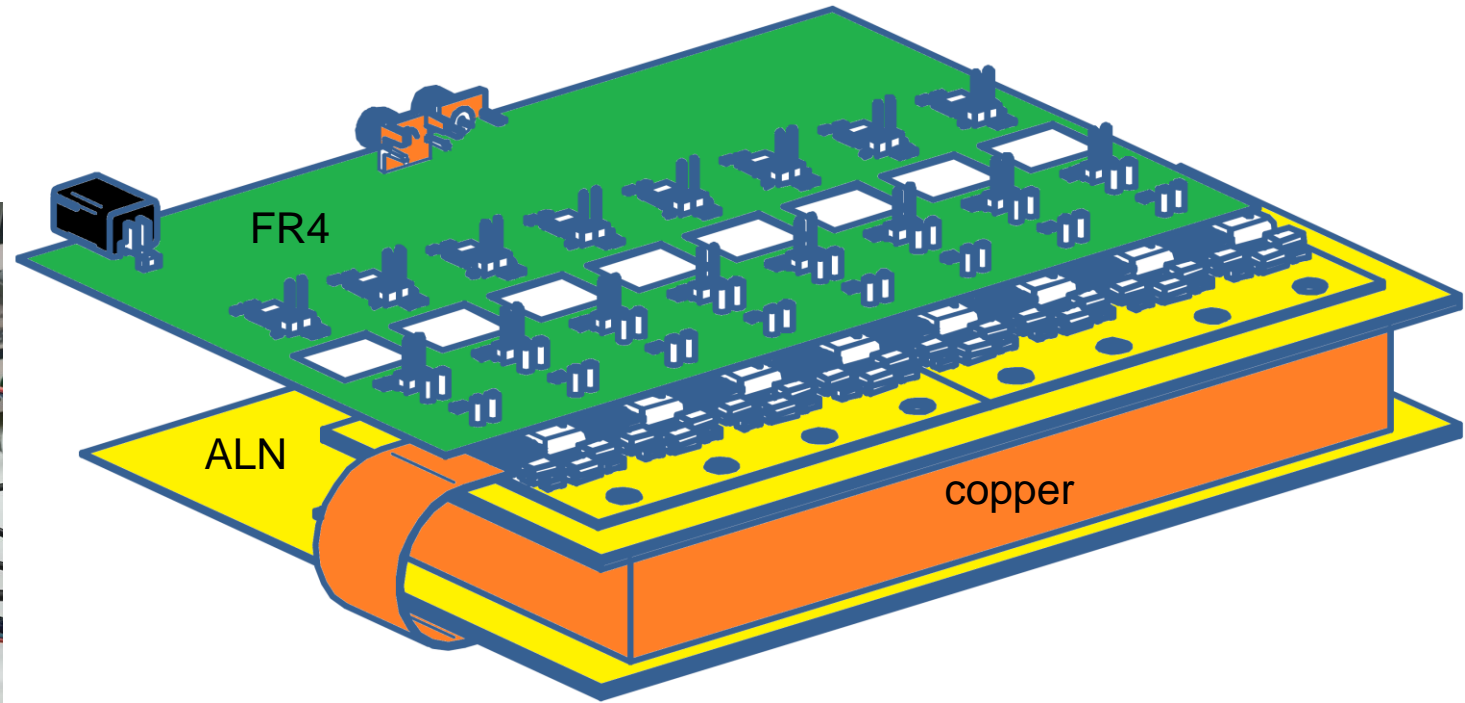
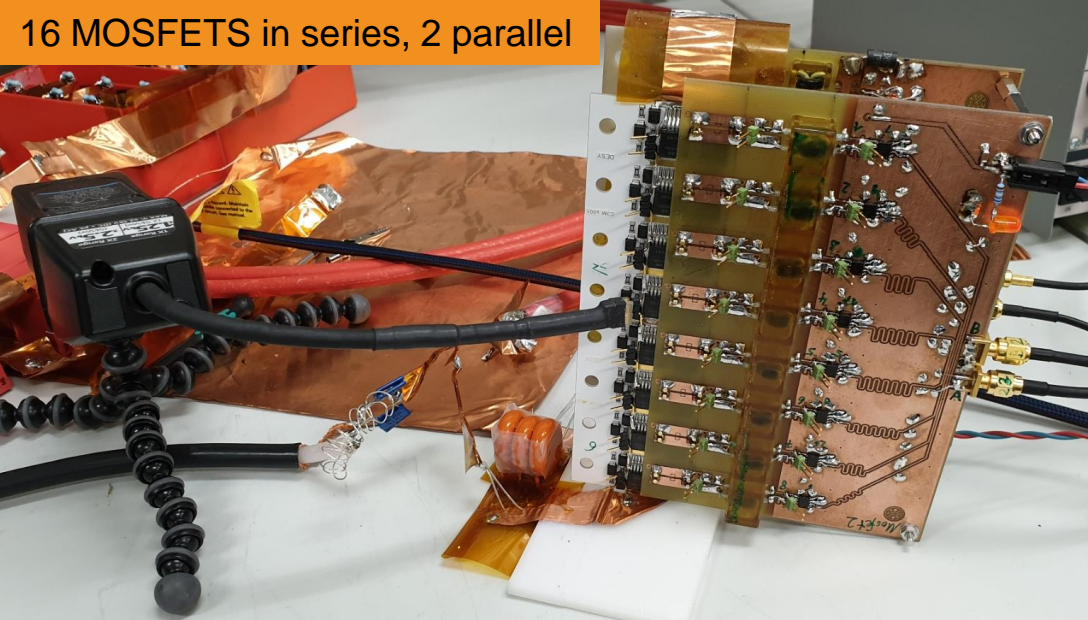


ferrites are glued in the holding device for reliable placement and high isolation

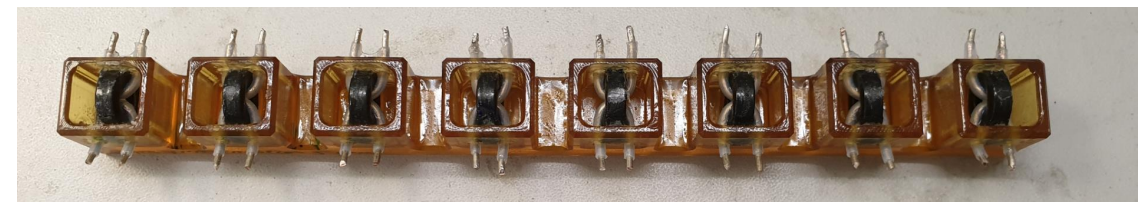
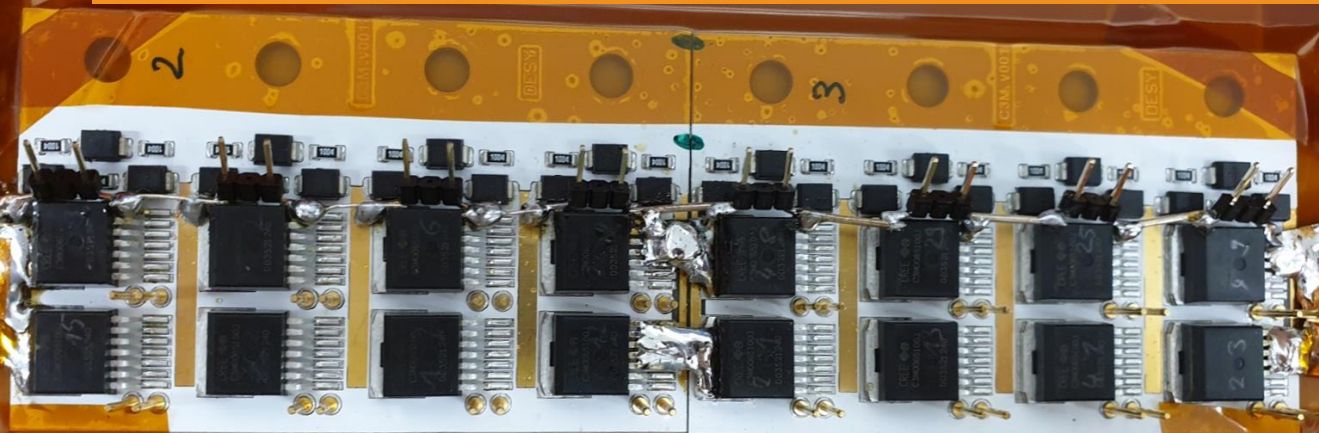
XFEL dump pulser

Development of a Mosfet Stack

16 MOSFETS in series, 2 parallel



Aluminium nitride PCBs mounted on a copper block for cooling



Summary

- The current design looks promising.
 - Several days of 5kV operation have been achieved with the current prototype
 - Can the prototype handle 27000 bunches per second?
 - More capacitors and a bigger power supply necessary
 - Oil isolation is still on the table
- Higher voltages only with reduced inductance of the pulser
 - More than 10kV are probably troublesome due to the high timing requirements
 - Higher voltage MOSFETS to reduce number of stages
- Higher voltage per pulser reduces the number of pulsers and reduces redundancy

***Thank you for
your
attention!***

Contact

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