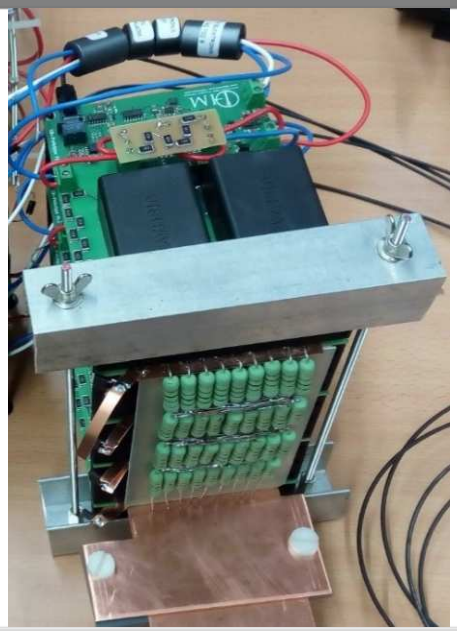
Karlsruher Institut für Technologie

A Solid State Pulse Generator for Driving Kicker Magnets

Martin Sack, Dennis Herzog, Martin Hochberg, Georg Müller (KIT/IHM)

Gregor Loisch, Frank Obier (DESY, Hamburg)

Institut für Hochleistungsimpuls- und Mikrowellentechnik



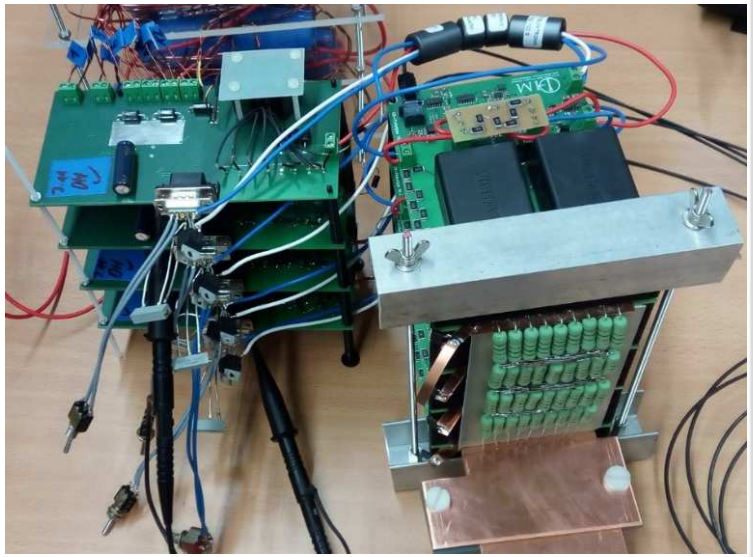
Outline of the Project

(Cooperation project with DESY, Hamburg).

- Design and setup of a solid-state pulse generator for driving a stripline kicker
- Goal for the generator design:
  - Ground-symmetric pulse generation (+/- 7 kV)
  - Load impedance 50 Ohm
- Status of the project: Component design

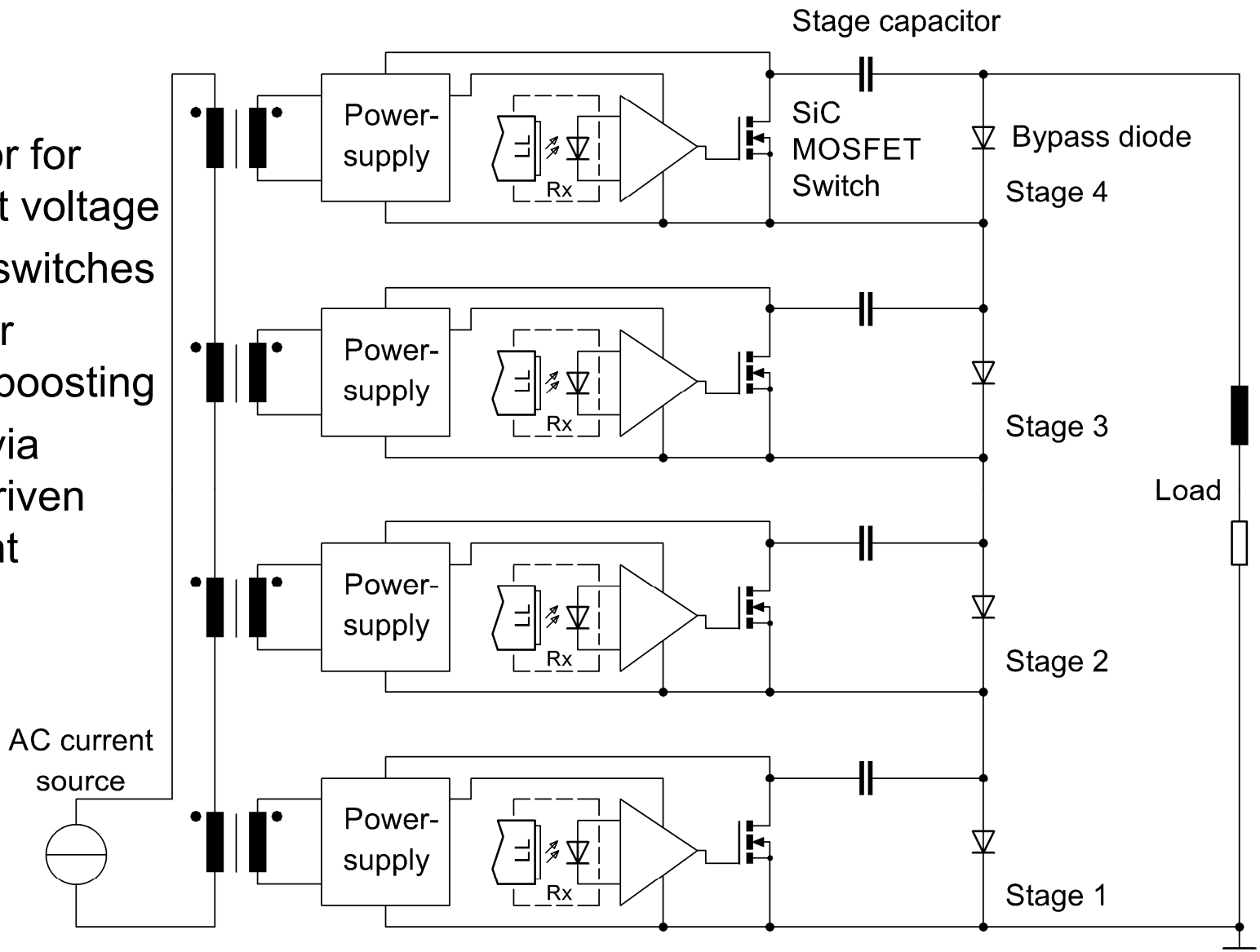
Outline of the Talk

- 4-stage pulse generator setup for design evaluation and components testing
  - Pulse generator with transformer-coupled power supply
  - SiC-MOSFET switch featuring capacitively coupled gate-boosting
- Gate-boosting circuit for GaN-HEMT
- Summary

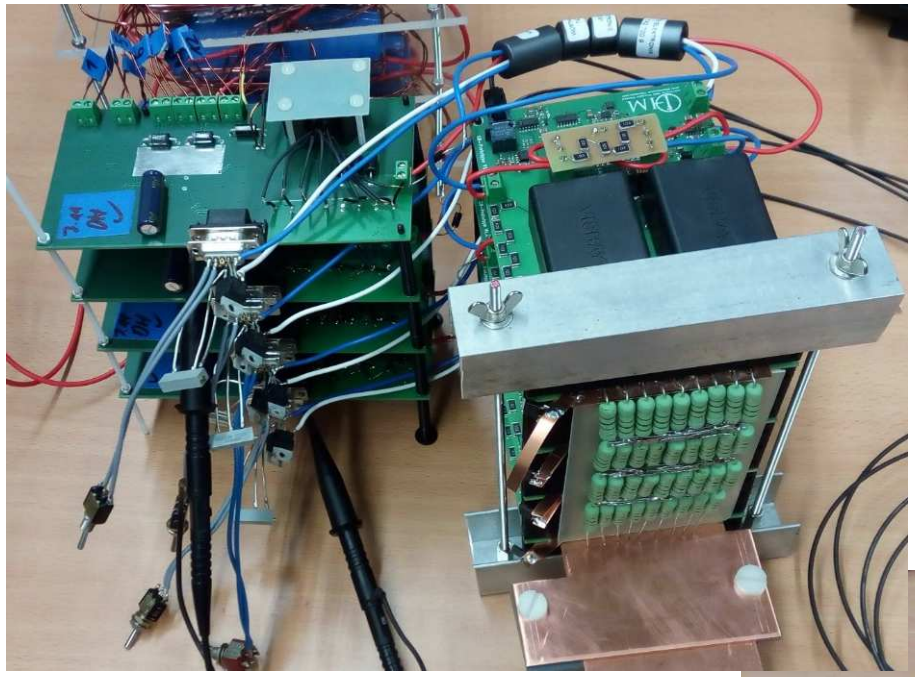


Generator for Design Evaluation and Component Testing

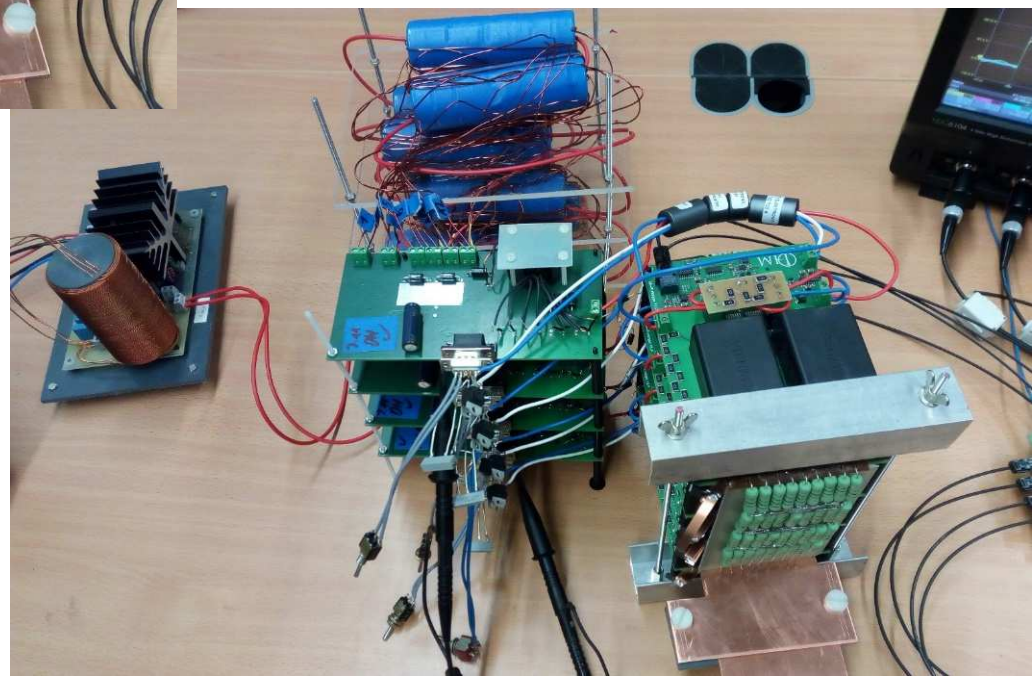
- 4-stage setup
- Pulse generator for negative output voltage
- SiC-MOSFET switches
- MOSFET driver featuring gate-boosting
- Power supply via transformers driven from AC current source.



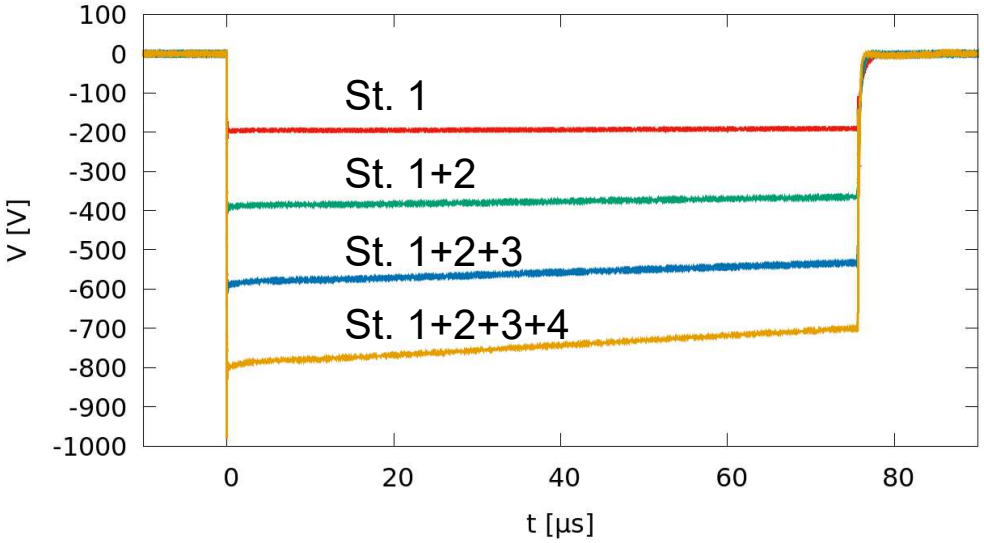
Setup of the Generator



- Stacked switch units connected to stacked power supply units.
- Resistive load R = 44 Ohm
- AC current source (I = 7 A)
- Primaries of transformers connected in series
- Control of switches via fiber-optic link

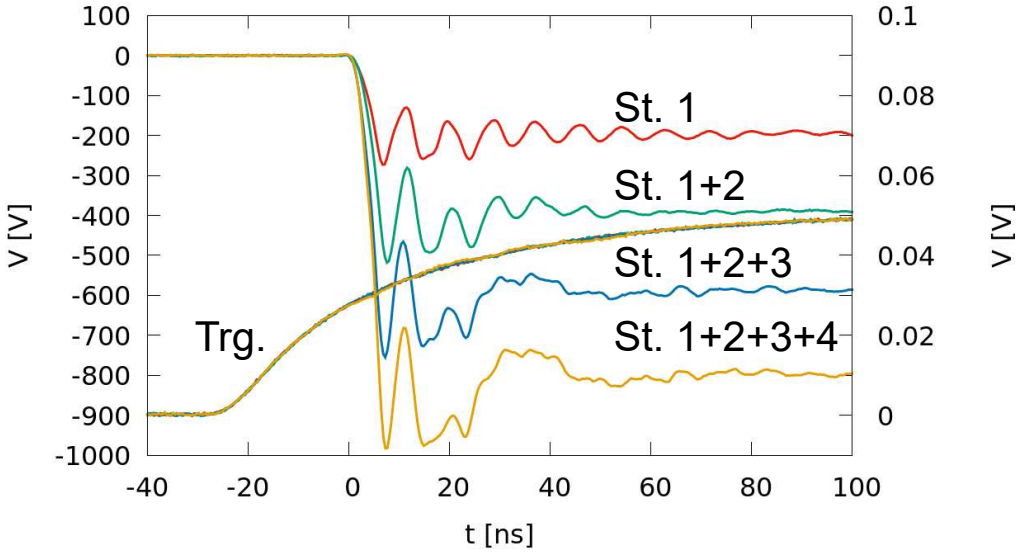


Operation of the Pulse Generator



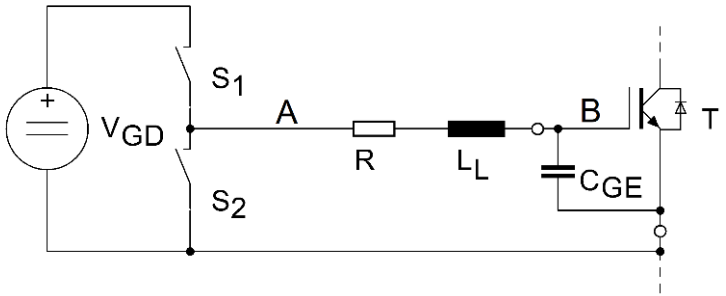
- Operation of one up to four stages
- Charging voltage per stage: 200 V
- Pulse length: 75 µs
- Rectangular pulse shape
- Voltage droop due to discharge of capacitors

- Pulse rise time: less than 5 ns
- Trigger signal occurs approximately 25 ns before begin of pulse generation

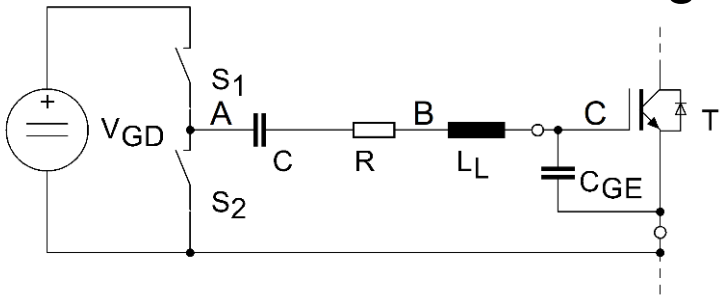


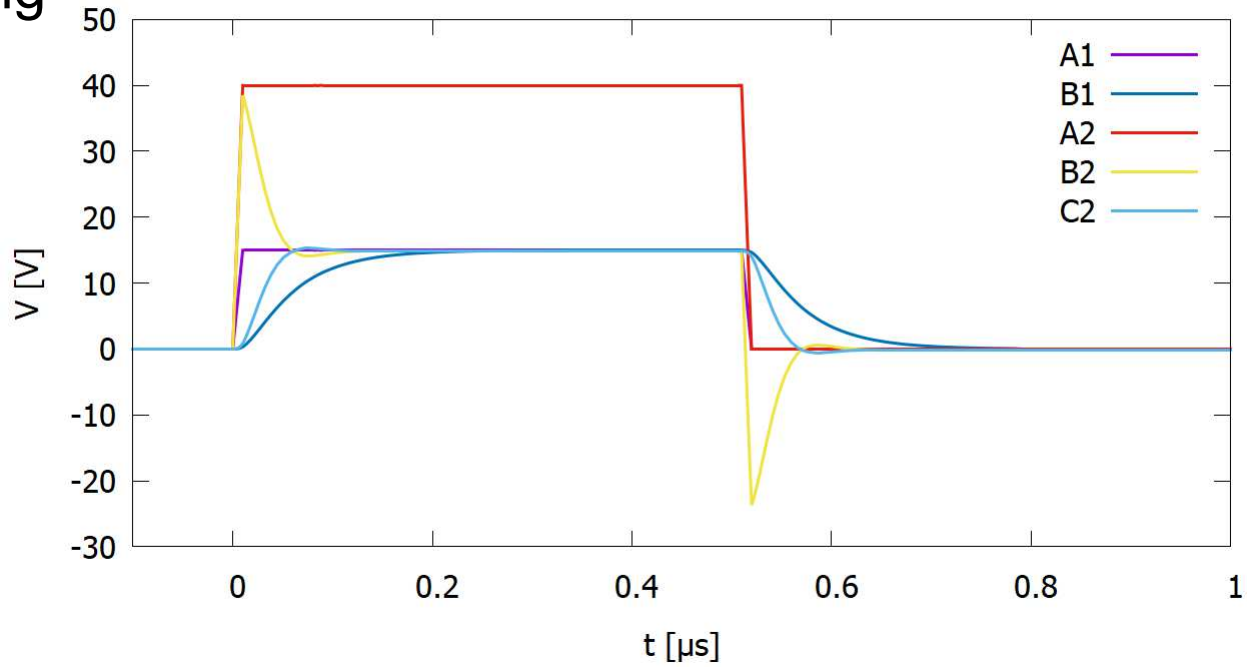
Capacitively Coupled Gate Boosting Circuit

1. Gate driver without boosting



2. Gate driver with boosting

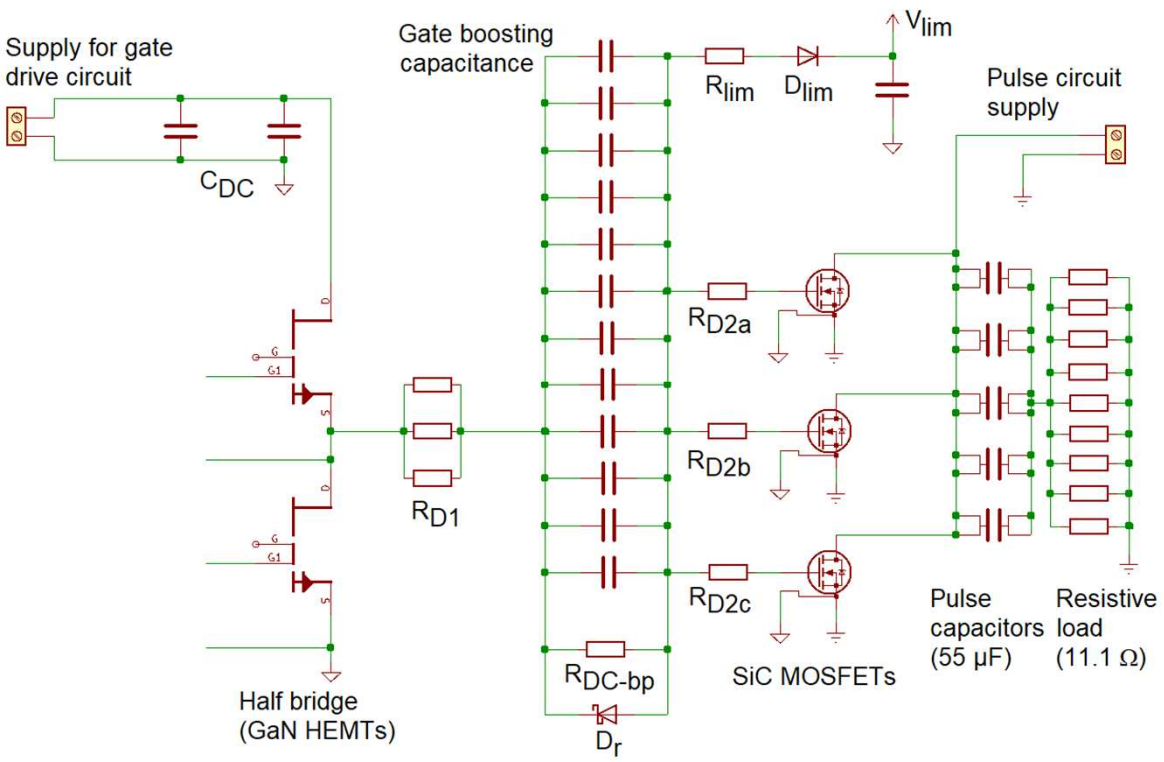




- Inductance of leads form together with R and C_{GE} a resonance circuit increasing the time for gate charging
- An additional capacitor C in series reduces the capacitance and, hence, increases the resonance frequency
- An increase in the driving voltage V_{GD} compensates for the voltage drop across C

Pulse Circuit Comprising SiC-MOSFET Switches

- Design goals:
  - Pulse voltage: 1 kV
  - Pulse current: 90 A
  - Resistive load

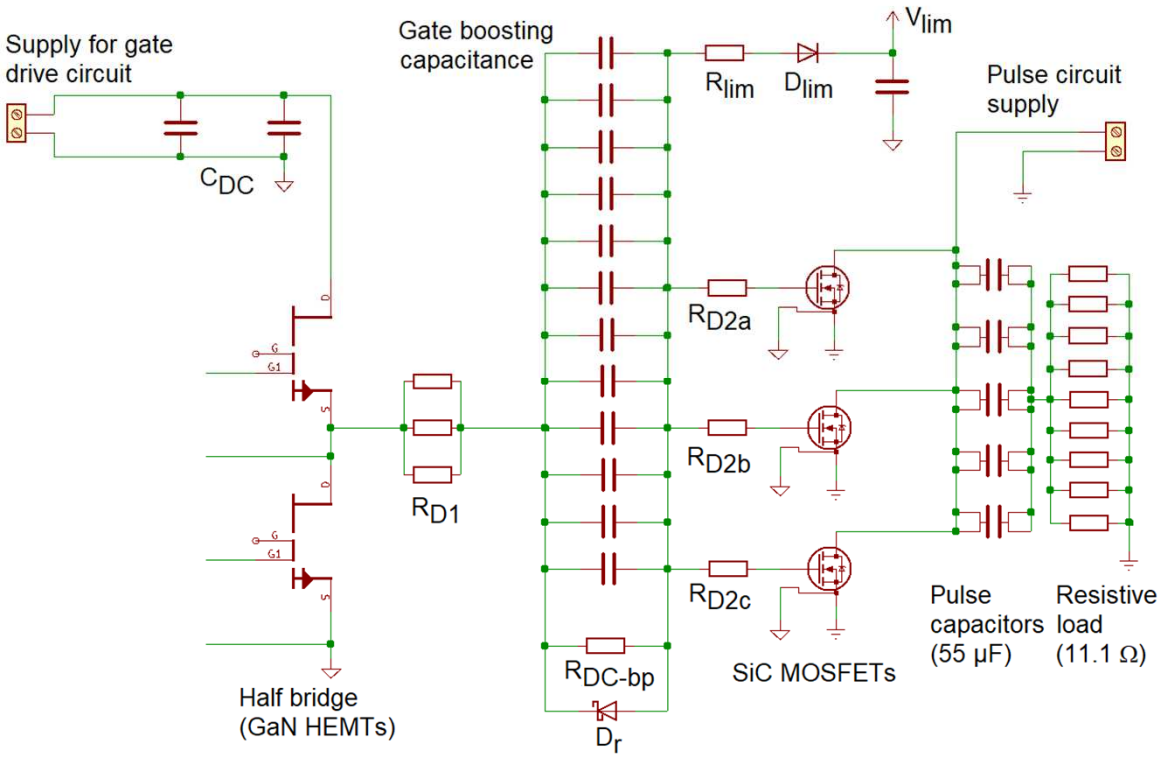


Simplified circuit diagram.

- SiC-MOSFETs
  - $V_{DS,max}$: 1.2 kV
  - I_D: 30 A
  - Parallel configuration of 3 MOSFETs
- Pulse capacitors
  - Total capacitance: 55 µF
  - Parallel configuration of 5 capacitors
- Load resistor
  - R = 11.1 Ω
  - Parallel configuration of 9 resistors

Gate-drive Circuit

- Design goals:
  - Rise time: 5 ns
  - Driving current: 30 A
  - Driving voltage: 150 V



Simplified circuit diagram.

- GaN-HEMT Switches
  - Rise time: 4 ns
  - I_D: 30 A
  - $V_{DS,max}$: 650 V
- Half-bridge configuration with integrated half-bridge driver
- Gate boosting capacitance 816 pF

Sack M.; Hochberg, M.; Herzog, D.; Müller, G.: Fast SiC-MOSFET Switch with Gate Boosting Technology, *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Online, 2021, pp. 1-7. https://ieeexplore.ieee.org/document/9472228

Printed Circuit Board Layout

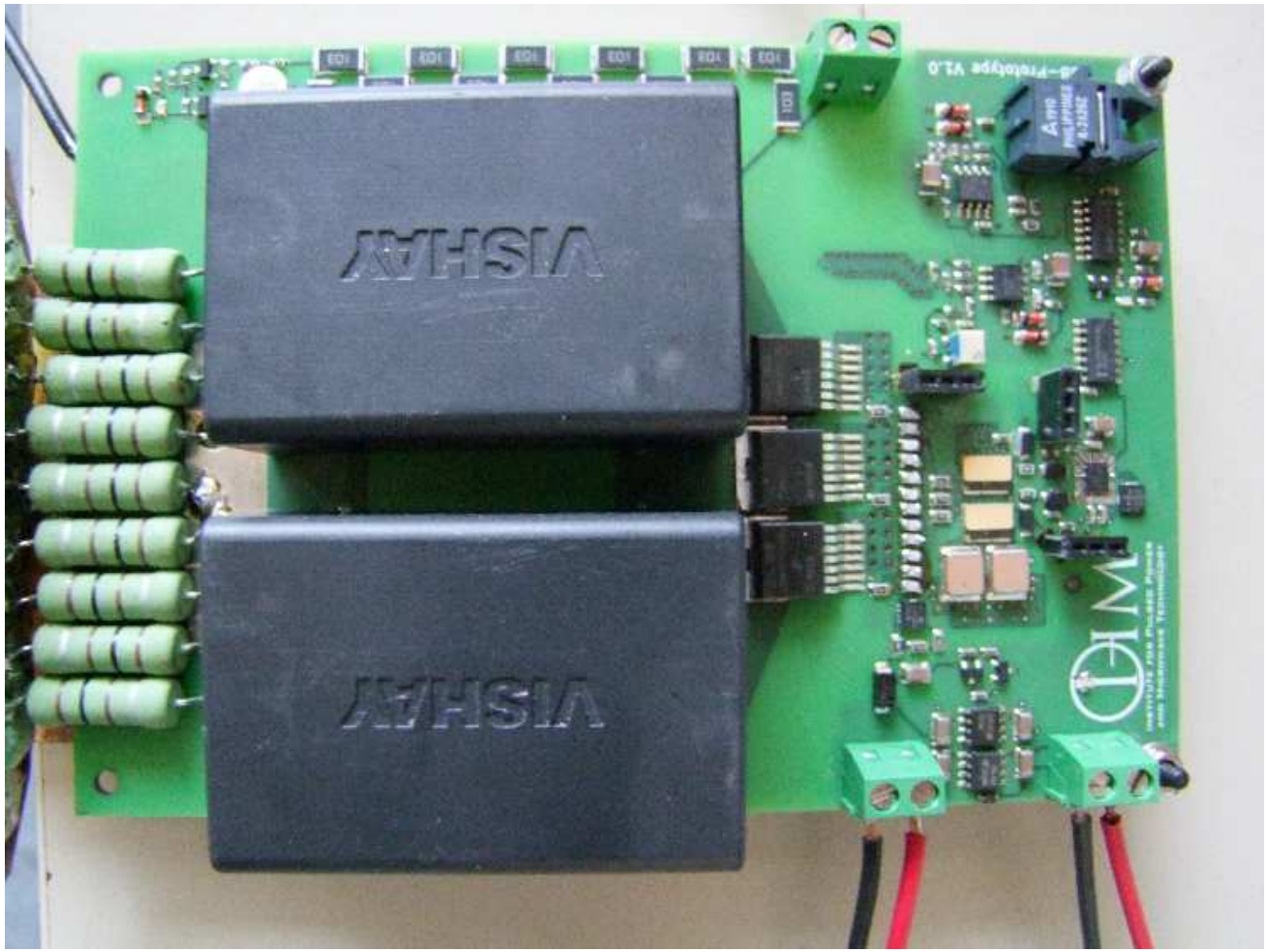
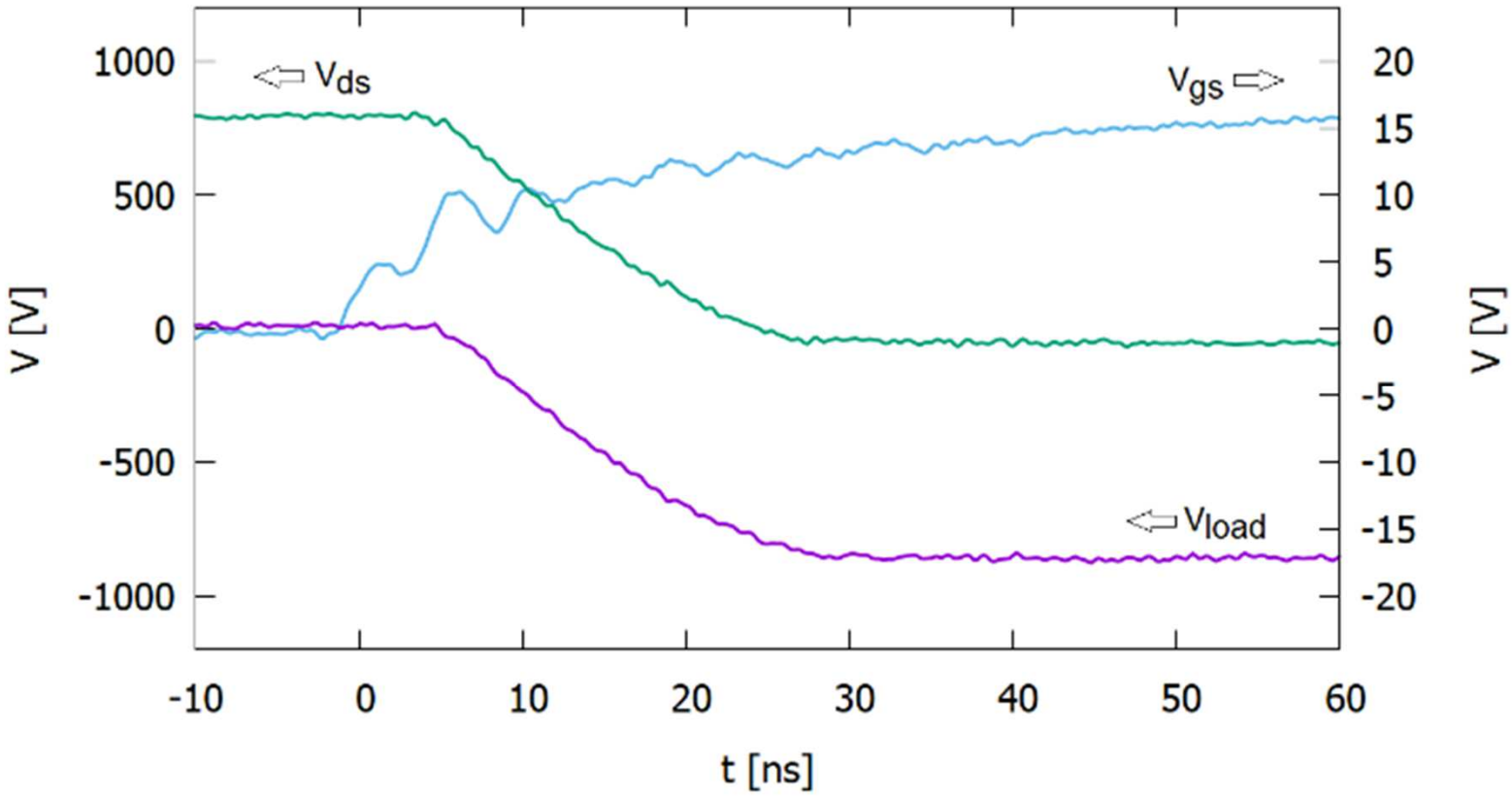


Photo of the test setup.

- Pulse circuit with low inductance:
  - parallel configuration of 5 capacitors (3.6 nH in total)
  - Ground plane and microstrip line (3.9 nH)
- Rise time $\tau = L/R = 0.7$ ns
- Gate drive circuit triggered via fiber-optic link

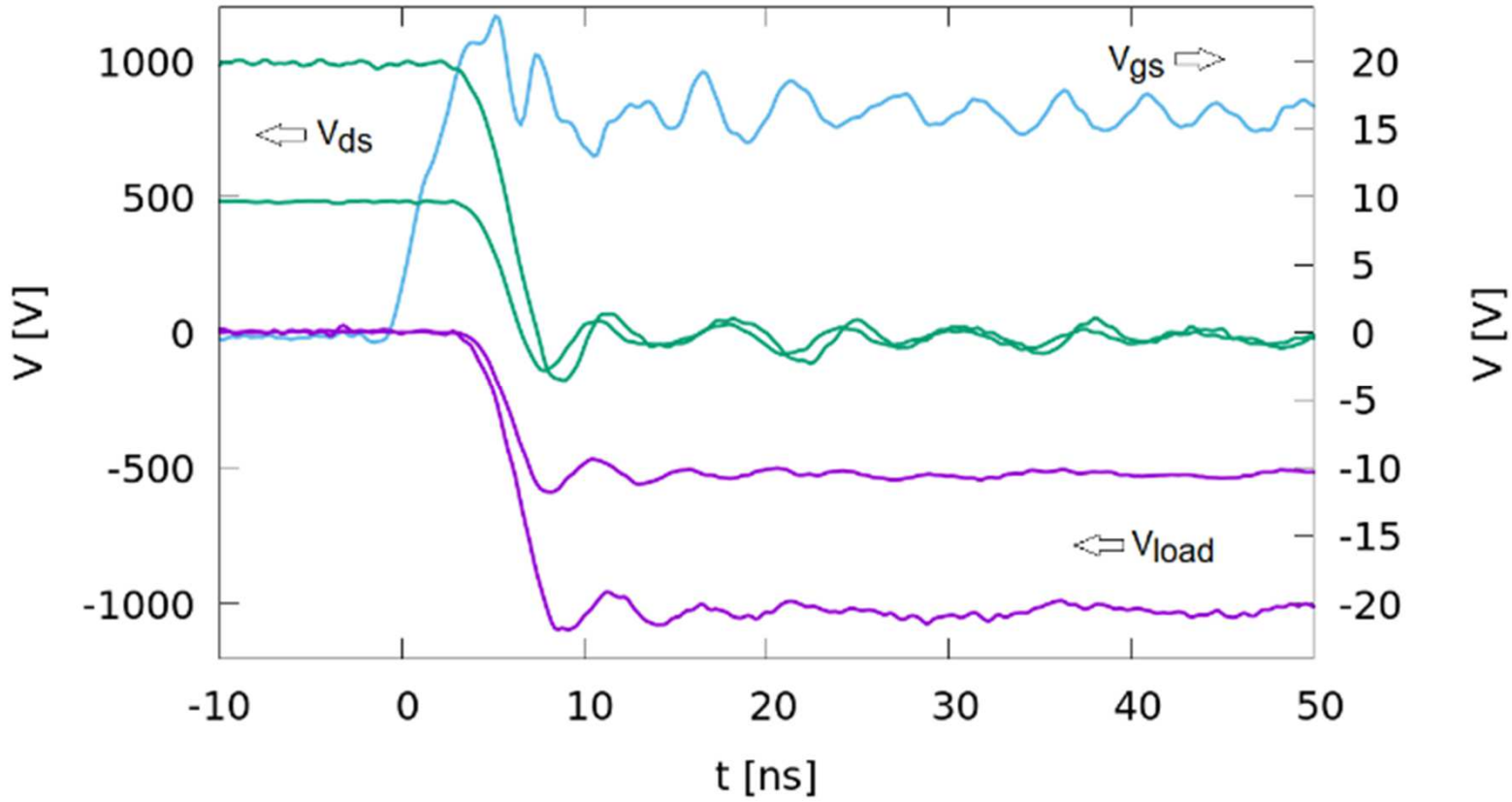
Operation Without Gate-Boosting at 800 V



V_{gs}, V_{ds}, and V_{load} while switching a voltage of 800 V without gate boosting.

- Rise time according data sheet: 15 ns (@ V_{ds} = 800 V, I_D = 20 A)
- Measured rise time: 14.7 ns (@ V_{ds} = 800 V, I_D = 24 A per transistor)

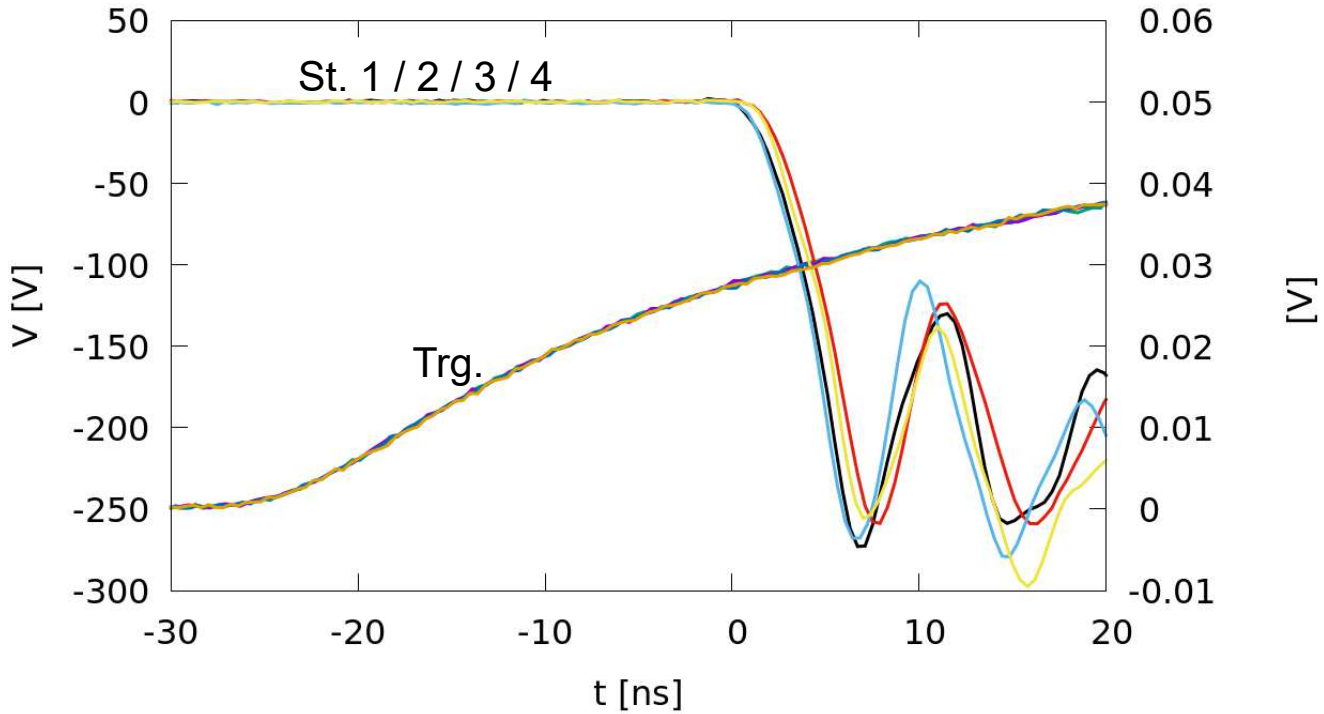
Operation with Gate-boosting



V_{gs}, V_{ds}, and V_{load} with gate boosting, charging voltage 500 V and 1000 V. (gate-boosting capacitance: 816 pF, driving voltage: 150 V).

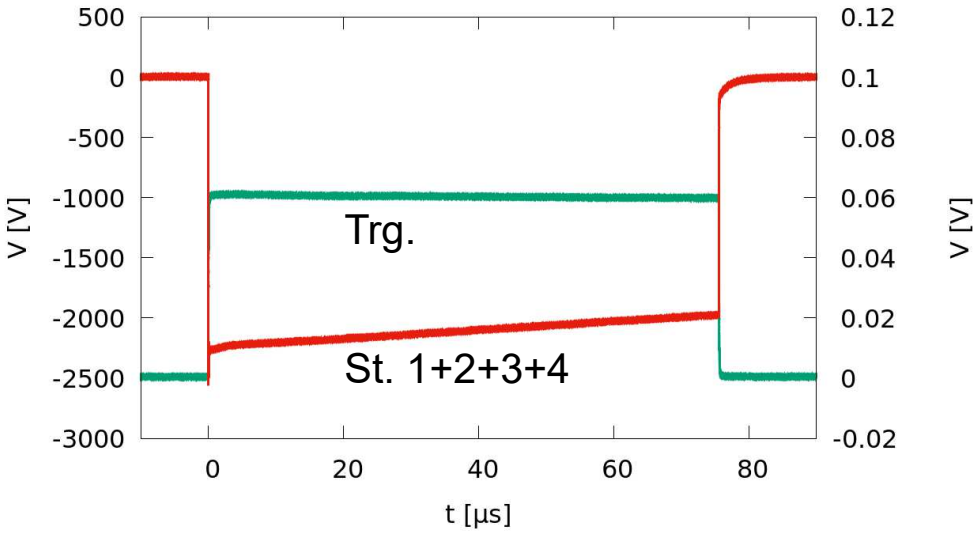
- Driving voltage of 150 V.
- Measured rise time at the load: 2.4 ns (@ 500 V), 3.3 ns (@ 1000 V)

Synchronisation of Stages



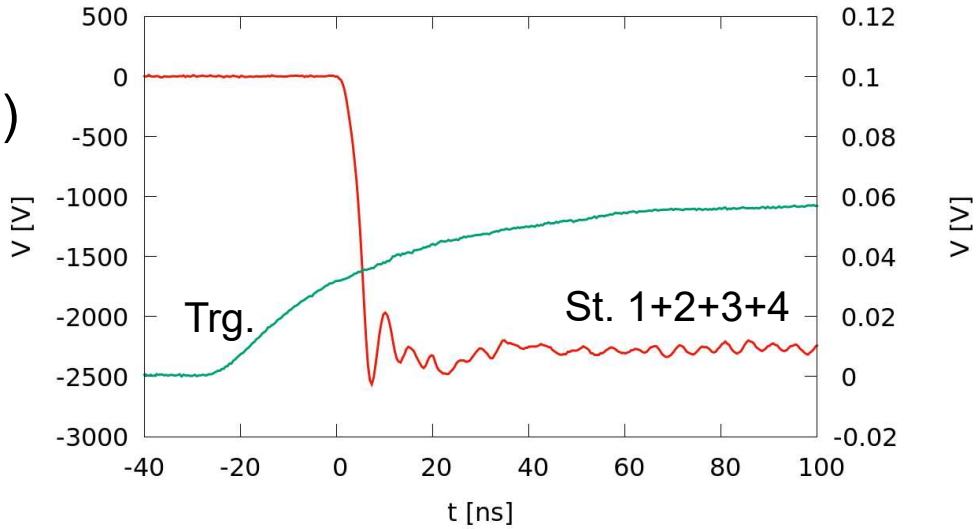
- Operation of single stages one after the other
- Trigger signal is well aligned
- Delays vary by 1 ns

Operation of the Pulse Generator



- Operation of four stages
- Charging voltage per stage: 600 V
- Pulse length: 75 µs
- Rectangular pulse shape
- Voltage droop due to discharge of capacitors

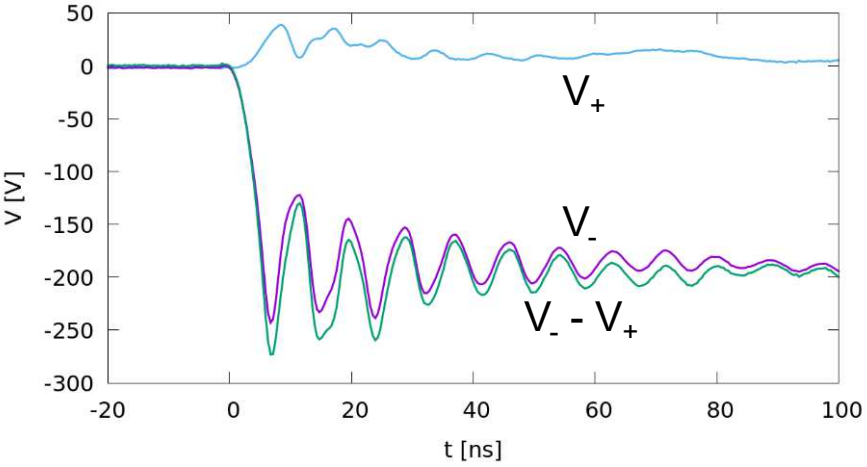
- Pulse amplitude: 2.4 kV
- Pulse rise time: 3.9 ns (10% -> 90%)
- Trigger signal occurs approximately 25 ns before begin of pulse generation



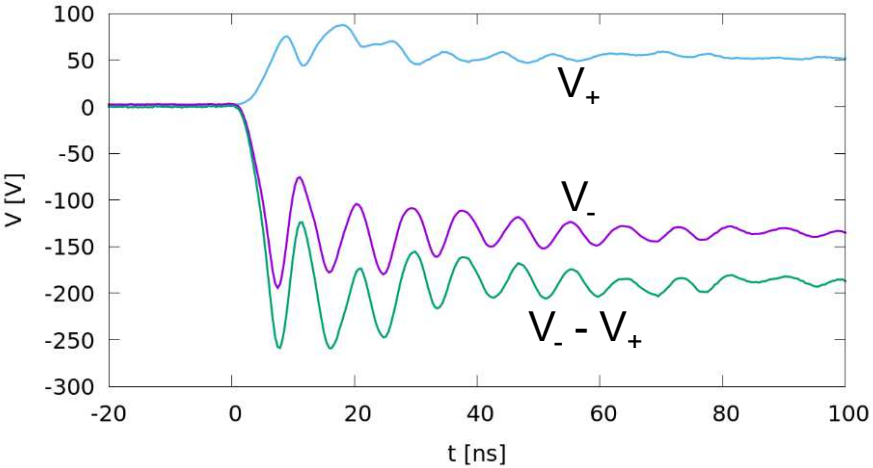
Floating Operation of Single Stages

Connection of the generator output to ground potential has been removed.
Voltage measurement at the output terminal with respect to far ground potential.

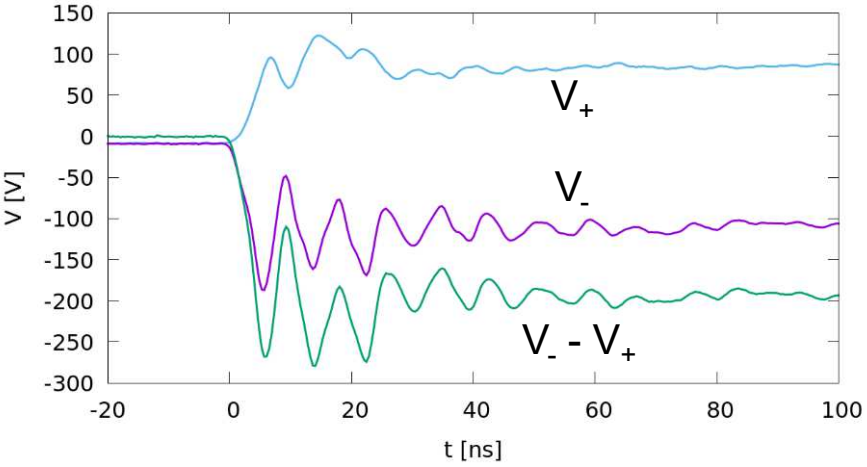
Top stage is active.



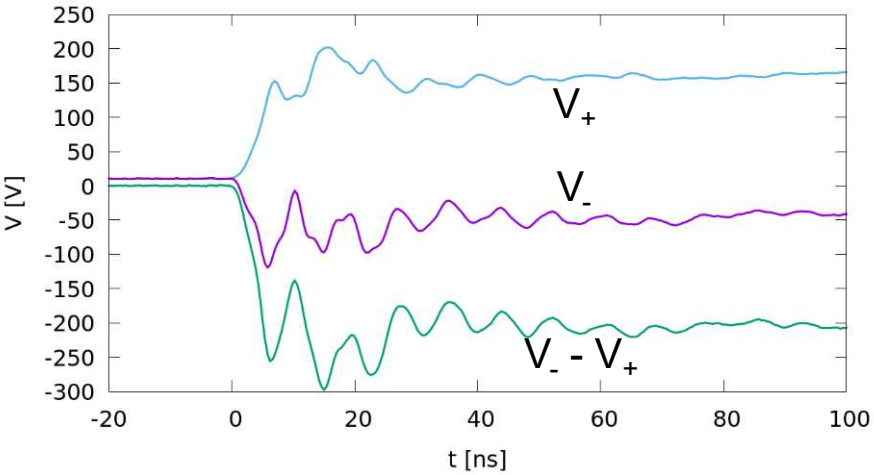
Stage below top stage is active.



Stage above bottom stage is active.

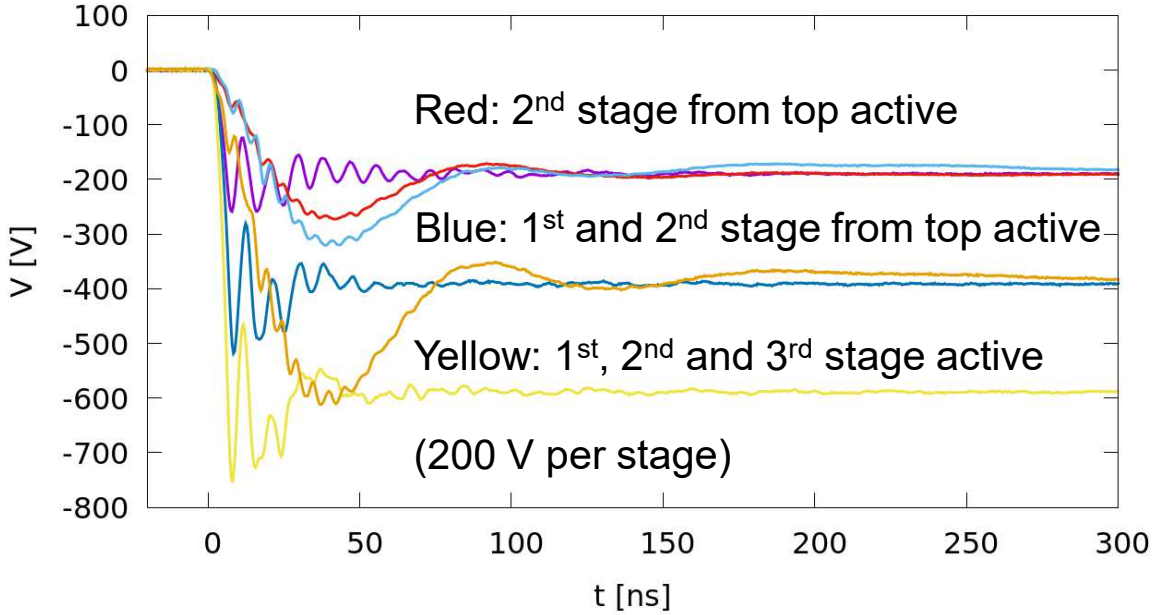


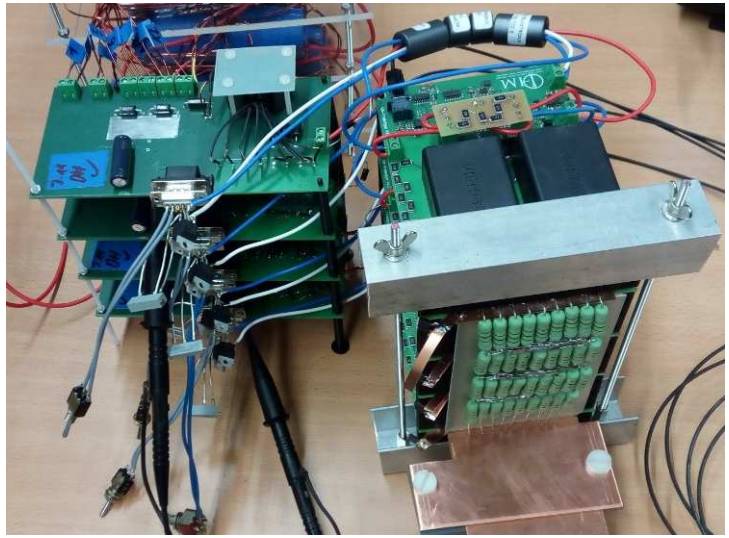
Bottom stage is active.



- Voltage distribution between the pins V_+ and V_- versus far ground potential is governed by stray capacitances with respect to the active stage.

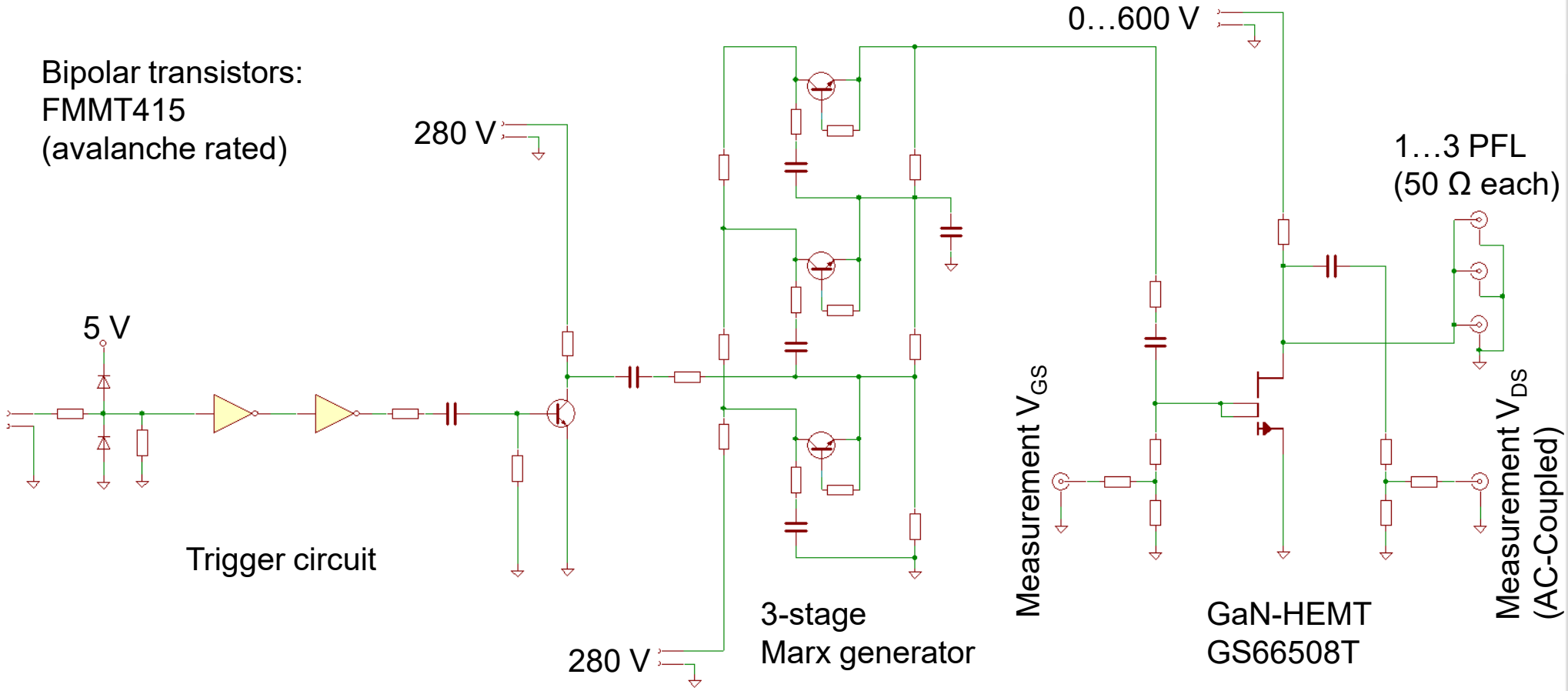
Pulse Voltage Measurement at Power Supplies





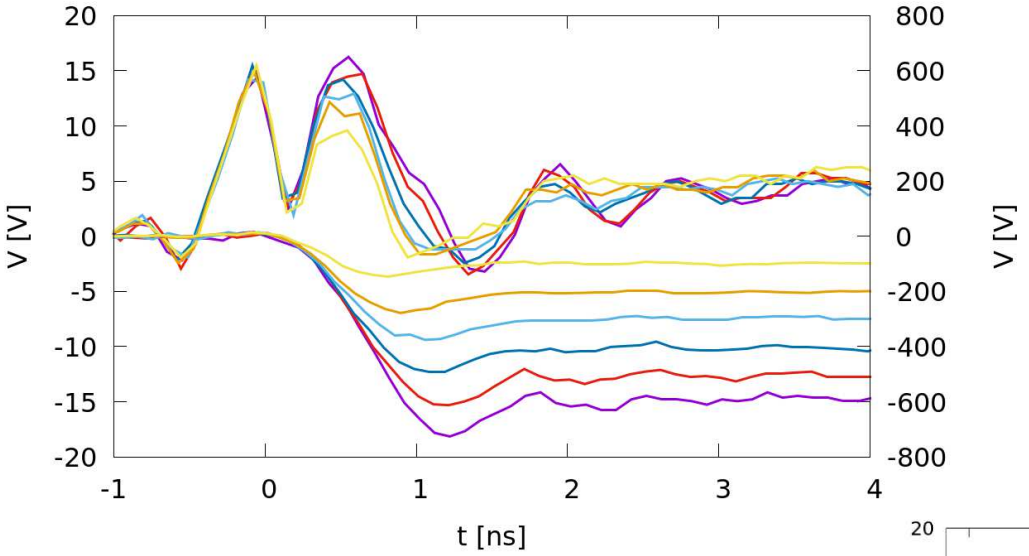
- Voltage measurement between ground planes of top and bottom power supply
- Signals at power supply stack low-pass filtered
- Ferrite rings across the connecting cables serve as current-compensated chokes
- Stray capacitances at the power supply stack and the common-mode impedance of ferrite rings form low-pass filter

Gate-boosting Circuit for GaN-HEMT



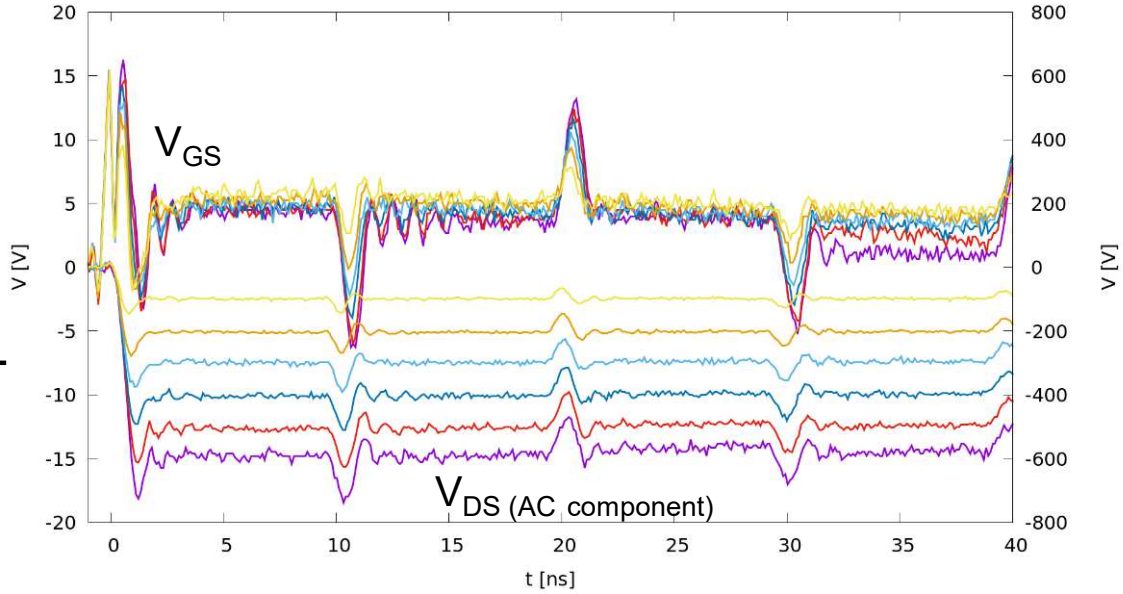
- 3-stage Marx circuit with avalanche transistors as switches
- Pulse-forming lines with open end (total impedance: 50 Ω, 25 Ω, 16.6 Ω)
- Measurement of gate-source voltage and AC component of drain-source voltage

Tests with 50 Ohm Load Impedance

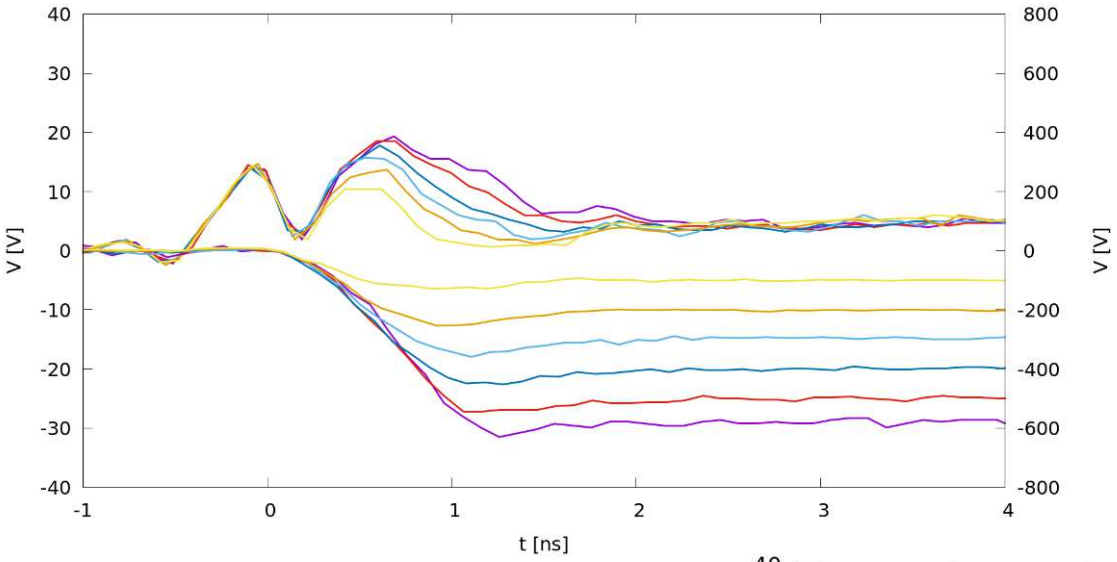


- Simultaneous measurements of gate-source voltage and AC components of drain-source voltage
- V_{DS} varied between 100 V and 600 V

- Rise time of V_{DS}: 586 ps (10% -> 90%)
- Travelling-wave oscillation: T = 4 x 5 ns = 20 ns (l = 1m)
- Current flow through GaN-HEMT in both directions

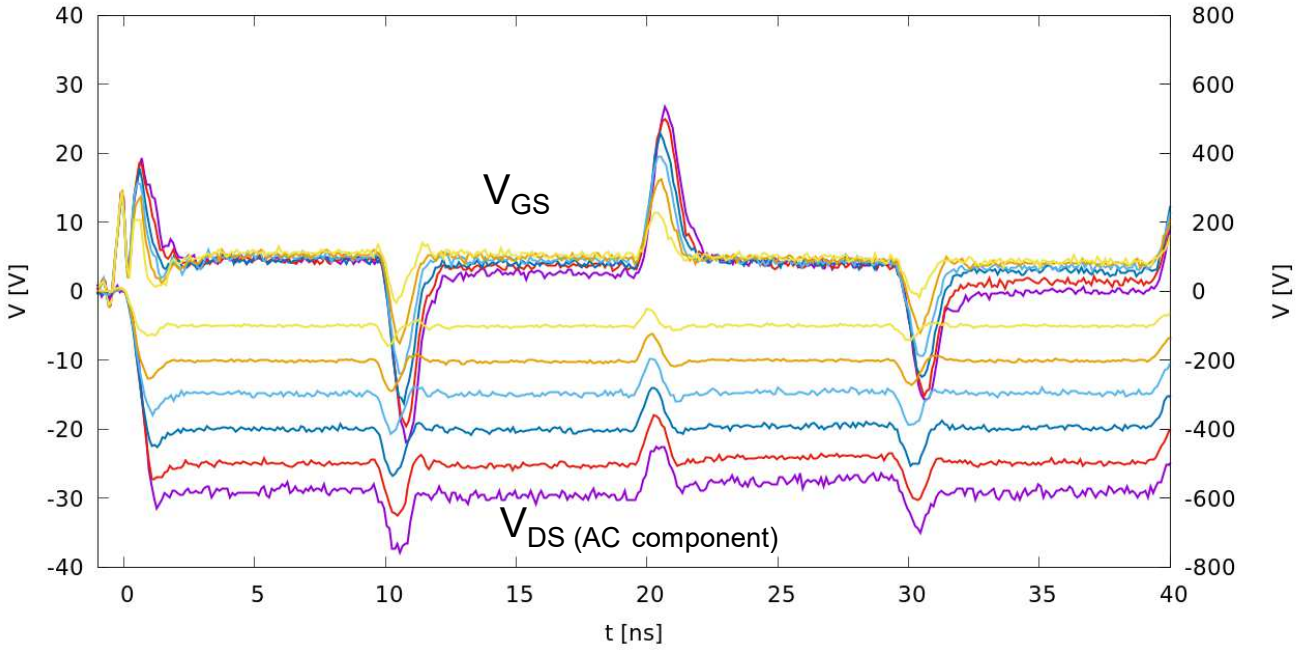


Tests with 16.6 Ohm Load Impedance



- Simultaneous measurements of gate-source voltage and AC components of drain-source voltage
- V_{DS} varied between 100 V and 600 V

- Rise time of V_{DS}: 691 ps (10% -> 90%)



Summary

- 4-stage pulse generator setup for design evaluation and components testing
  - Fast SiC-MOSFET switch
  - Gate boosting enables rise time of less than 5 ns for a single stage
  - Fiber-optic transmission of trigger signals: Mismatch of propagation delay: 1 ns
  - Power supply via transformers
- Gate-boosting circuit for GaN-HEMT
  - Pulse rise time of 691 ps @ 16.6 Ohm and 586 ns @ 50 Ohm measured.