Ultra-fast generator for impact ionization triggering

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Abstract

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In recent years, it has been discovered that **triggering thyristors in impact ionization** mode can greatly boost their dI/dt capability, by up to three orders of magnitude. This innovative triggering method involves applying a high overvoltage with a slew rate >1 kV/ns on the thyristor's anode-cathode. The use of compact pulse generators, based on commercial off-the-shelf components (COTS), would allow this technology to be used in various applications, including fast kicker generators for particle accelerators.

Our approach for a compact pulse generator starts with a high-voltage SiC MOS with an **ultra-fast super-boosting gate driver**. Super boosting the gate of a 1.7 kV rated SiC MOS can reduce its rise time by a factor of approximately 30 (datasheet tr = 20 ns vs measured tr < 680 ps), resulting in an output voltage slew rate >1 kV/ns and an amplitude >1 kV.
Here we present an upgraded board design with a higher current output capacity.

Introduction

Thyratrons are currently used to produce high voltage and current levels in particle accelerator facilities, but they have various drawbacks, making it necessary to consider alternatives.

Recent studies have shown that **thyristors switched in impact ionization mode could replace thyratrons**, and they offer advantages such as lower cost and higher current density.

Previous triggering generators for impact ionization are not commercially available (DSRD, SOS), require bulky designs, and have relatively long pre-charging phases, so **a new approach using COTS in a compact topology** is proposed.

The triggering circuit needs to apply a voltage on the anode-cathode of the thyristor that exceeds twice its static breakdown voltage, and a slew rate of over 1 kV/ns is required for the triggering voltage.

Our current focus is on enhancing the output voltage, slew rate, and current of the super-boosting driver to accelerate the commutation time of the SiC MOS and prepare the driver for higher MOS gate loads.

Results

The different tests have been done using a 6 GHz oscilloscope with a series of 10-18GHz, 50 ohm attenuators used as output loads.

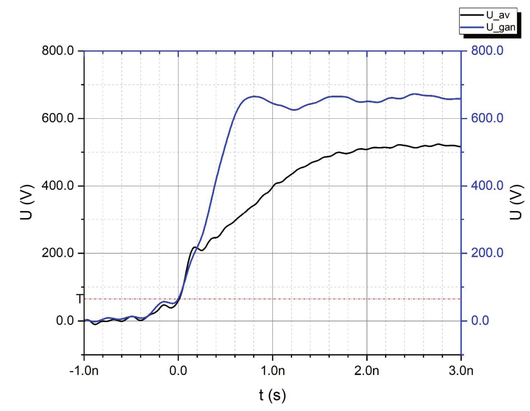

Figure 3: Output waveform of the second avalanche transistor (black) and the GaN FET (blue), respectively on a 50 ohm load.

Figure 3 shows the output voltage of the second avalanche transistor (TP1, C6 and R12 disconnected) compared to that of the output at the source of the GaN FET (TP2, C8 and R15' disconnected). Tests run independently.

2nd avalanche transistor:
- **520 V max**
- **Rise time 1.4 ns**

GaN FET at 690V:
- **670 V max**
- **1.1 kV/ns fastest section**

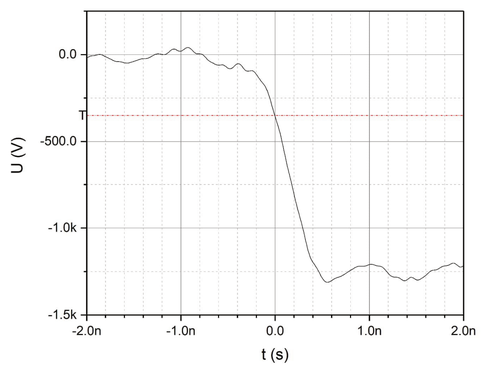

Figure 4: Output waveform of the 1.7kV SiC MOS on a 50 ohm load.

Figure 4 shows the output voltage of the SiC MOS (TP3, after C9), biased at 1.3kV.

- **550 ps rise time**
- **Accelerated 36x factor**
- **1.3 kV max amplitude**
- **2.2 kV/ns max slew rate**

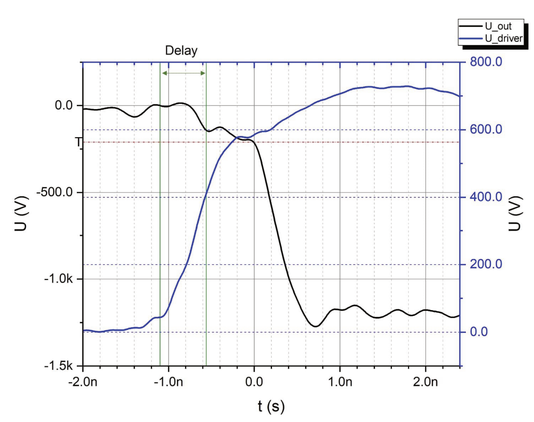

Figure 5: Output voltage of the 1.7kV SiC MOS (black) and 650V GaN FET (blue) on a 50 ohm load.

Figure 5 shows the output voltage of the GaN FET (TP2) and the SiC MOS (TP3), both measurements taken simultaneously.

GaN FET at 690V:
- **670 V max**
- **1.1 kV/ns fastest section**

SiC output at 1.3kV:
- **1.27 kV "max"**
- **2 kV/ns fastest section**

Methodology

In previous works we described a gate boosting technology for thyristor triggering that enhances the gate driver's maximum output voltage and output voltage slew rate.

This approach involves applying a significant overvoltage to the MOS gate during commutation time and then reverting to manufacturer-recommended specifications after completion. The rise time acceleration was found to be **a factor of approximately 30**, and a specialized driver was designed to deliver the necessary output voltage.

However, the **output current limitation** presented a bottleneck when driving high gate charge SiC MOS with one or multiple parallel circuits. To overcome this issue, we propose a driver upgrade with **a GaN FET current boosting stage in source follower configuration**, which amplifies the output current, reduces the output stage's output impedance, and decreases its stray inductance.

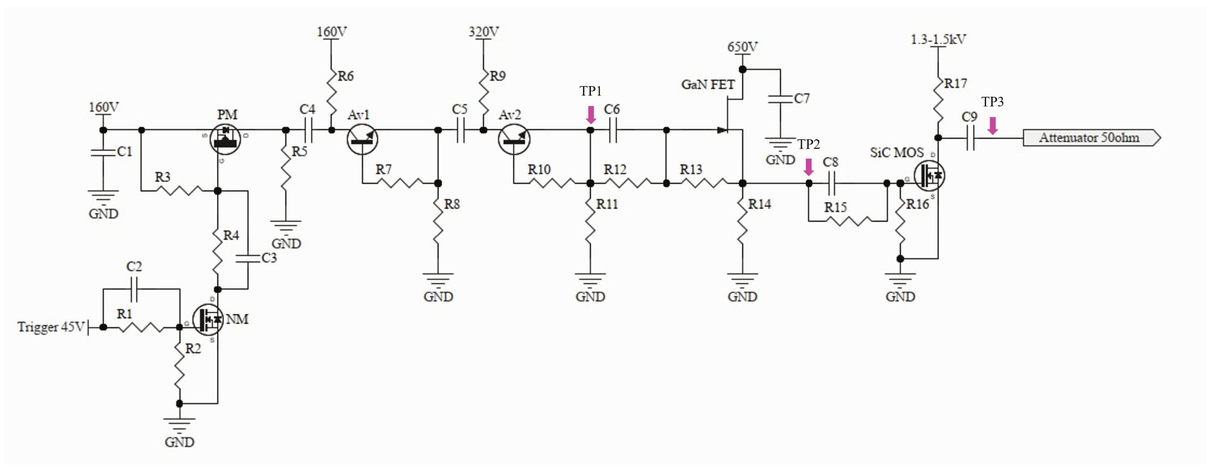

Figure 1: Schematic with test points indicated.

The GaN FET driver comprises a **super boosted Si PMOS** that triggers a two-stage Marx generator, where two avalanche transistors act as switches (as illustrated in Fig. 1).

The PMOS drain's fast rising pulse (voltage on C1 = 160 V) is added to the collector-emitter voltage of Av1, which is biased to 160 V (voltage on its energy storage capacitor C4) and **triggers an avalanche phenomenon** on it.

This voltage sum is then added to the collector-emitter voltage of Av2, which is biased to 320 V, and **triggers again an avalanche breakdown** on it.

Finally, the sum of voltages on C1, C4, and C5 is applied to the GaN FET gate and forces its source to follow it (minus gate-source biasing voltage). On its source we have then sum voltages on capacitors C1, C4 and C5, minus its own gate-source biasing voltage, the voltage drops on PM, Av1, Av2 and voltage drops of the series resistances of capacitors C1, C4, and C5 - under the condition that GaN drain voltage is high enough (Ud > Us). **The resulting voltage drives the gate of a 1.7kV SiC MOS**.

Adding this step in the driver after the avalanche transistors offers the advantage of **reducing the load on the Marx generator** by using the GaN FET in a source follower configuration.

This leads to a lower voltage drop on all transistors and energy storage capacitors in series, along **with low output impedance** and reduced output loop surface (contributing to reducing inductance).

As a result, the output voltage swing, slew rate, and maximum available current are greatly improved. **The lower output impedance provides a higher current pulse**, which, combined with the sharpened voltage triggering the gate of the SiC MOS, guarantees better performance.

Conclusion

We have presented a new method for increasing the current output of our driver circuit, with a highly performant outcome.

These ultra-boosted components will be utilized to trigger an ultra-fast Marx generator capable of generating higher output voltage and current, in view of triggering a high voltage, 5cm diameter puck thyristor.

Our ultimate goal is to trigger a larger stack of thyristors, reaching higher output voltage and current. This advancement has the potential to replace thyratrons in beam transfer facilities for particle accelerators, offering a more reliable and cost-effective alternative to traditional thyratron-based systems.