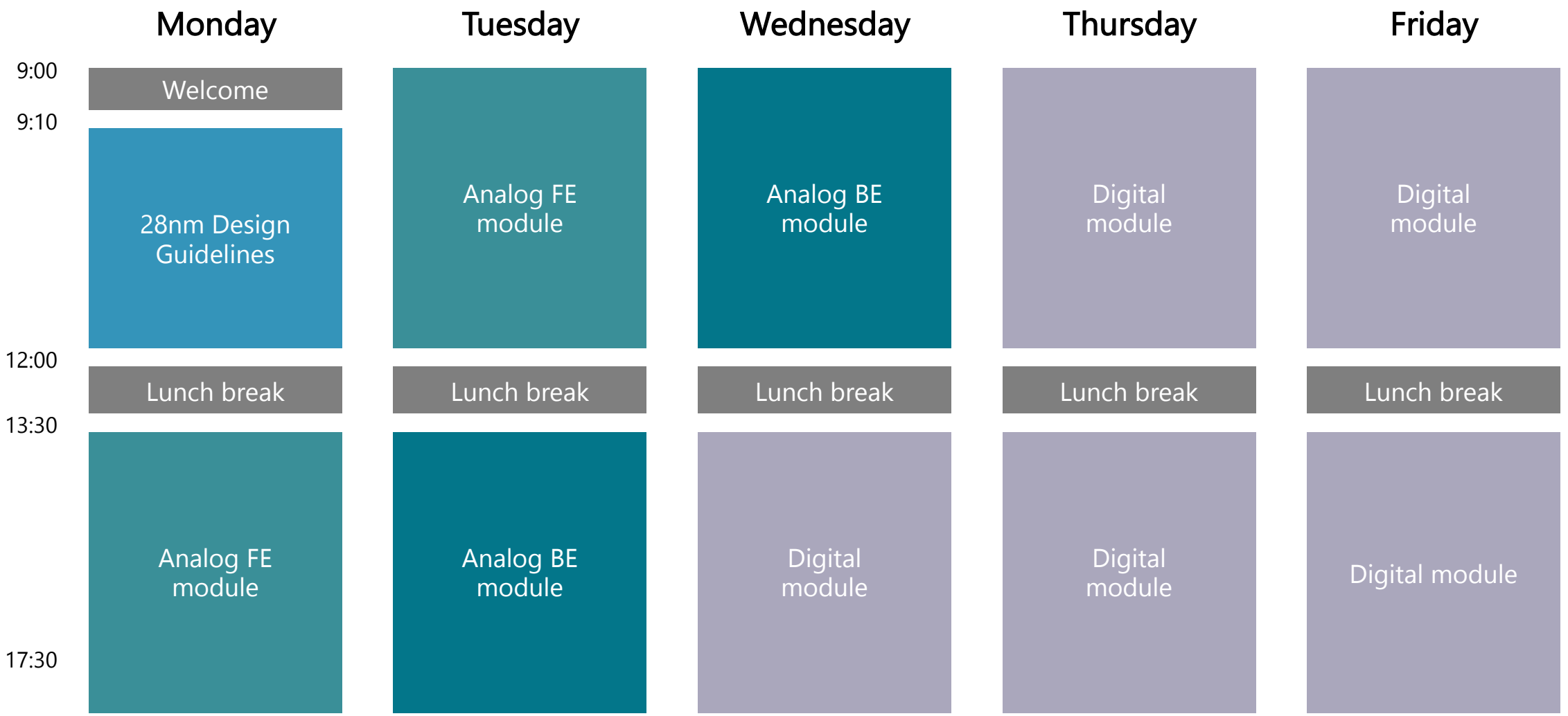
28nm mixed-signal workshop

Alessandro Caratelli [CERN ASIC Support]
CERN - Feb. 2023

Timetable of the workshop



Timetable of the workshop

28nm Design Guidelines

- 28nm technology guidelines
  Franco BANDI (CERN)
- Overview of the 28nm common design platform
  Marco ANDORNO (CERN)
- Total Ionizing Dose response of the 28nm technology
  Giulio BORGHELLO (CERN)
- Single event effects hardening in digital design
  Alessandro CARATELLI (CERN)

Analog module

- Analog simulation with Explorer and Assembler
  Helga DORNELAS (CADENCE)

  Lab exercises
- Mixed-signal simulation in Virtuoso (analog on top)
  Helga DORNELAS (CADENCE)
- Mixed-signal simulation in Xcelium (digital on top)
  Helga DORNELAS (CADENCE)

  Lab exercises
- Analog Backend VXL Best Practices
  Philippe CARRIERE (CADENCE)

  Lab exercises
- DRC/LVS with PVS
  Philippe CARRIERE (CADENCE)

  Lab exercises

Digital module

- Synthesis
  Bertrand GENNERET (CADENCE)
  - Synthesis: from RTL to Gate level netlist
  - SDC constraints and Timing Analysis

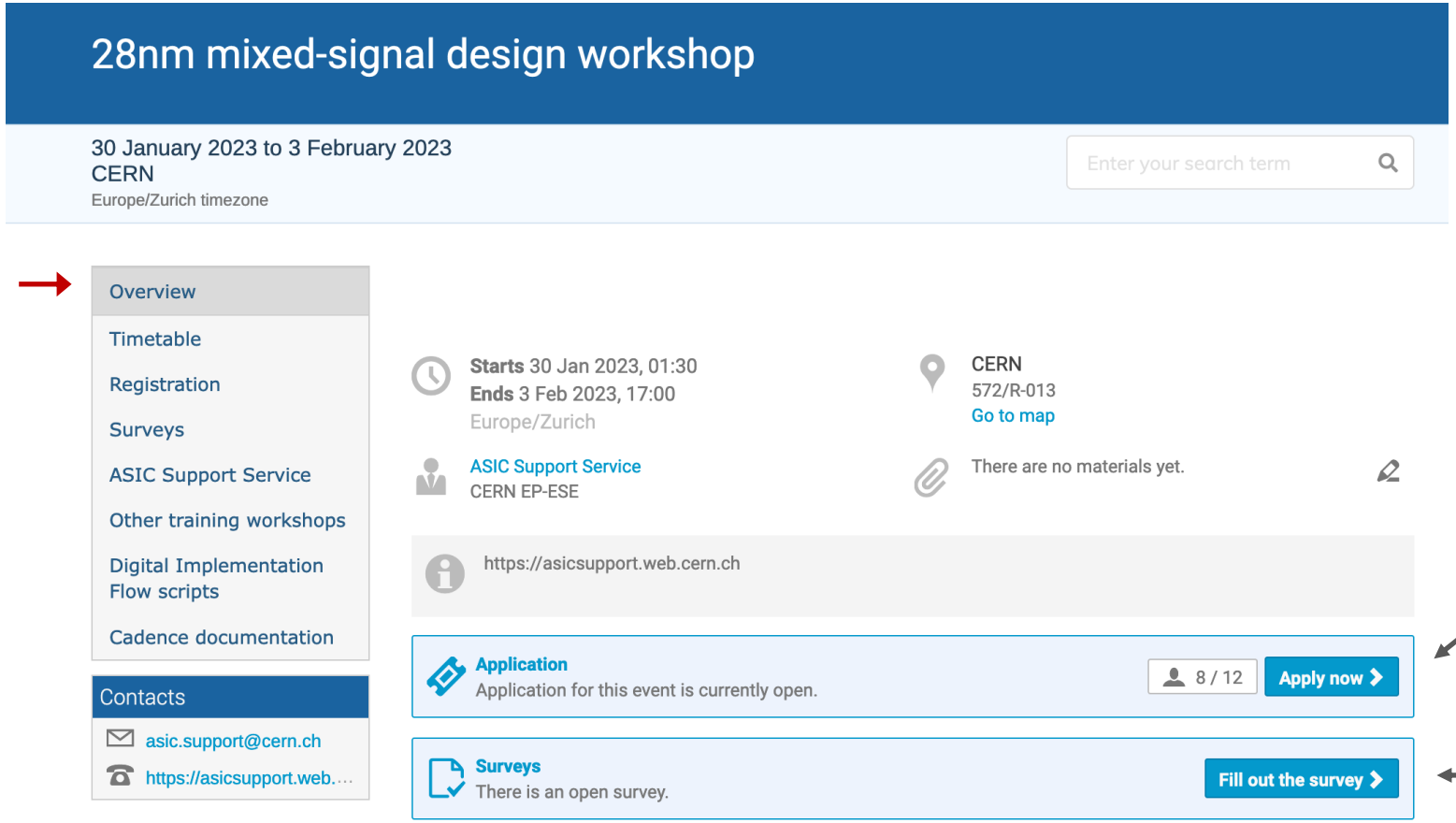
  Lab exercises
- Block level flat physical design
  Bertrand GENNERET (CADENCE)
  - Floor-planning
  - Clock Tree Synthesis
  - Routing and Optimizations

  Lab exercises
- Hierarchical implementation
  Bertrand GENNERET (CADENCE)

  Lab exercises
- Signoff analysis
  Bertrand GENNERET (CADENCE)
  - Power analysis
  - Signoff STA in Tempus
  - Physical verification (DRC / LVS)

  Lab exercises

Some practical information about the workshop



REGISTRATION

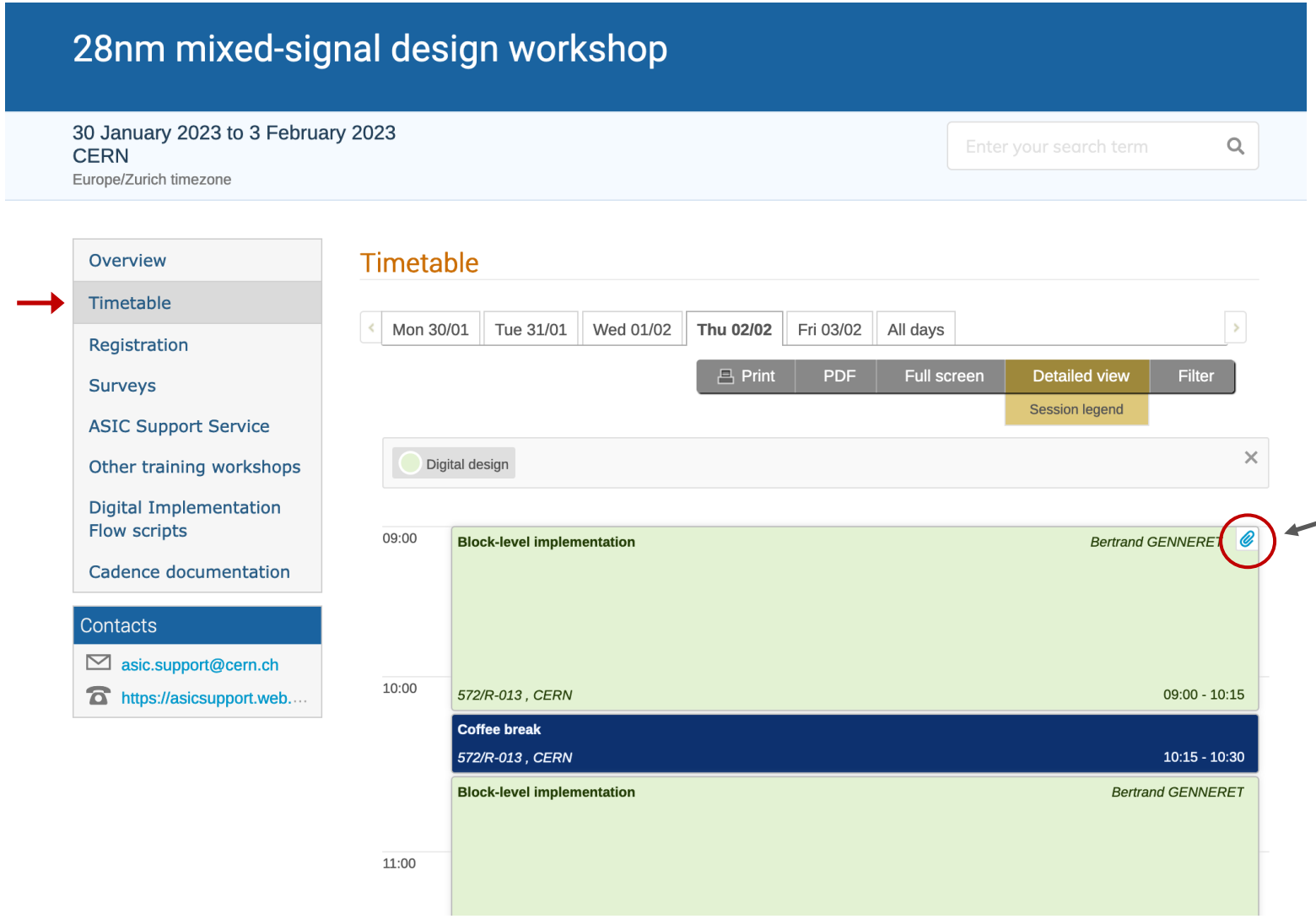
To get access to the course material please register with this link

SURVEY

You are kindly invited to complete the survey at the end of the course to help us improving next session

Link to the workshop material: https://indico.cern.ch/e/28nm-workshop-1

Some practical information about the workshop

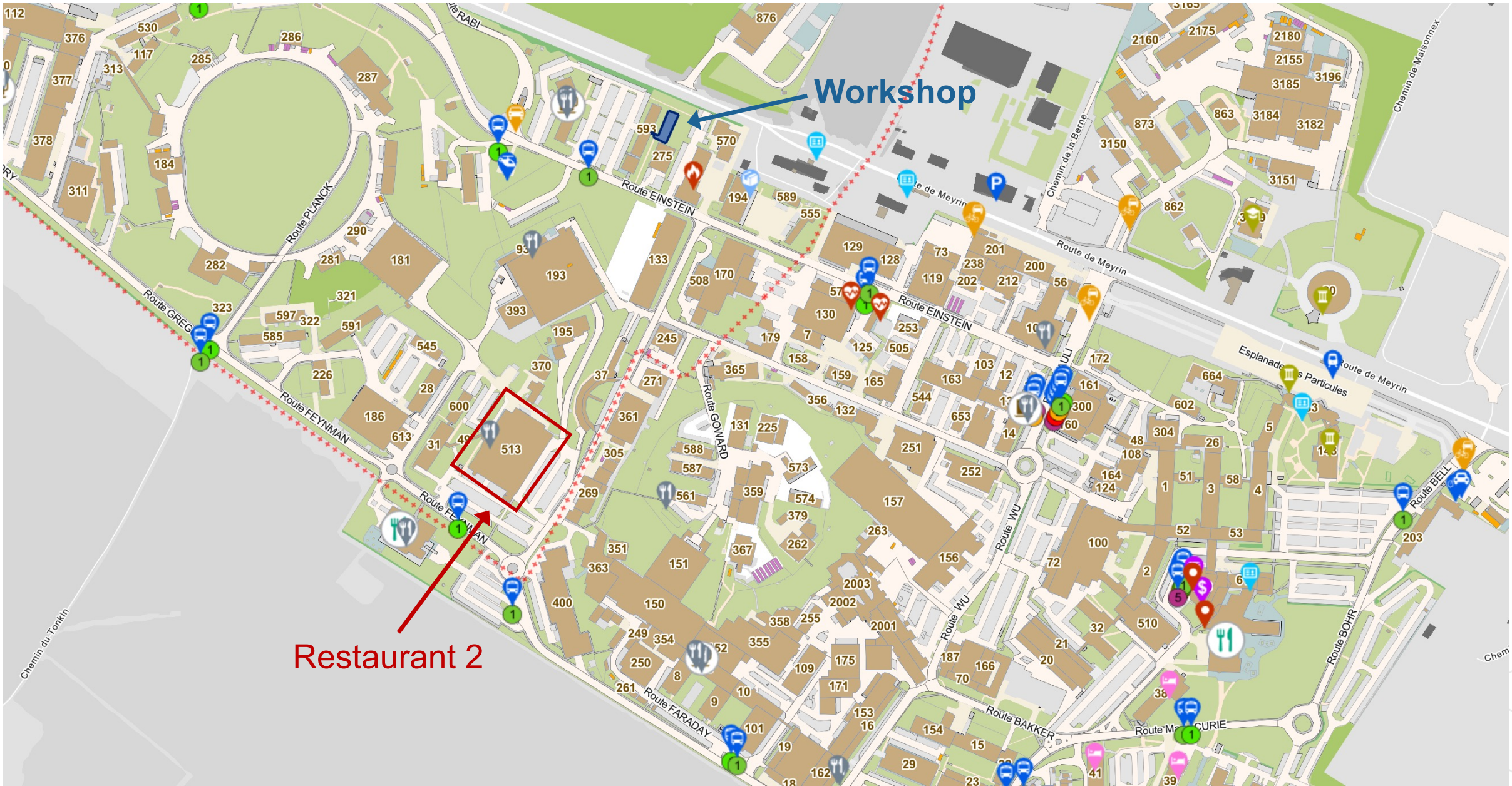


WORKSHOP MATERIAL DOWNLOAD

To download the slides and the lab instruction to follow during the course

Material download is protected by NDA

Some practical information about the workshop



Certificates

- Certificates of attendance will be distributed at the end of the course
- If you need a certificate for ECTS credits please contact asic.support@cern.ch
  - 35h training course + mini-exam ➔ usually recognized as 2 ECTS credits

Training courses catalog

Digital-on-top hierarchical Implementation in workshop

DoT Workshop
(3 days)

- Learn the main concepts for designing in 65nm for the High energy Physics environment
- Learn the main concepts of the digital implementation from the synthesis, physical implementation and signoff (RTL to GDS)
- Perform synthesis, physical implementation and signoff steps
- Exercise bottom-up and top-down hierarchical design approaches
- Co-developed between CERN EP-ESE ASIC Support service and Cadence VCAD

2 TIMES PER YEAR FOR THE LAST 3 YEARS

Workshop on Mixed-Signal design in 28nm process

Designing in 28nm
(5 days)

- Learn the main concepts for designing in 28nm for the High energy Physics environment
- Learn the main concepts of the digital implementation from the synthesis, physical implementation and signoff (RTL to GDS)
- Learn the main concepts of the analog and Mixed-Signal design in 28nm
- Learn main concepts about TIDs and SEUs tolerance design
- Co-developed between CERN EP-ESE ASIC Support service and Cadence VCAD

NEW - FIRST SESSION IN DECEMBER 2022

System Verilog Advanced Verification Environment using UVM workshop

Verification / UVM
(3 days)

- Learn the main concepts of functional verification for the High energy Physics
- Learn the main concepts of digital design verification
- Learn about the Universal Verification Methodology (UVM)
- In the lab sessions you will learn how to build your own UVC and verification environment
- A Cadence Training Course adapted for the High Energy Physics community requirements

1 TIME PER YEAR

The CERN ASIC Support Service

- Promote the collaborative works and knowledge sharing
- Provide support to HEP community for technology and EDA tool usage
- Enhance, update and maintain the PDKs for commonly used technologies in HEP environment
- Develop and distribute the Common Design Platforms for mixed-signal ASICs design
- Distribution and maintenance of common macro blocks
- Preparation and maintenance of design flows of general use
- Organize training workshops for HEP specific

CORE TEAM: Marco Andorno, Wojciech Bialas, Alessandro Caratelli, Kostas Kloukinas

CONTACTS: asic.support@cern.ch

The CERN Foundry Service

Establish Commercial Contracts with silicon vendors

Establish NDAs that allow for collaborative work

Organize & coordinate silicon fabrication

For silicon fabrication services (MPWs, engineering & production runs)
please contact foundry.services@cern.ch

CORE TEAM: Kostas Kloukinas, Maxence Ledoux, Cinzia Pinzoni

CONTACTS: foundry.services@cern.ch

Technical support

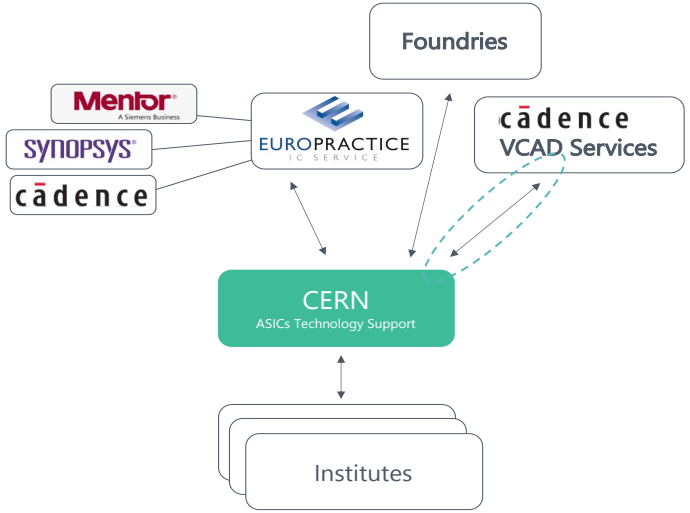
You can contact asic.support@cern.ch
for requests related to:

- Support for the **EDA tools** usage, **Design Flows** and the **Design Kits**
- Support **for design specific** issues
- **Distribution of shared IP blocks** (i.e. generation of SRAM blocks and assistance for design integration).
- Administrative requests (process of **signing NDAs**, **technology information** access, **PDK requests**).

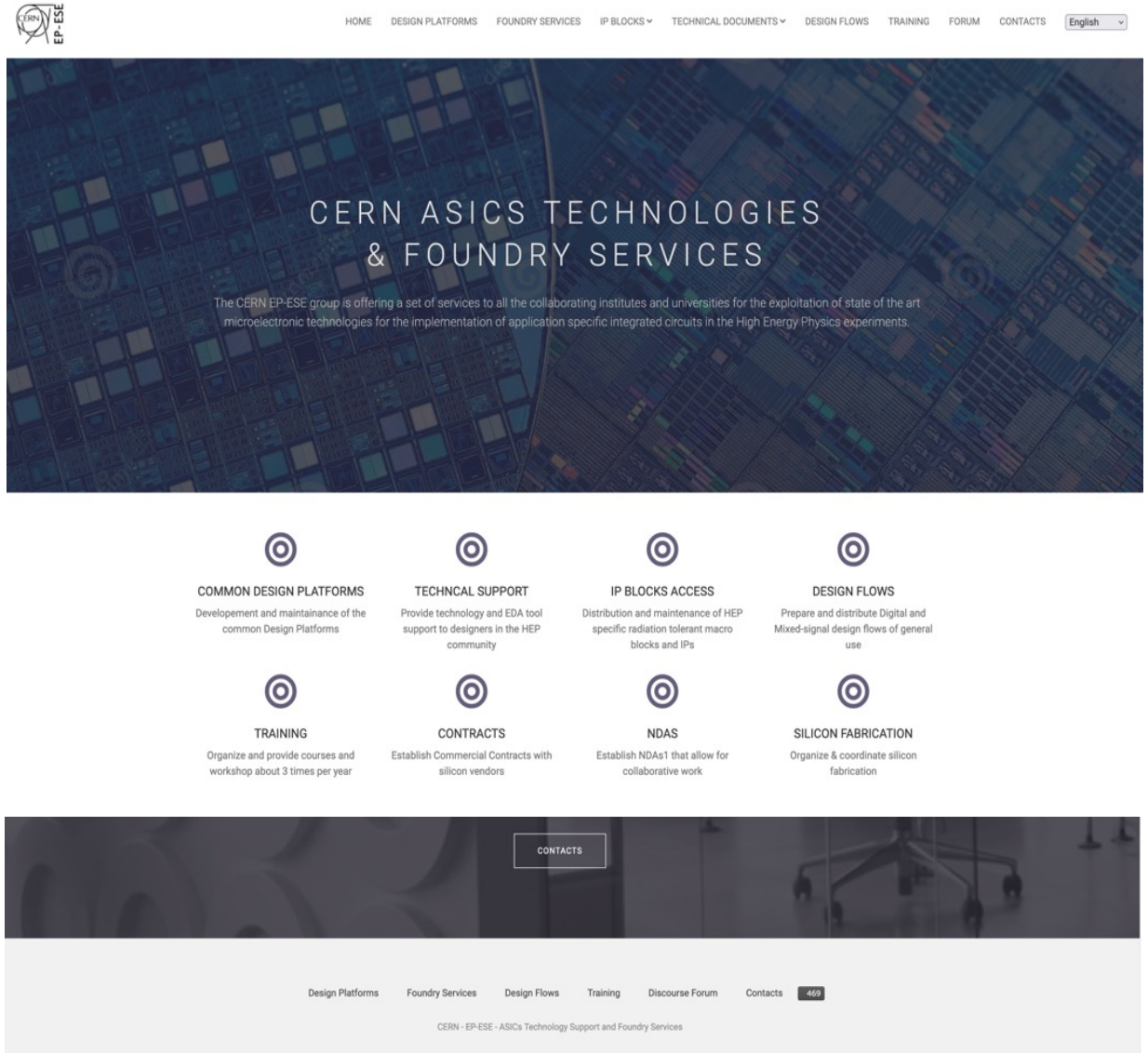
If you are in need of specific design assistance and implementation or verification tasks, please contact instead the chips.service@cern.ch

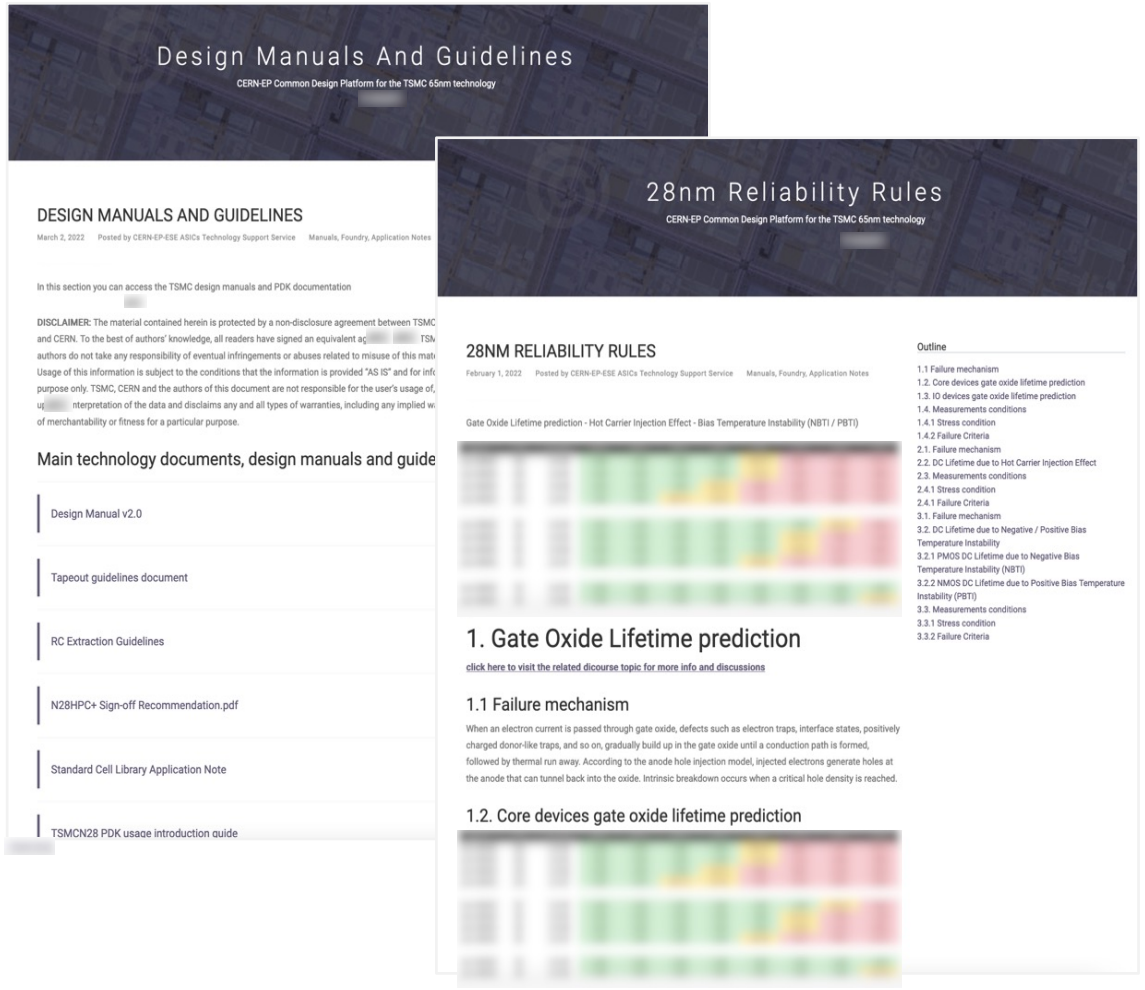
If needed for solving your issue, we can as well:

- put you **in contact with CERN designers** with experience in the field
- Involve **CADENCE VCAD Service** with which we have a support contract in place



Resources





https://asicsupport.web.cern.ch

Resources

The HEP designers forum

a place where to share information and search solutions

https://asicsupport-community.web.cern.ch

- Design and EDA tools Tutorials
- Additional documentation
- Design practices suggestions
- Exchange of information
- Everybody can benefits from the findings, solutions and scripts of the others without having to deal with the same issues
- 28nm dedicated section