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# 28nm mixed-signal workshop

Alessandro Caratelli [CERN ASIC Support]  
CERN - Feb. 2023



# Timetable of the workshop

|       | Monday                 | Tuesday          | Wednesday        | Thursday       | Friday         |
|-------|------------------------|------------------|------------------|----------------|----------------|
| 9:00  | Welcome                |                  |                  |                |                |
| 9:10  | 28nm Design Guidelines | Analog FE module | Analog BE module | Digital module | Digital module |
| 12:00 | Lunch break            | Lunch break      | Lunch break      | Lunch break    | Lunch break    |
| 13:30 | Analog FE module       | Analog BE module | Digital module   | Digital module | Digital module |
| 17:30 |                        |                  |                  |                |                |

# Timetable of the workshop

## 28nm Design Guidelines

- 28nm technology guidelines  
Franco BANDI (CERN)
- Overview of the 28nm common design platform  
Marco ANDORNO (CERN)
- Total Ionizing Dose response of the 28nm technology  
Giulio BORGHELLO (CERN)
- Single event effects hardening in digital design  
Alessandro CARATELLI (CERN)

## Analog module

- Analog simulation with Explorer and Assembler  
Helga DORNELAS (CADENCE)  
**Lab exercises**
- Mixed-signal simulation in Virtuoso (analog on top)  
Helga DORNELAS (CADENCE)
- Mixed-signal simulation in Xcelium (digital on top)  
Helga DORNELAS (CADENCE)  
**Lab exercises**
- Analog Backend VXL Best Practices  
Philippe CARRIERE (CADENCE)  
**Lab exercises**
- DRC/LVS with PVS  
Philippe CARRIERE (CADENCE)  
**Lab exercises**

## Digital module

- Synthesis  
Bertrand GENNERET (CADENCE)
  - Synthesis: from RTL to Gate level netlist
  - SDC constraints and Timing Analysis**Lab exercises**
- Block level flat physical design  
Bertrand GENNERET (CADENCE)
  - Floor-planning
  - Clock Tree Synthesis
  - Routing and Optimizations**Lab exercises**
- Hierarchical implementation  
Bertrand GENNERET (CADENCE)  
**Lab exercises**
- Signoff analysis  
Bertrand GENNERET (CADENCE)
  - Power analysis
  - Signoff STA in Tempus
  - Physical verification (DRC / LVS)**Lab exercises**

# Some practical information about the workshop

## 28nm mixed-signal design workshop

30 January 2023 to 3 February 2023  
CERN  
Europe/Zurich timezone

- Overview
- Timetable
- Registration
- Surveys
- ASIC Support Service
- Other training workshops
- Digital Implementation
- Flow scripts
- Cadence documentation

**Contacts**

- asic.support@cern.ch
- https://asicsupport.web...

**Starts** 30 Jan 2023, 01:30  
**Ends** 3 Feb 2023, 17:00  
Europe/Zurich

**CERN**  
572/R-013  
[Go to map](#)

**ASIC Support Service**  
CERN EP-ESE

There are no materials yet.

<https://asicsupport.web.cern.ch>

**Application**  
Application for this event is currently open. 8 / 12 [Apply now >](#)

**Surveys**  
There is an open survey. [Fill out the survey >](#)

## REGISTRATION

To get access to the course material please register with this link

## SURVEY

You are kindly invited to complete the survey at the end of the course to help us improving next session

Link to the workshop material: <https://indico.cern.ch/e/28nm-workshop-1>

# Some practical information about the workshop

## 28nm mixed-signal design workshop

30 January 2023 to 3 February 2023  
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Europe/Zurich timezone

Enter your search term

Overview

→ Timetable

Registration

Surveys

ASIC Support Service

Other training workshops

Digital Implementation  
Flow scripts

Cadence documentation

Contacts

✉ [asic.support@cern.ch](mailto:asic.support@cern.ch)

☎ <https://asicsupport.web...>

### Timetable

< Mon 30/01 Tue 31/01 Wed 01/02 **Thu 02/02** Fri 03/02 All days >

Print PDF Full screen Detailed view Filter

Session legend

● Digital design

|       |                                   |                   |
|-------|-----------------------------------|-------------------|
| 09:00 | <b>Block-level implementation</b> | Bertrand GENNERET |
| 10:00 | 572/R-013 , CERN                  | 09:00 - 10:15     |
|       | <b>Coffee break</b>               |                   |
|       | 572/R-013 , CERN                  | 10:15 - 10:30     |
| 11:00 | <b>Block-level implementation</b> | Bertrand GENNERET |

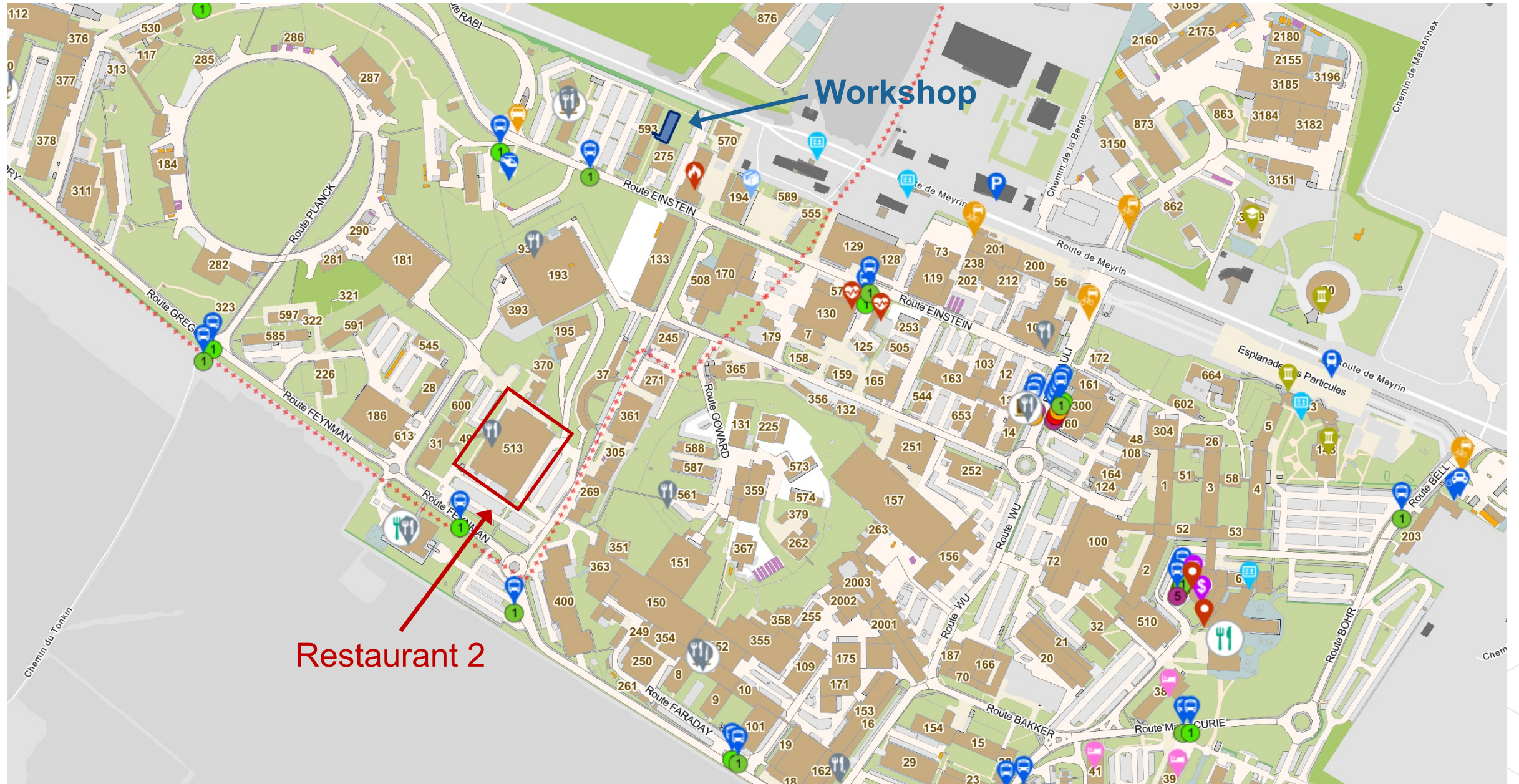
### WORKSHOP MATERIAL DOWNLOAD

To download the slides and the lab instruction to follow during the course

Material download is protected by NDA



# Some practical information about the workshop



# Certificates

- Certificates of attendance will be distributed at the end of the course
- If you need a certificate for ECTS credits please contact [asic.support@cern.ch](mailto:asic.support@cern.ch)
  - 35h training course + mini-exam → usually recognized as 2 ECTS credits



# Training courses catalog

Digital-on-top hierarchical  
Implementation in workshop

## DoT Workshop (3 days)

- Learn the main concepts for designing in 65nm for the High energy Physics environment
- Learn the main concepts of the digital implementation from the synthesis, physical implementation and signoff (RTL to GDS)
- Perform synthesis, physical implementation and signoff steps
- Exercise bottom-up and top-down hierarchical design approaches
- Co-developed between CERN EP-ESE ASIC Support service and Cadence VCAD

2 TIMES PER YEAR FOR THE LAST 3 YEARS

Workshop on Mixed-Signal design  
in 28nm process

## Designing in 28nm (5 days)

- Learn the main concepts for designing in 28nm for the High energy Physics environment
- Learn the main concepts of the digital implementation from the synthesis, physical implementation and signoff (RTL to GDS)
- Learn the main concepts of the analog and Mixed-Signal design in 28nm
- Learn main concepts about TIDs and SEUs tolerance design
- Co-developed between CERN EP-ESE ASIC Support service and Cadence VCAD

**NEW** - FIRST SESSION IN DECEMBER 2022

System Verilog Advanced Verification  
Environment using UVM workshop

## Verification / UVM (3 days)

- Learn the main concepts of functional verification for the High energy Physics
- Learn the main concepts of digital design verification
- Learn about the Universal Verification Methodology (UVM)
- In the lab sessions you will learn how to build your own UVC and verification environment
- A Cadence Training Course adapted for the High Energy Physics community requirements

1 TIME PER YEAR



# The CERN ASIC Support Service



Promote the collaborative works and knowledge sharing



Provide support to HEP community for technology and EDA tool usage



Enhance, update and maintain the PDKs for commonly used technologies in HEP environment



Develop and distribute the Common Design Platforms for mixed-signal ASICs design



Distribution and maintenance of common macro blocks



Preparation and maintenance of design flows of general use



Organize training workshops for HEP specific

CORE TEAM: Marco Andorno, Wojciech Bialas, Alessandro Caratelli, Kostas Kloukinas

CONTACTS: [asic.support@cern.ch](mailto:asic.support@cern.ch)

# The CERN Foundry Service



Establish Commercial Contracts with silicon vendors



Establish NDAs that allow for collaborative work



Organize & coordinate silicon fabrication

For silicon fabrication services (MPWs, engineering & production runs)  
please contact [foundry.services@cern.ch](mailto:foundry.services@cern.ch)

CORE TEAM: Kostas Kloukinas, Maxence Ledoux, Cinzia Pinzoni

CONTACTS: [foundry.services@cern.ch](mailto:foundry.services@cern.ch)

# Technical support

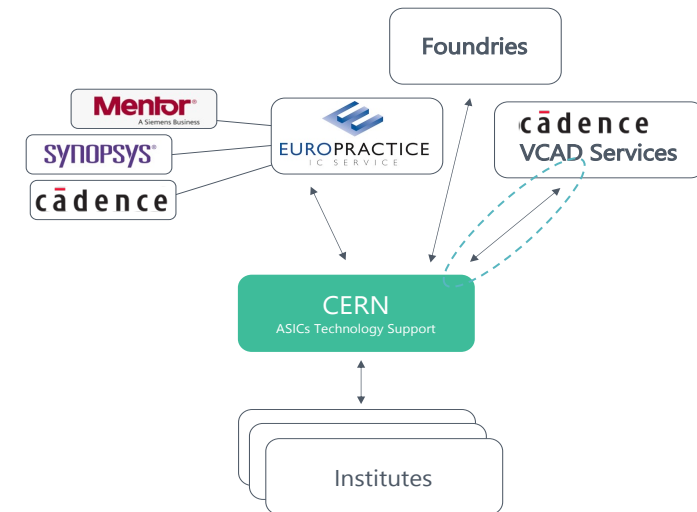
You can contact [asic.support@cern.ch](mailto:asic.support@cern.ch) for requests related to:

- Support for the **EDA tools** usage, **Design Flows** and the **Design Kits**
- Support **for design specific** issues
- **Distribution of shared IP blocks** (i.e. generation of SRAM blocks and assistance for design integration).
- Administrative requests (process of **signing NDAs**, **technology information** access, **PDK requests**).

If you are in need of specific design assistance and implementation or verification tasks, please contact instead the [chips.service@cern.ch](mailto:chips.service@cern.ch)

If needed for solving your issue, we can as well:

- put you **in contact with CERN designers** with experience in the field
- Involve **CADENCE VCAD Service** with which we have a support contract in place

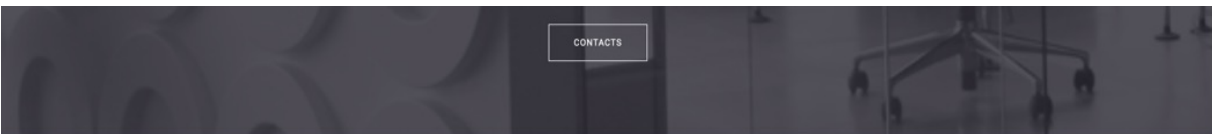


# Resources

## CERN ASICS TECHNOLOGIES & FOUNDRY SERVICES

The CERN EP-ESE group is offering a set of services to all the collaborating institutes and universities for the exploitation of state of the art microelectronic technologies for the implementation of application specific integrated circuits in the High Energy Physics experiments.

- COMMON DESIGN PLATFORMS**  
Development and maintenance of the common Design Platforms
- TECHNICAL SUPPORT**  
Provide technology and EDA tool support to designers in the HEP community
- IP BLOCKS ACCESS**  
Distribution and maintenance of HEP specific radiation tolerant macro blocks and IPs
- DESIGN FLOWS**  
Prepare and distribute Digital and Mixed-signal design flows of general use
- TRAINING**  
Organize and provide courses and workshop about 3 times per year
- CONTRACTS**  
Establish Commercial Contracts with silicon vendors
- NDAS**  
Establish NDAs that allow for collaborative work
- SILICON FABRICATION**  
Organize & coordinate silicon fabrication



CONTACTS

## Design Manuals And Guidelines

CERN-EP Common Design Platform for the TSMC 65nm technology

### DESIGN MANUALS AND GUIDELINES

March 2, 2022 Posted by CERN-EP-ESE ASICs Technology Support Service Manuals, Foundry, Application Notes

In this section you can access the TSMC design manuals and PDK documentation

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### Main technology documents, design manuals and guides

- Design Manual v2.0
- Tapeout guidelines document
- RC Extraction Guidelines
- N28HPC+ Sign-off Recommendation.pdf
- Standard Cell Library Application Note
- TSMCN28 PDK usage introduction guide

## 28nm Reliability Rules

CERN-EP Common Design Platform for the TSMC 65nm technology

### 28NM RELIABILITY RULES

February 1, 2022 Posted by CERN-EP-ESE ASICs Technology Support Service Manuals, Foundry, Application Notes

Gate Oxide Lifetime prediction - Hot Carrier Injection Effect - Bias Temperature Instability (NBTI / PBTI)



### 1. Gate Oxide Lifetime prediction

[click here to visit the related discourse topic for more info and discussions](#)

#### 1.1 Failure mechanism

When an electron current is passed through gate oxide, defects such as electron traps, interface states, positively charged donor-like traps, and so on, gradually build up in the gate oxide until a conduction path is formed, followed by thermal run away. According to the anode hole injection model, injected electrons generate holes at the anode that can tunnel back into the oxide. Intrinsic breakdown occurs when a critical hole density is reached.

#### 1.2. Core devices gate oxide lifetime prediction



#### Outline

- 1.1 Failure mechanism
- 1.2 Core devices gate oxide lifetime prediction
- 1.3 ID devices gate oxide lifetime prediction
- 1.4 Measurements conditions
- 1.4.1 Stress condition
- 1.4.2 Failure Criteria
- 2.1 Failure mechanism
- 2.2 DC Lifetime due to Hot Carrier Injection Effect
- 2.3 Measurements conditions
- 2.4.1 Stress condition
- 2.4.1 Failure Criteria
- 3.1 Failure mechanism
- 3.2 DC Lifetime due to Negative / Positive Bias Temperature Instability
- 3.2.1 PMOS DC Lifetime due to Negative Bias Temperature Instability (NBTI)
- 3.2.2 NMOS DC Lifetime due to Positive Bias Temperature Instability (PBTI)
- 3.3 Measurements conditions
- 3.3.1 Stress condition
- 3.3.2 Failure Criteria

<https://asicsupport.web.cern.ch>

# Resources

## The HEP designers forum

a place where to share information and search solutions

<https://asicsupport-community.web.cern.ch>

- Design and EDA tools Tutorials
- Additional documentation
- Design practices suggestions
- Exchange of information
- Everybody can benefit from the findings, solutions and scripts of the others without having to deal with the same issues
- 28nm dedicated section

CERN Accelerating science

### HEP ASIC designers community forum

HOME TECHNOLOGIES FOUNDRY SERVICES DESIGN TOOLS AND FLOWS FORUM CONTACTS

all categories Categories Latest + New Topic

Category Latest

**28nm**  
Here you can find design material and documentation for designing with the 28nm process. The access to this area is limited to the designers who have signed the 28nm NDA.  
28nm NEWS 28nm tech-resources-restricted

**65nm**  
Here you can find design material for developing circuits in the 65nm process. A site is limited to the TSMC designers group who have signed the 65nm NDA.  
65 PDK Updates 65nm Macro-Cells 65nm TechLibrary  
65nm Tutorials TID Models

**130nm**  
Here you can find design material for developing circuits in the 130nm process. A site is limited to the TSMC designers group who have signed the 130nm NDA.  
130nm Macro-Cells 130nm TechLibrary 130nm Tutorials  
Radiation tolerance

**Radiation tolerance**  
In this category you can find and share material concerning radiation tolerance and hardening. Since the access to this category is not protected, please do not post NDA protected material.

**Digital**  
\*\* Digital Design strategies and tools usage\*\*  
Soft-Macro-Cells Flow and Scripts

**Analog and Mixed Signal**  
\*\* Analog design related topics \*\*

**MIC Cluster and Repositories**  
\*\* CERN ME computing infrastructure and repos related topics \*\*

**Generic**  
Welcome to the CERN ASIC-Support documentation forum. In this page, you can find suggestions, discussions and solutions for various ASIC design issues.

**Fix VIA array DRC Issue in Innovus flow**  
As was reported by some colleagues, the Innovus generation of the via arrays between metal-v (6) and metal-u (7) generated a DRC error. According to the new increased spacing requirements, the following code snippet can be used to fix the issue.  
VIA6.S.2 {  
// ( ( 3 -  
MinArray =  
// get array  
VIA6Array  
VIA6InArray  
EXT VIA6InArray  
}

**N28HPC+ PVS LVS and Quantus parasitic extraction for Mixed-Signal designs**

**Run-to-run TID-induced variability in 65 nm CMOS technology**  
By Giulio Borghello

- To monitor the run-to-run variability in the TID-response of MOS transistors, the same test chip is added at every prototyping and production run
- The test structure contains nMOS, pMOS, core and I/O transistors of various sizes
- The test chips are exposed to increasing levels of total ionizing dose. For each step of TID,  $I^*(V)$  and  $I^{sat}(V)$  measurements are performed

Reported parameters:

- $I_{ON}^{sat}$
- $I_{OFF}^{sat}$

During irradiation:

- diode configuration, i.e.  $|V_{DS}| = |V_{GS}| = 1.2 V$
- $T = 25^\circ C$

Many samples in 130 nm CMOS technology  
3 manufacturing plants (Fabs)  
(Fab 6, 12 and 14)



