EDIT 2011 Excellence in Detectors and Instrumentation Technologies
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Silicon Strips and Pixel Technologies

Present & Future Pixel Systems at LHC

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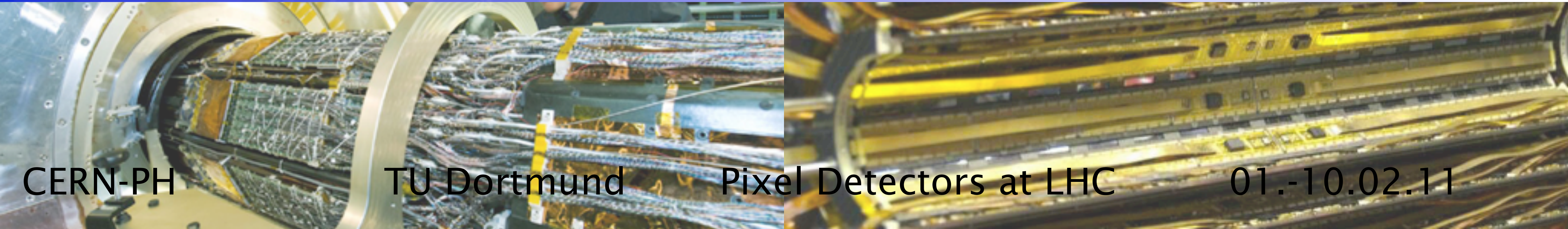
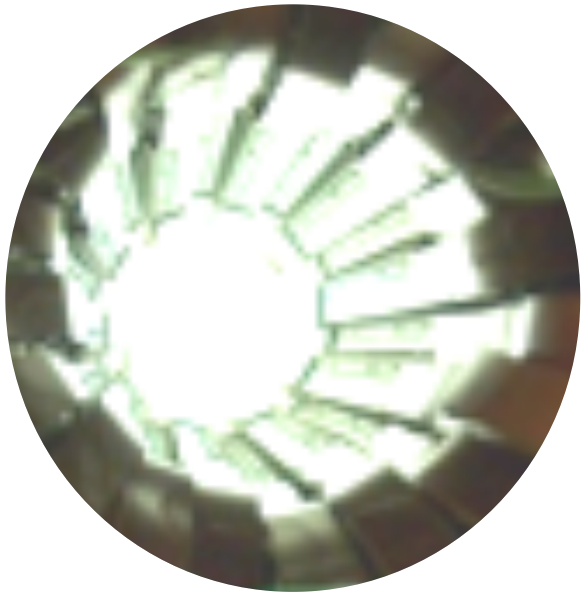
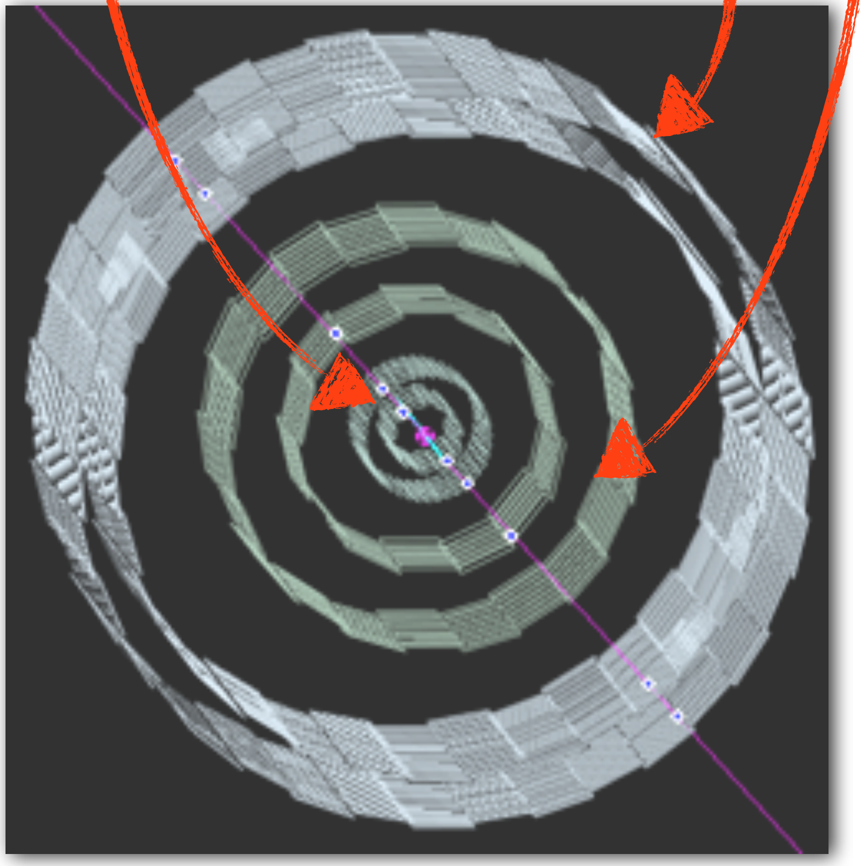


ALICE Pixels



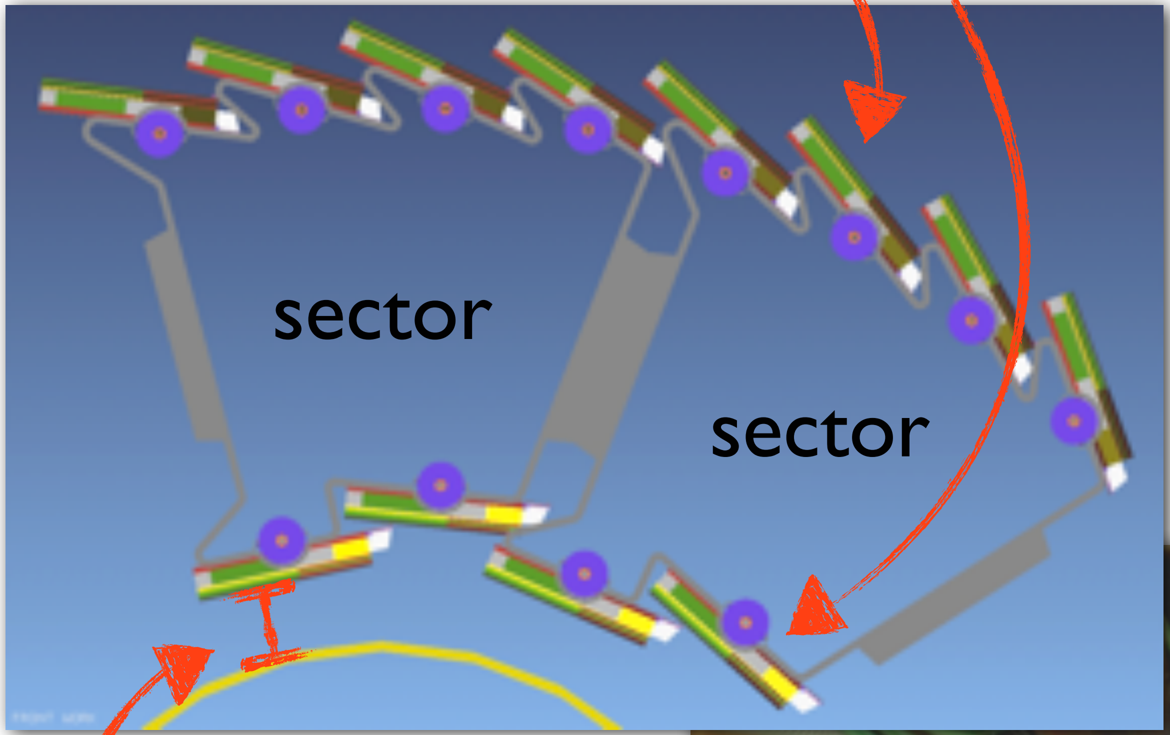
ALICE Inner Tracker & Silicon Pixel Detector

- ☑ 6 layer ITS (Inner Tracking System)
- ☑ consists of 2 layers of silicon pixel (SPD), 2 layers of silicon drift (SDD) and 2 layers of silicon strip detectors (SSD)

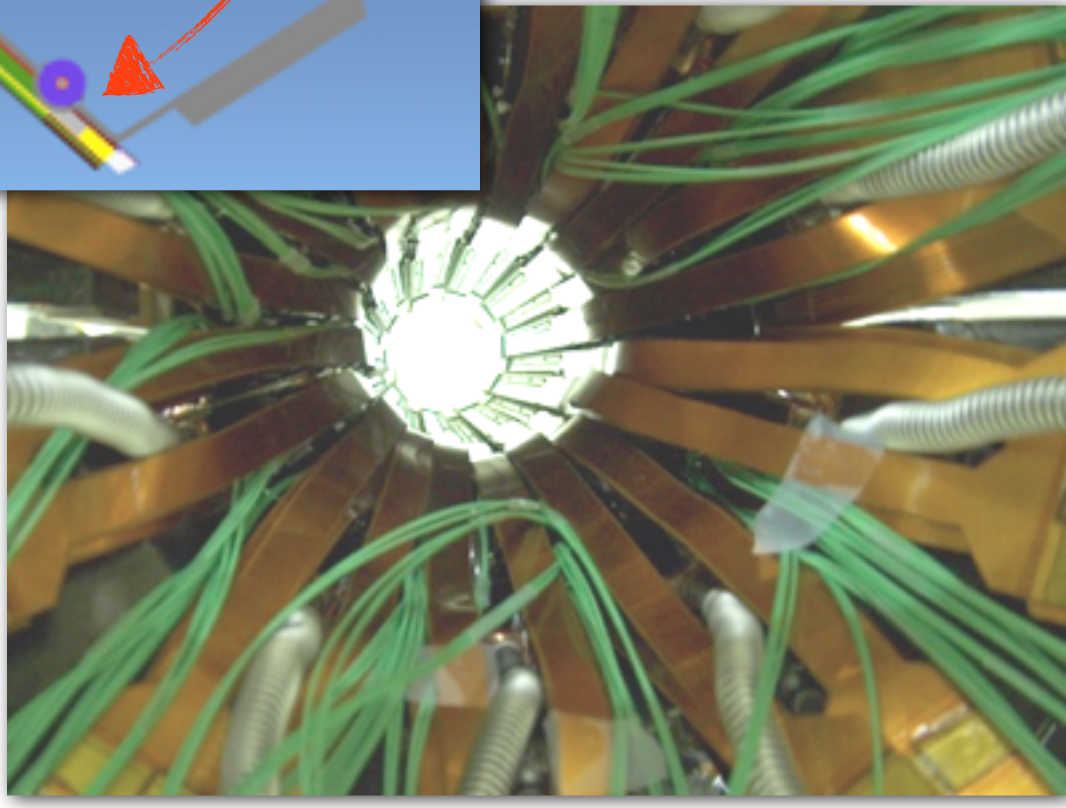


2 barrel layers formed by 10 carbon fiber sectors:

- ☑ $R_{\text{inner layer}}$: 3.9 cm
- ☑ $R_{\text{outer layer}}$: 7.6 cm

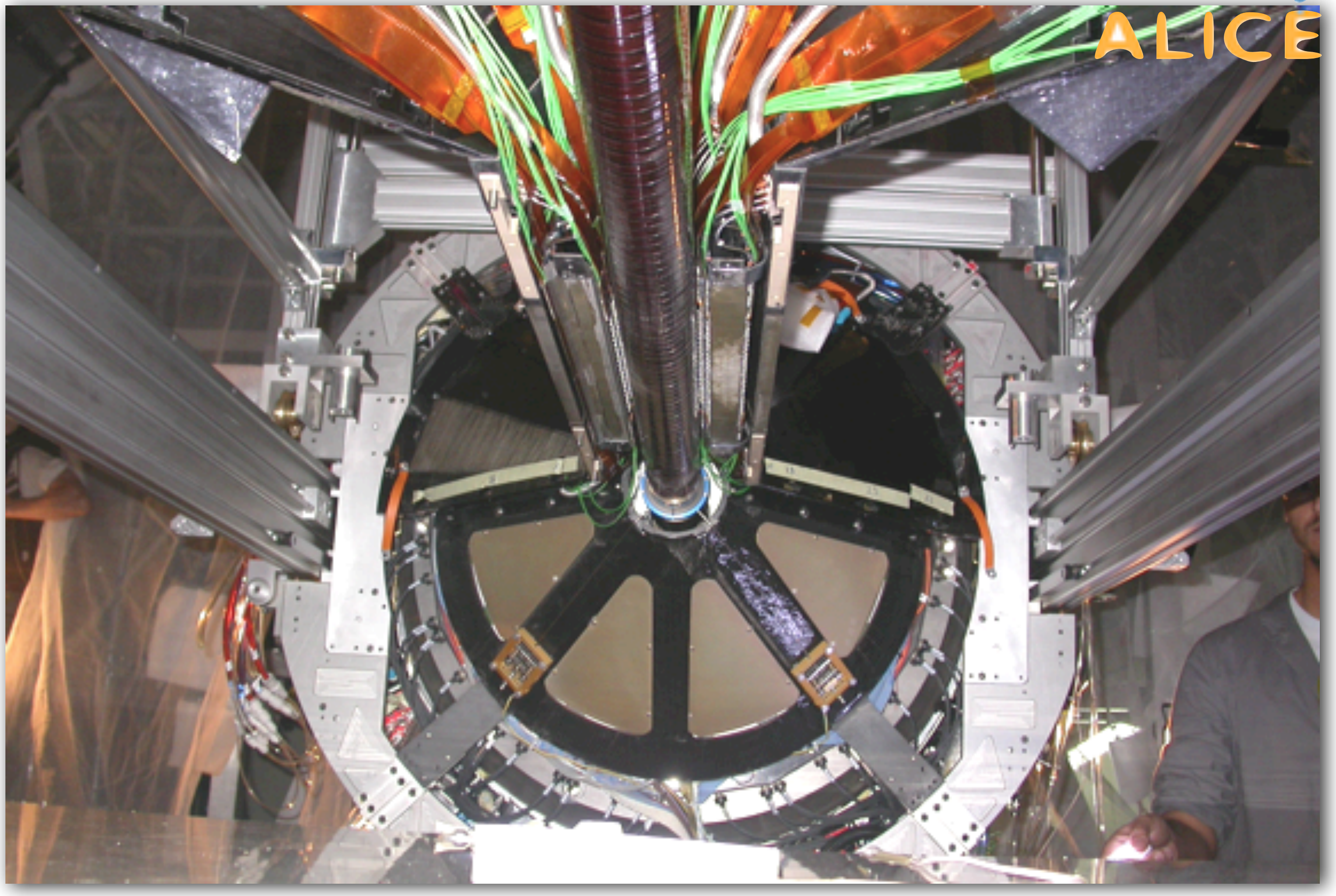


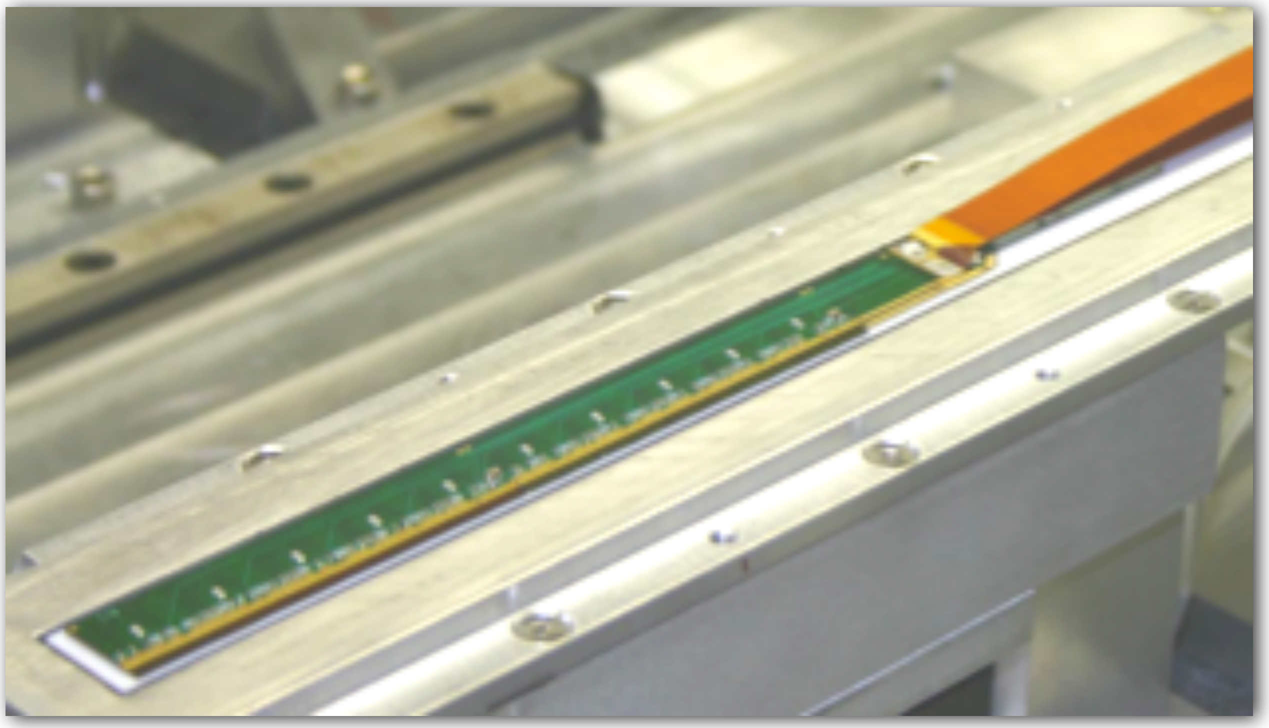
Min. clearance of closest component to beam-pipe: ~ 5 mm



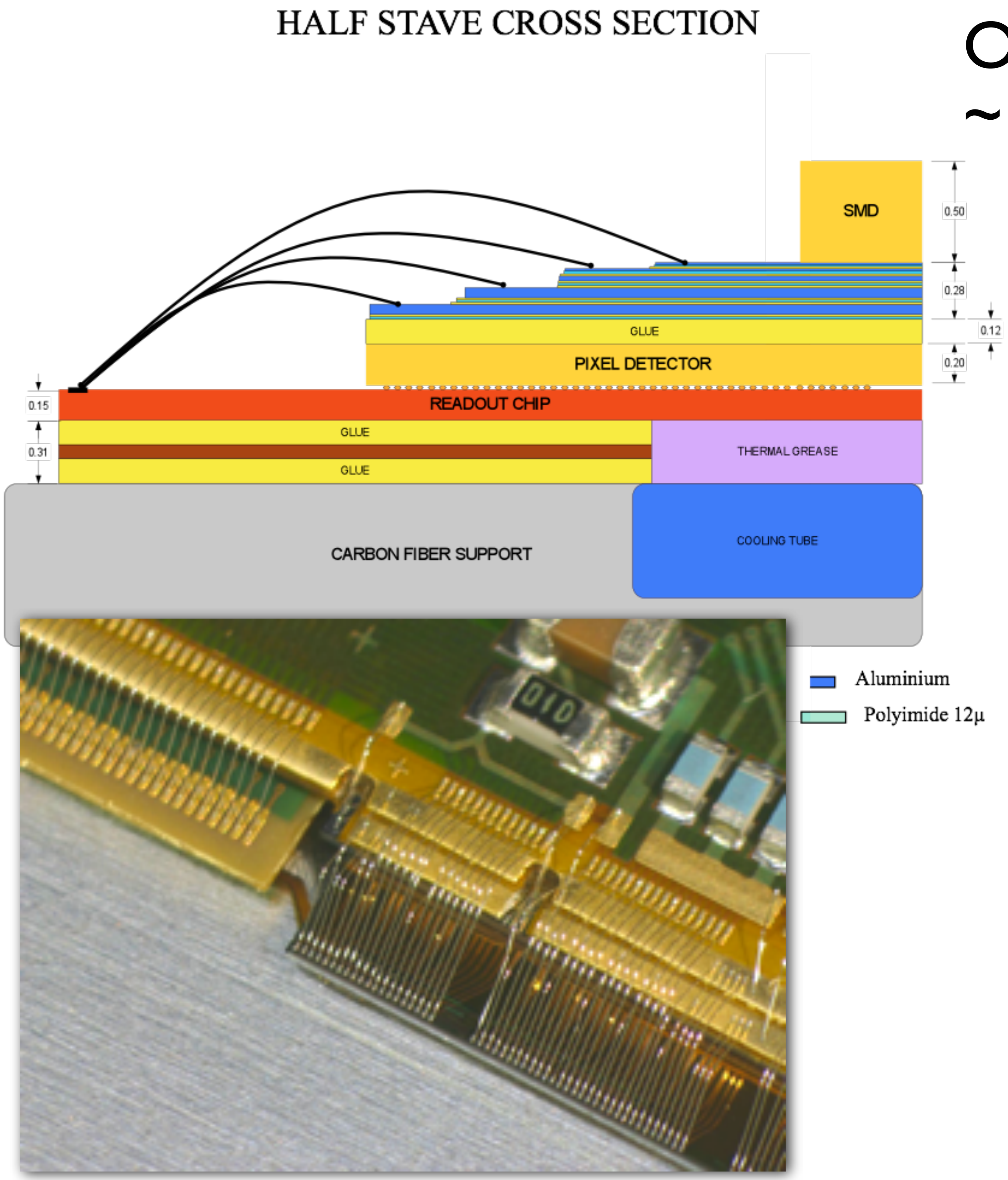
ALICE Silicon Pixel Detector

- ☑ Smallest building block: half-stave
- ☑ 120 half-staves (40 inner + 80 outer)
- ☑ Each half-stave consists of:
  - 1 MCM
    - max. height: 5 mm
  - 2 fc bonded ladders
    - 5 chips + 1 sensor
  - 1 multilayer bus
- ☑ 1200 pixel chips
- ☑ 9.83 x 10^6 pixels





ALICE Silicon Pixel Detector Half Stave

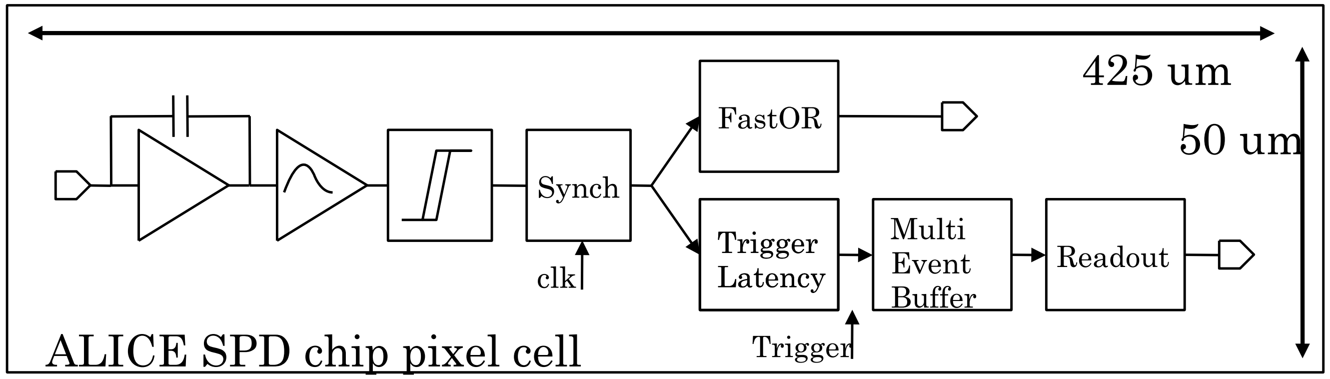

HALF STAVE CROSS SECTION

Optimize material budget: ~1.1% X0 per layer

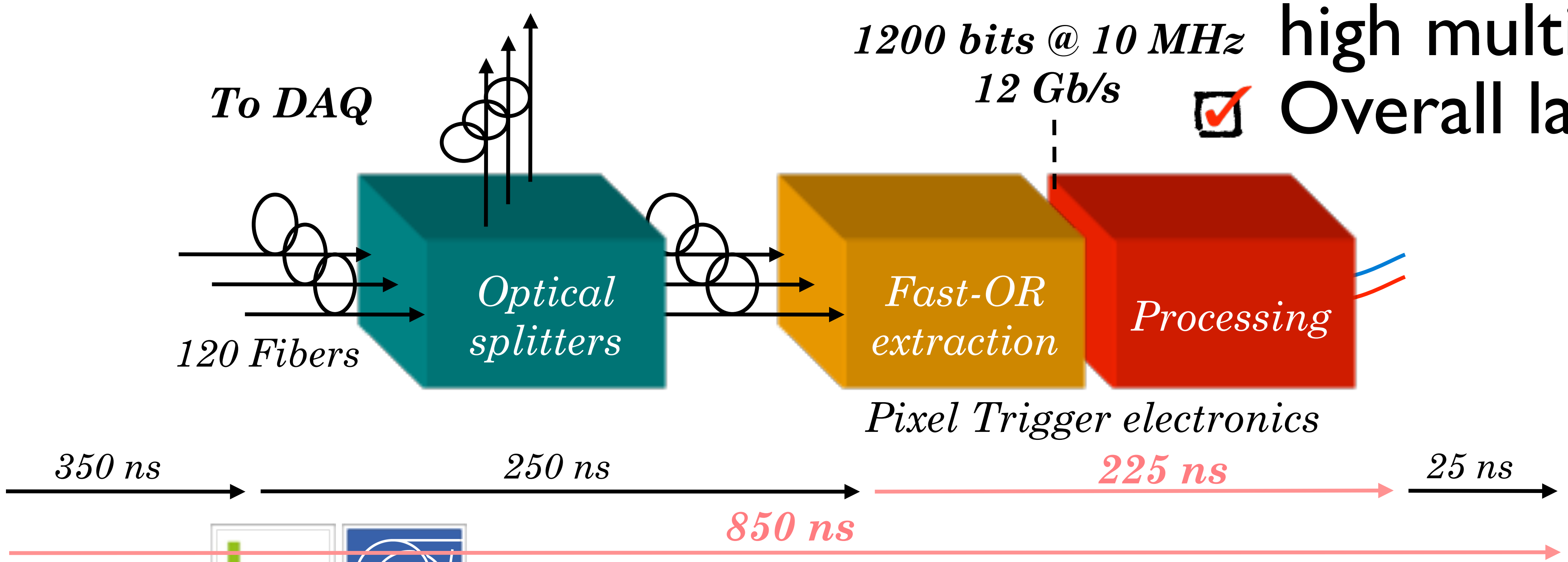
- ☑ Carbon fibre: 200 μm
- ☑ Cooling tube (Phynox): 40 μm wall thickness
- ☑ Grounding foil (Al-Kapton): 75 μm
- ☑ Pixel chip (Silicon): 150 μm
- ☑ Bump bonds (Pb-Sn): diameter ~15-20 μm
- ☑ Silicon sensor: 200 μm
- ☑ Pixel bus (Al+Kapton): 280 μm
- ☑ SMD components
- ☑ Glue (Eccobond 45) and thermal grease

ALICE Silicon Pixel Detector Tigger and DAQ

- ☑ Dedicated FastOr (FO) circuitry in each pixel cell
- ☑ Active if at least one pixel per chip is hit
- ☑ Transmitted every 100 ns
- ☑ Two data streams: data + FO
- ☑ Low latency pad detector with 1200 pads
- ☑ Used for L0 trigger decisions (cosmics, pp, HI)



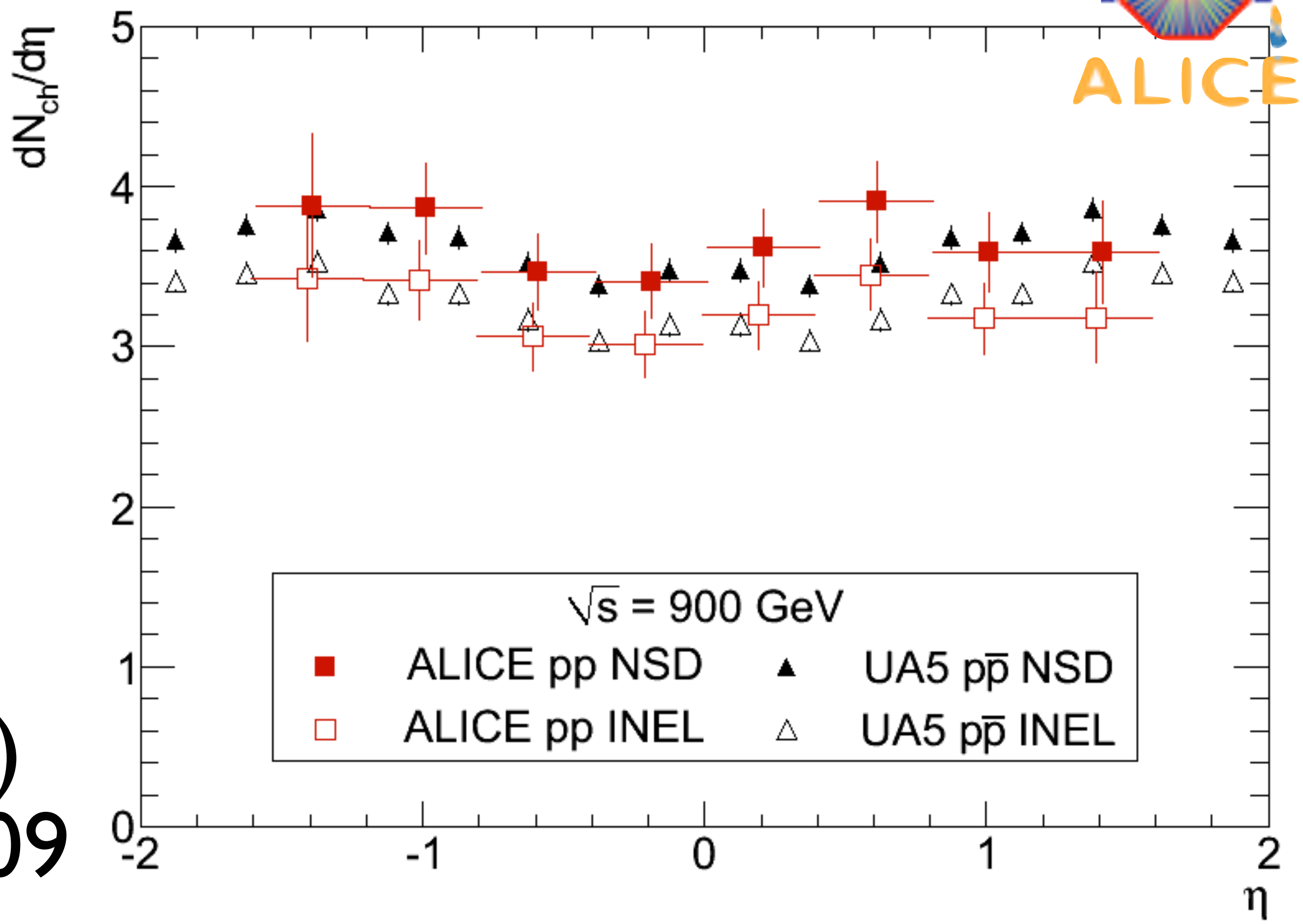
- ☑ Extract and synchronize 1200 FO bits every 100 ns
- ☑ User defined and programmable algorithms (MB, topological trigger, high multiplicity trigger,..)
- ☑ Overall latency: 850 ns

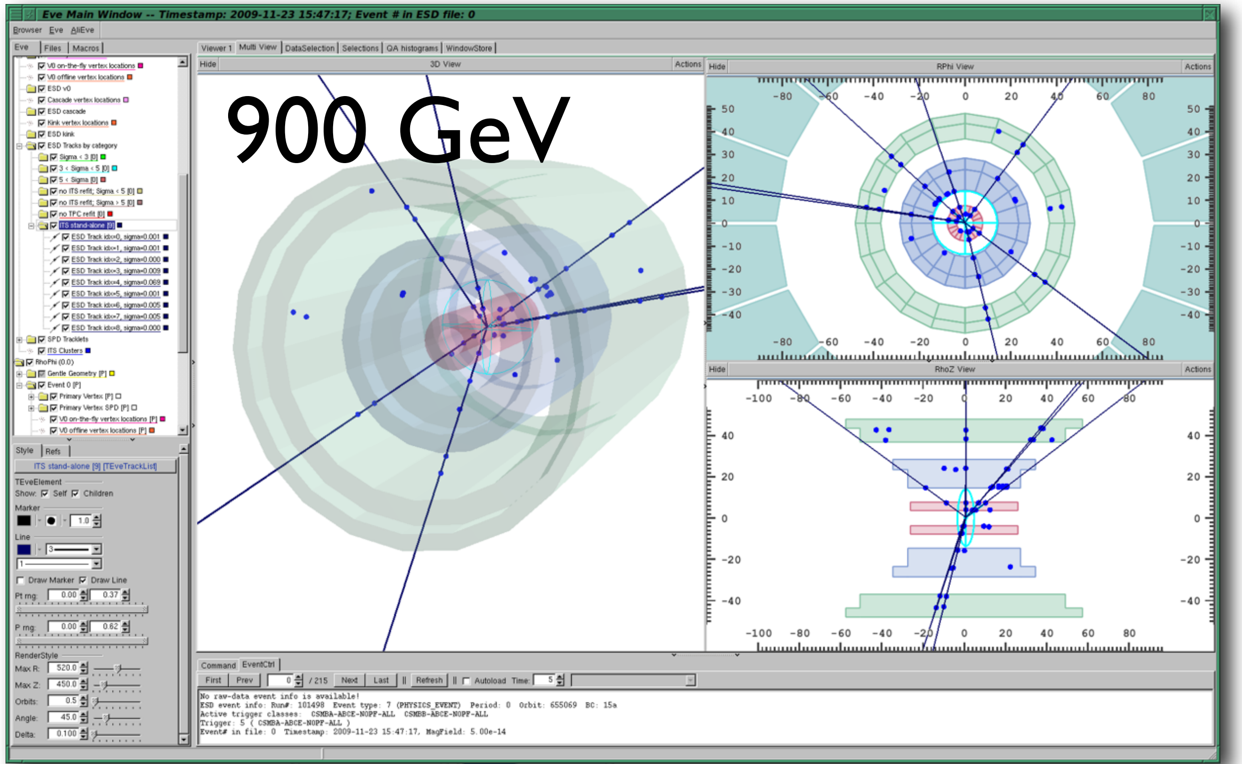


ALICE Silicon Pixel Detector Events & Results

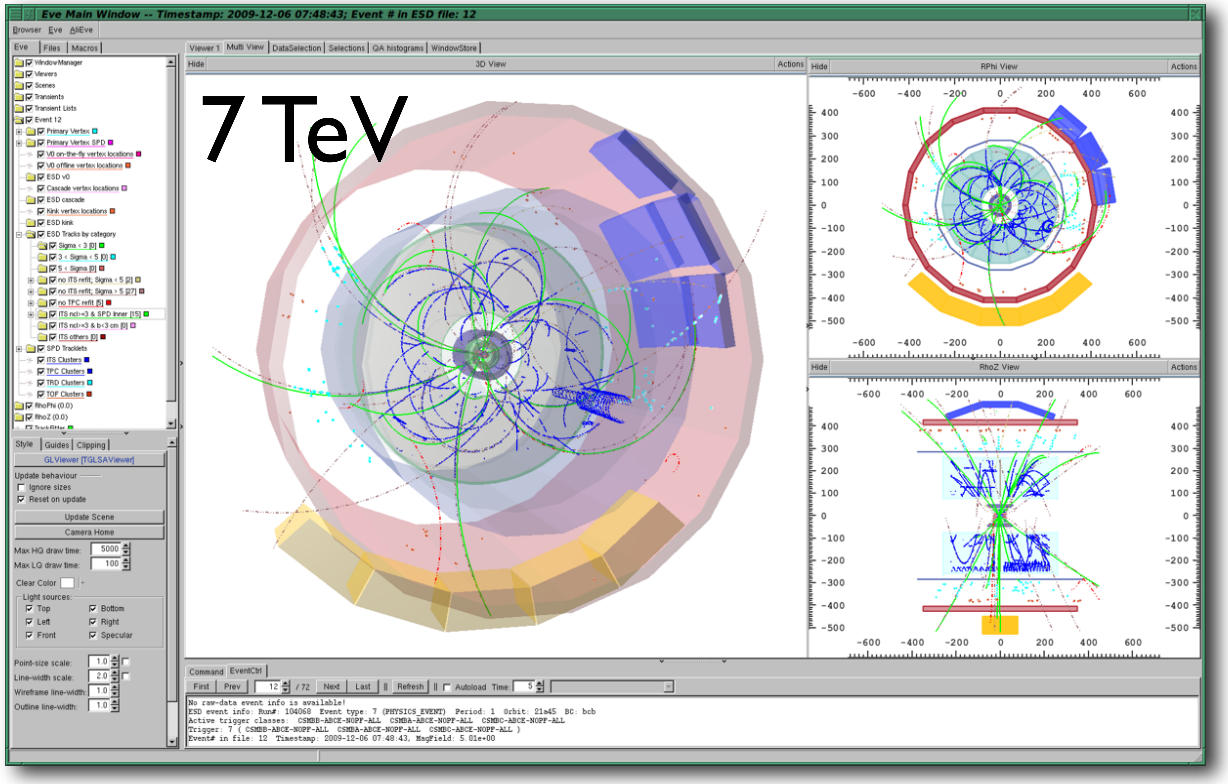
- ☑ 1st paper shows pseudorapidity density based on SPD data at 900 GeV (using SPD trigger in L0 decision)

EPJ C:Vol.65, 1 (2010)
284 events, 23/11/2009





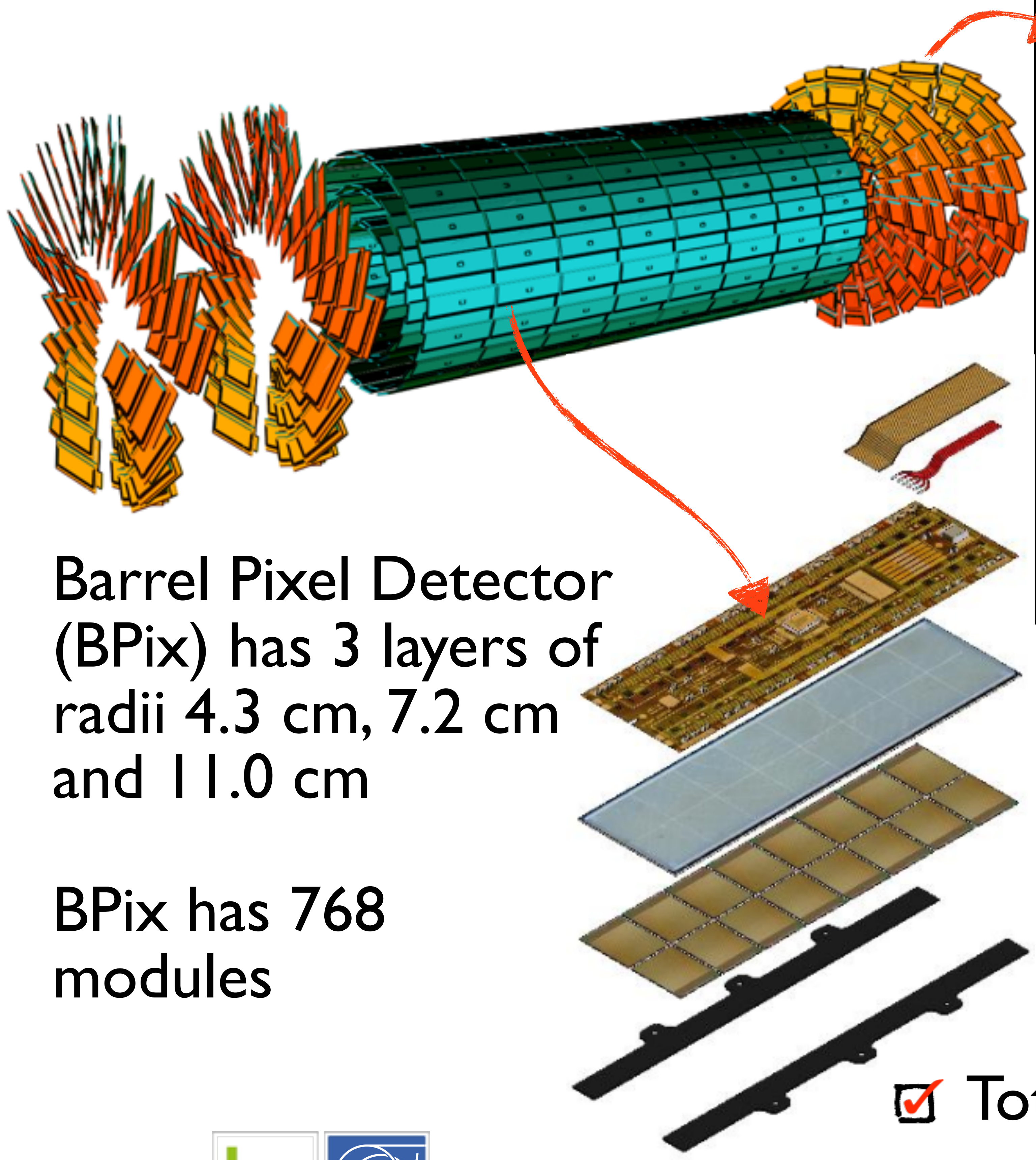
```
No raw-data event info is available!
ESD event info: Run#: 101498  Event type: 7 (PHYSICS_EVENT)  Period: 0  Orbit: 655069  BC: 15a
Active trigger classes:  CSMBA-ABCE-NOPF-ALL  CSMBB-ABCE-NOPF-ALL
Trigger: 5 ( CSMBA-ABCE-NOPF-ALL )
Event# in file: 0  Timestamp: 2009-11-23 15:47:17, MagField: 5.00e-14
```



```
No raw-data event info is available!
ESD event info: Run#: 104068  Event type: 7 (PHYSICS_EVENT)  Period: 1  Orbit: 21a45  BC: bcb
Active trigger classes:  CSMBB-ABCE-NOPF-ALL  CSMBA-ABCE-NOPF-ALL  CSMBC-ABCE-NOPF-ALL
Trigger: 7 ( CSMBB-ABCE-NOPF-ALL  CSMBA-ABCE-NOPF-ALL  CSMBC-ABCE-NOPF-ALL )
Event# in file: 12  Timestamp: 2009-12-06 07:48:43, MagField: 5.01e+00
```

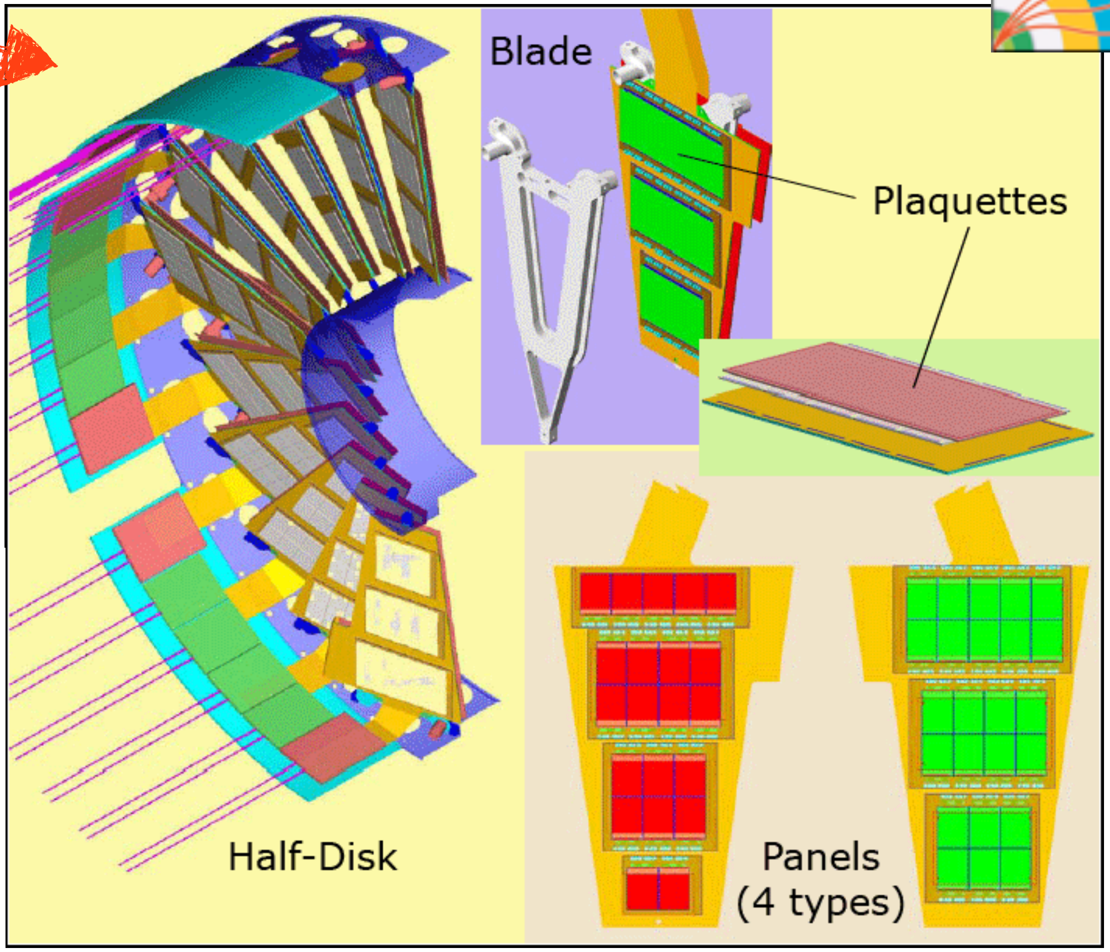
CMS Pixels

CMS Silicon Pixel Detector



Barrel Pixel Detector (BPix) has 3 layers of radii 4.3 cm, 7.2 cm and 11.0 cm

BPix has 768 modules

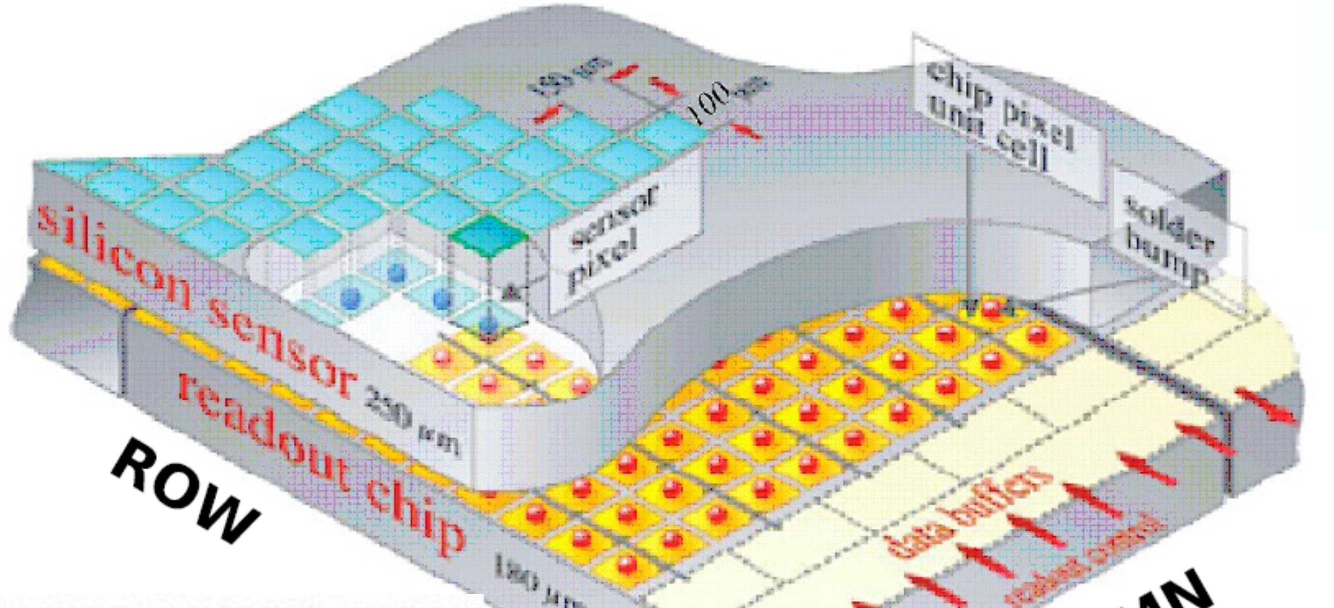


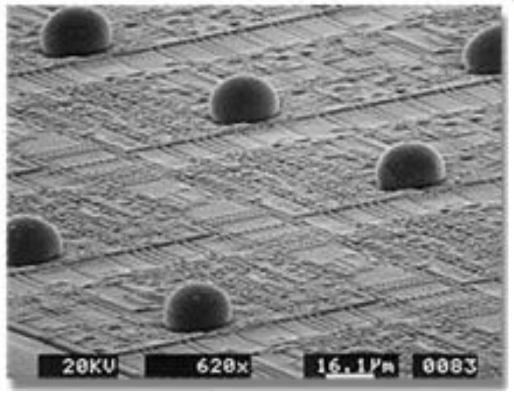
Forward Pixel Detector (FPix) has 2disks on each side at 34.5 cm and 46.5 cm

FPix has 672 modules

☑ Total of ~15,840 Readout Chip

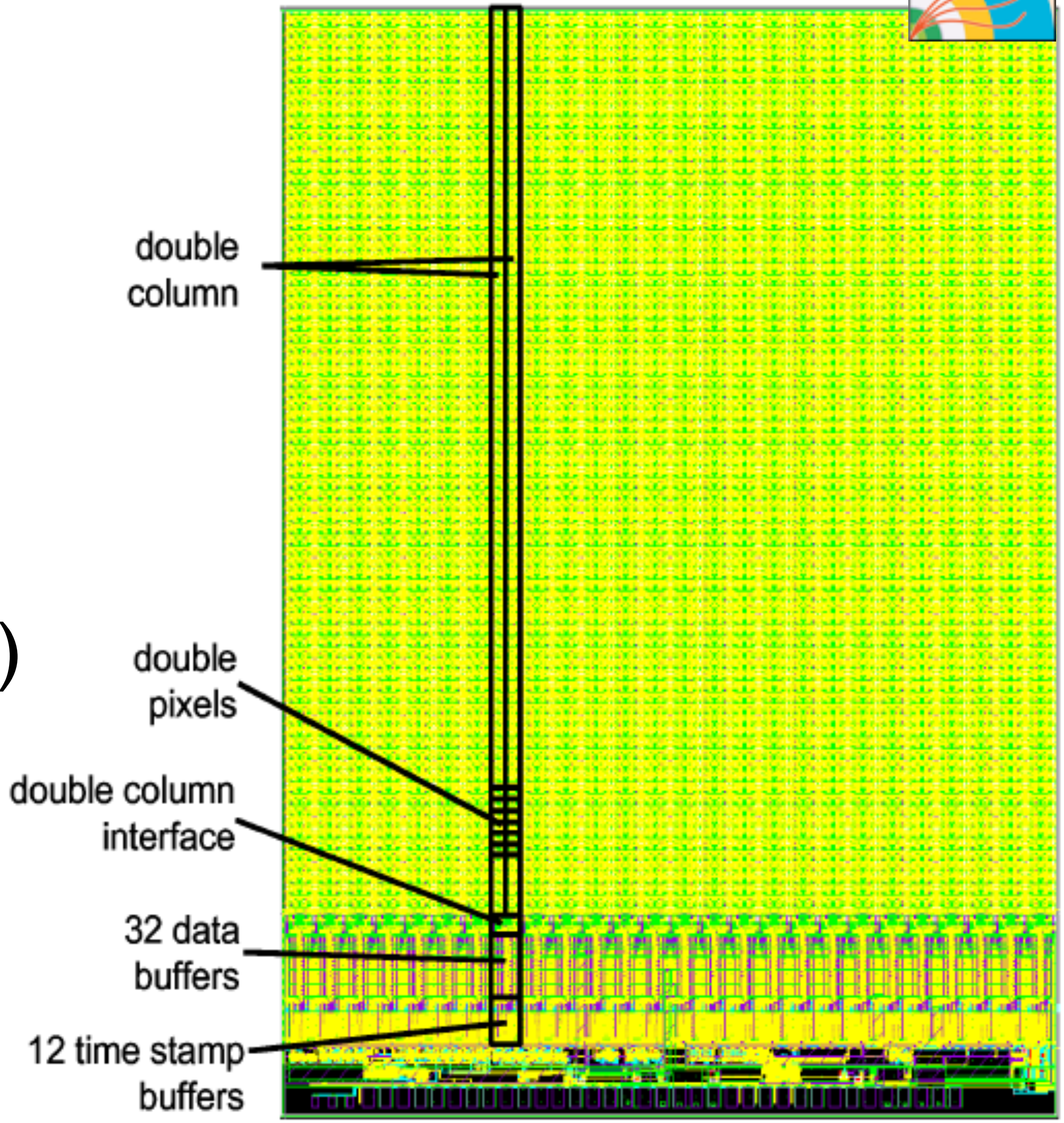
CMS Pixel Sensor Detector





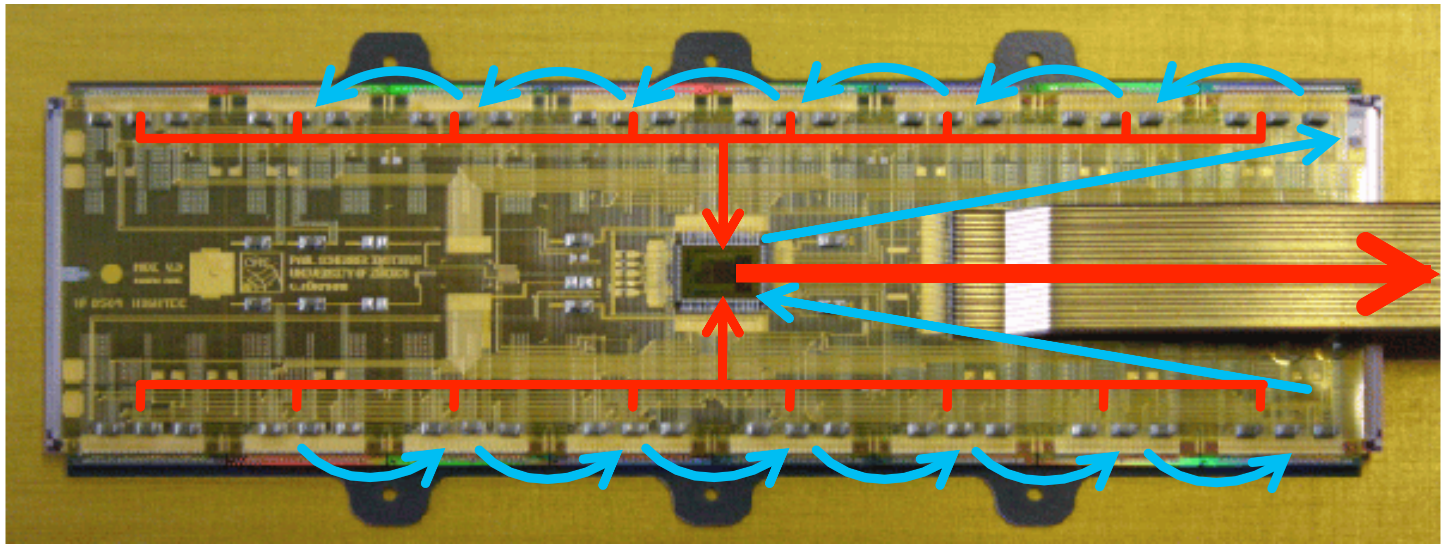
ReadOut Chip (ROC) bump bonded sensor pixels.

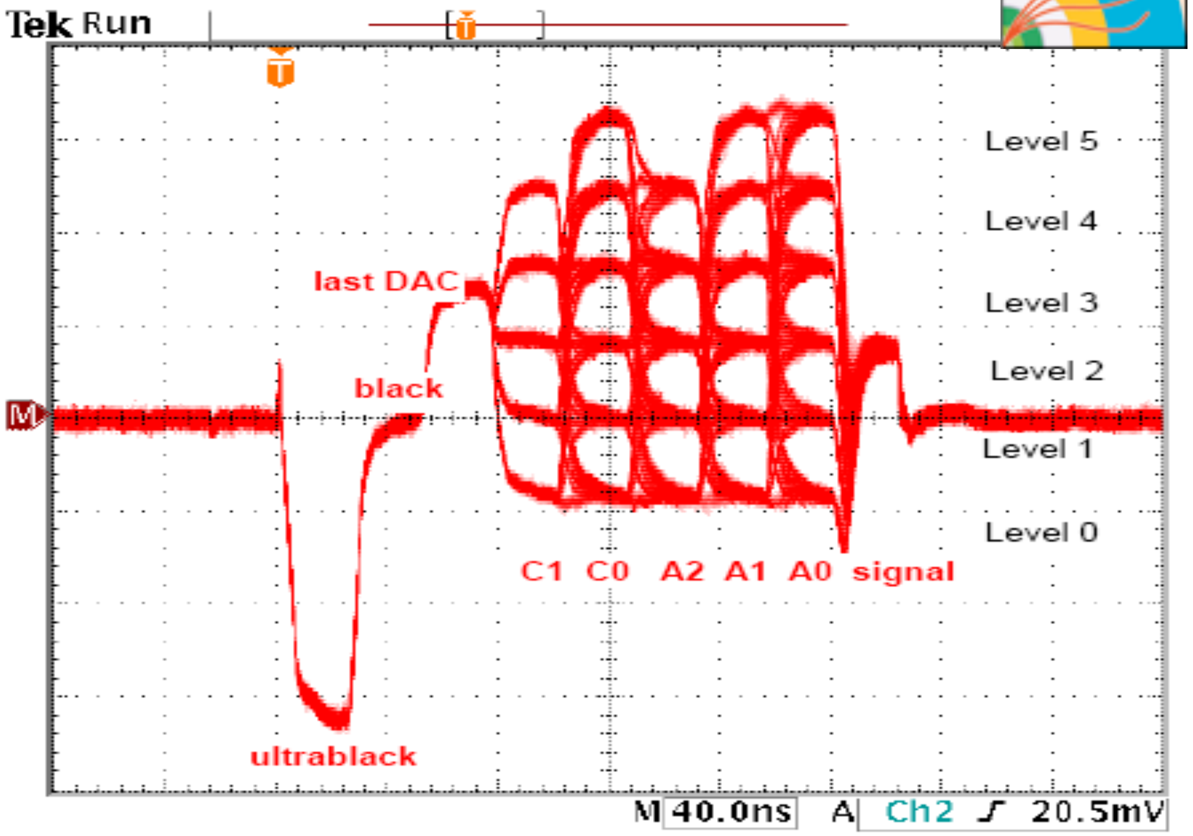
52 × 80 = 4160 pixels per ROC
15,840 ROCs
66 million pixels
Automatic zero-suppression
Double column drain architecture
40 MHz analog readout

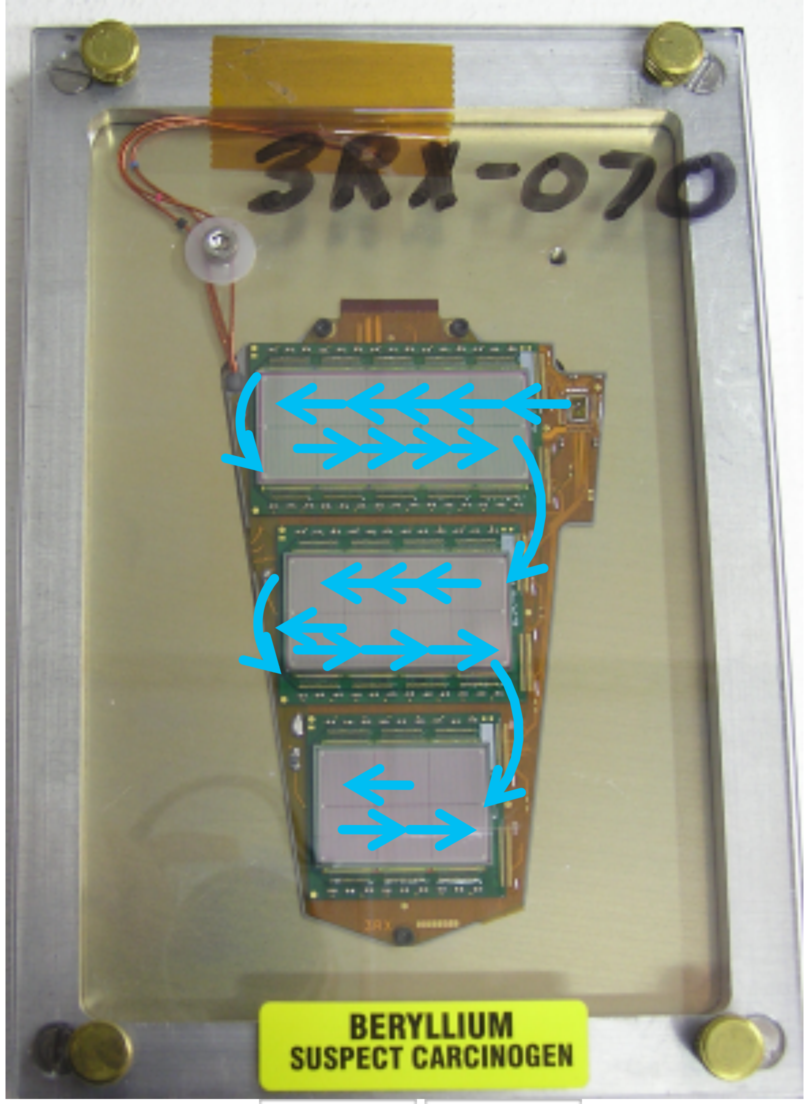


Each pixel has a programmable threshold (adjusting called trimming)

CMS Pixel Detector Analogue Readout

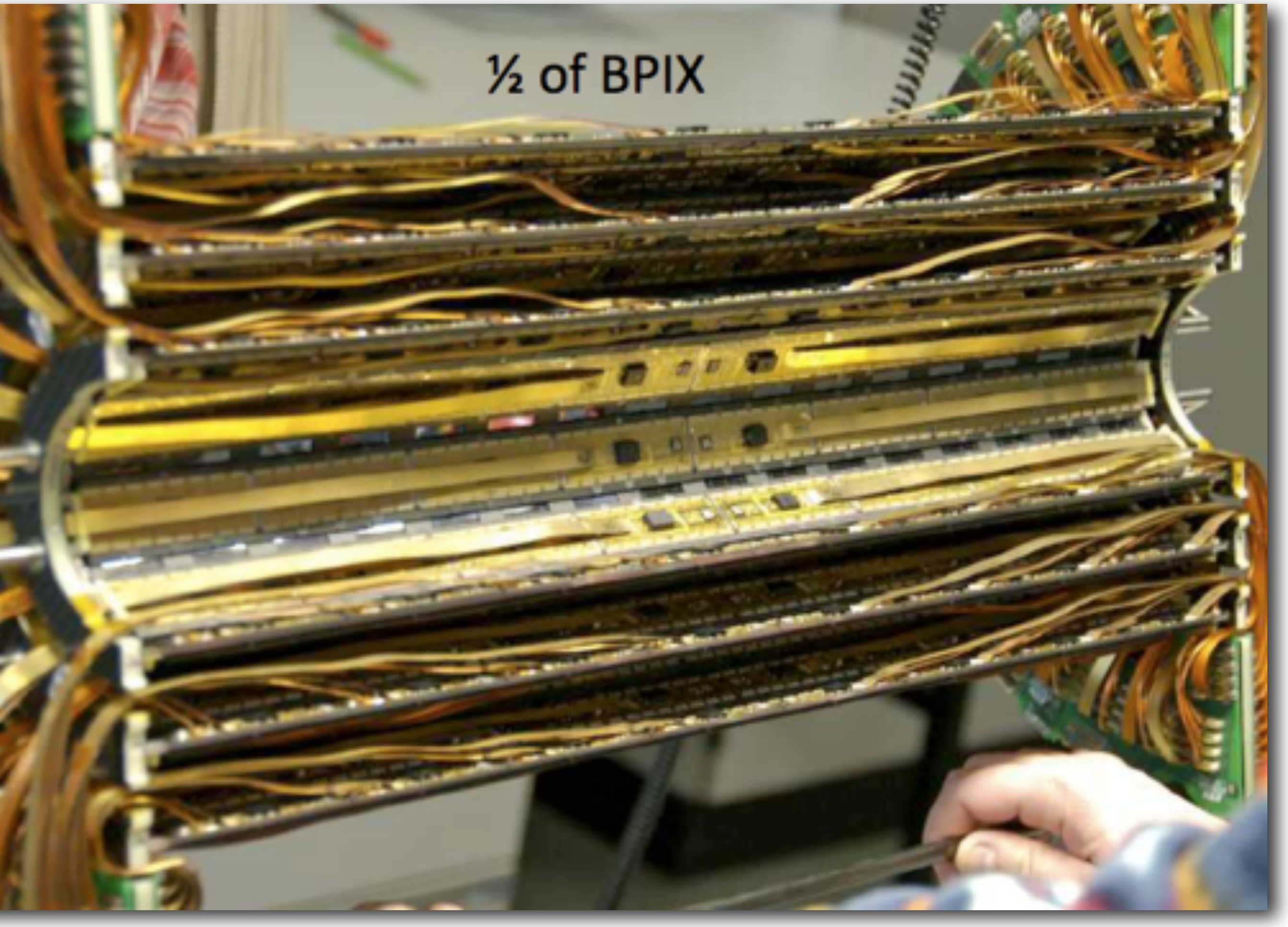


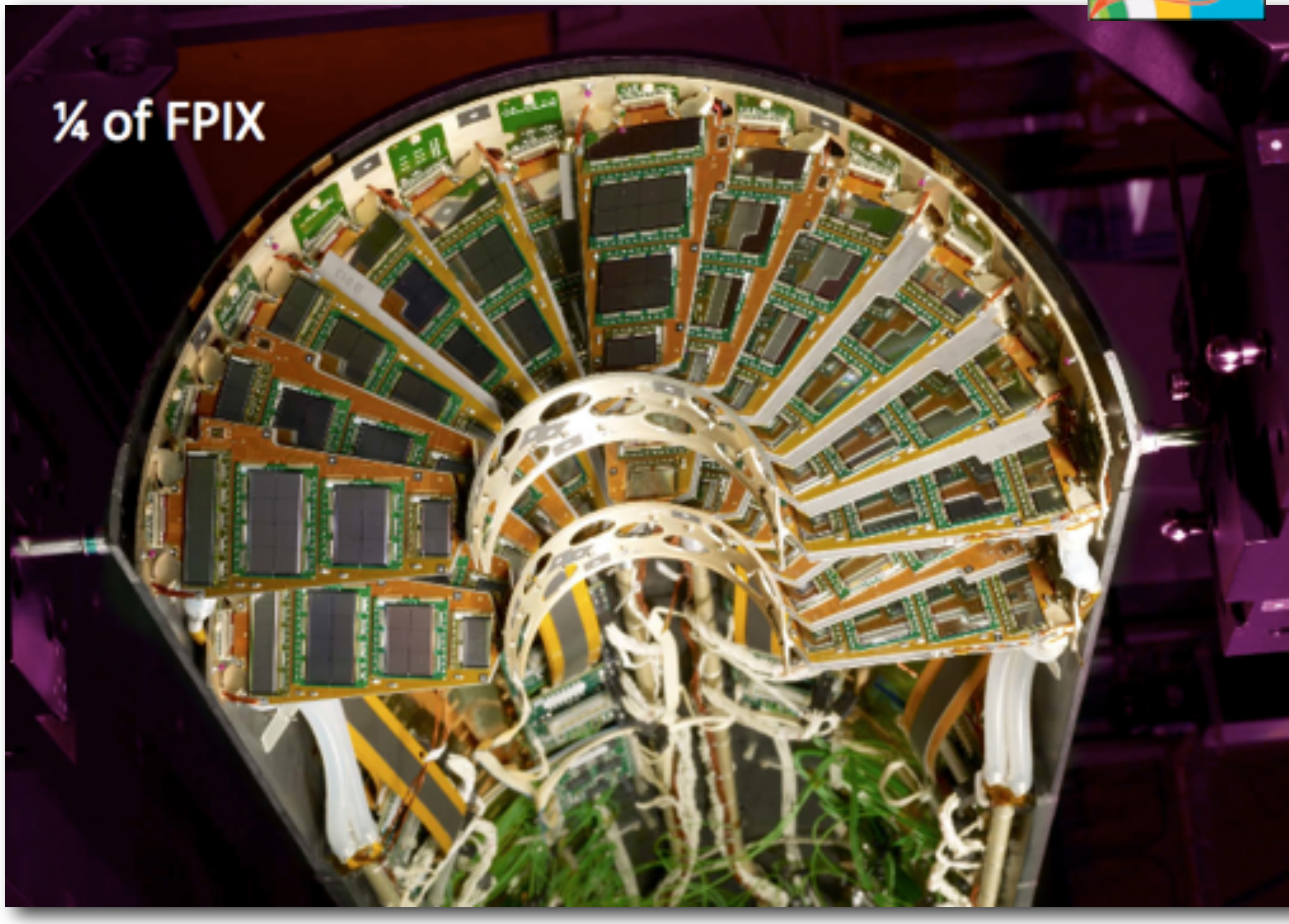




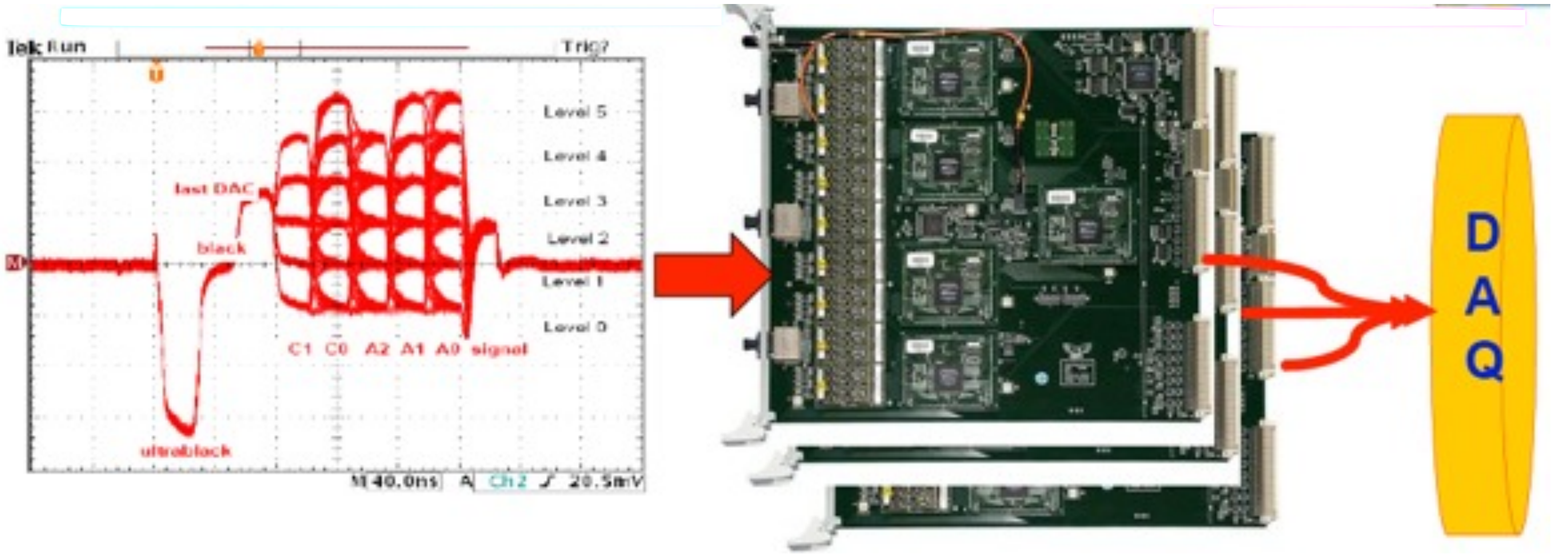
- On receiving a L1 trigger, the Token Bit Manager (TBM) initiates a Chinese-whisper of “token bits” that instruct each ROC to send its hit data to the TBM
- The signal from the TBM is electrical and analog. It encodes the ROC #, row and column and charge deposit of each pixel hit
- The electrical signal from the TBM is converted to optical by the Analog-Optical Hybrid (AOH)

CMS BPIX & FPIX and their DAQ

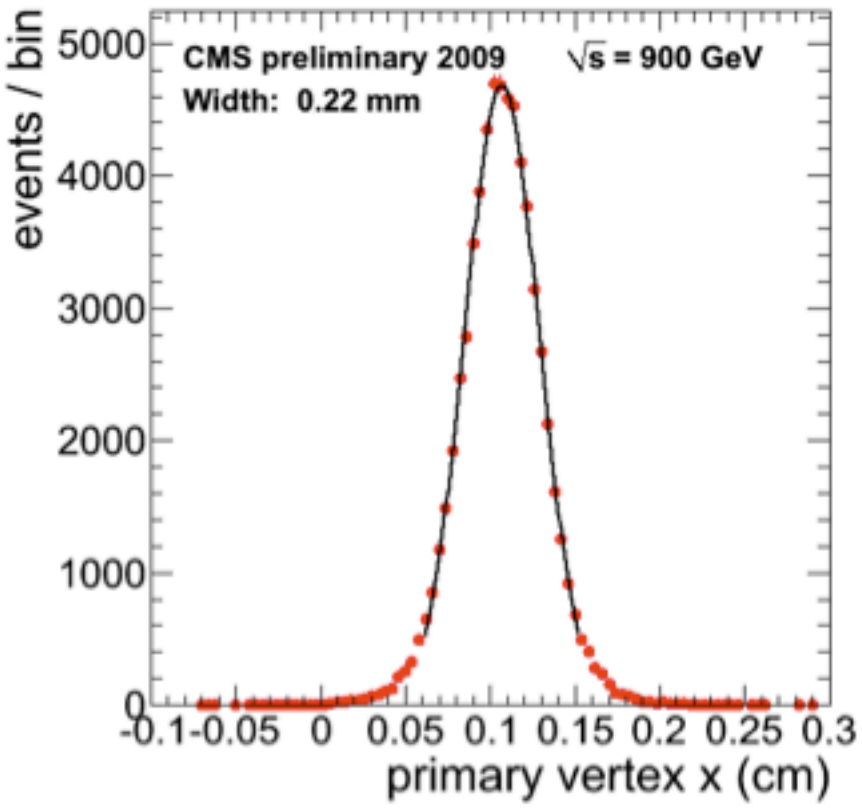


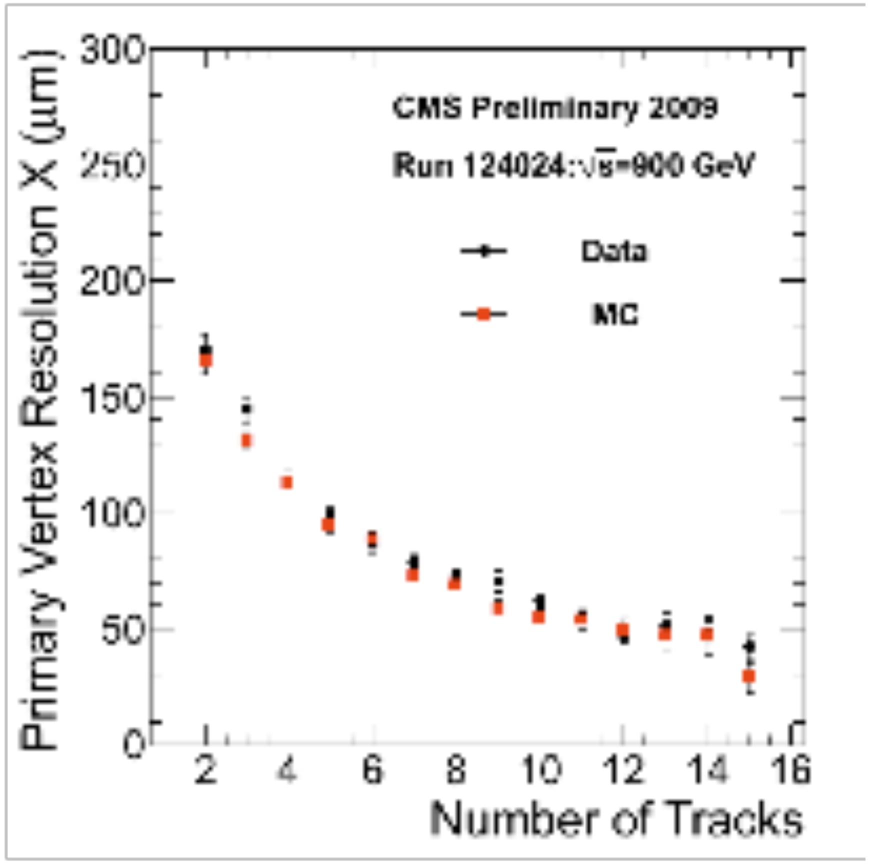


- Pixel Front End Driver (FED) digitizes analog signals given the level thresholds for decoding.
- FEDs send digitized data down S-Link cables to the Data Acquisition System (DAQ).

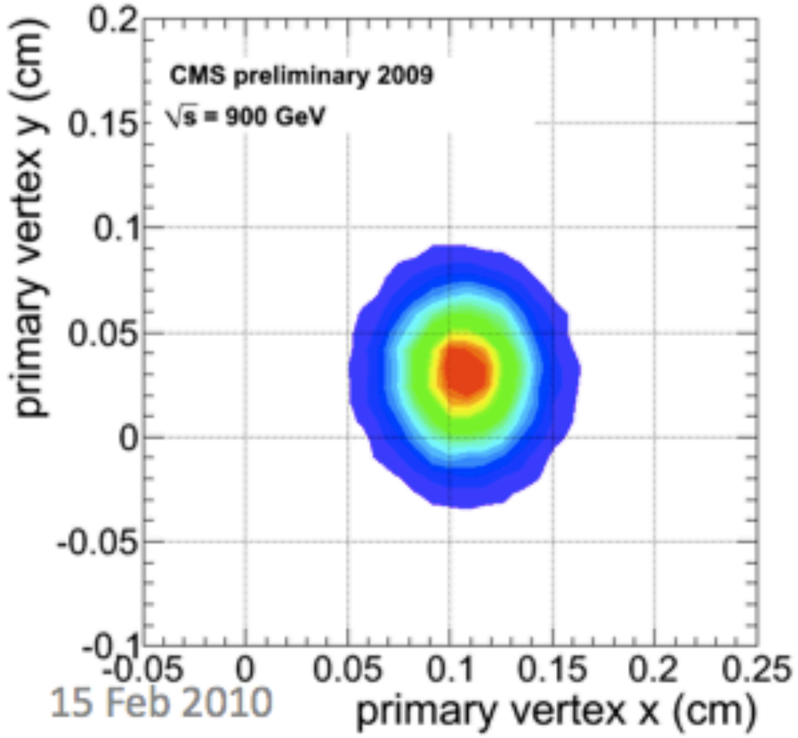


CMS Primary Vertex & Neutral Kaon Reconstruction

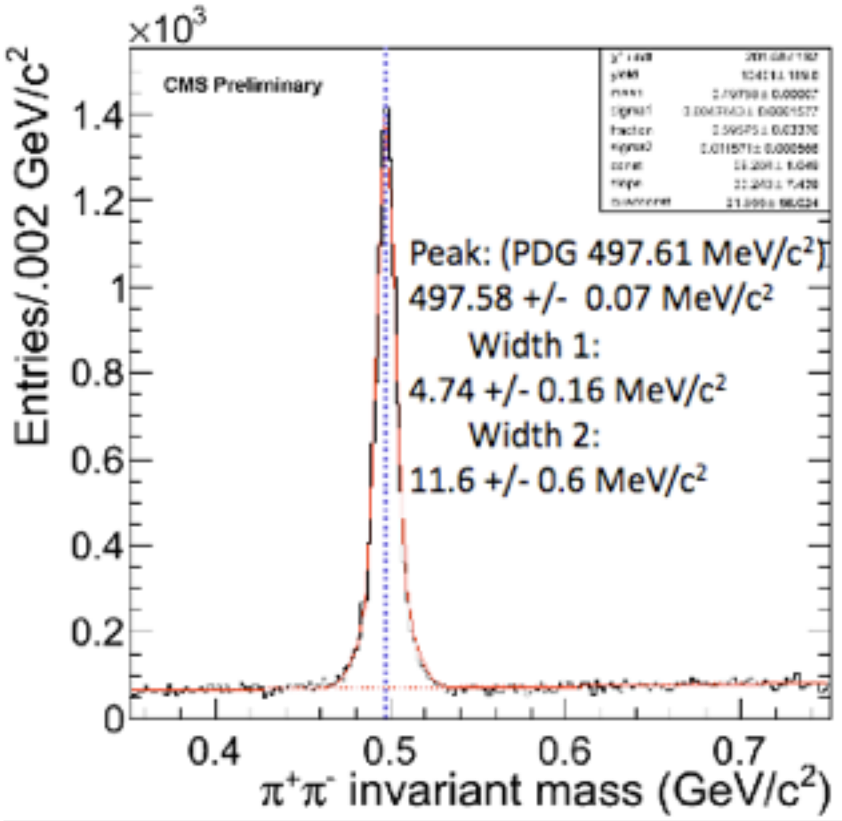


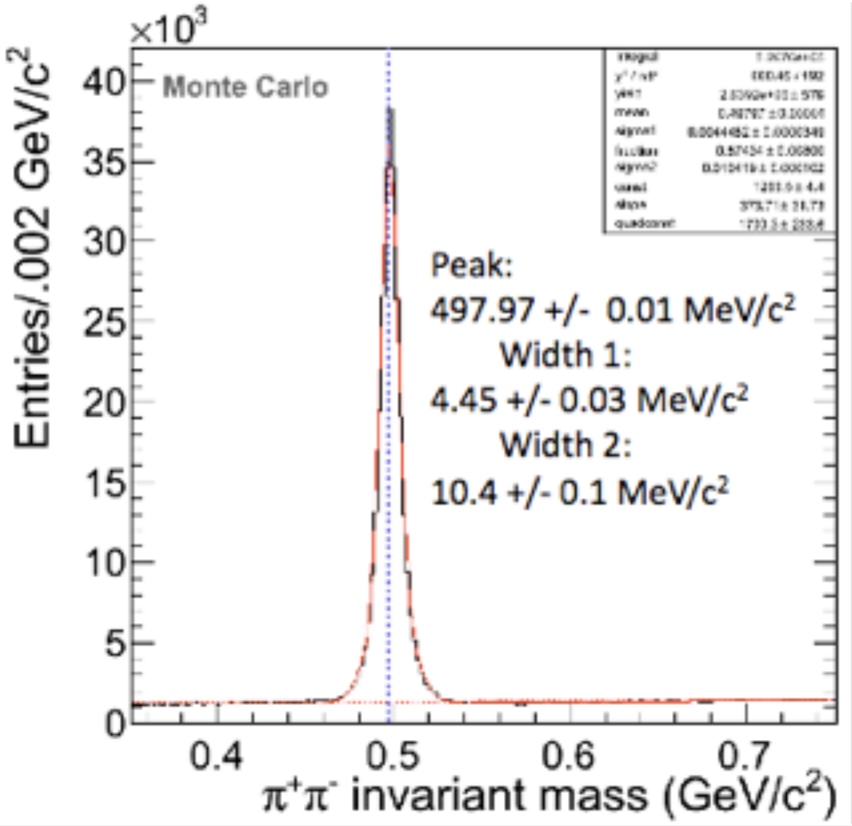


- encouraging primary vertex resolution agreement
- good neutral kaon reconstruction



15 Feb 2010





Diamond Detectors

ATLAS
Diamond
Pixel
Upgrade

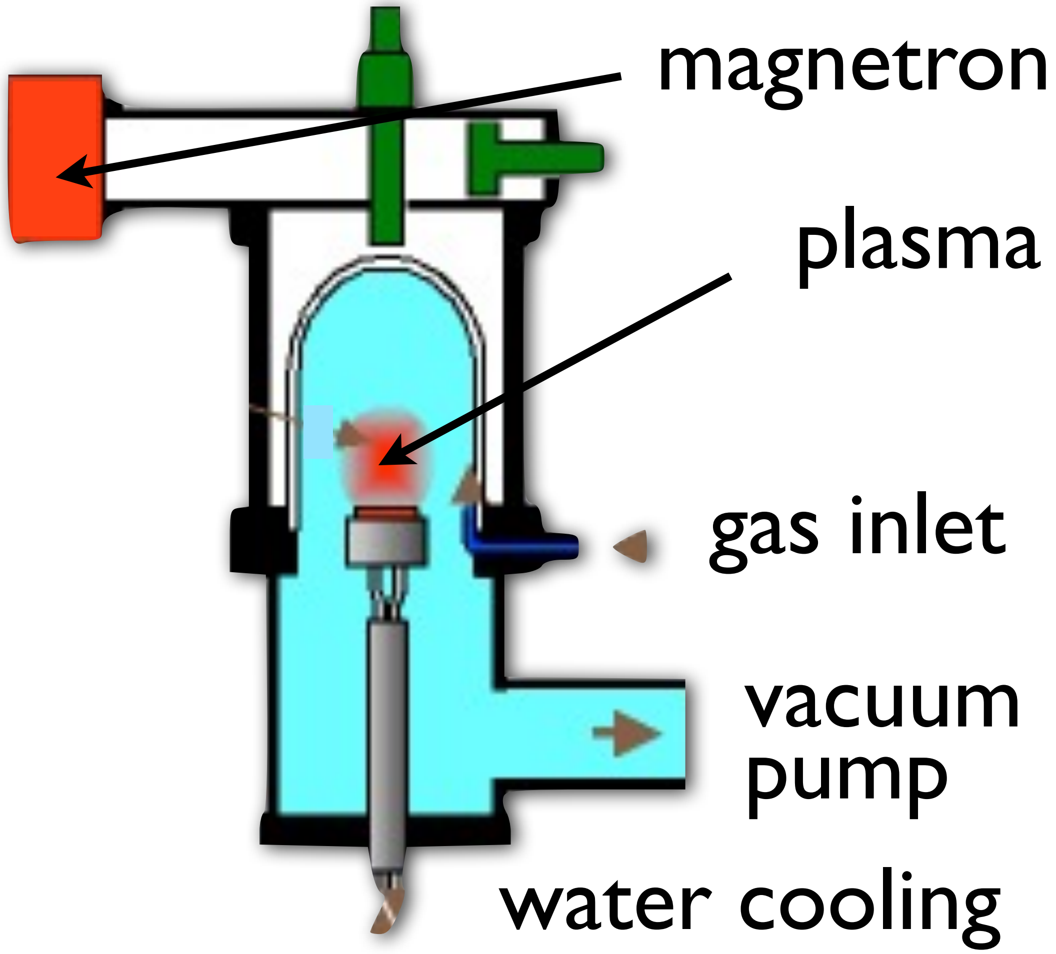
Super
ATLAS

Diamond Properties and Grow

Why diamond?

- ☑ high band gap (5.5 eV), breakdown field (10^7 V/cm) & resistivity ($>10^{11}$ Ω cm) → low leakage current
- ☑ low dielectric constant (5.7) → low capacitance
- ☑ high displacement energy (43 eV/atom) → radiation hard
- ☑ high thermal conductivity (~2k W/m.K) → no cooling
- ☐ high energy to create e/h pair (13 eV) & low average created signal (36 e_0 / µm) → low signal, but also low noise

Microwave CVD Plasma Reactor

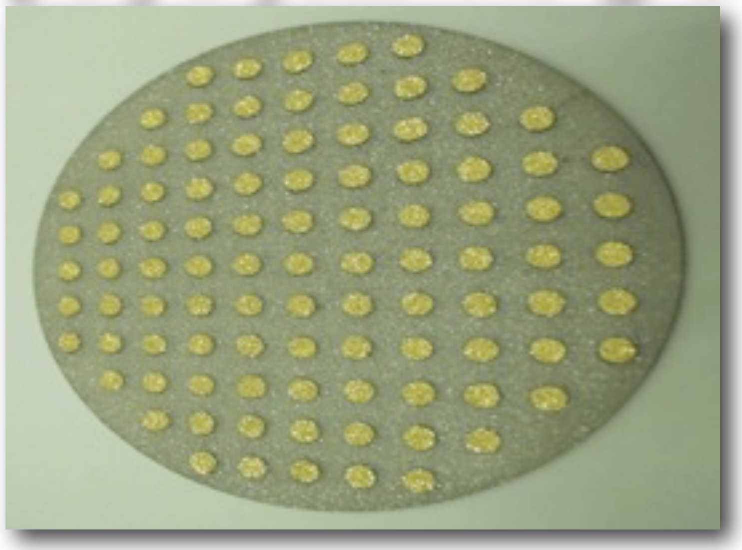


Metallization

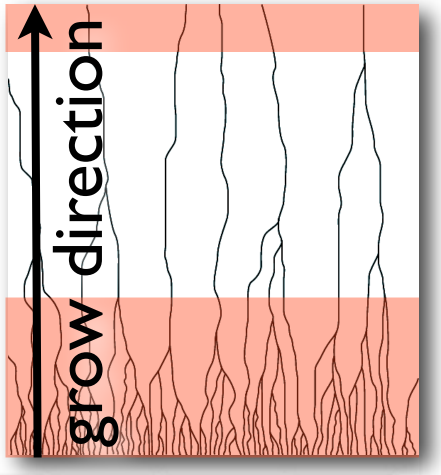
- ☑ no doping needed
- ☑ metal contacts (pads, strips, pixels) sputtered or evaporated

Diamond Detector Materials

polycrystalline (pCVD):

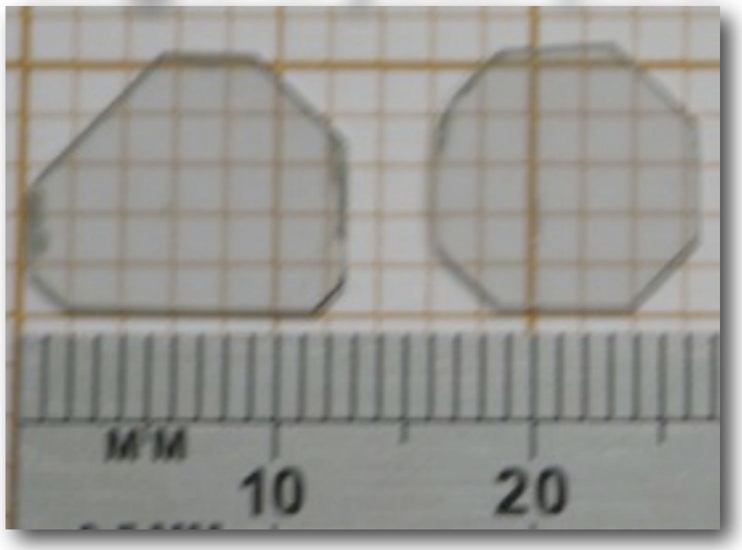


grown on non-diamond substrate



> 12 cm ∅
> 2 mm thickness

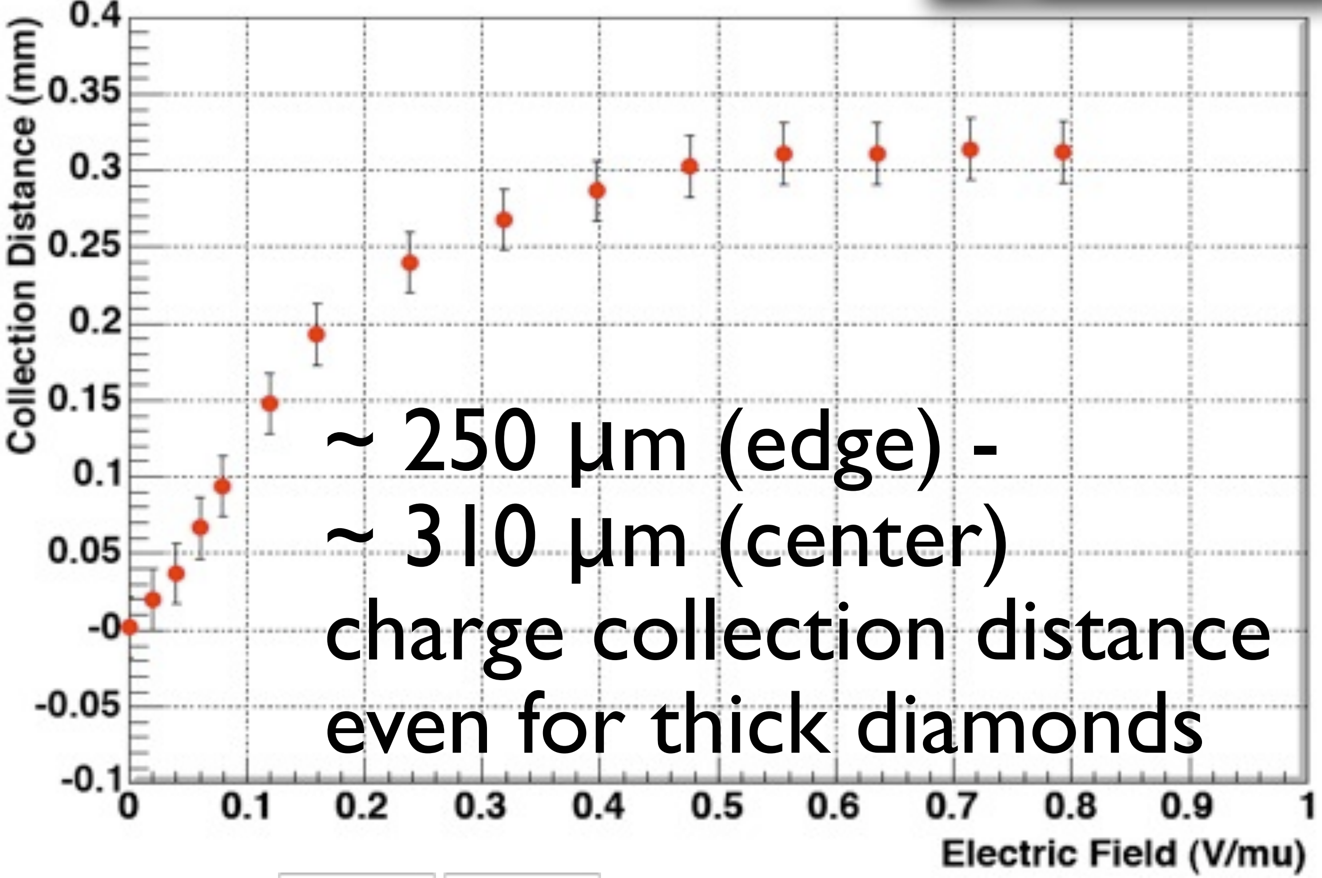
single crystal (scCVD):



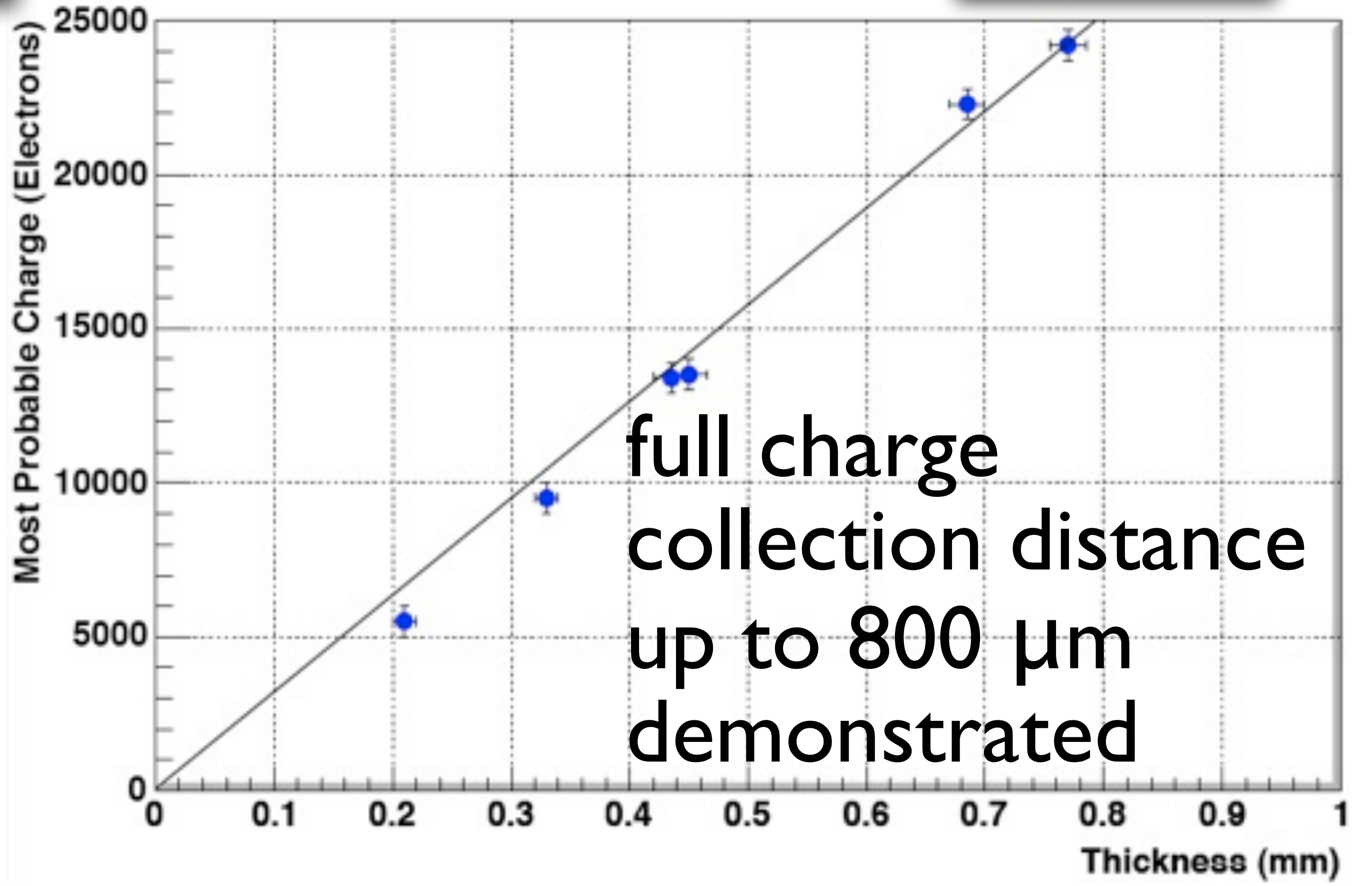
grown on HTHP diamond substrate

~ 1 cm^2
> 1 mm thickness

real single crystal

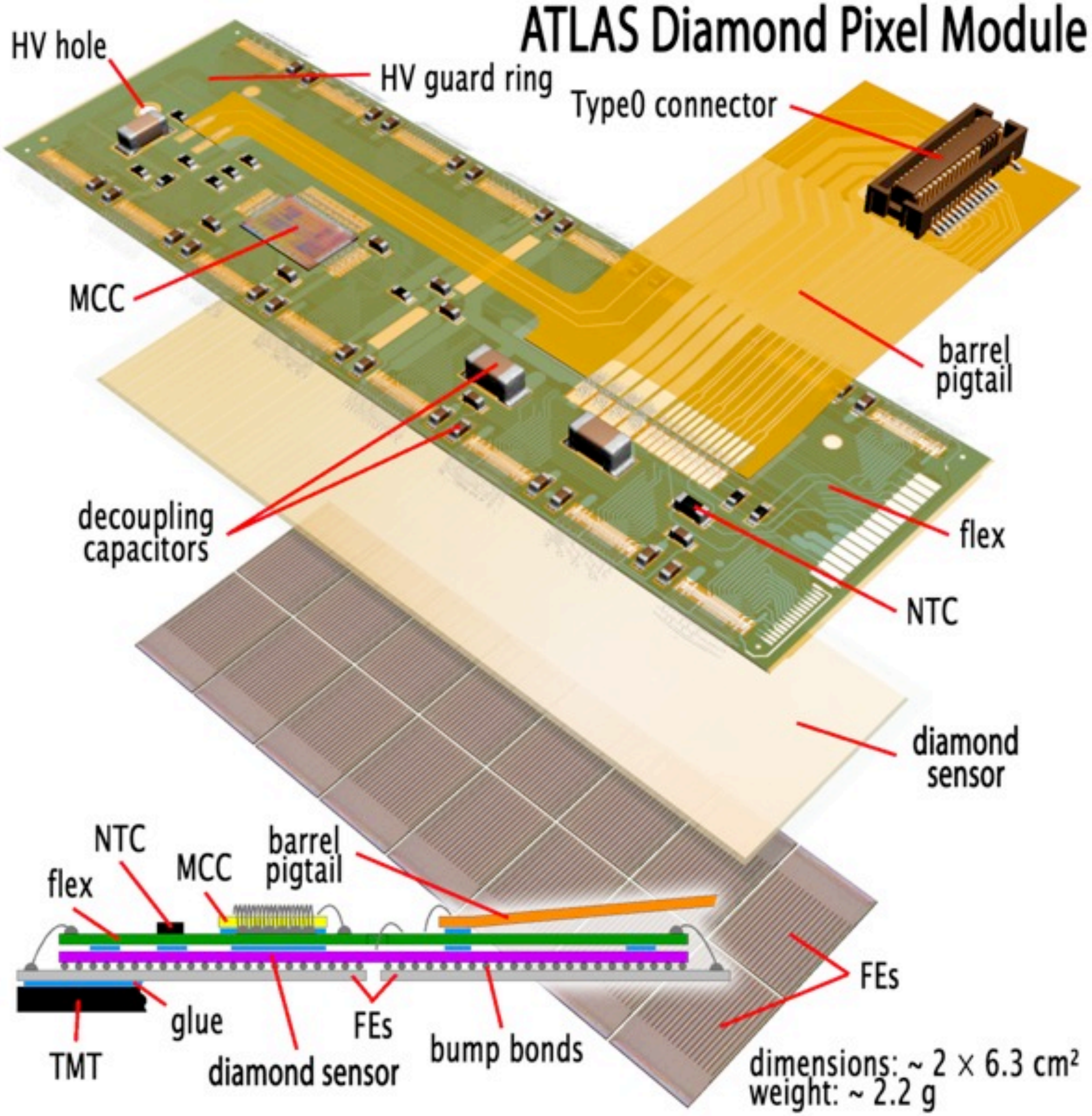


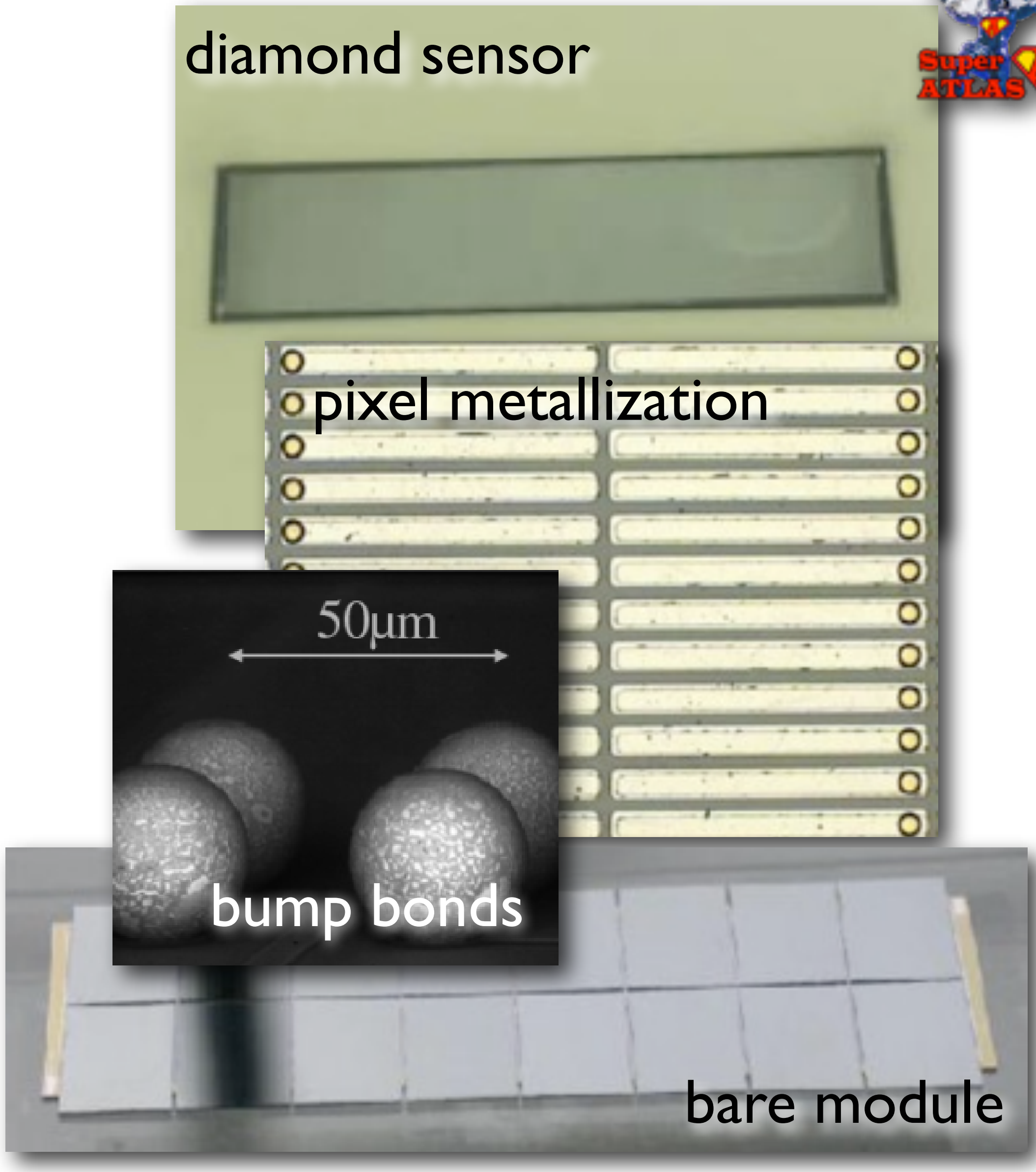
~ 250 µm (edge) -
~ 310 µm (center)
charge collection distance even for thick diamonds



full charge collection distance up to 800 µm demonstrated

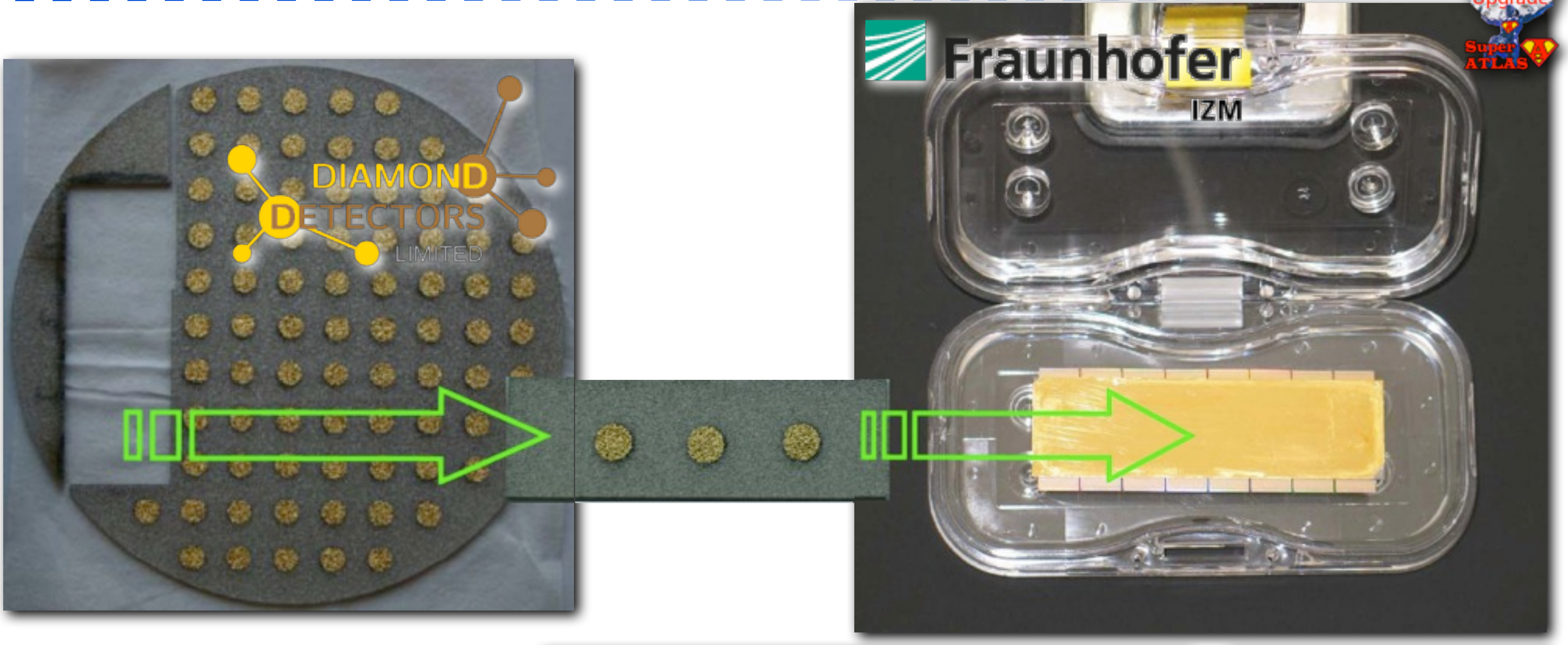
ATLAS pCVD Diamond Pixel Module



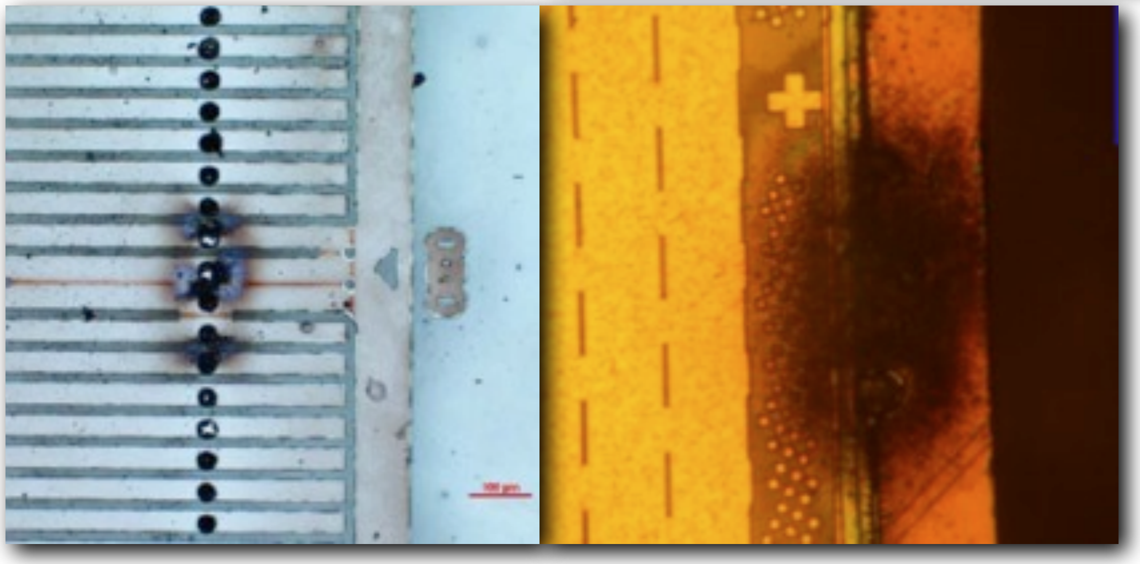


- 800 µm pCVD diamond
- 50×400(600) µm pixels
- 16 ATLAS FE-13 chips
- active area: 61×16.5 mm^2

Diamond Pixel Module - Industrialization



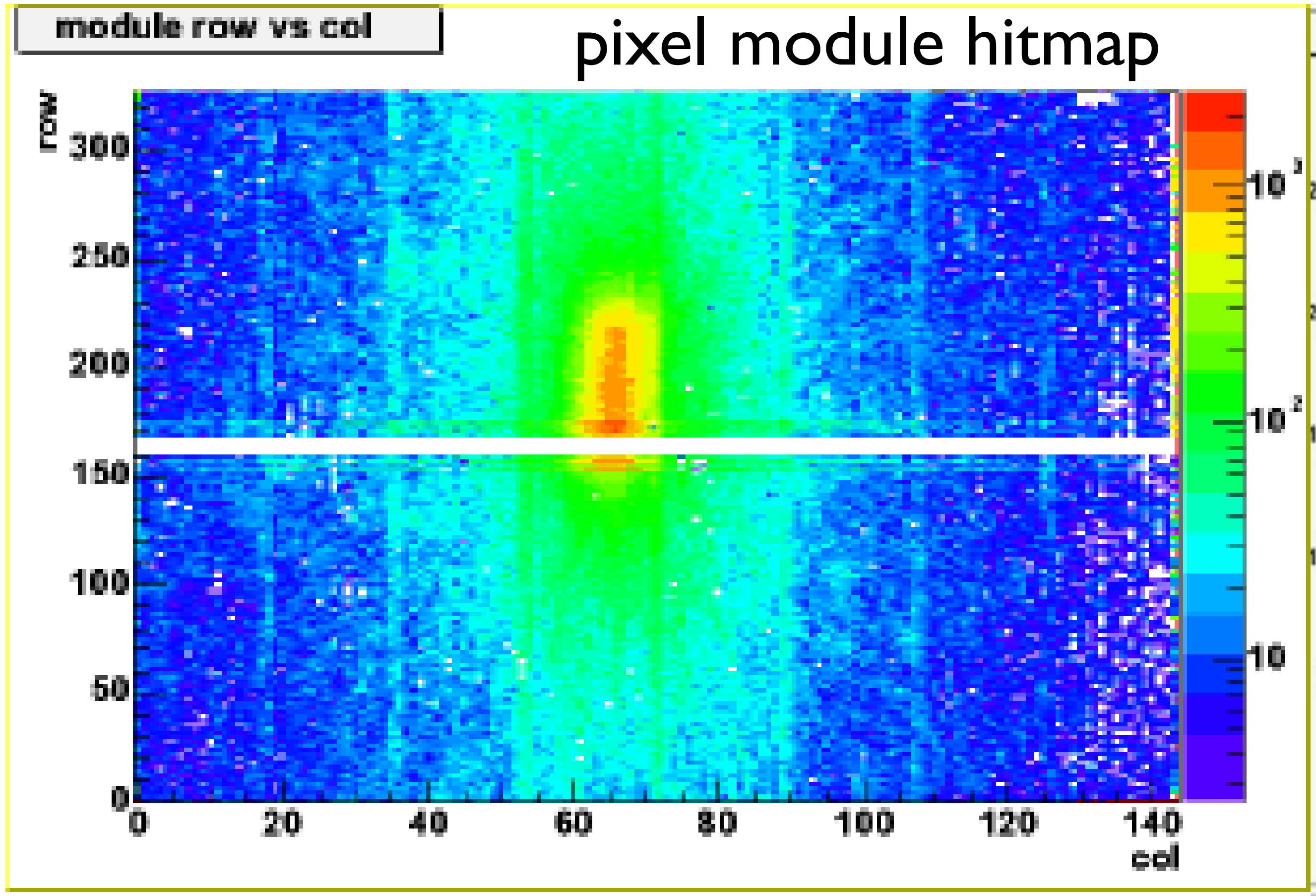
- diamond sensor can be reused if module QA fails



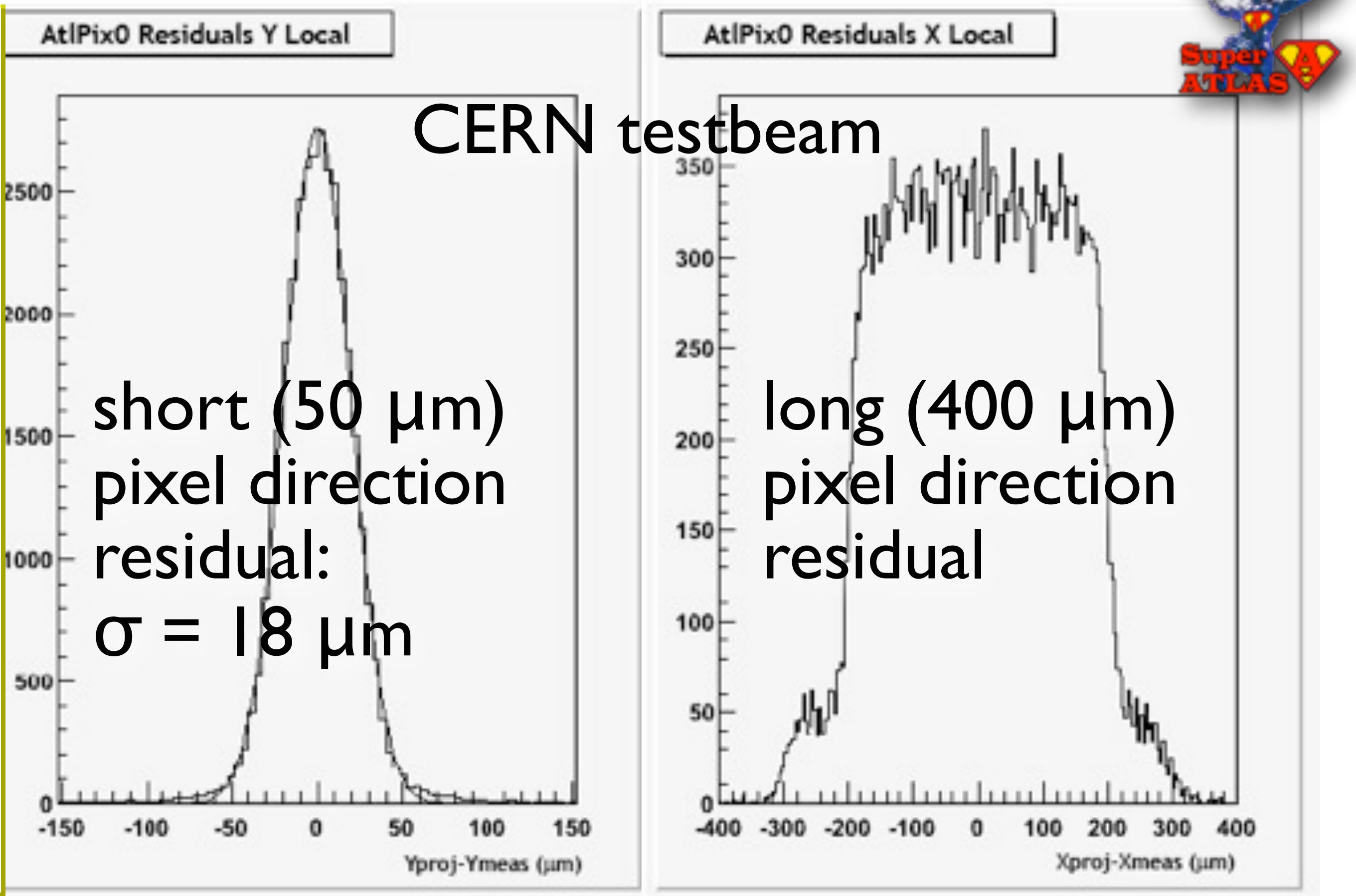
before rework

after rework

pCVD Diamond Module: Resolution & Efficiency



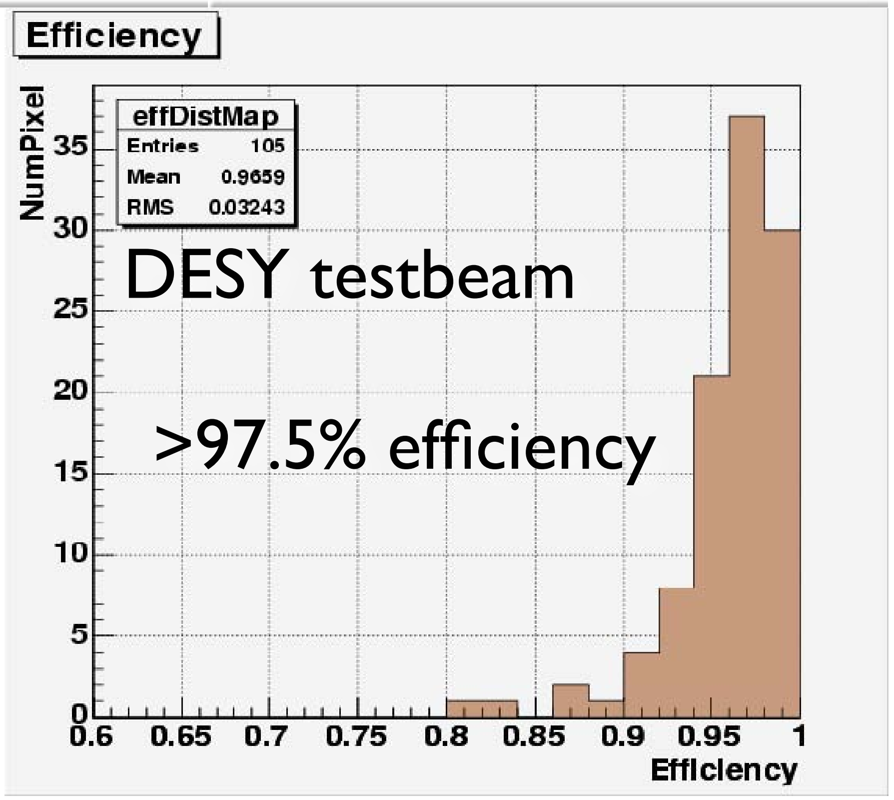
pixel module hitmap



CERN testbeam

short (50 µm) pixel direction residual: σ = 18 µm

long (400 µm) pixel direction residual

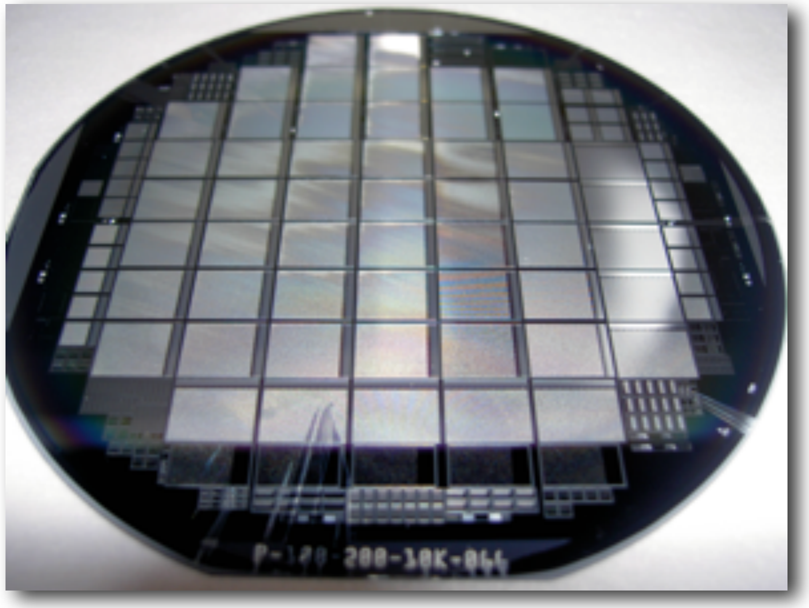


DESY testbeam

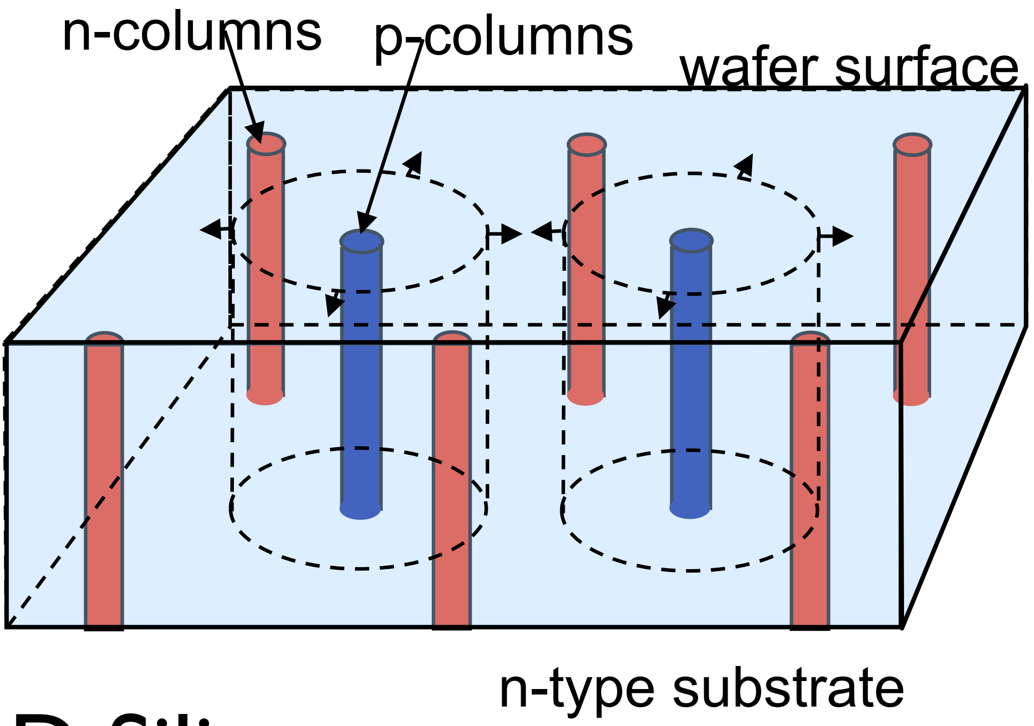
>97.5% efficiency

- residuals show expected behavior: 18 µm → unfold telescope resolution → 14 µm as expected from 50 µm/√12
- 97.5% efficiency lower limit due to scattered tracks (4 GeV electrons)

3D Silicon Detectors



Silicon 3D Detectors Basics & History

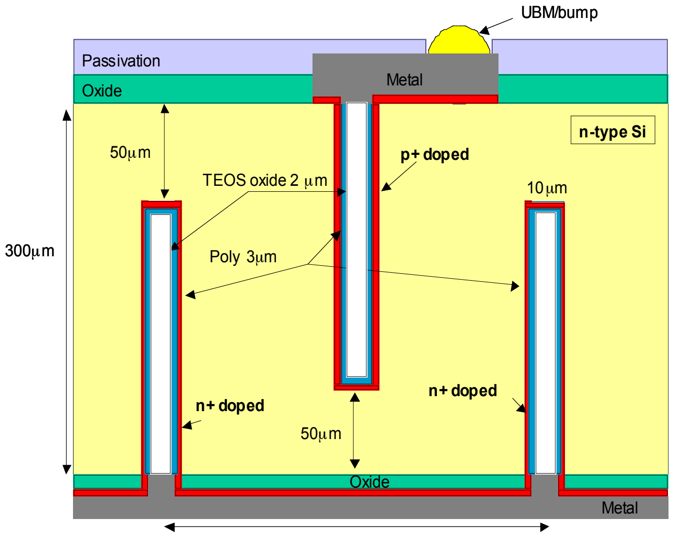


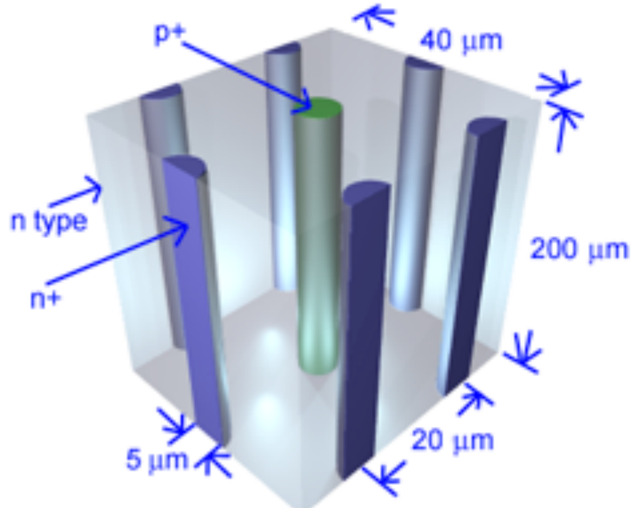
3D Silicon:

- Integrate the implants not on the surface but through the detector
- Allows highly segmented pixel detectors, but additionally:
- Distance from n- to p-column small: low depletion voltage!
- Short drift distance = fast signal = high rate capable!

3D Silicon History

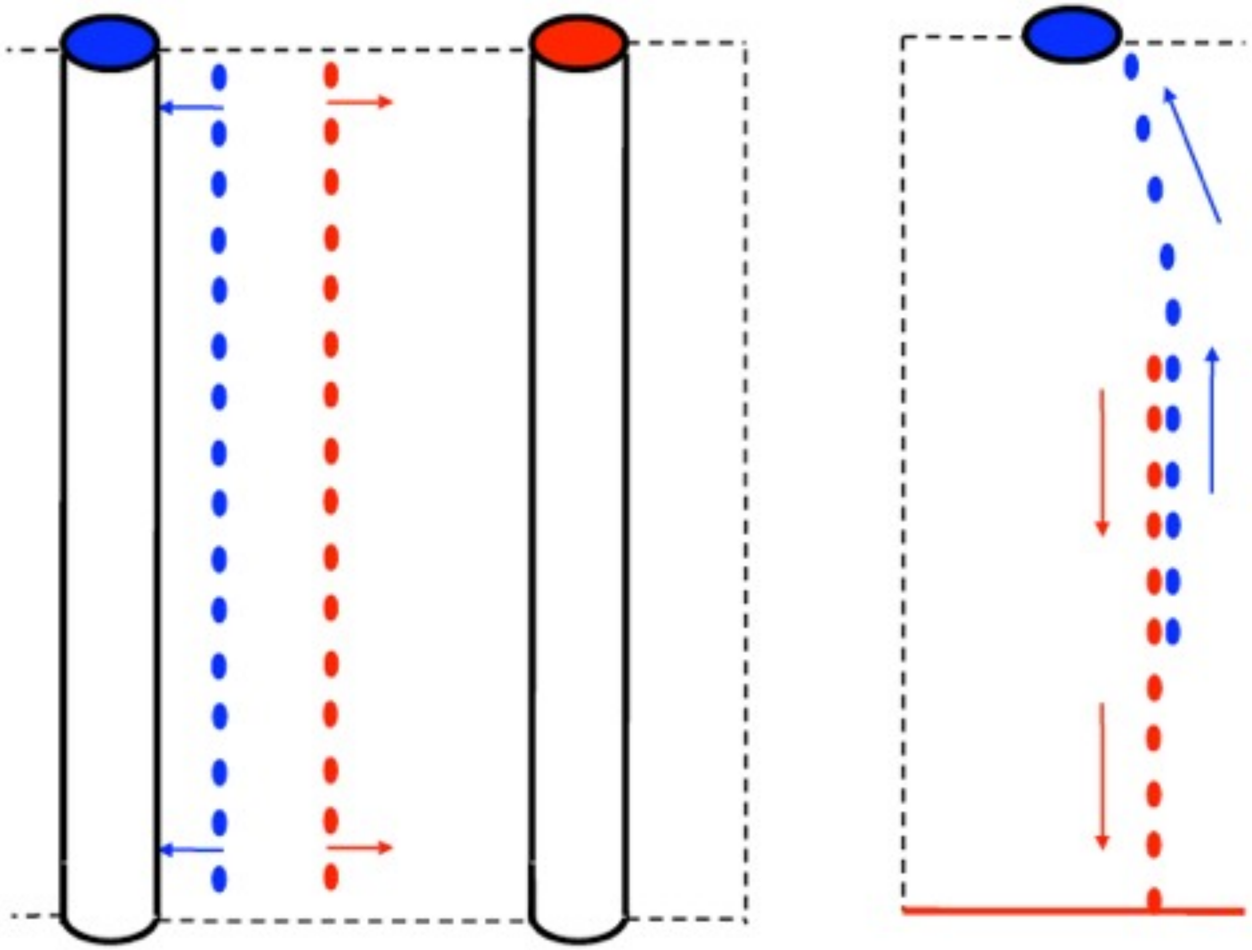
- MEMS technology + VLSI to sensor fab: Deep Reactive Ion Etching (DRIE)
- Electrode implants: etched, doped, filled columns (S. Parker 1995)
- Dicing: etched, doped edge trench (C. Kenney 1997)
- Key benefits: Radiation hardness and active edges





Silicon 3D Radiation Hardness

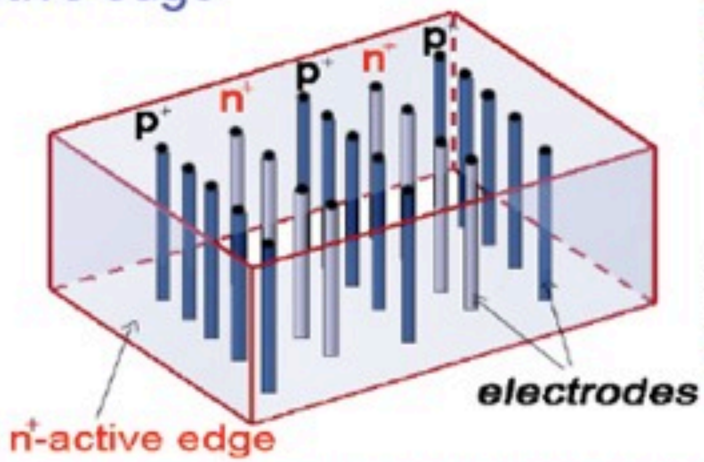
- Decoupled directions: track traversal versus drift field
- Low depletion voltage
- Short charge collection path, fast signal
- Retain full charge from MIP in 250µm Si
- Signal loss dominated by trapping



Silicon 3D Sensor Family

The 3D sensors family:

Full 3D
Active edge

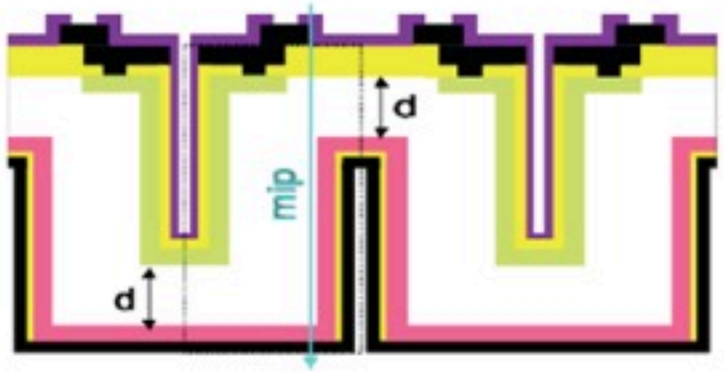


3DC Fabricated at Stanford and tested with Atlas pixel Readout – and SLHC fluences Design at its 5th Generation

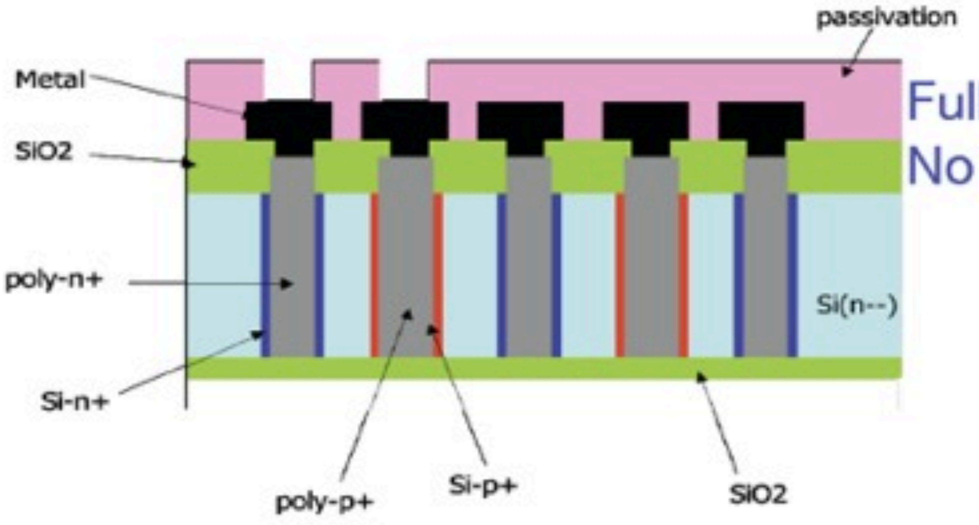
Being also fabricated at SINTEF in the ATLAS Upgrade framework as part of the 3DC Consortium.
(No data available yet)

IRST and separately CNM.
Being presently fabricated
(No data available yet)

Double column
No active edge



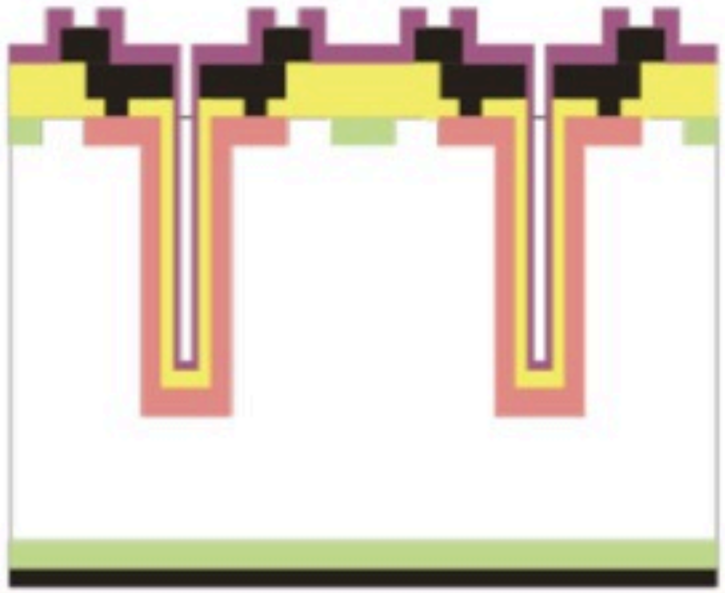
iceMOS- Being presently fabricated
Work performed in the RD50 framework
(No data available yet)



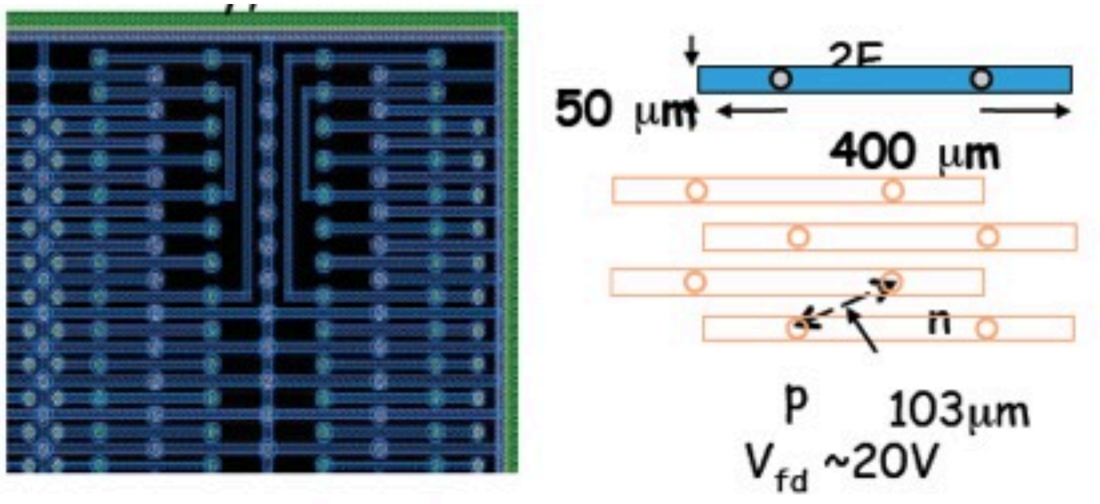
Full 3D
No active edge

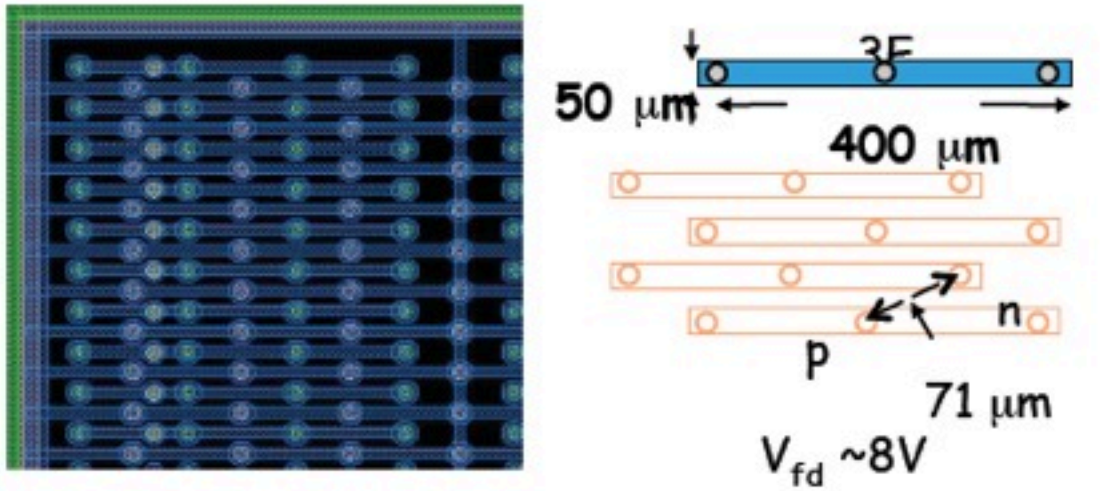
IRST/CNM fabricated in the RD50 Framework in 2005 Tested with SCTA readout Electronics. Data and Simulations show that the design is NOT radiation hard For B-layer replacement.

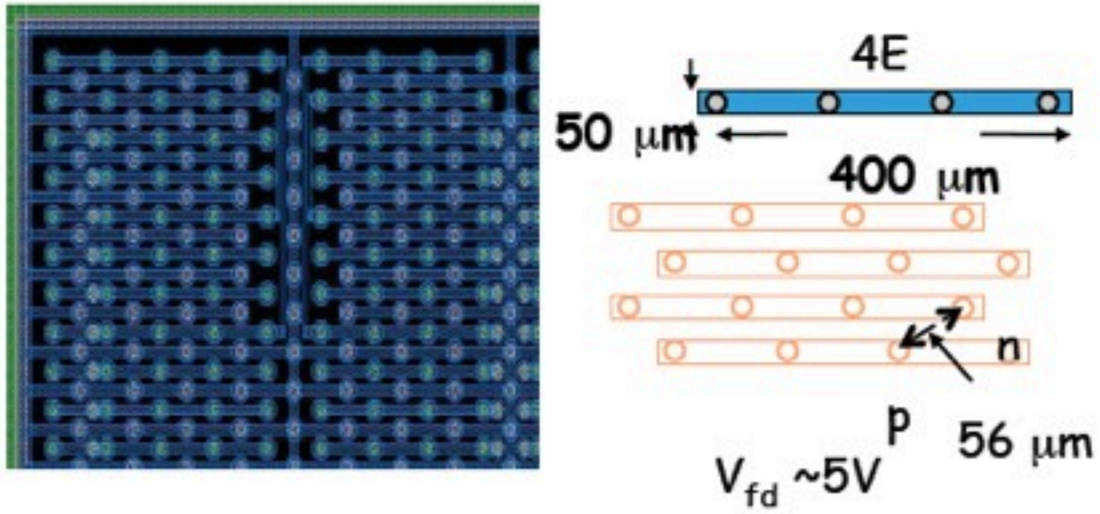
Single column
No active edge

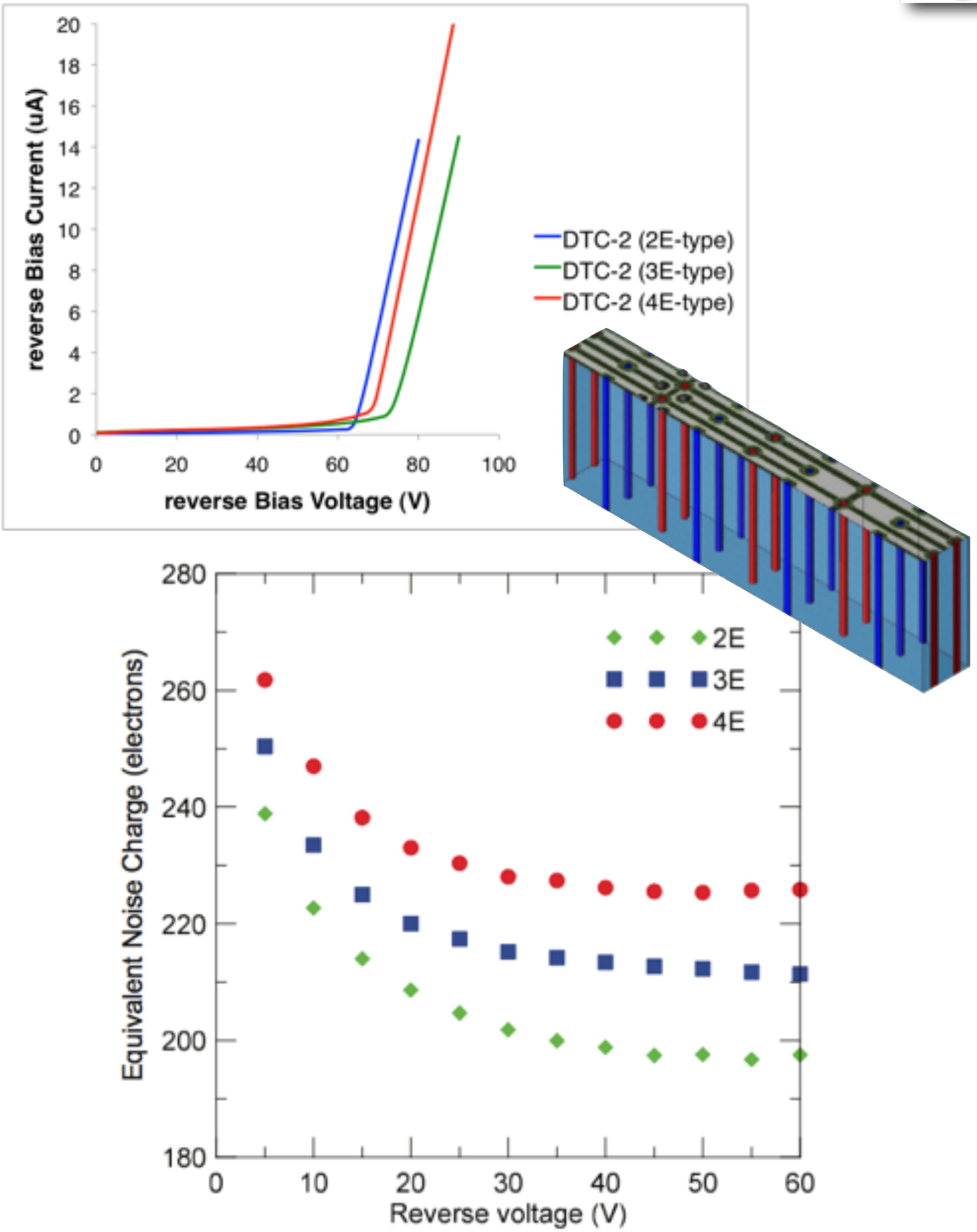


Silicon 3D Sensor Electrode Configurations

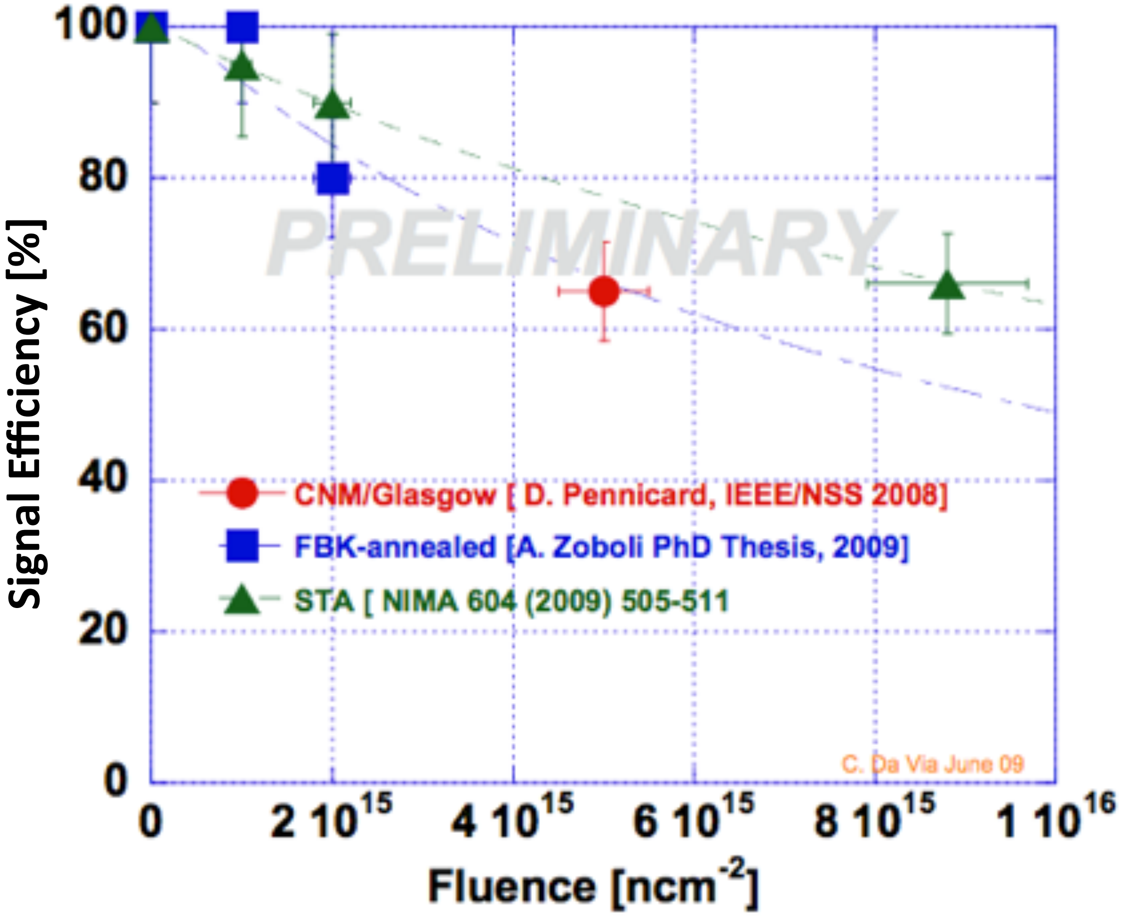


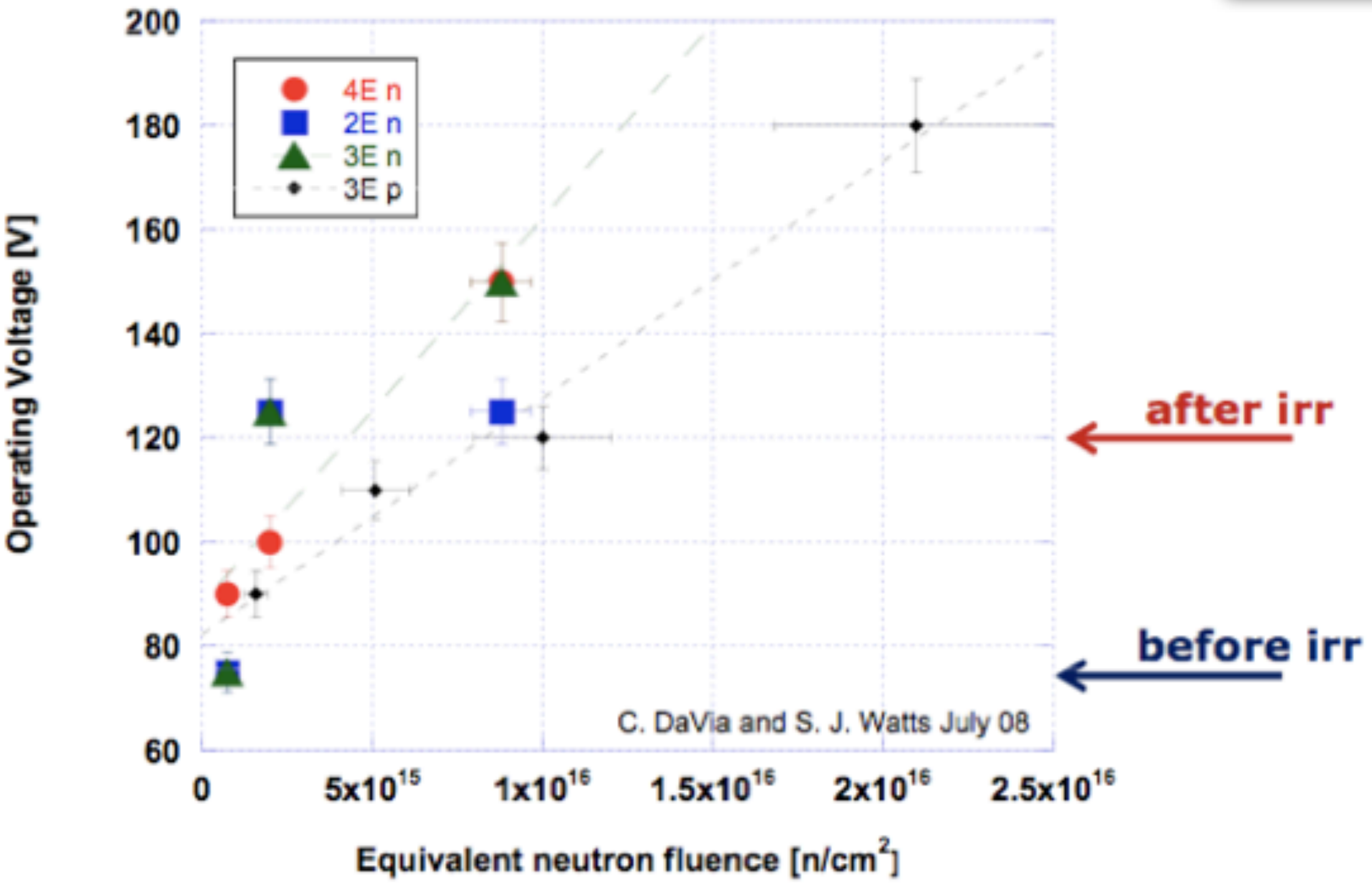




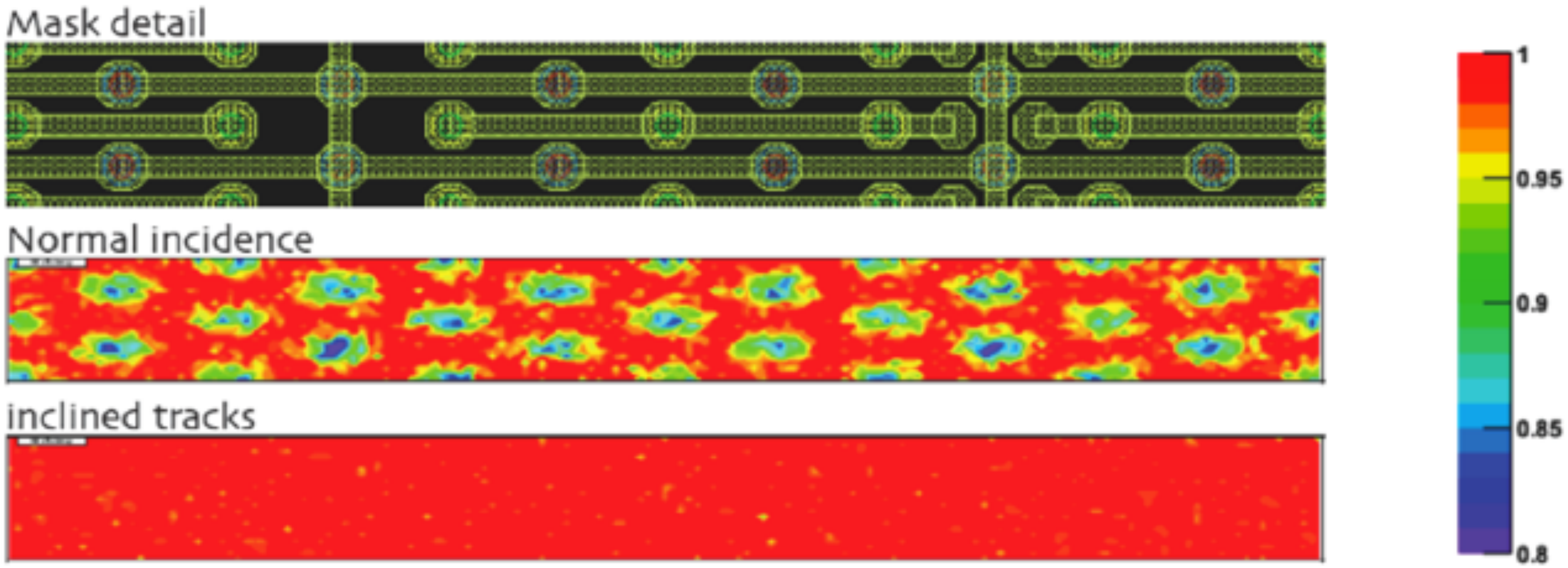


Silicon 3D Sensor Radiation Hardness & Efficiency



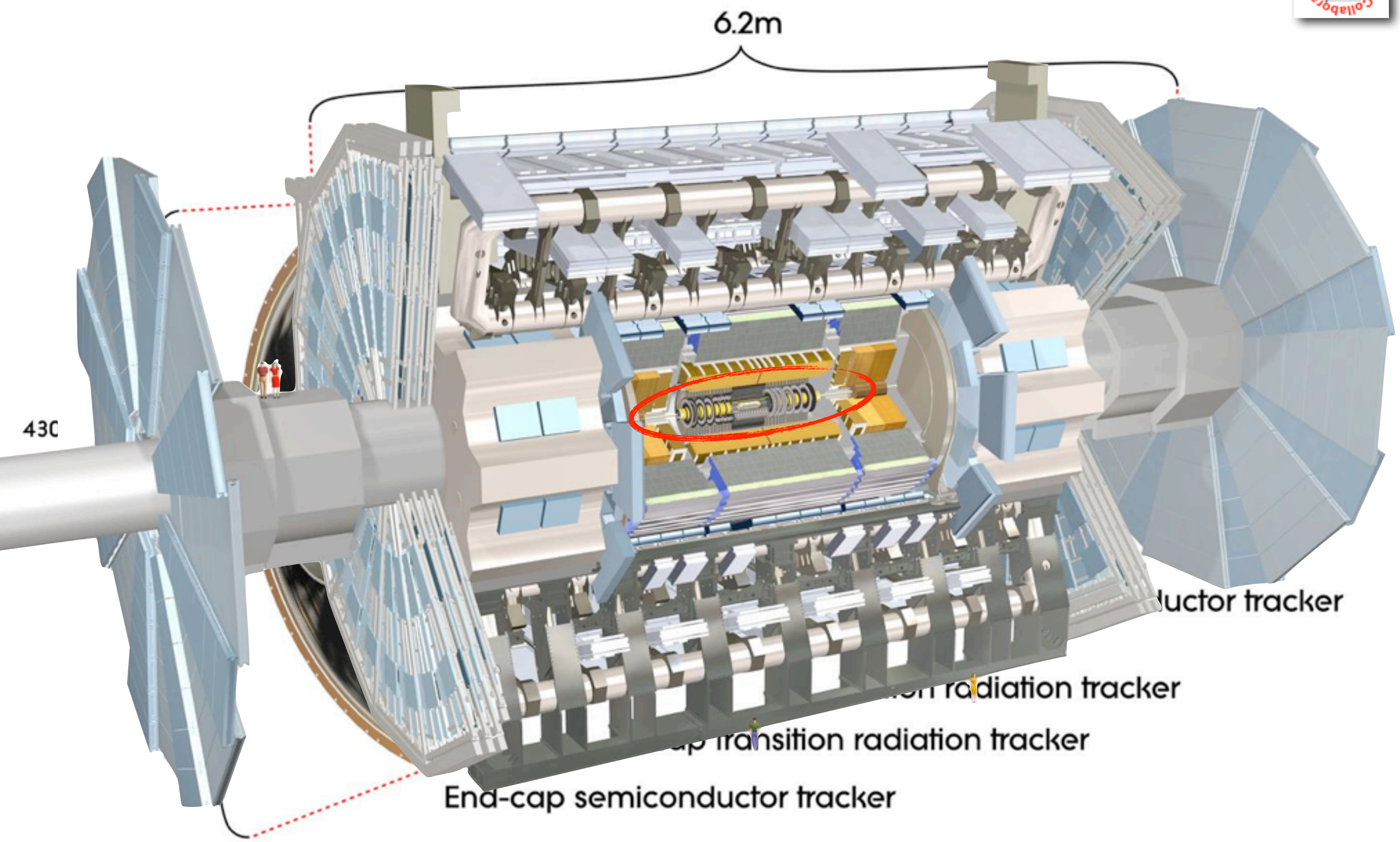


- radiation tolerance up to 3-5x10^{15} n$_{eq}$/cm^{2}
- for inclined tracks 3D sensors have similar efficiency and spatial resolution as planar silicon sensors



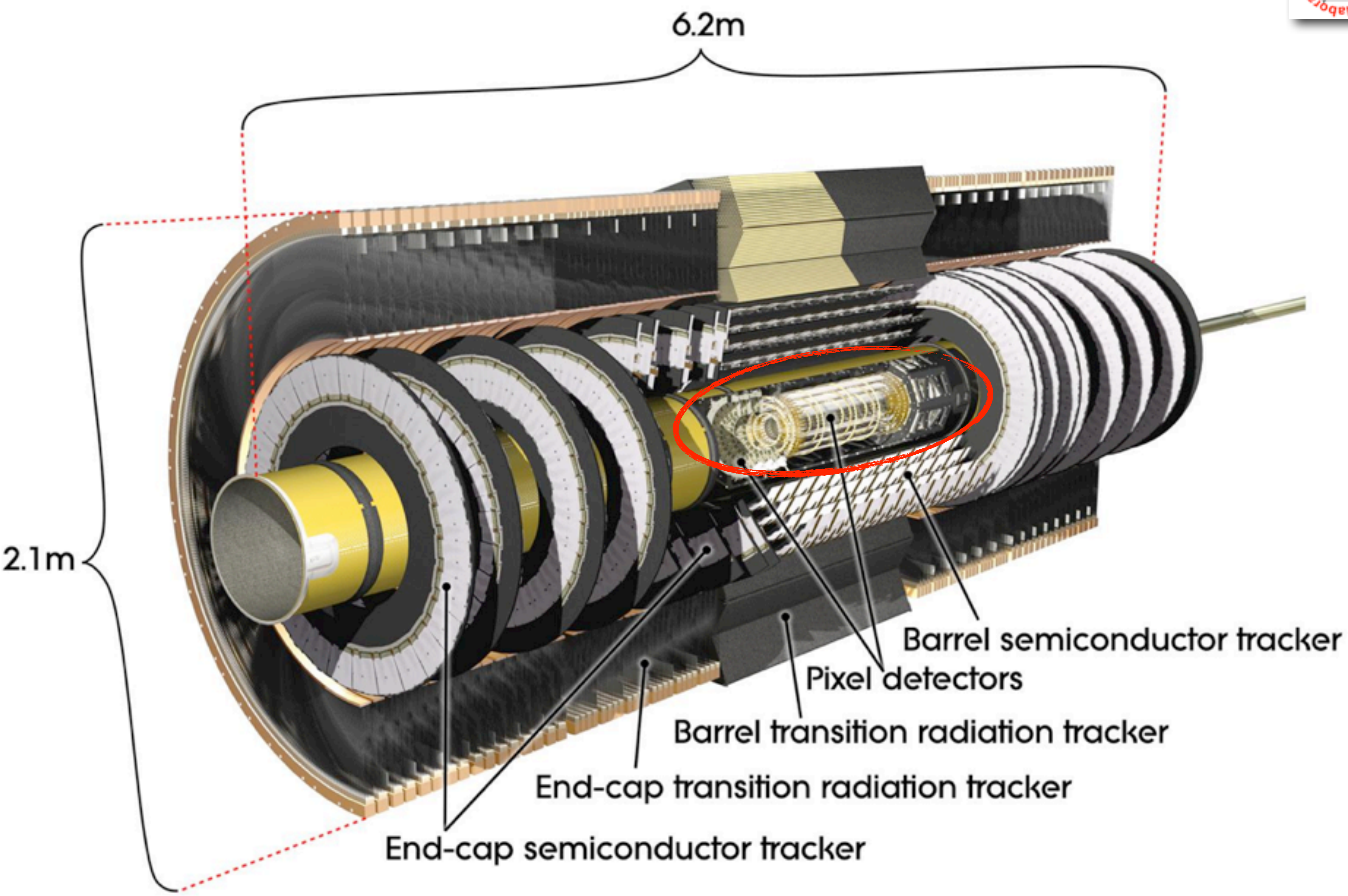
Hand-On:
Pixel Detectors at LHC
e.g. ATLAS Pixel FE-I3

ATLAS Pixel Detector

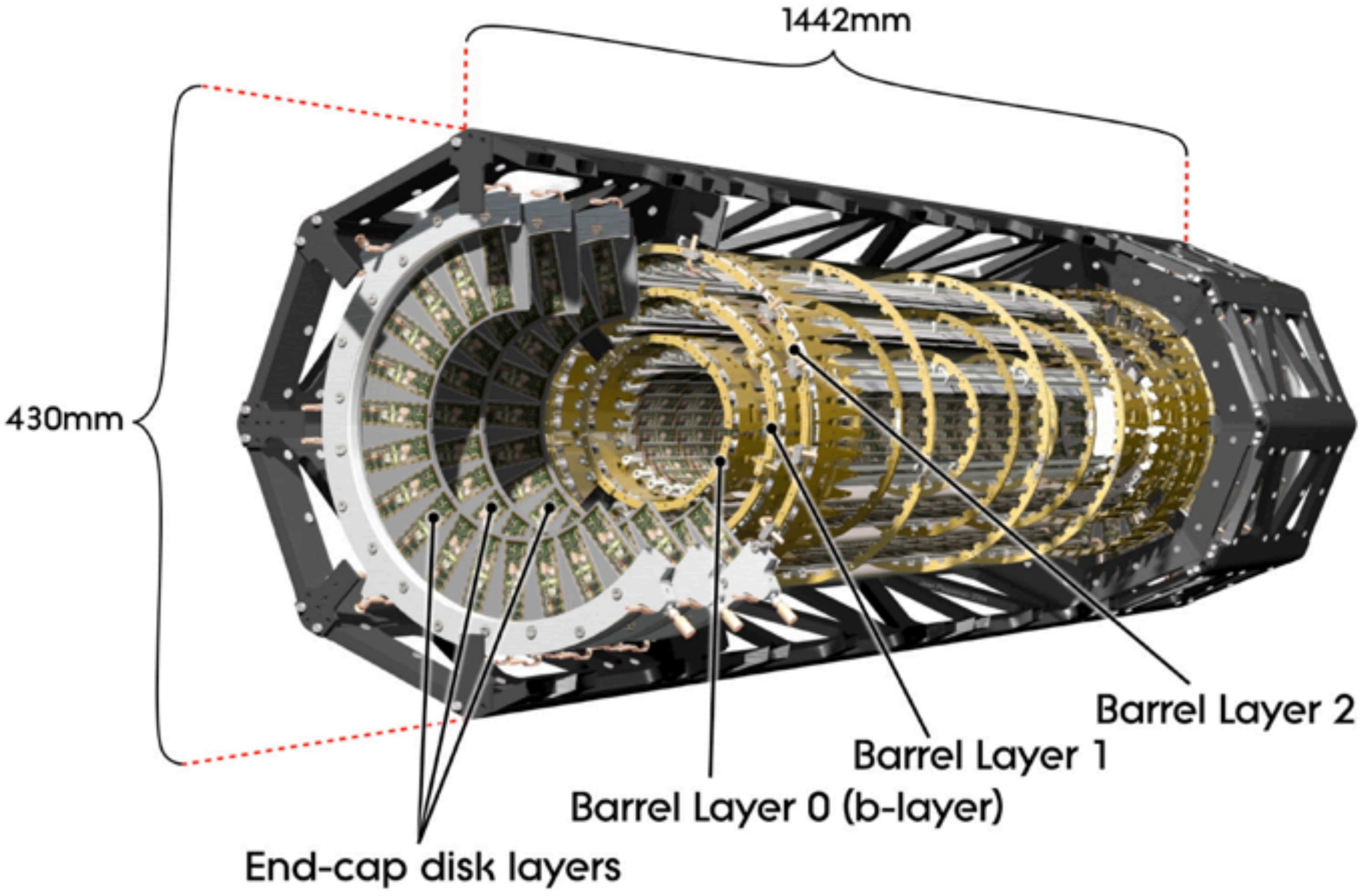


ATLAS Pixel Detector

430



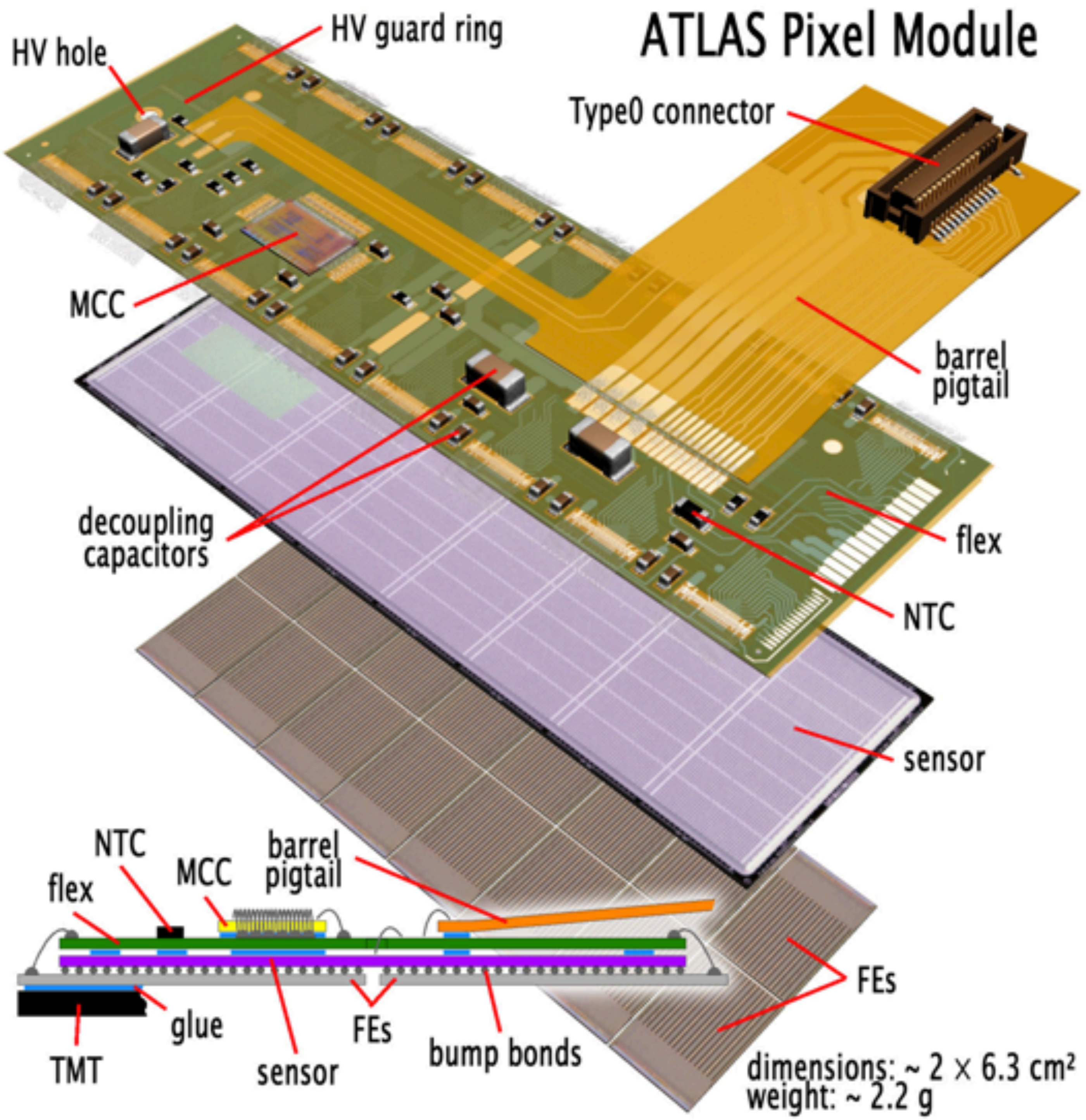
ATLAS Pixel Detector



ATLAS Pixel Detector

- 3 barrels + 3 forward/ backward disks
- 112 stave and 4 sectors
- 1744 modules
- 80 million channels

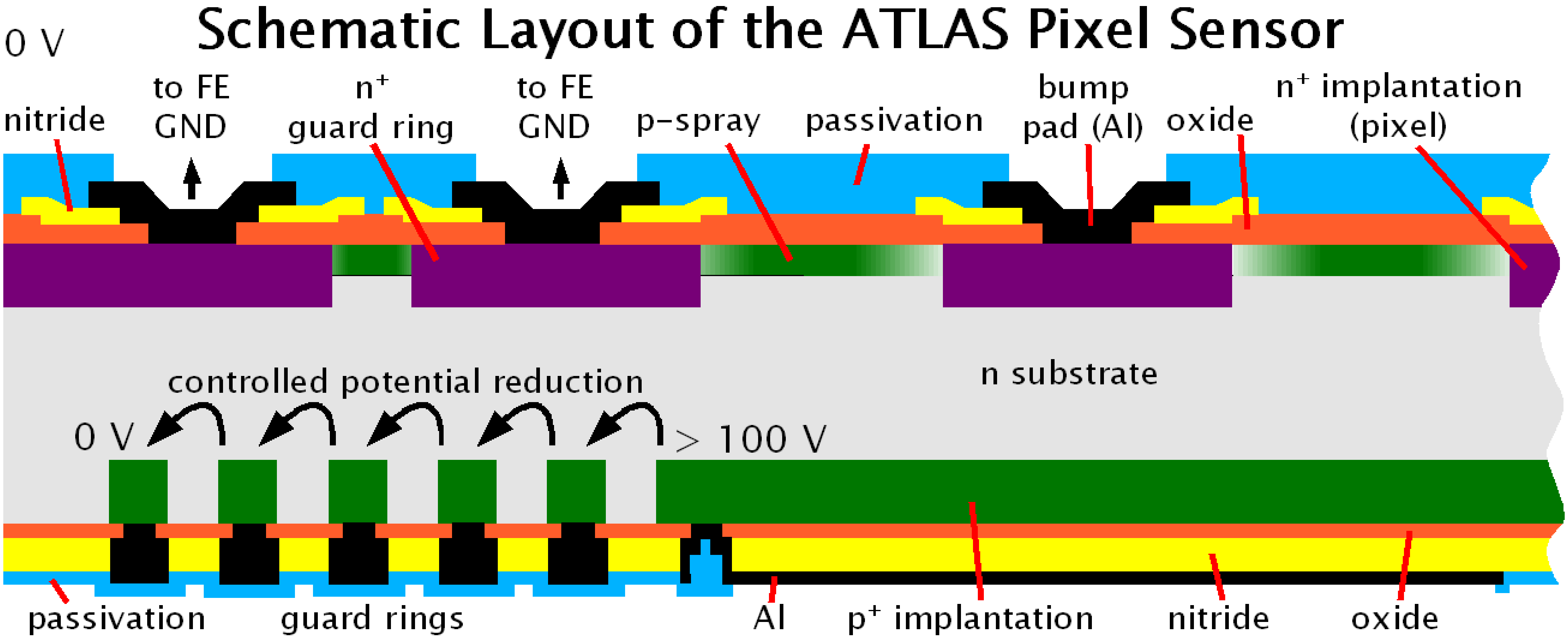
ATLAS Pixel Module



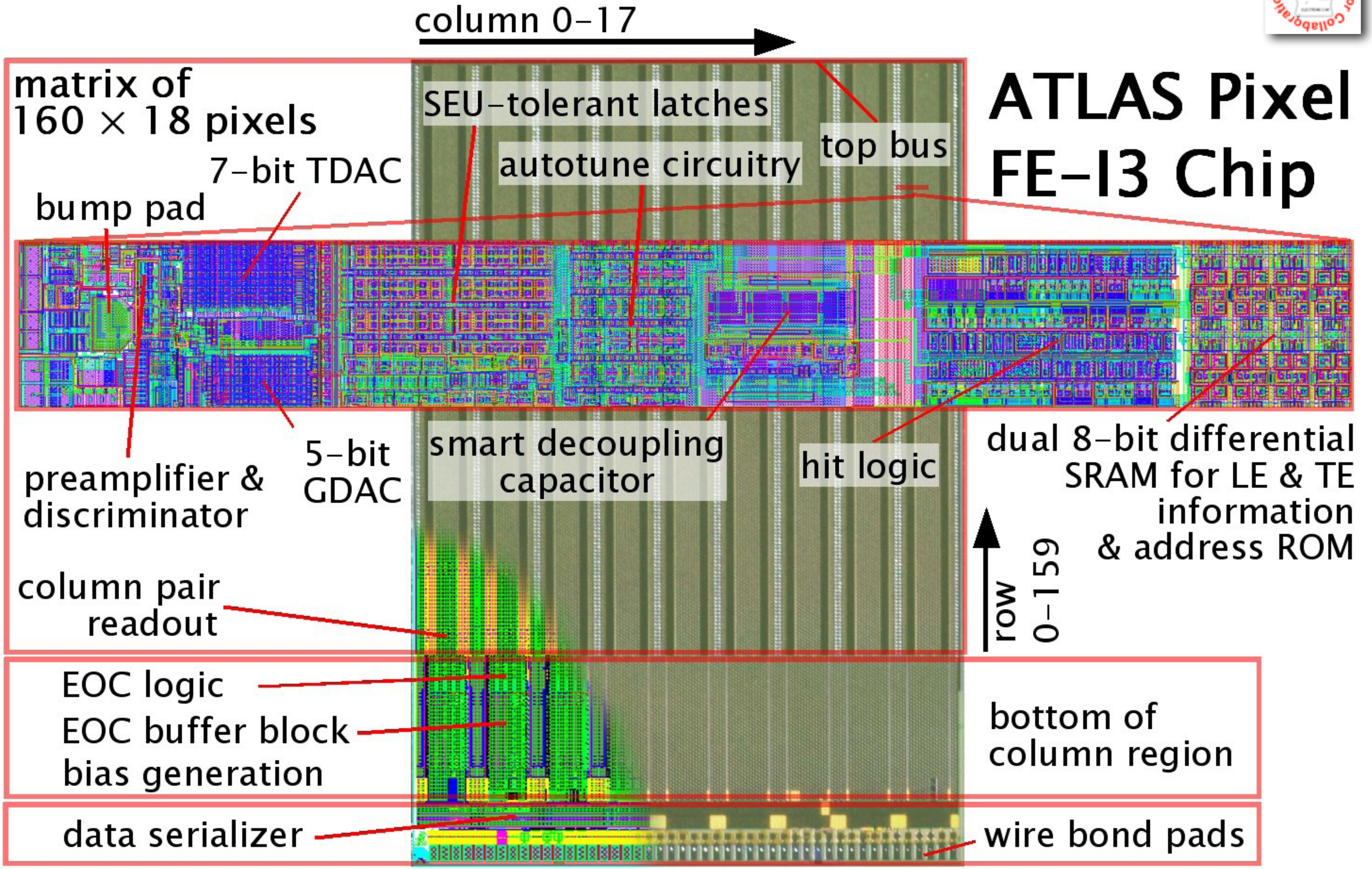
ATLAS Pixel Module

- 16 front-end chips (FE-I3) module with a Module Controller Chip (MCC)
- 46080 R/O channels 50 µm x 400 µm (50 µm x 600 µm for edge pixel columns between neighboring FE-I3 chips)
- Planar n-in-n DOFZ silicon sensors, 250um thick
- Designed for 1×10^{15} 1MeV fluence and 50 Mrad
- Optolink R/O: 40-80 Mb/link

ATLAS Pixel FE-I3 Sensor



ATLAS Pixel FE-I3 Chip



column 0–17

matrix of
160 × 18 pixels

SEU–tolerant latches

top bus

autotune circuitry

7–bit TDAC

bump pad

ATLAS Pixel
FE–I3 Chip

preamplifier &
discriminator

5–bit
GDAC

smart decoupling
capacitor

hit logic

dual 8–bit differential
SRAM for LE & TE
information
& address ROM

row
0–159

column pair
readout

EOC logic

EOC buffer block

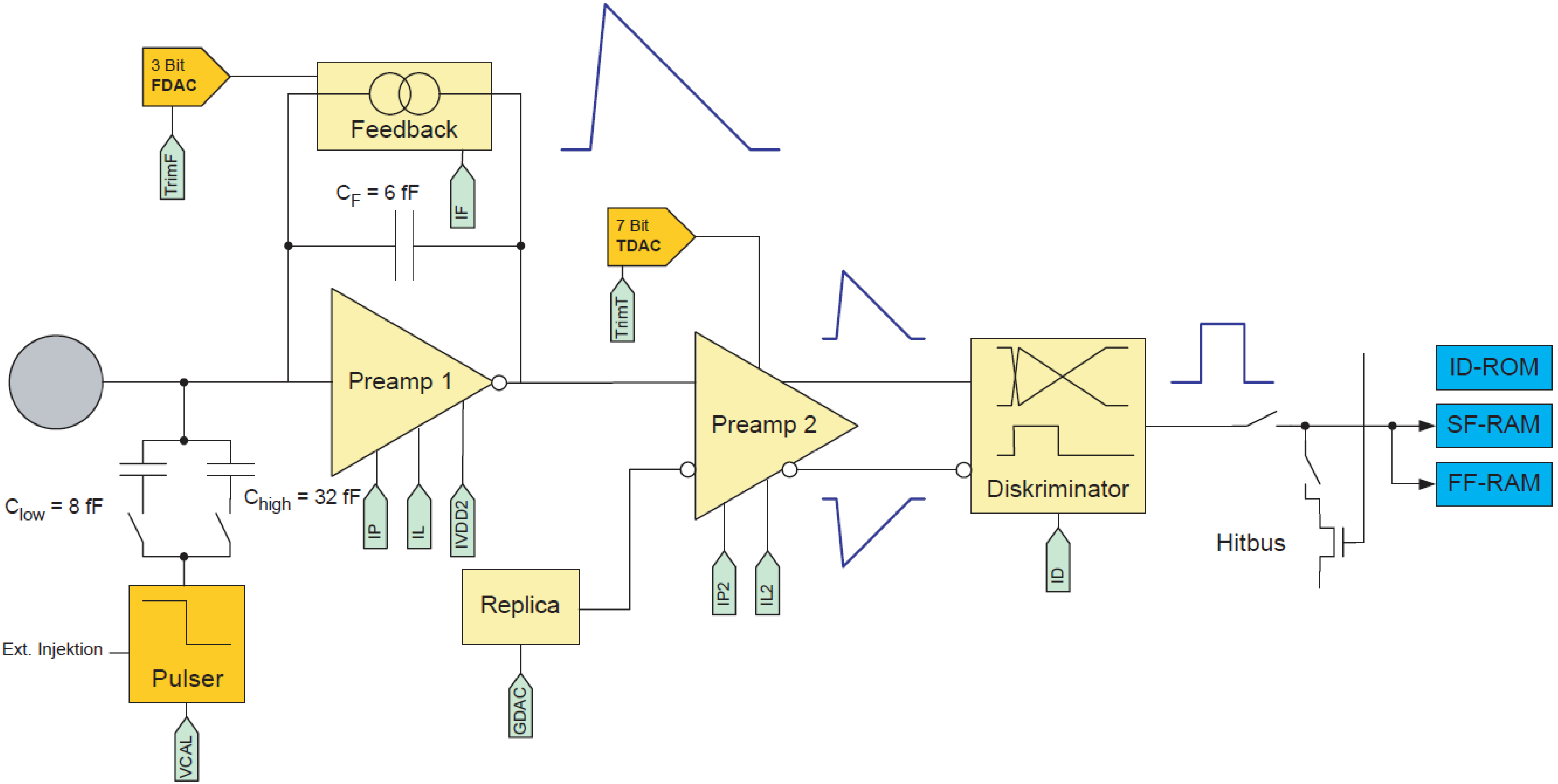
bias generation

bottom of
column region

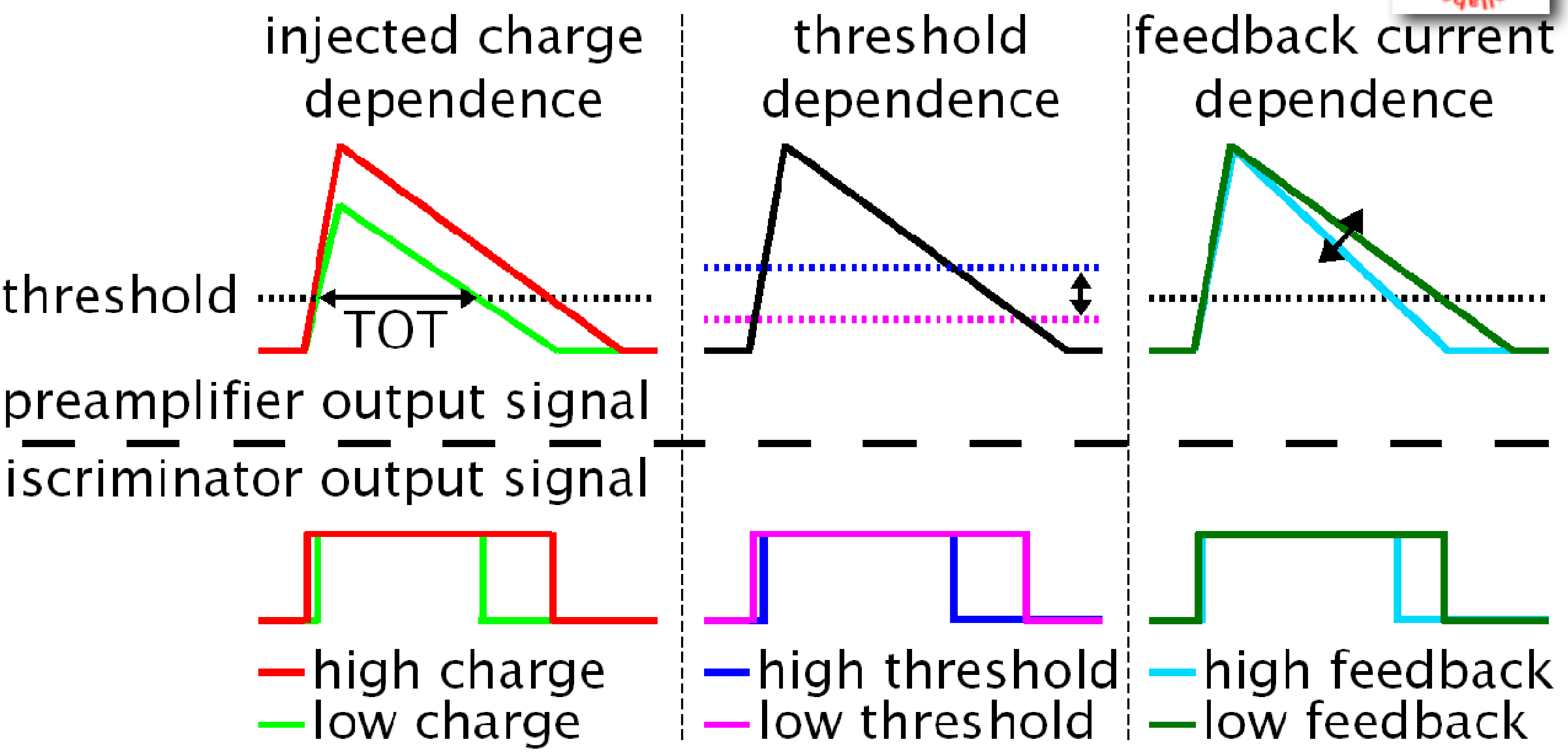
data serializer

wire bond pads

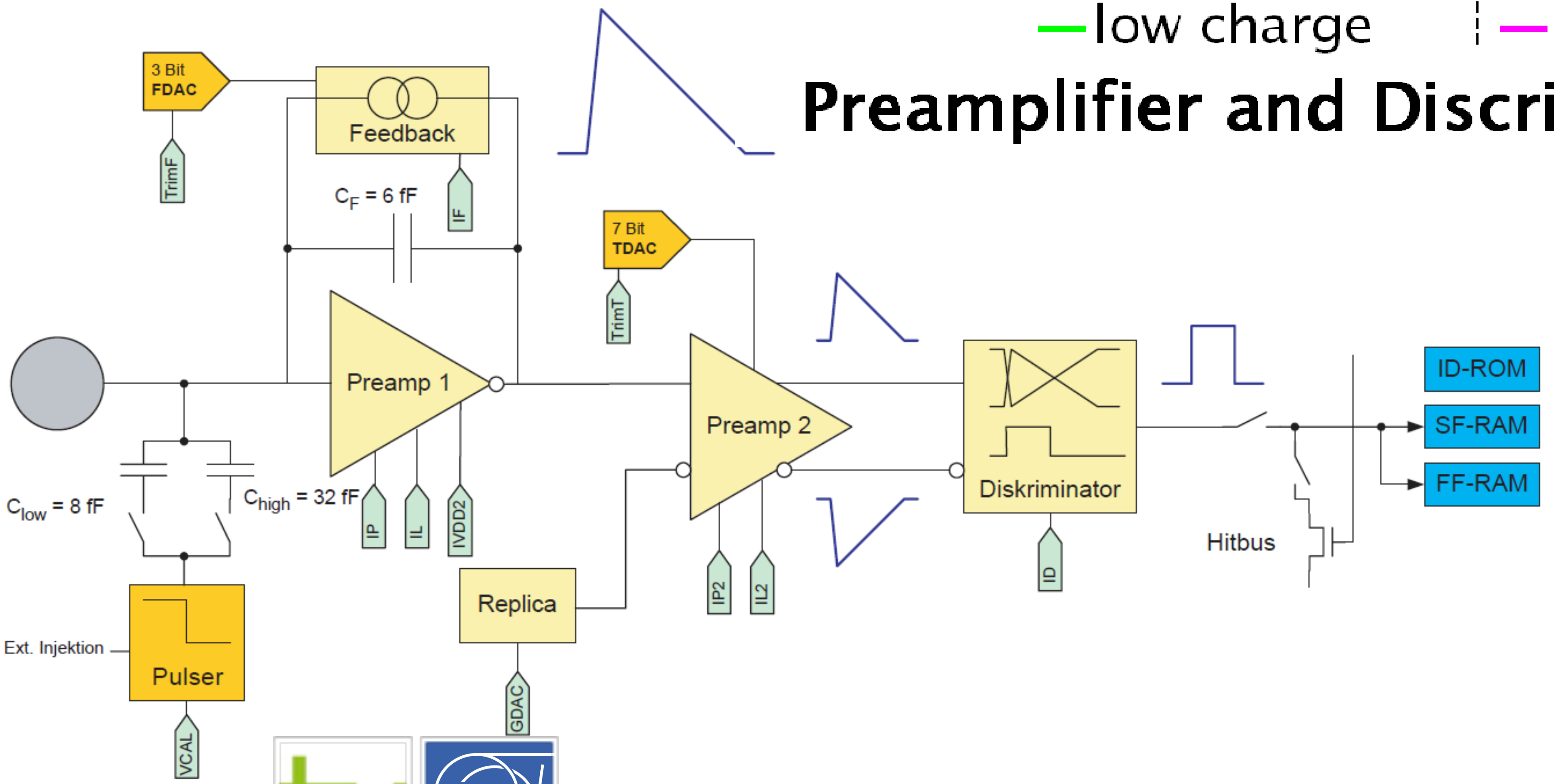
FE-I3 Pixel Cell Block Diagram



FE-I3 Pixel Signal Shapes



Preamplifier and Discriminator Signal Shapes

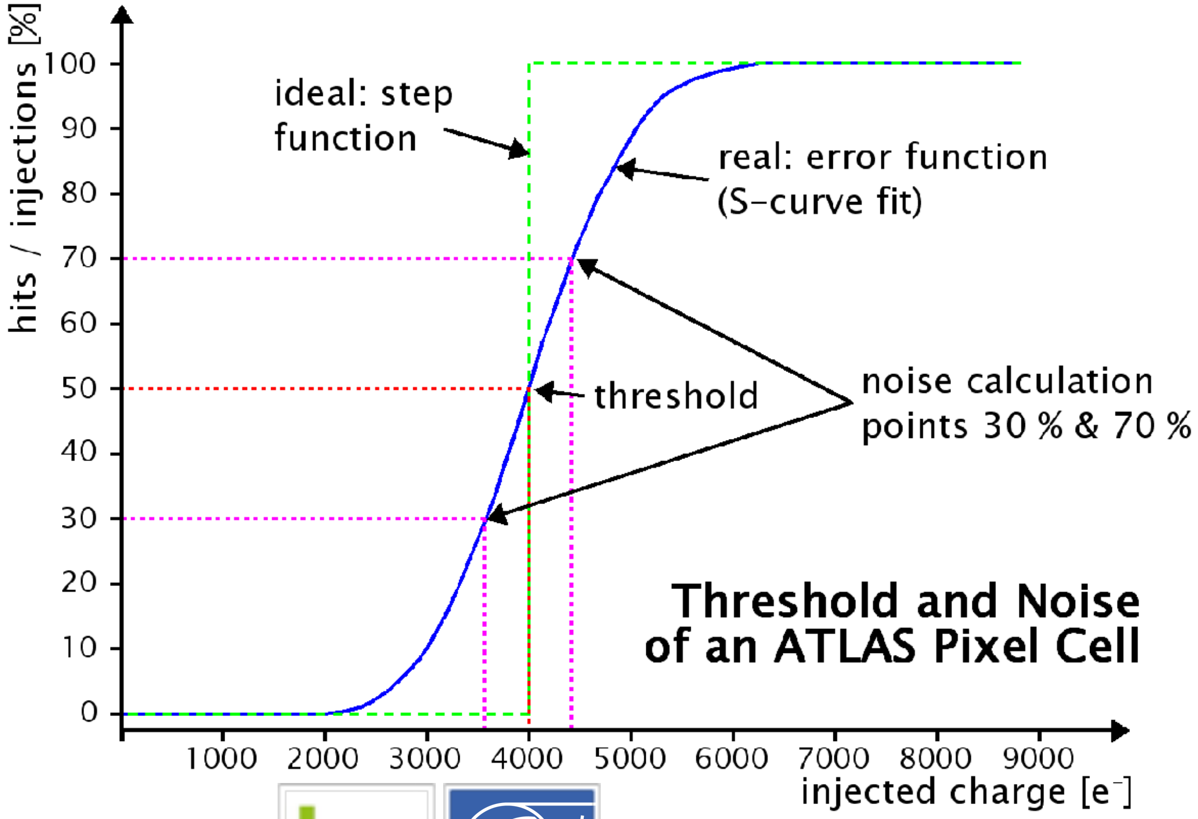


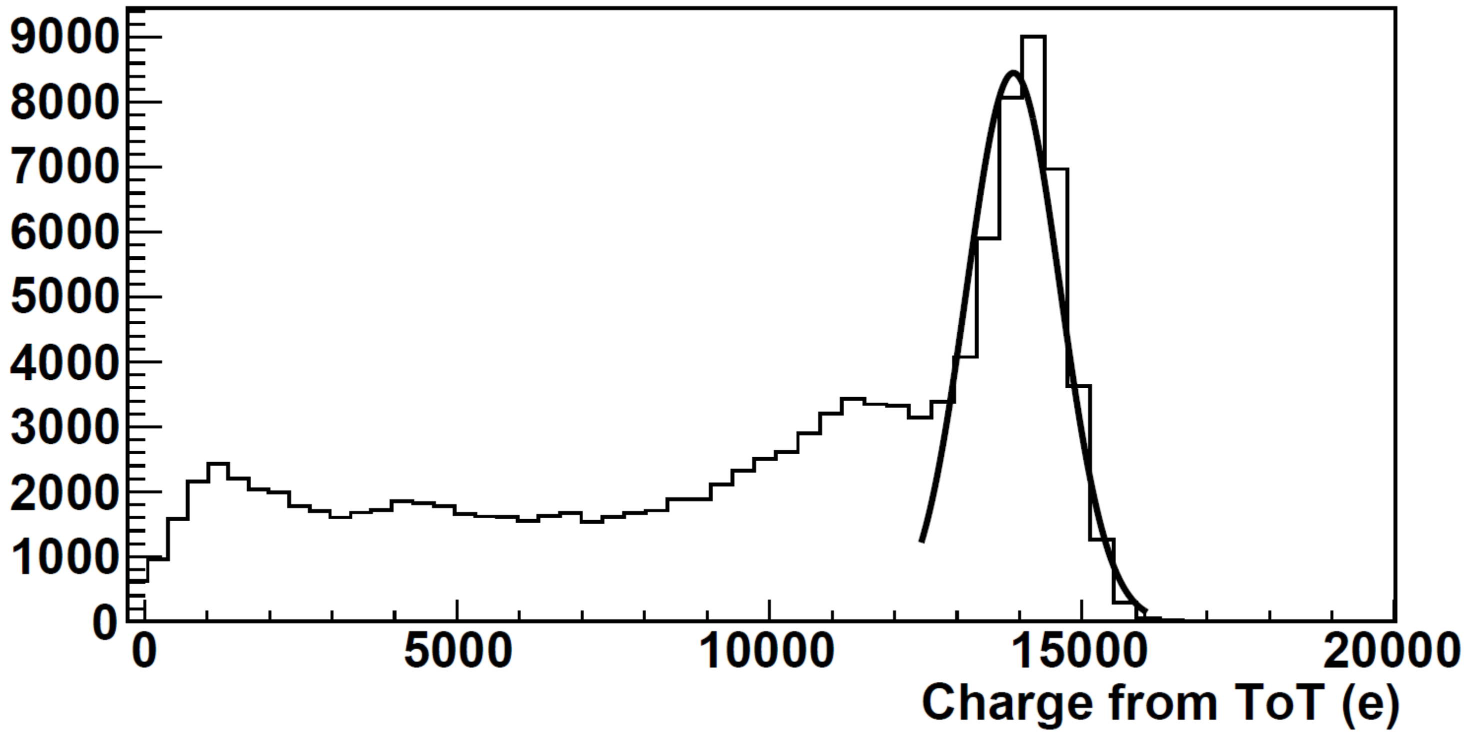
Hand-On Measurement Program

Front-end Tuning (selected steps of a many tuning, calibration and quality assurance steps program):

1. Digital test
2. Threshold Scan
3. Time-Over-Threshold Calibration
4. Source Scan

$$ToT = A + \frac{B}{C + Q_{inj}}$$

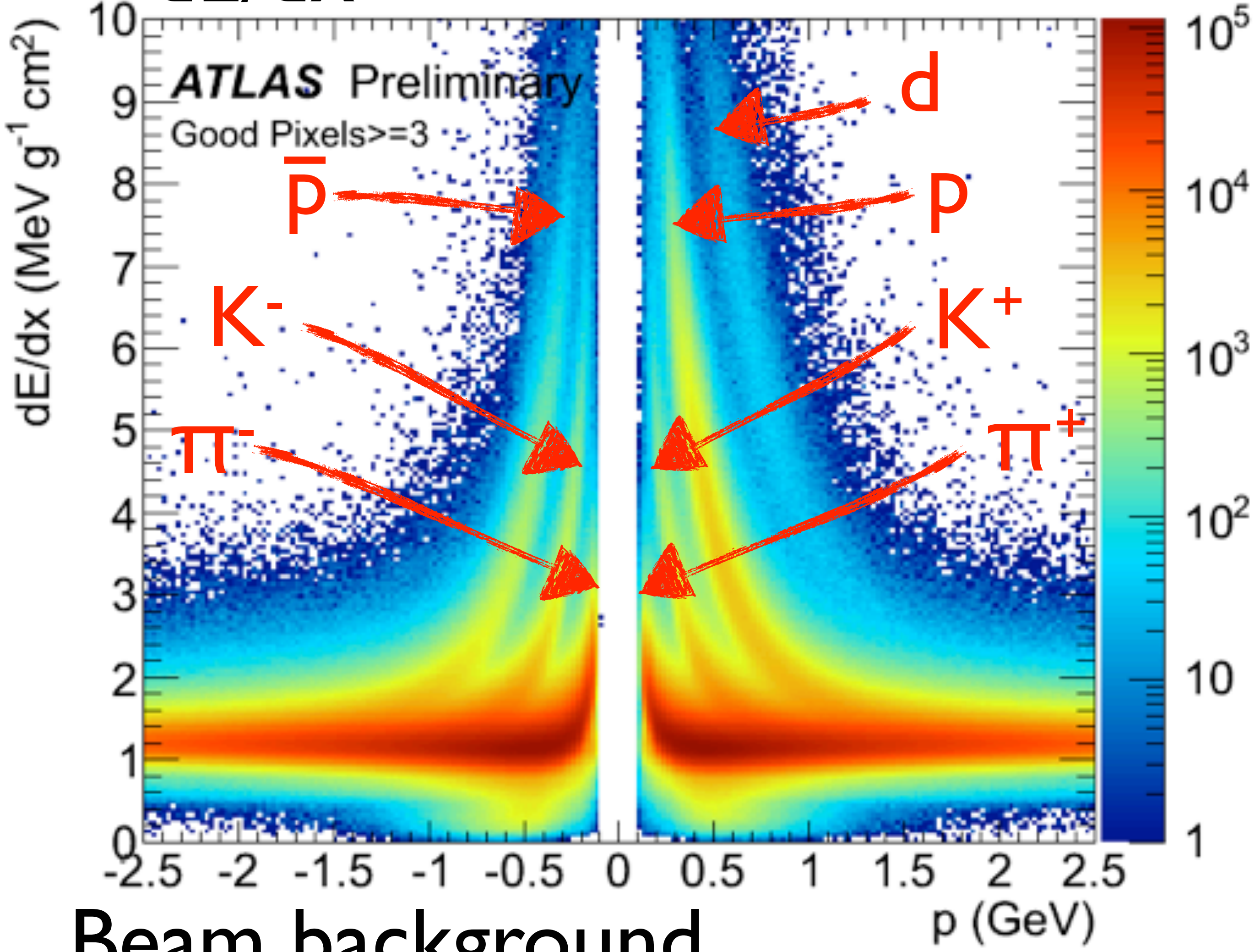




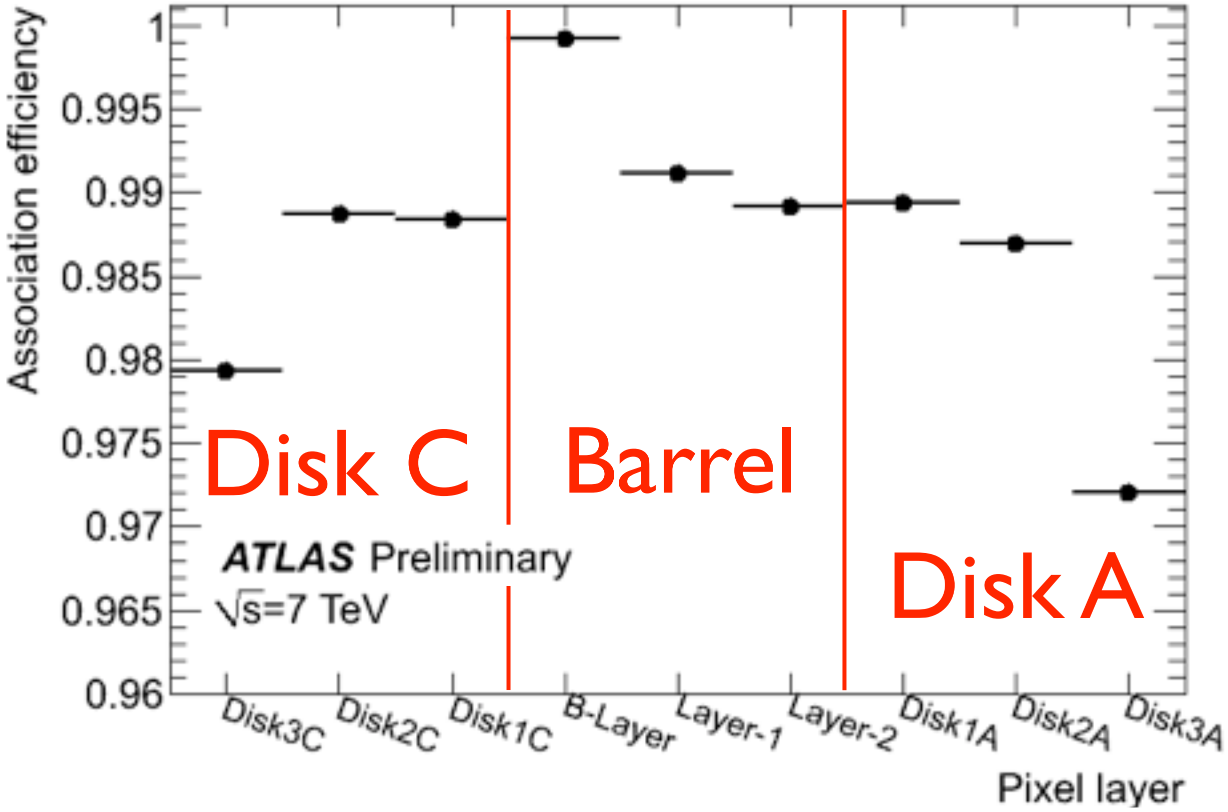
Backup Slides

Pixel Detector Performance

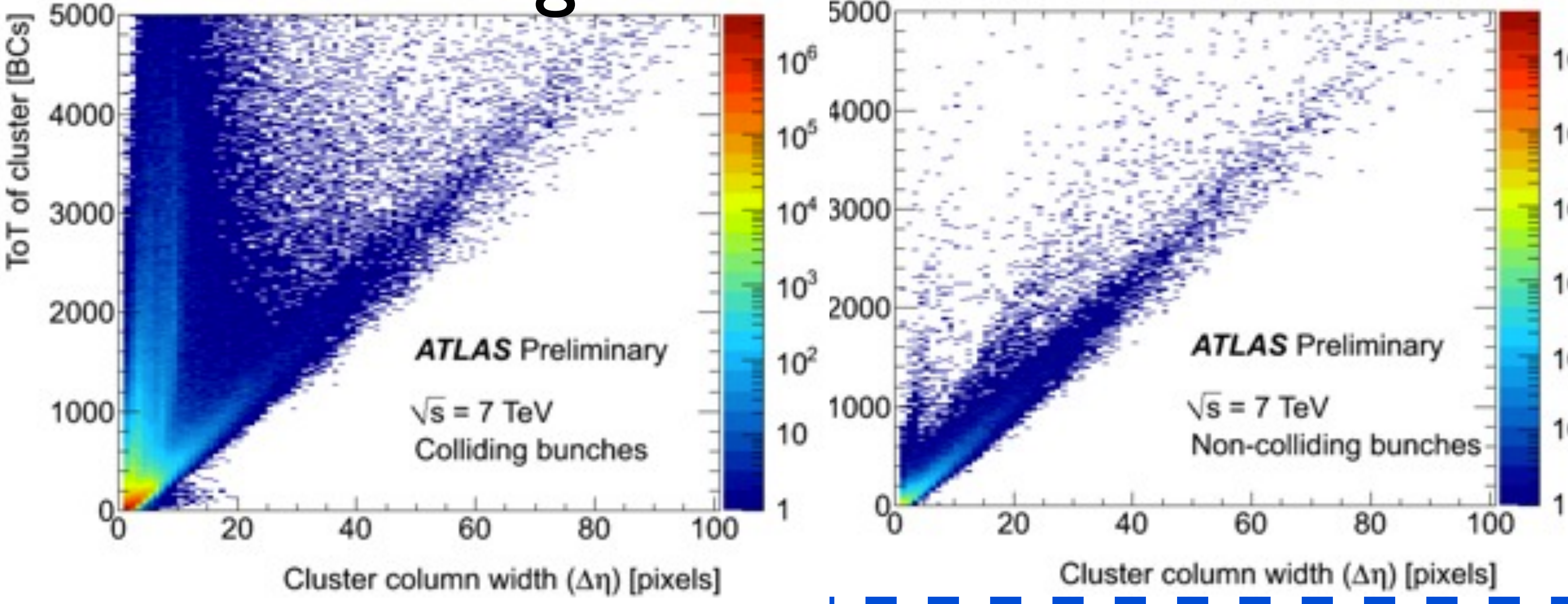
dE/dx



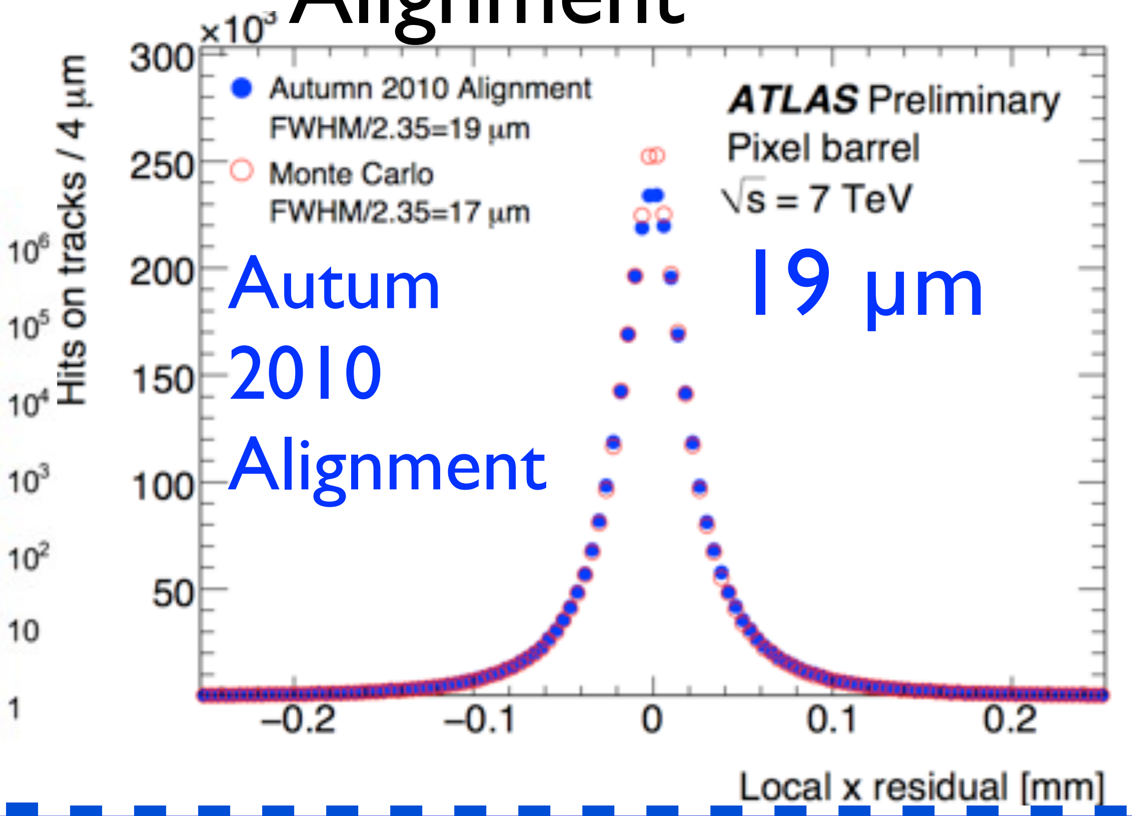
Efficiency



Beam background

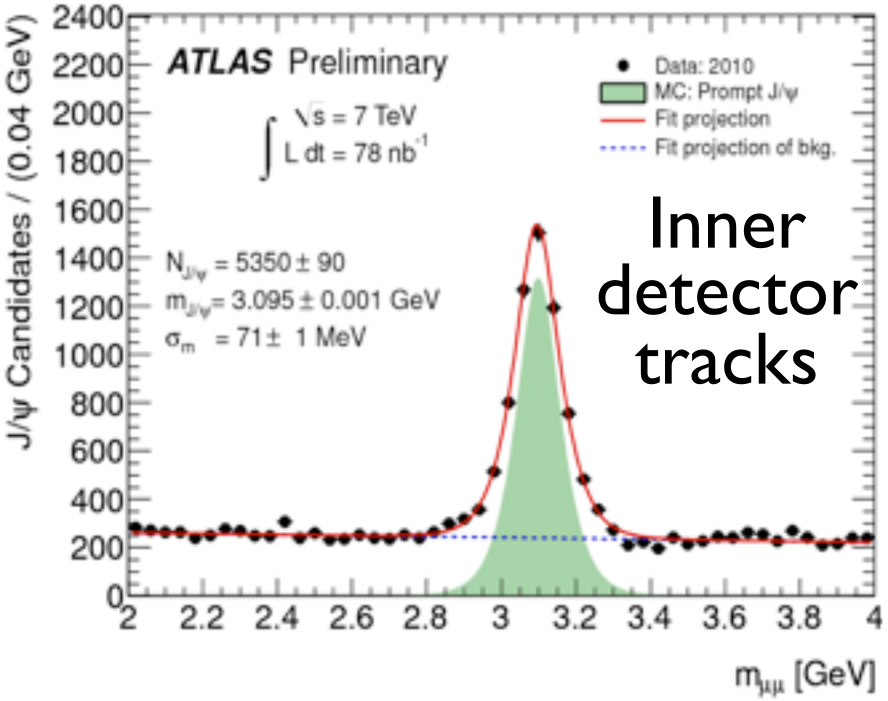


Alignment

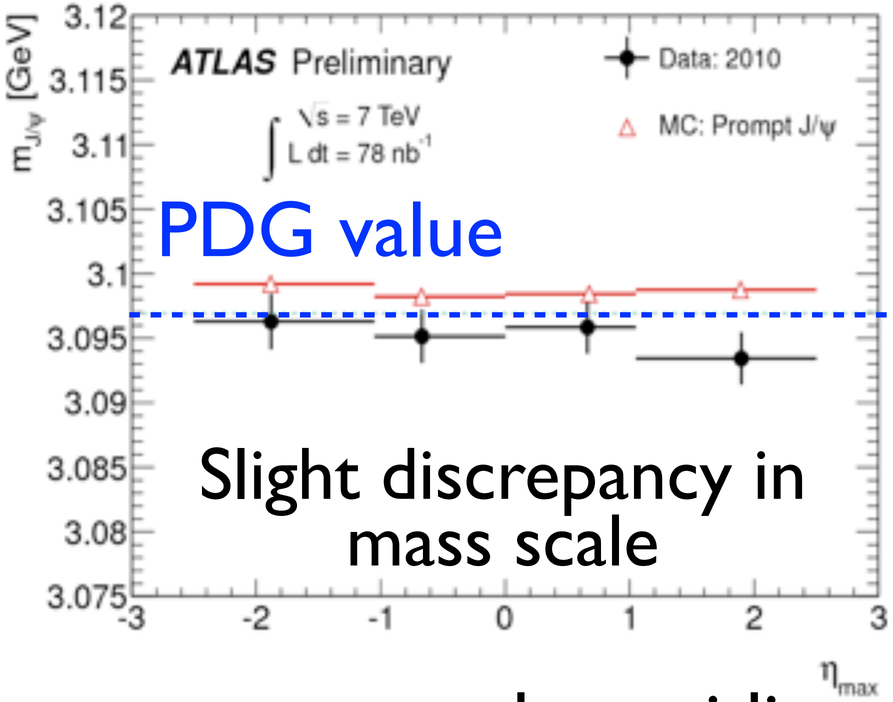


Inner Detector Tracking Performance

Momentum resolution and scale using resonances: J/ψ example

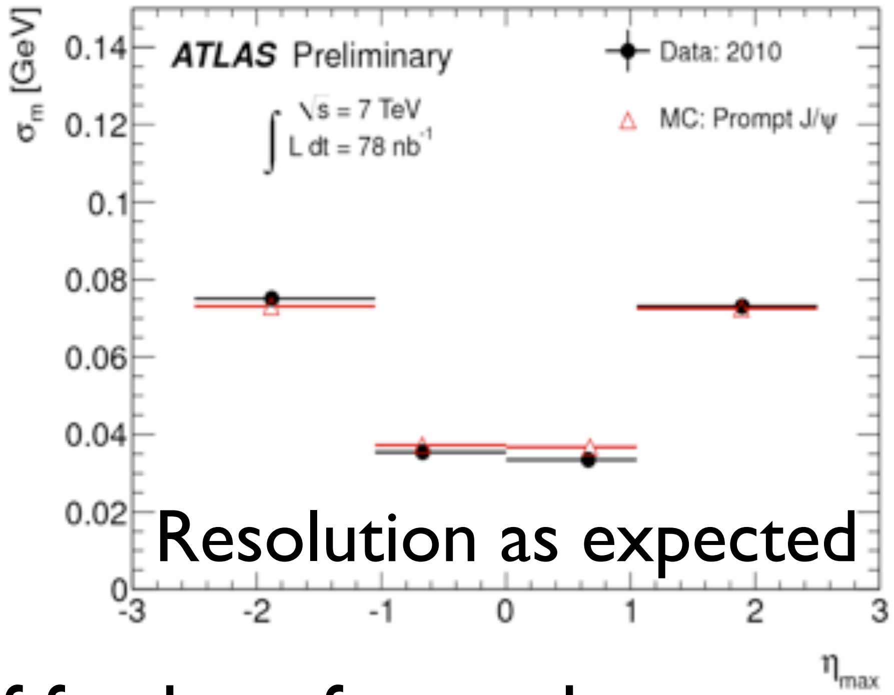


Inner detector tracks



PDG value

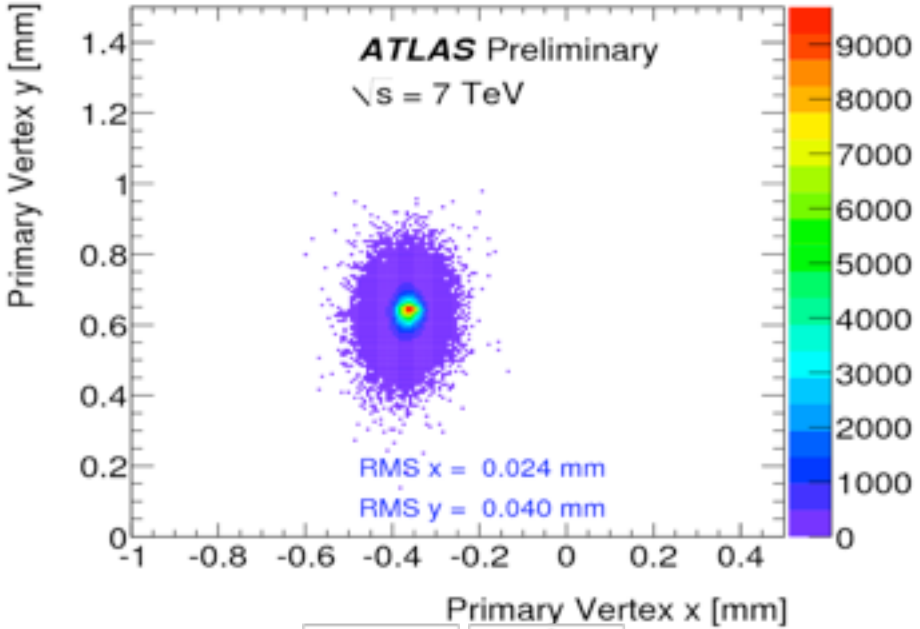
Slight discrepancy in mass scale

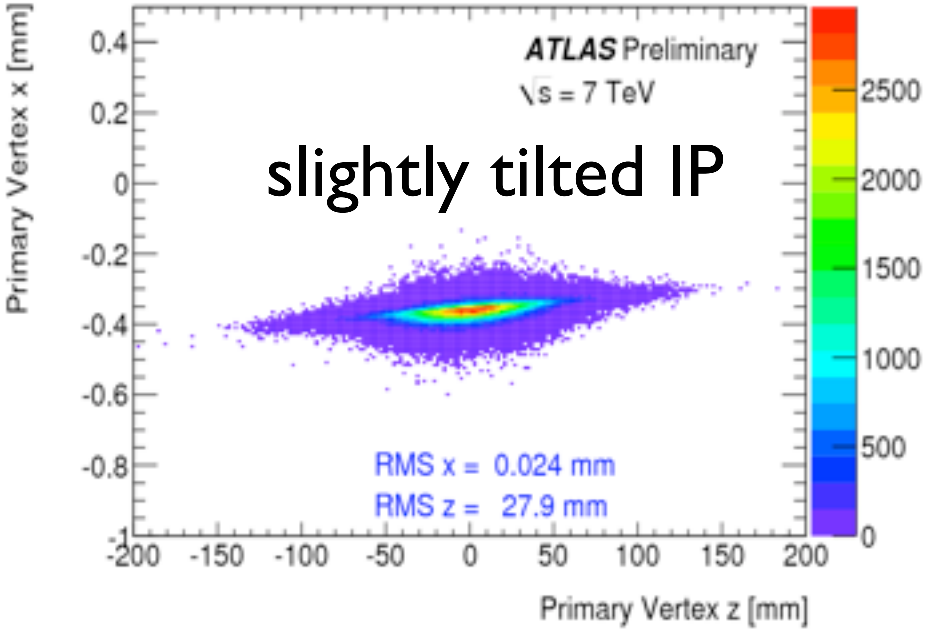


Resolution as expected

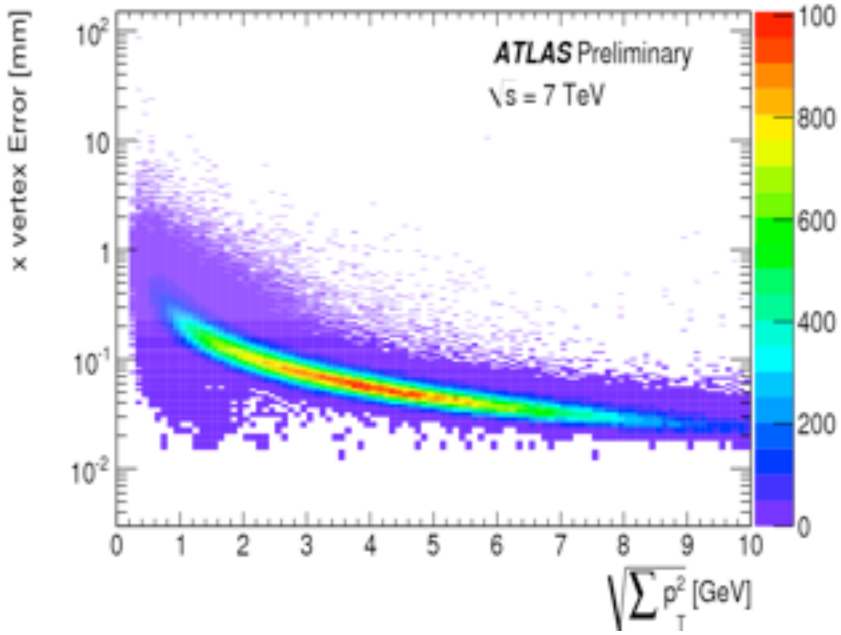
pseudo-rapidity of furthest forward muon

Primary vertex reconstruction





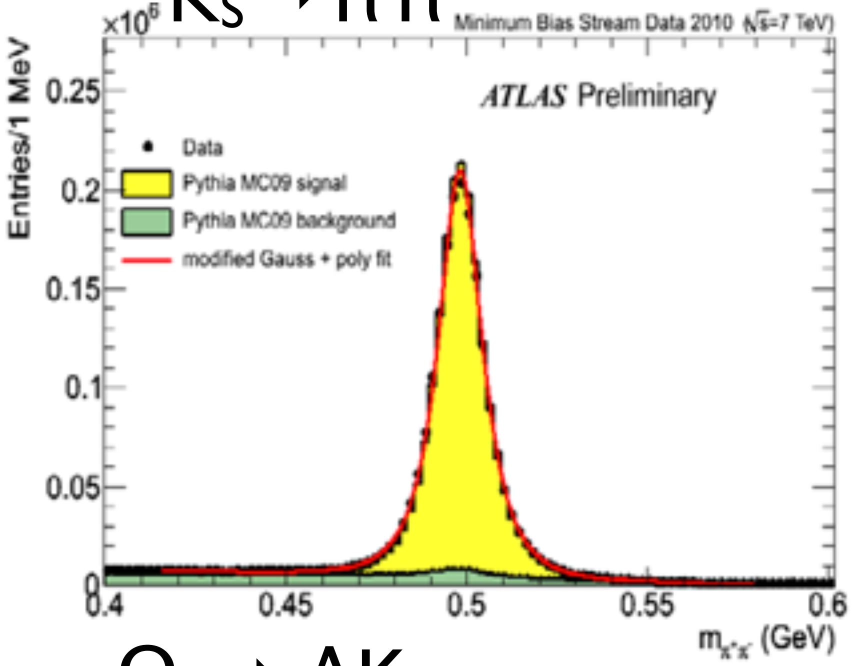
slightly tilted IP



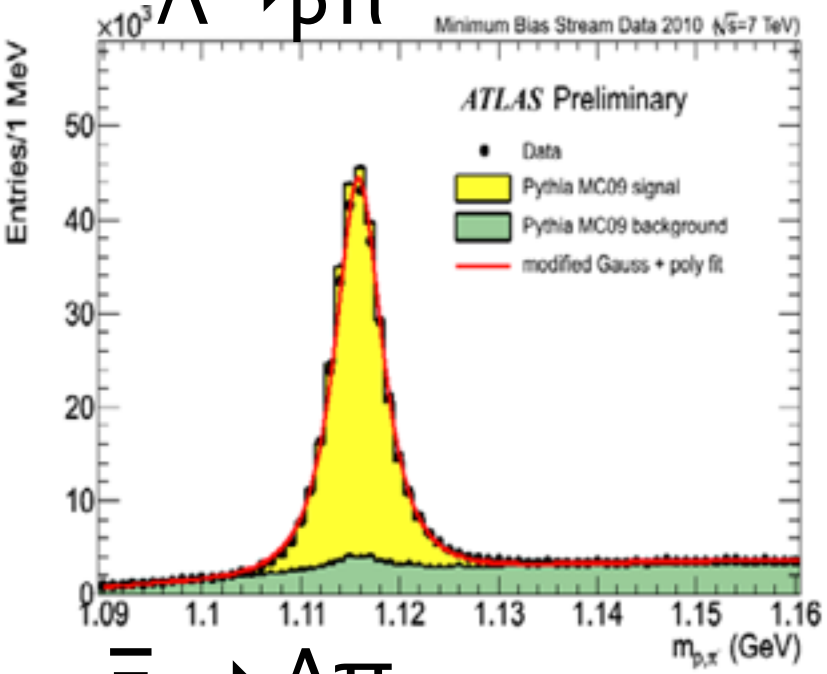
Tracking Performance: Peaks, Cascades & J/ψ→ee

Observed all most classic resonances:
Ks, K*, φ, Λ, Ω, Ξ, D, D* and J/Ψ
Momentum scale known to permil in this mass region.

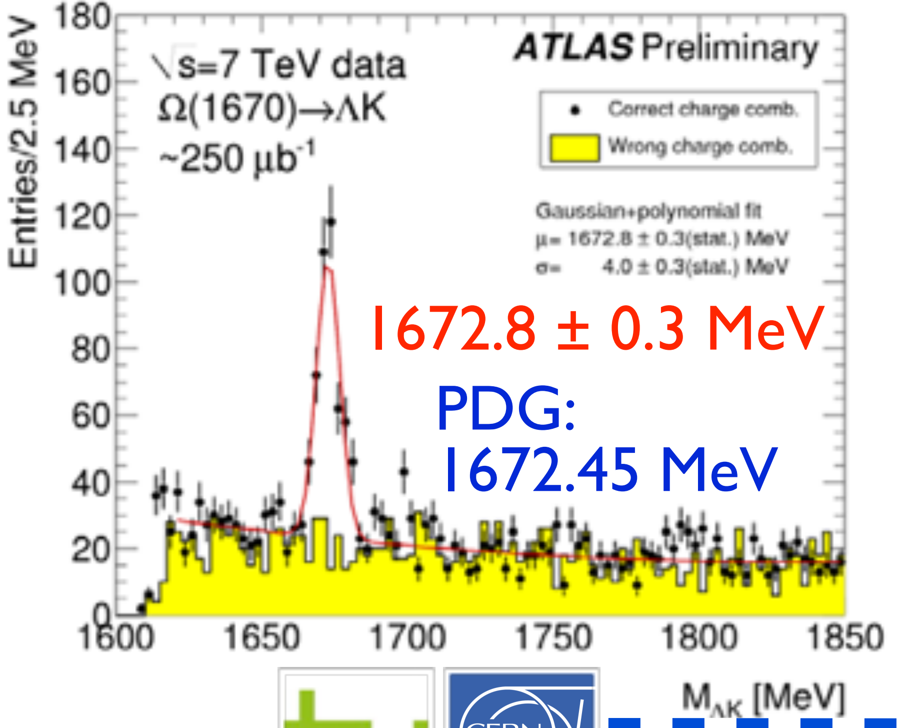
$K_S \to \pi\pi$



$\Lambda \to p\pi$



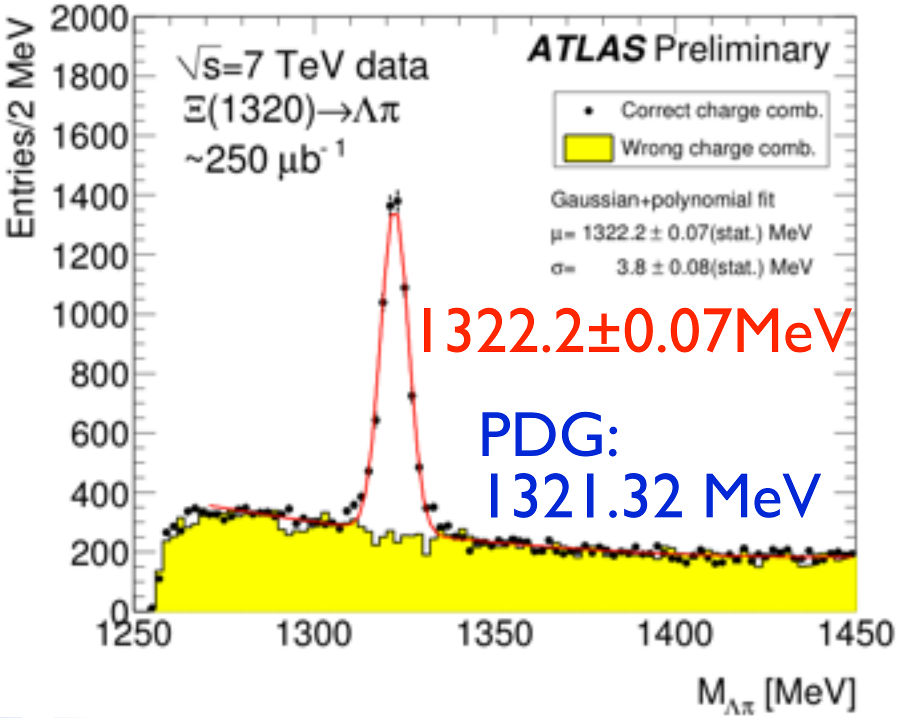
$\Omega \to \Lambda K$



1672.8 ± 0.3 MeV

PDG:
1672.45 MeV

$\Xi \to \Lambda\pi$

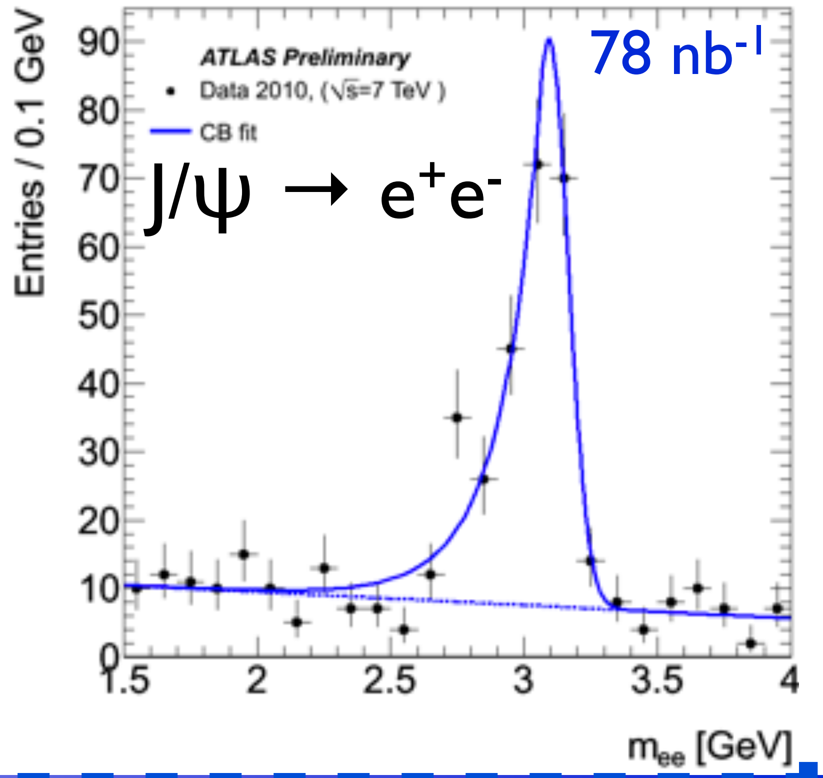


1322.2±0.07MeV

PDG:
1321.32 MeV

Extract signal from background:

- 2 EM clusters (track-match)
- p_T (e± tracks) > 4, 2 GeV
- track quality, calo shower shapes
- key handle: large transition radiation in TRT
- invariant mass from track parameters after
- Bremsstrahlung recovery (Gaussian Sum Filter)
- Signal: 222 ± 11 events
- Background: 28 ± 2 events
- Mass peak: 3.09 ± 0.01 GeV
- Mass resol.: 0.07 ± 0.01 GeV

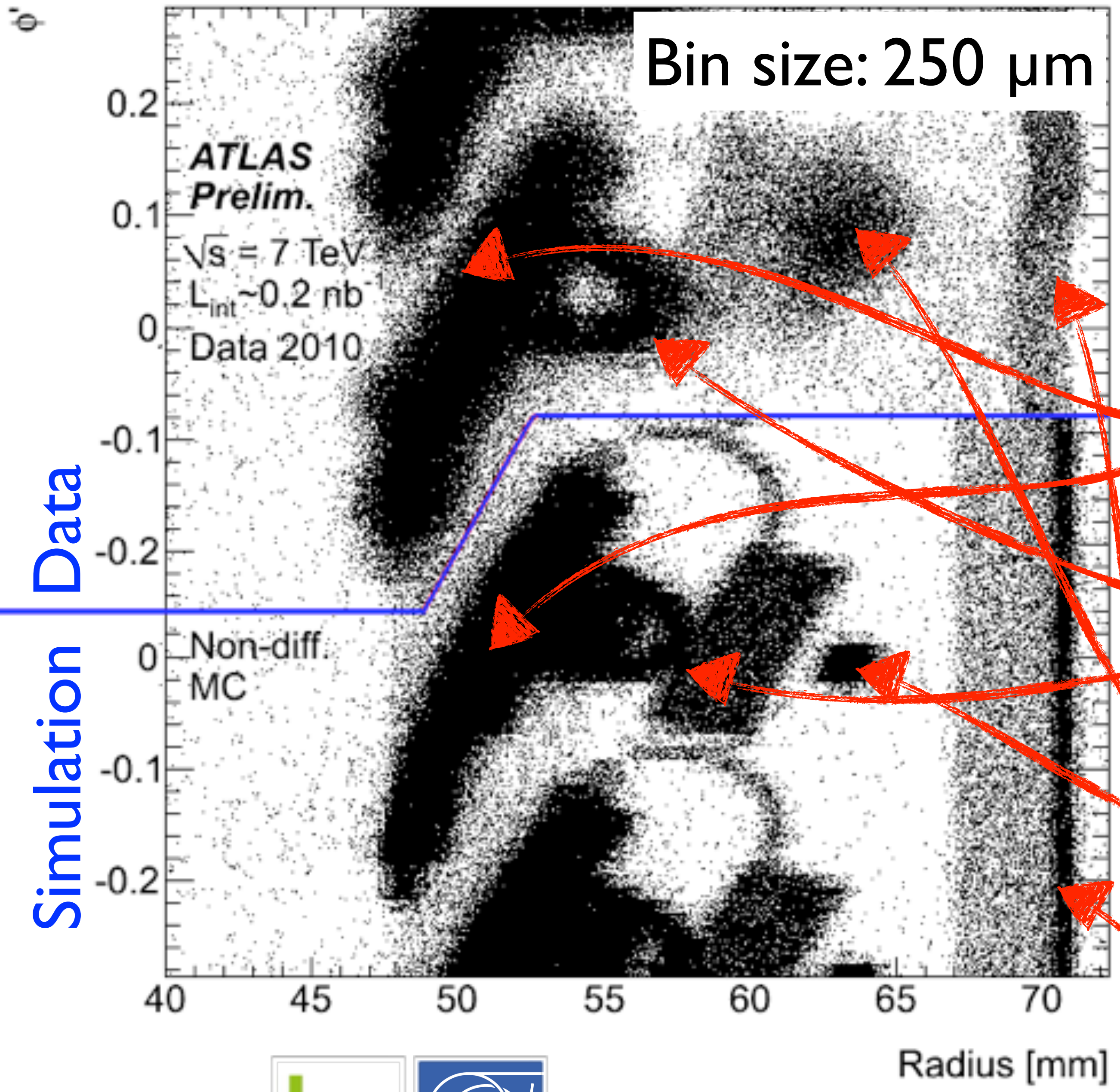


78 nb⁻¹

$J/\psi \to e^+e^-$

Inner Detector Material Mapping: hadron interactions

- Reconstructed secondary vertices due to hadronic interactions in minimum-bias events (sensitive to interaction length λ → complementary to γ conversion studies)
- Vertex mass veto against γ → e^+e^-, K_S^0 and Λ



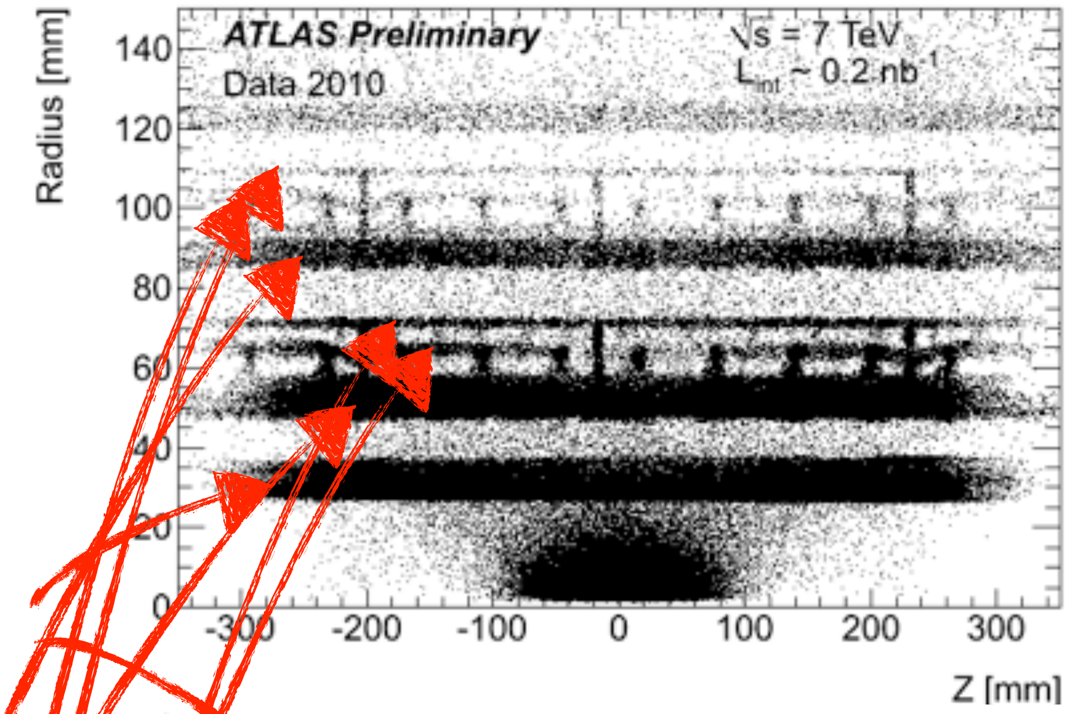
Beam Pipe

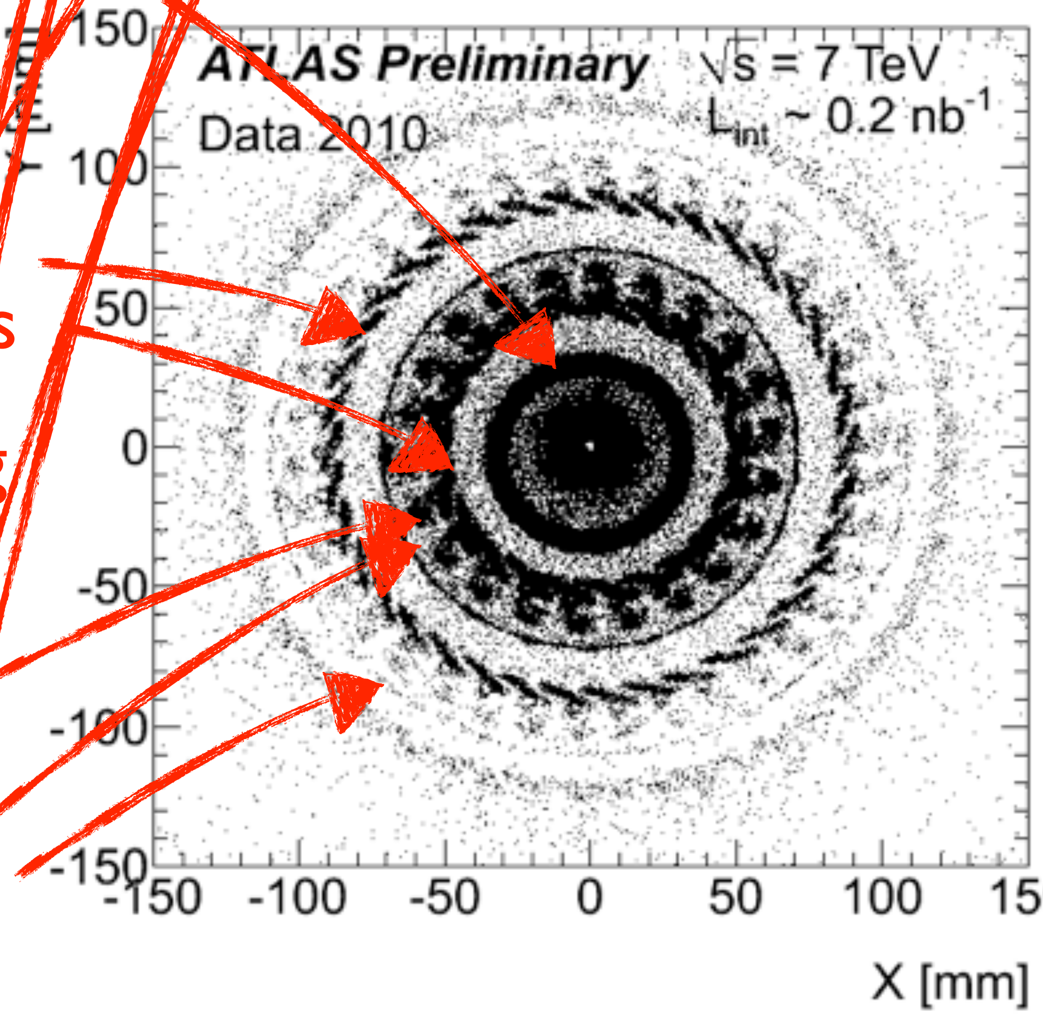
Pixel Modules

Cooling pipe

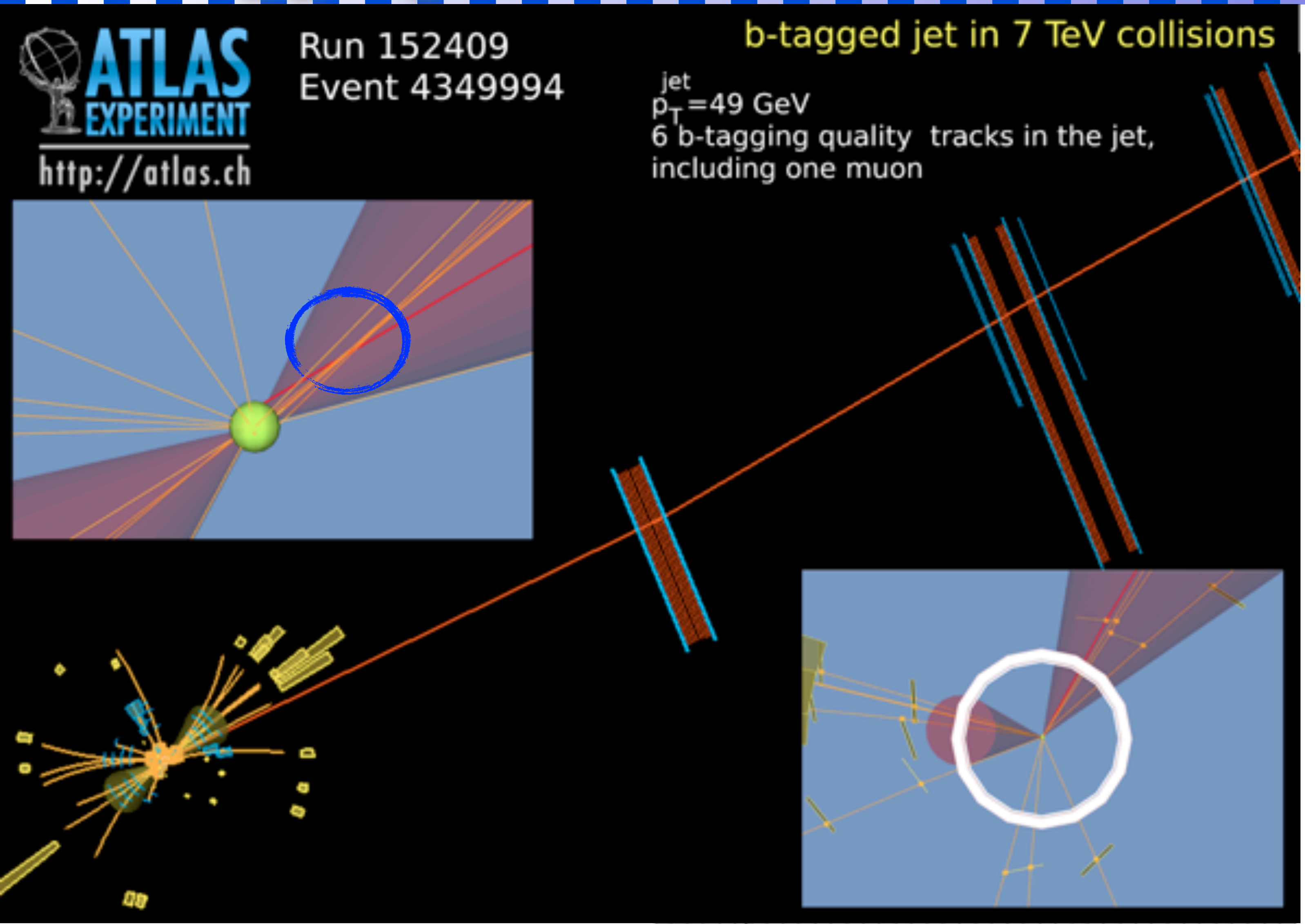
Cables

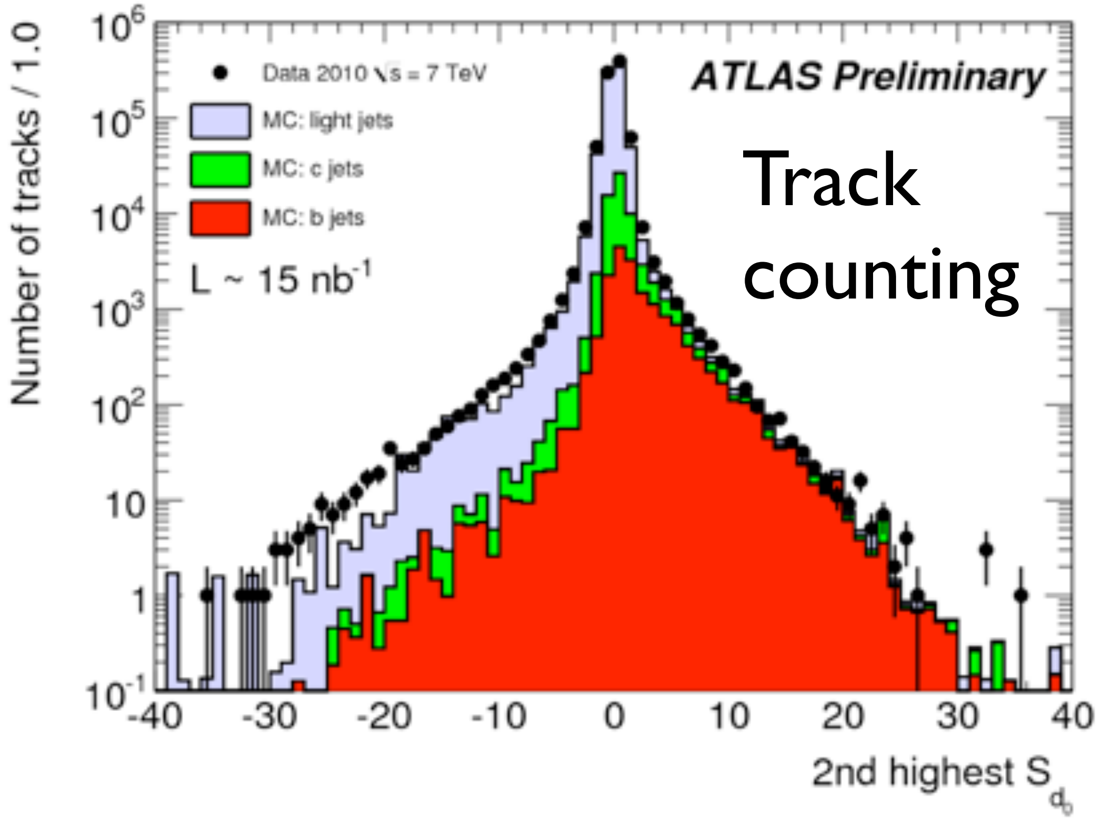
C-fiber shell



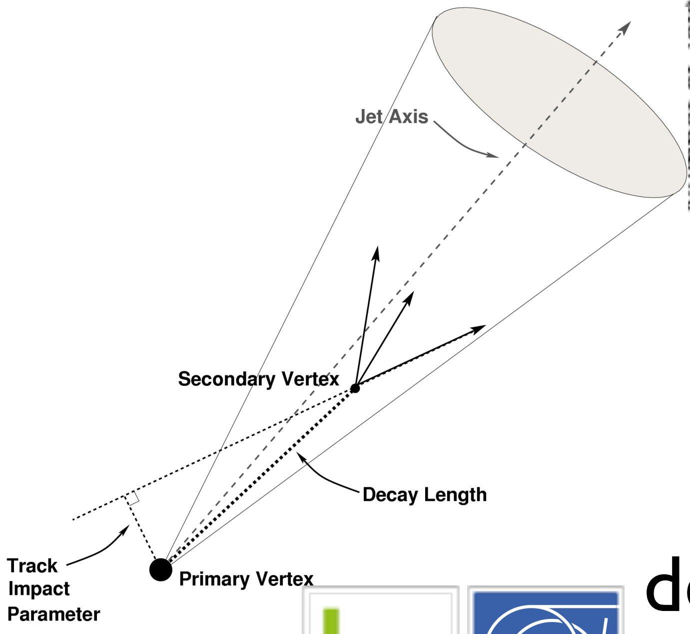


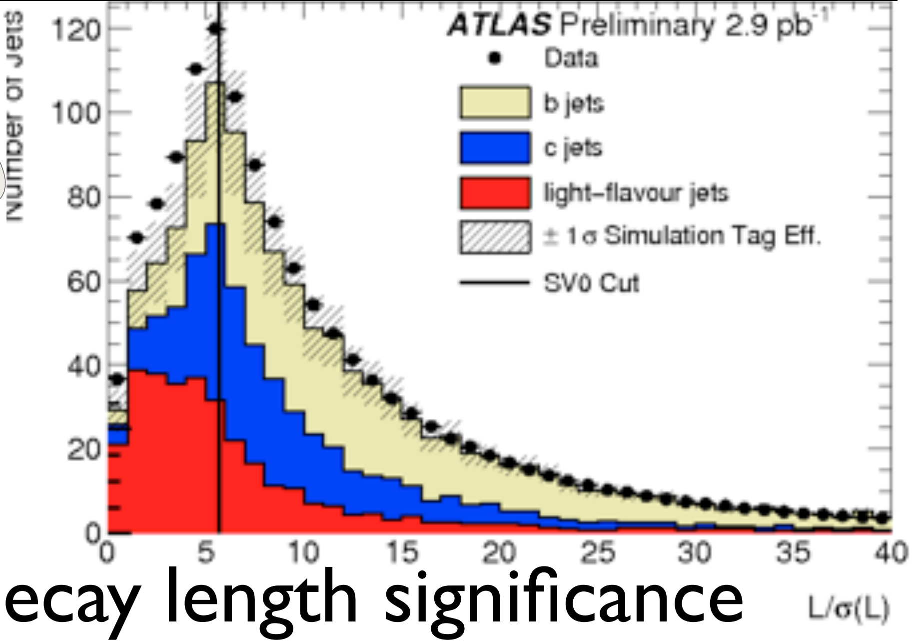
B-Tagging



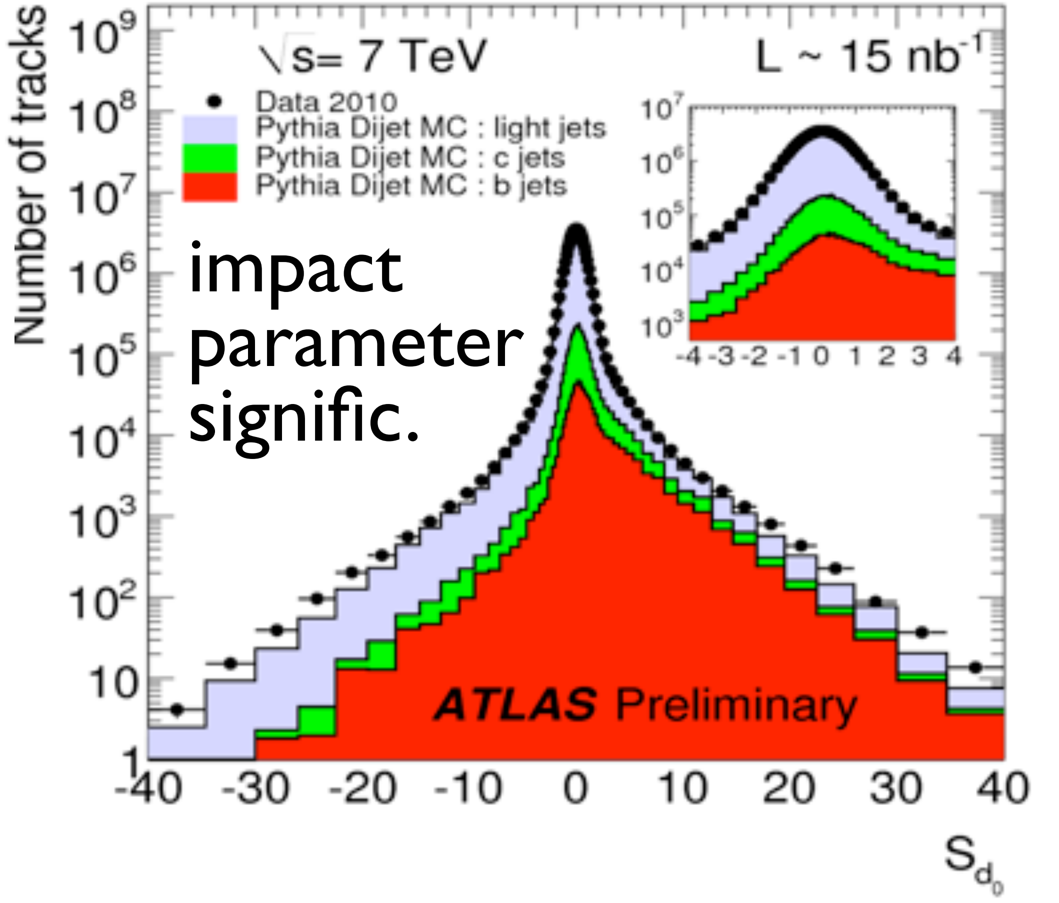


Track counting





decay length significance

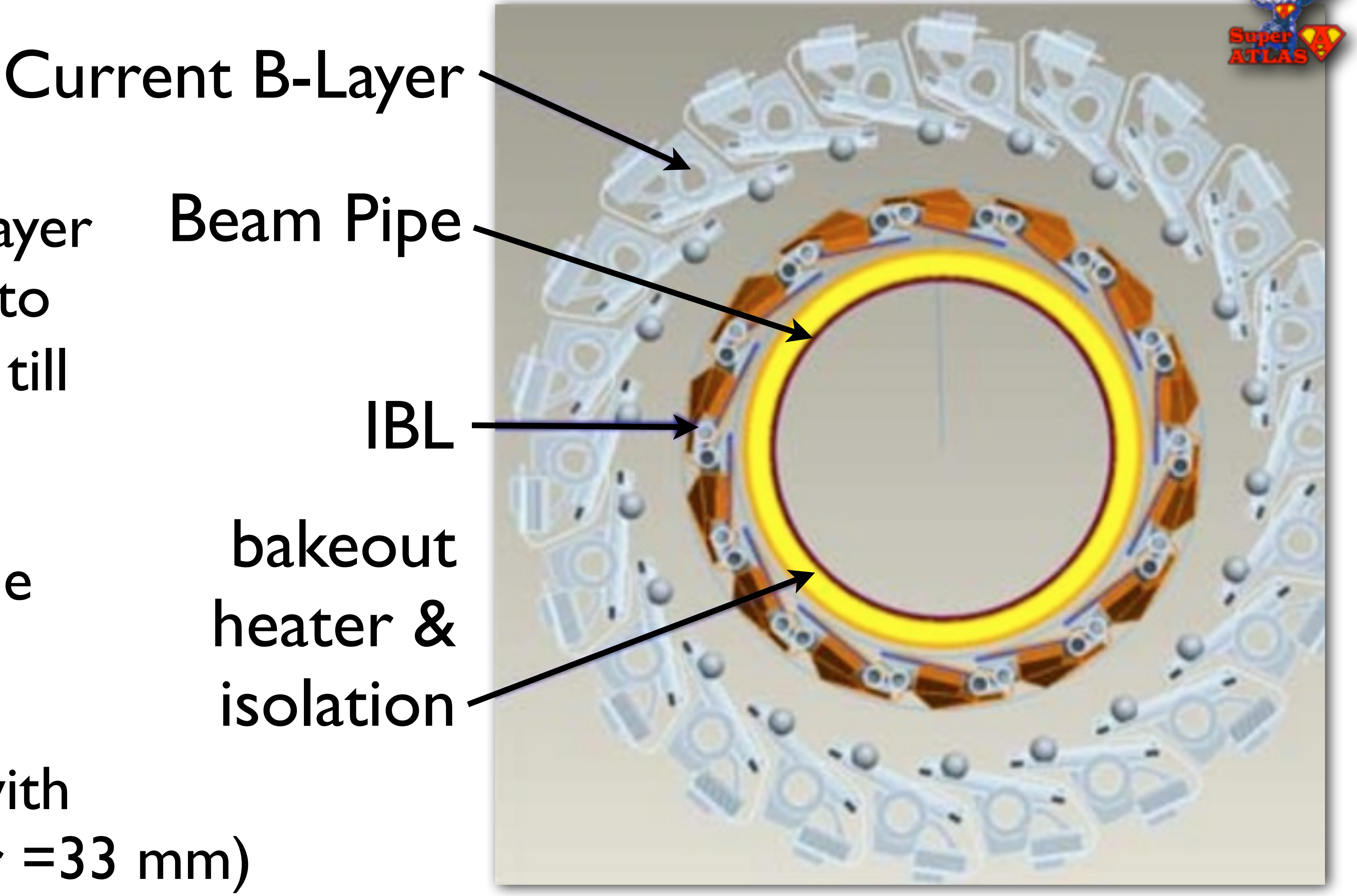


impact parameter signific.

Motivation: ATLAS Insertable B-Layer (IBL)

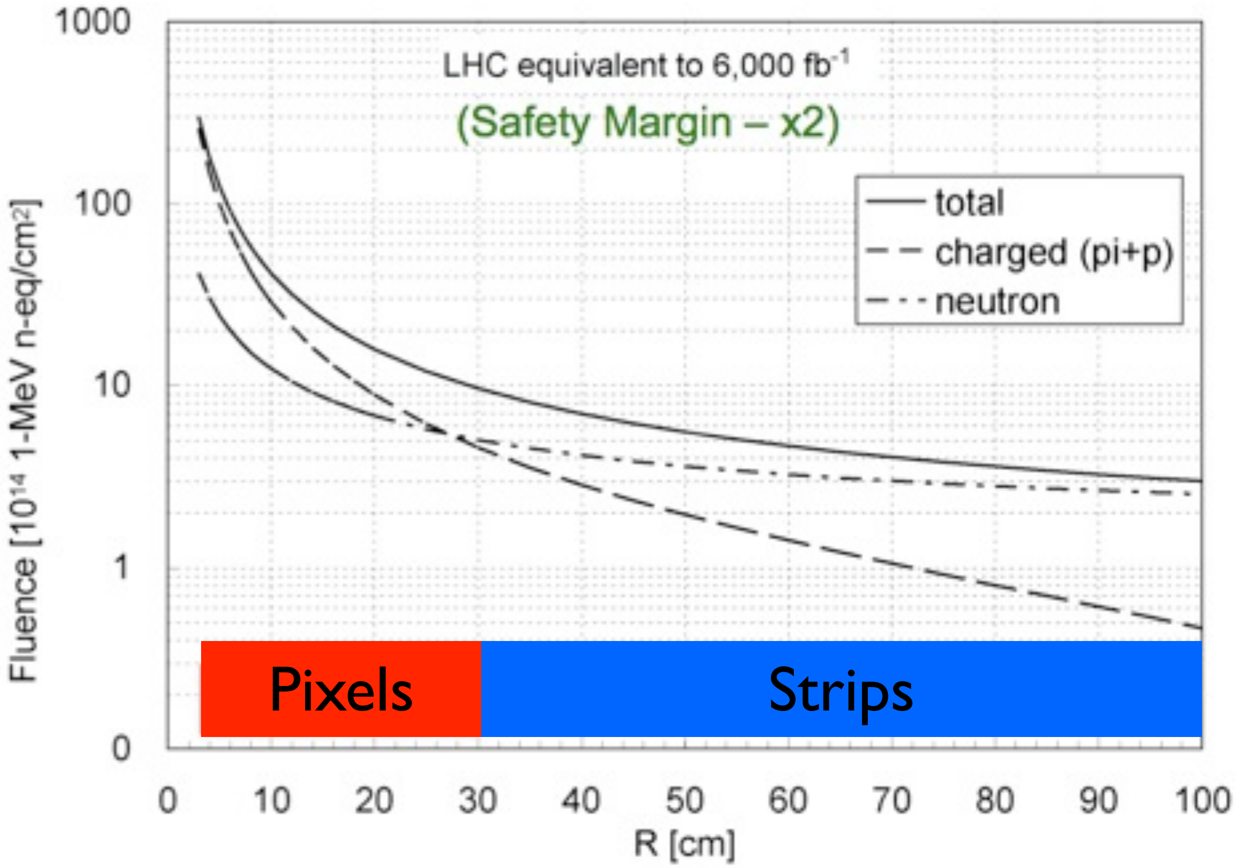
ATLAS Phase I upgrade:

- current innermost layer (B-Layer) usable up to 10^{15} n_{eq}/cm^2 → fine till Phase I upgrade
- originally planned exchange not feasible (>1 year)
- Insertable B-Layer:
  - new beam pipe with additional layer (r =33 mm)
  - tight space → no shingling, slim or active edges
  - 1-1.5 % X_0 material budget
  - 5×10^{15} n_{eq}/cm^2 requirement



- beam pipe radius can be reduced from 29 to 25 mm

Motivation: ATLAS for sLHC: Layout & Fluences

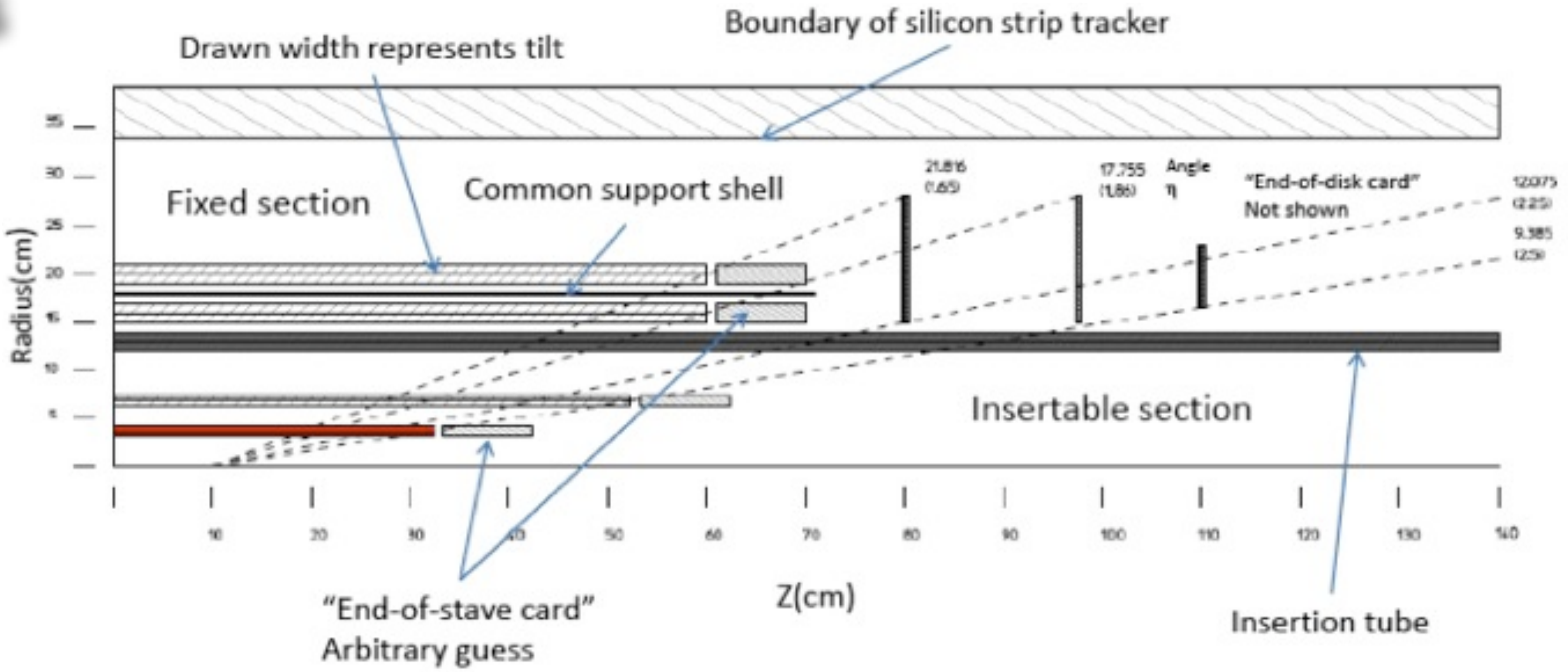


sLHC ATLAS Layout Snapshot

- 3 - 30 cm Pixels
- 30 - 100 cm strips
- Pixel layer 1: ~ 60 cm long staves at r ~ 3 cm
- multiple of 0.12 m² sensor material in innermost layer
- NIEL ~ 1.5×10^{16} cm^{-2} (3000 fb^{-1})

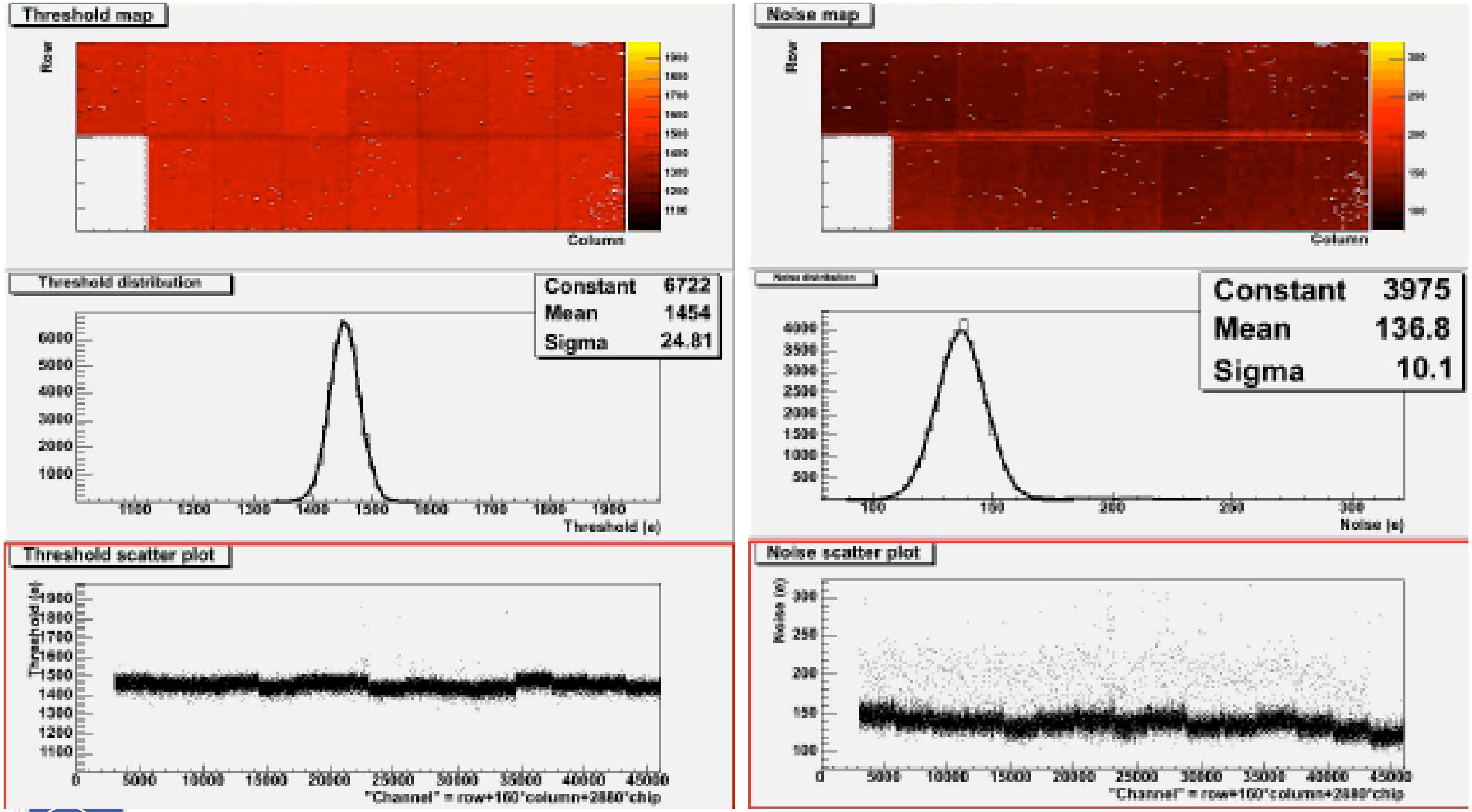
sLHC ATLAS Fluences

- below 25 cm charged particles dominate (90% π,k,p - 10% n)
- different inner pixel technologies ?



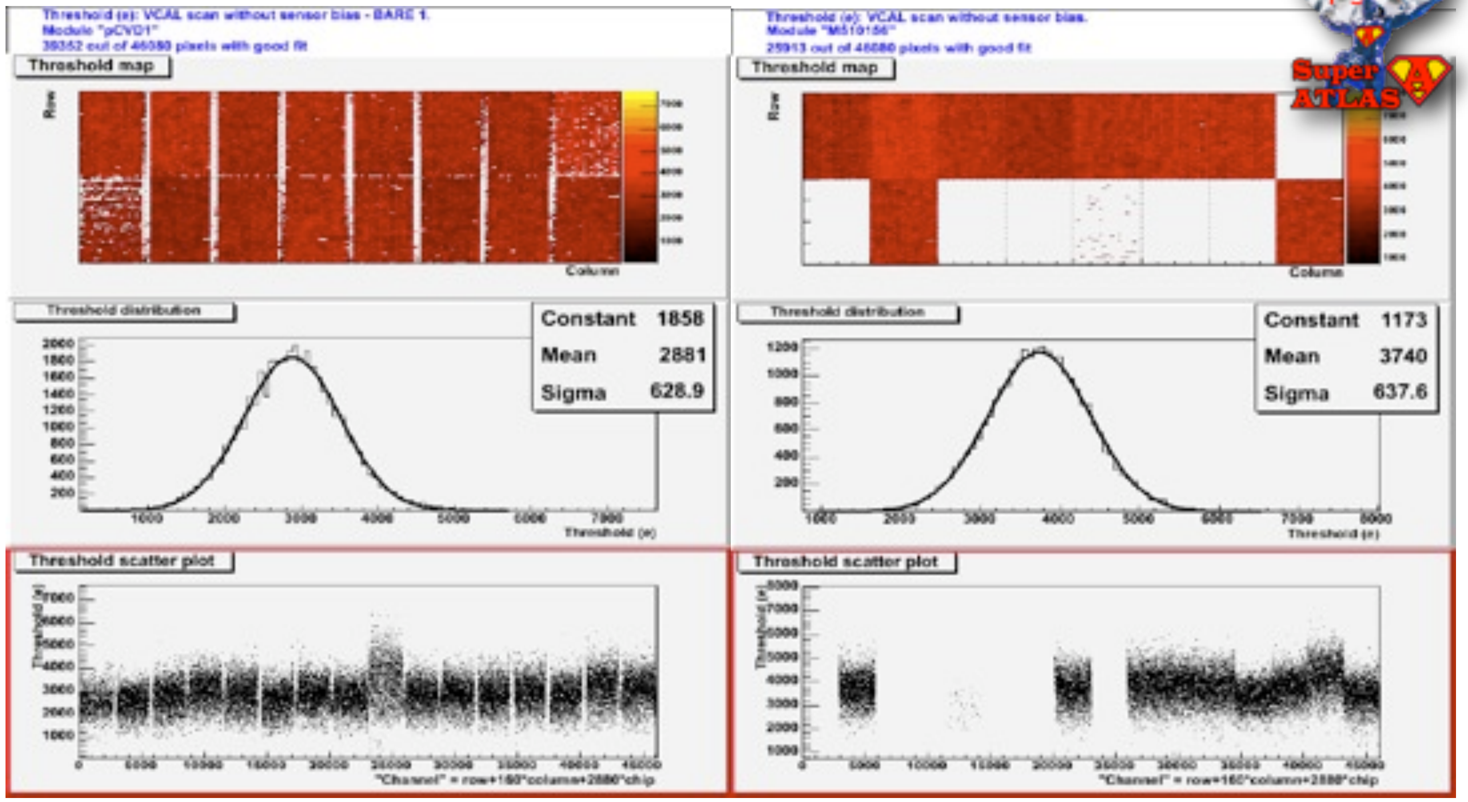
Threshold and Noise

- excellent threshold and noise performance:
- threshold: 1450 ± 25 e^-, noise: 137 ± 10 e^- & overdrive 800 e^-
- no changes from bare FEs (1497 ± 26 e^-; 138 ± 8 e^-) to module
- "invisible sensor": low capacitance C & leakage current I_{leak}



Industrialization: Rework of Diamond Sensors

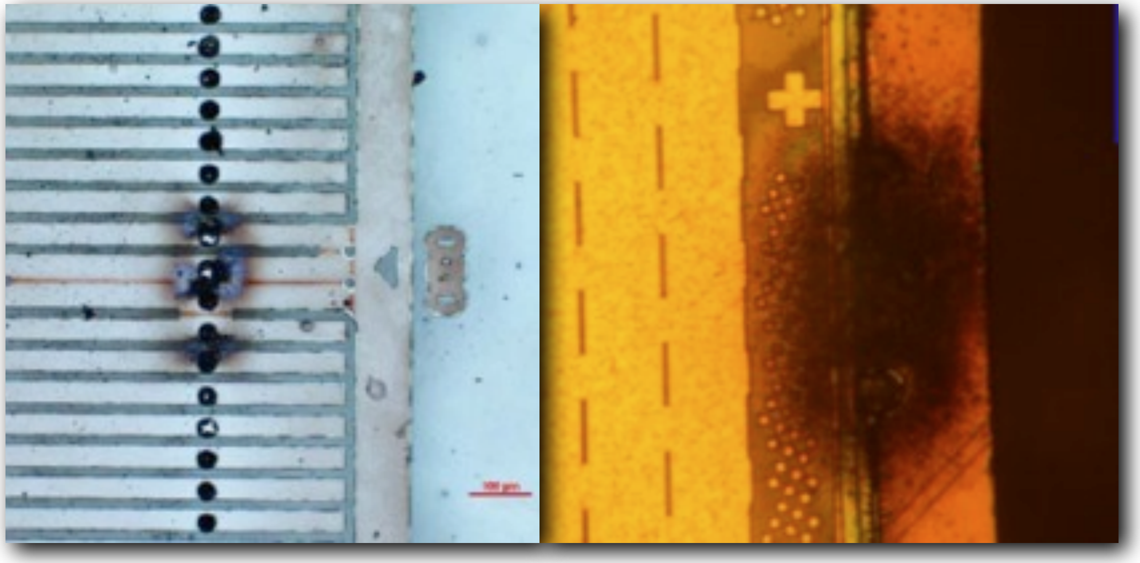
- diamond edge left metallized
- module shorted: 10V bias
- 7/16 FEs damaged
- reworked at IZM
  - backside metallization redone
  - module rim plasma etching
  - all FEs replaced



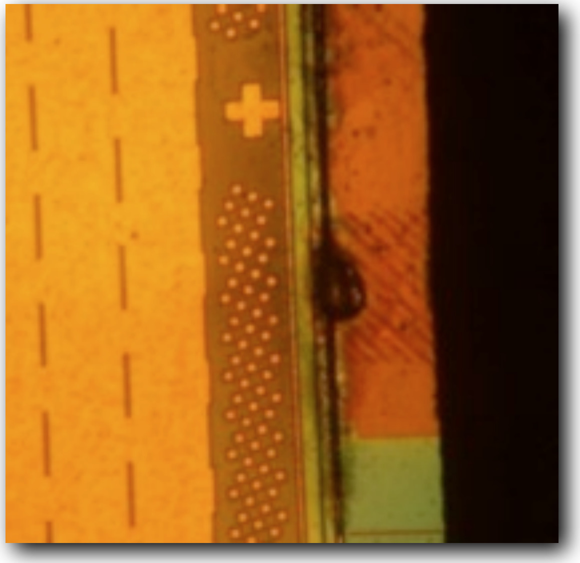
before

after applying 10V

- diamond sensor can be reused if module QA fails



before rework



after rework