

# Hybrid Pixel Detectors

Markus Keil

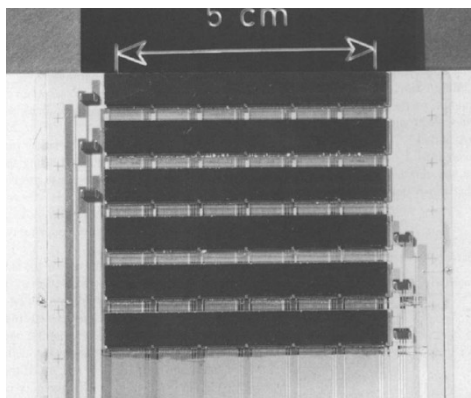
2<sup>nd</sup> Institute of Physics, Georg-August-Universität Göttingen  
and CERN

**EDIT 2011**

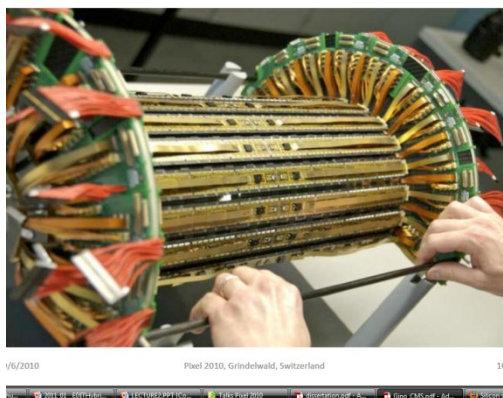
Excellence in Detectors and Instrumentation Technologies  
CERN, Geneva, Switzerland - 31 January - 10 February 2011

**Silicon Strips and Pixel Technologies**

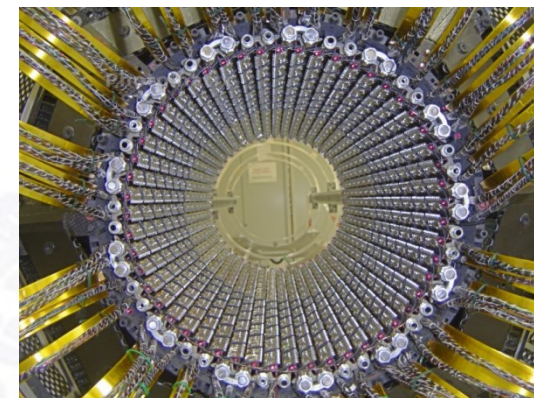
# Introduction: Hybrid Pixel Detectors



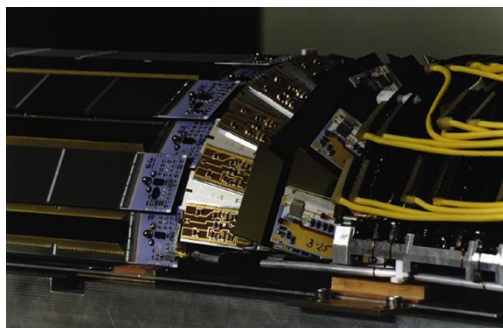
WA97 (1995)



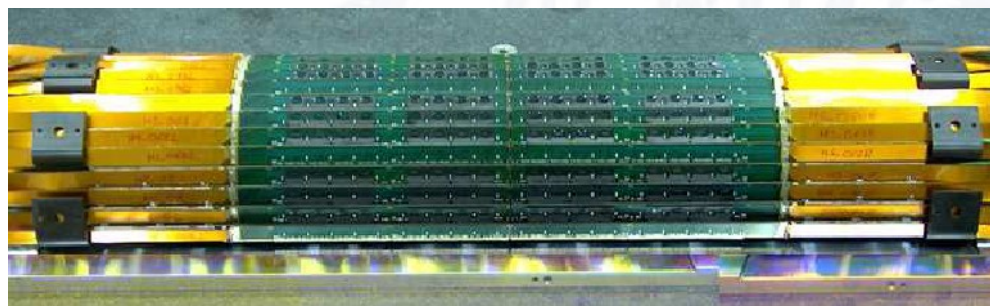
CMS Barrel



ATLAS Barrel Layer

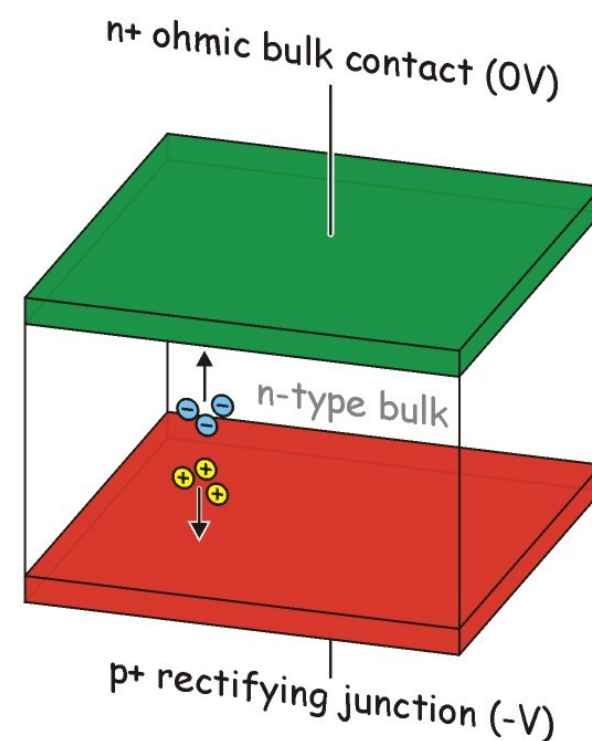


DELPHI VFT (1996)



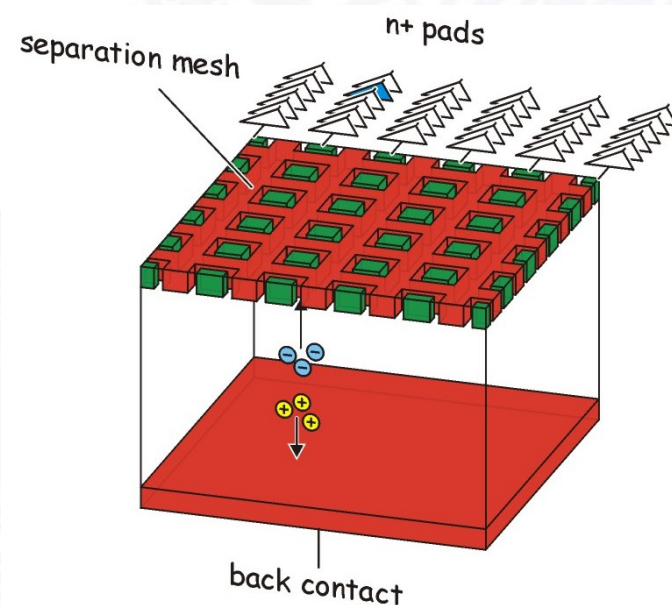
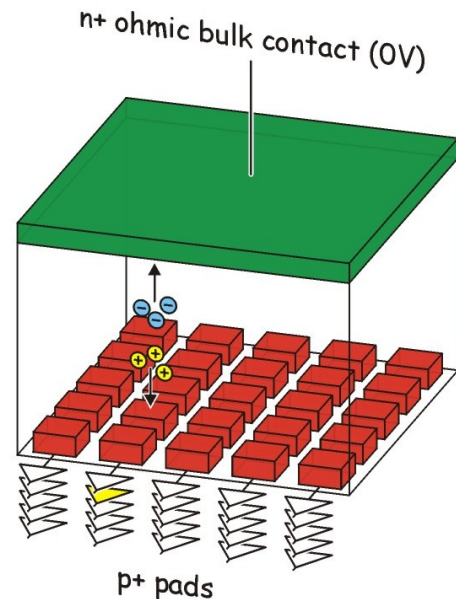
ALICE SPD Half Barrel

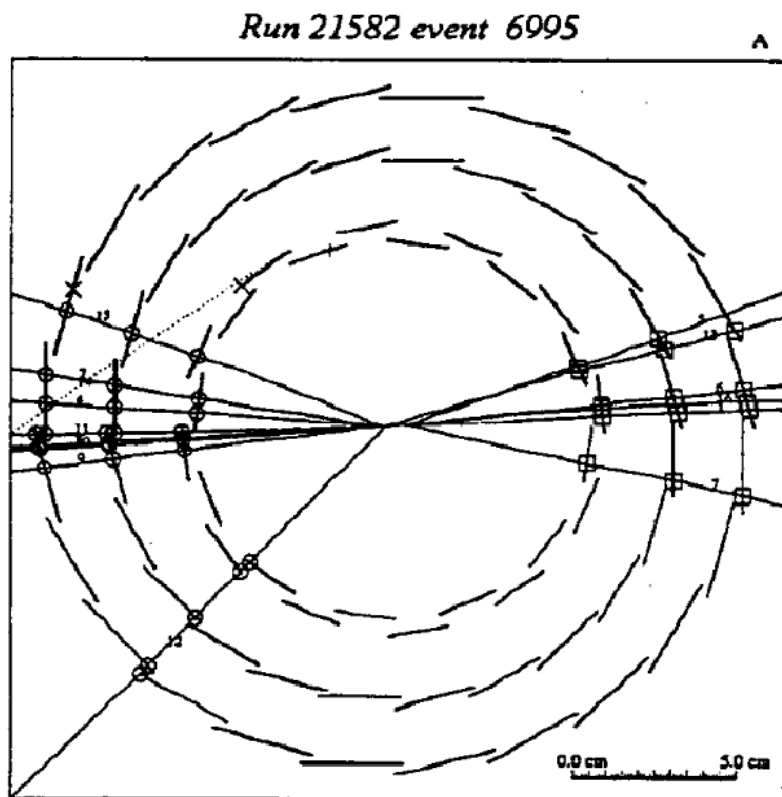
- Reverse-biased p-n-junction  
(cf. lecture of M. Krammer)
  - Zone with electrical field, free of movable charge carriers
  - Minimum ionising particle generates approximately  $10^4$  eh-pairs / %  $X_0$
  - Ideal as a particle detector, but no spatial information yet
- Help came from IC industry:
  - Planar process allows “cheap” large scale production of segmented Si detectors



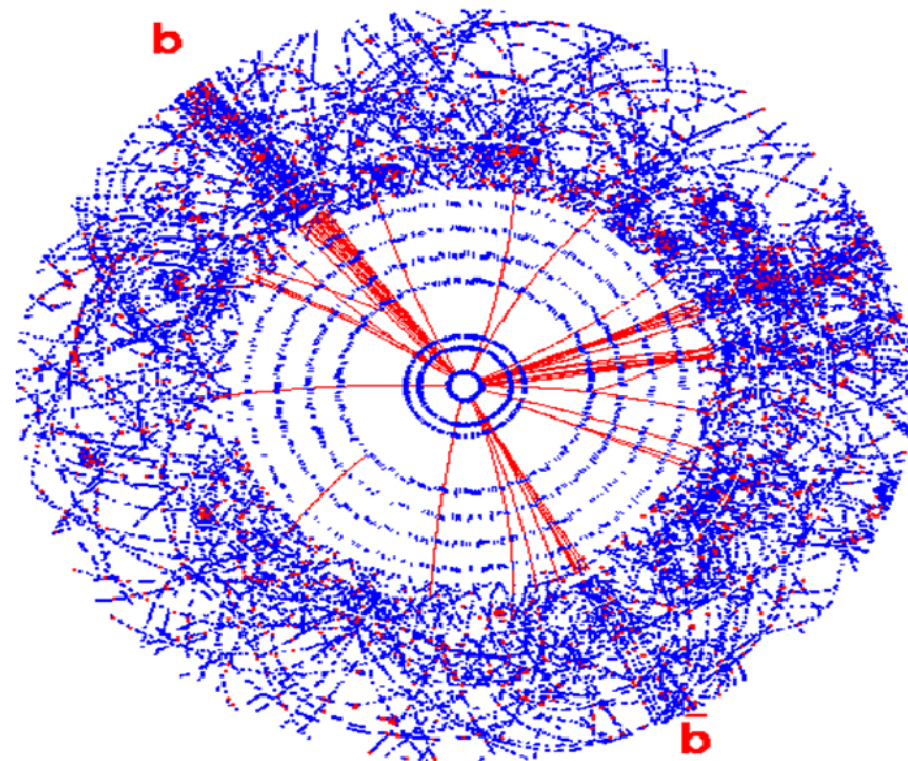


- Segment one electrode into pixels
  - True 2D-information, no problem of ambiguities at high track densities
- Smaller electrode size brings other benefits
  - Lower leakage current → lower noise, better radiation tolerance
  - Lower capacitance → lower noise
- ... but also complications
  - Large number of channels, proportional to sensor area
  - Signals of each channel needs to be processed



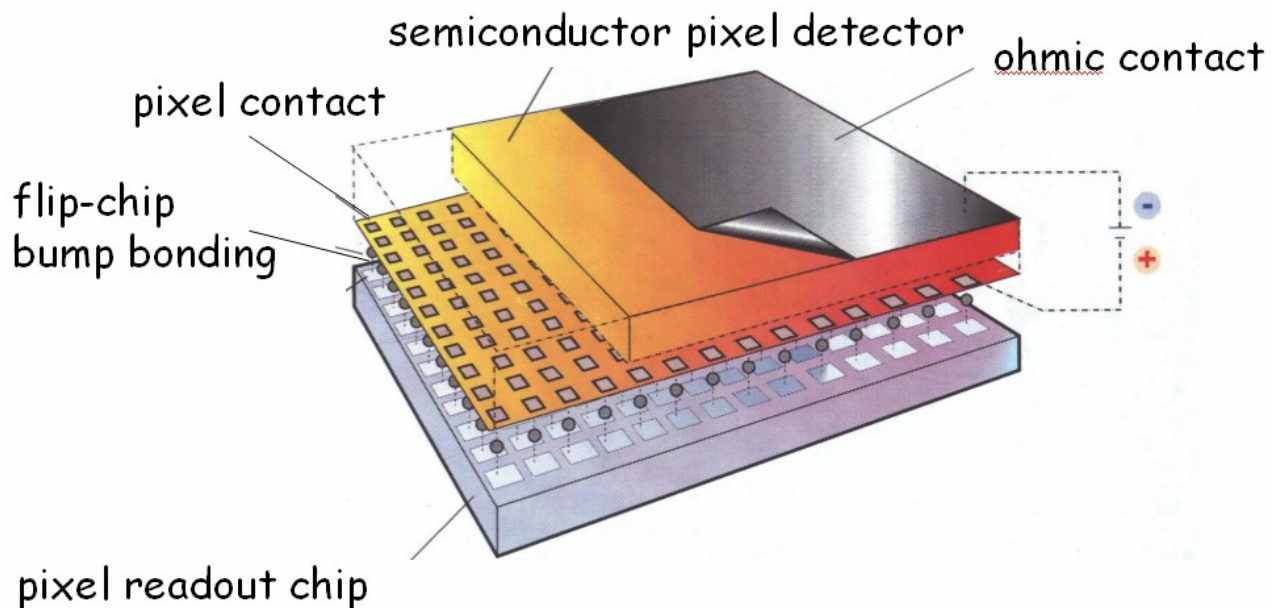
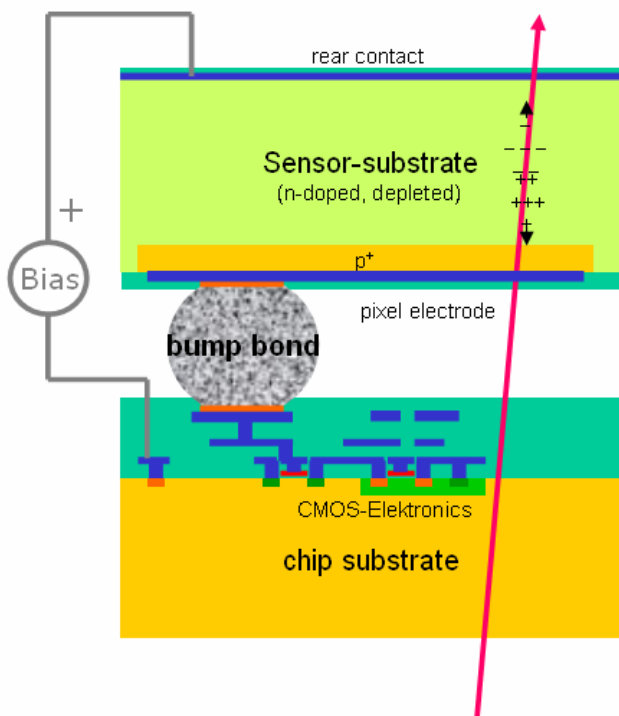


P. Weilhammer, NIM A 342 (1994) 1



- $Z^0 \rightarrow b\bar{b}$  candidate at LEP (DELPHI Experiment)

- Simulated  $H \rightarrow b\bar{b}$  event at LHC in the ATLAS tracker
- Including 22 pile-up collisions
- No chance without 2D-information



- A hybrid pixel detector is made from two separate chips
  - Signal is generated in the sensor chip, 200 – 300  $\mu\text{m}$  thick
  - Amplification and signal processing in a dedicated readout chip
- 1:1 cell-correspondence between sensor and readout chip
- Connections between sensor and electronics pixels are established with bump bonds

- Advantages:

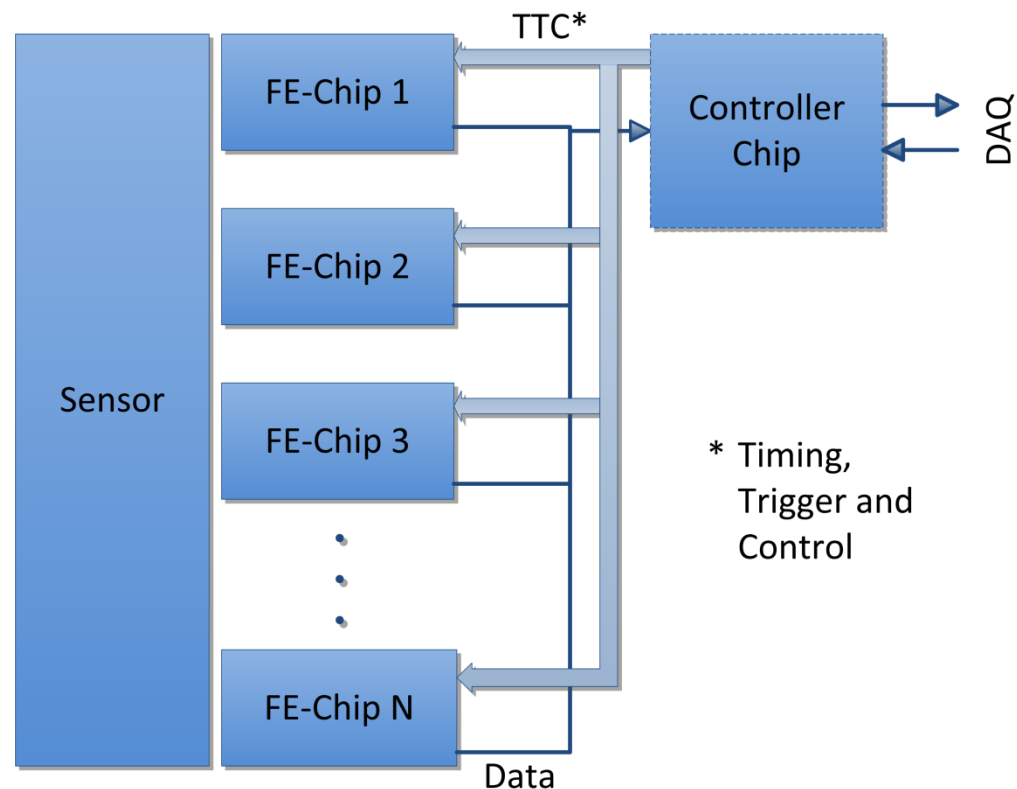
- Chip and sensor can be optimised separately for the requirements of the experiment, in particular in terms of radiation hardness
- Fast parallel readout
- Relatively large signal, low noise (S/N ~ 100)
- Mature technology

- Challenges:

- Complex interconnection necessary
- Readout chip heats sensor → Good cooling necessary
- High material budget in the sensitive volume (Sensor + Readout chip + Support + Cooling)

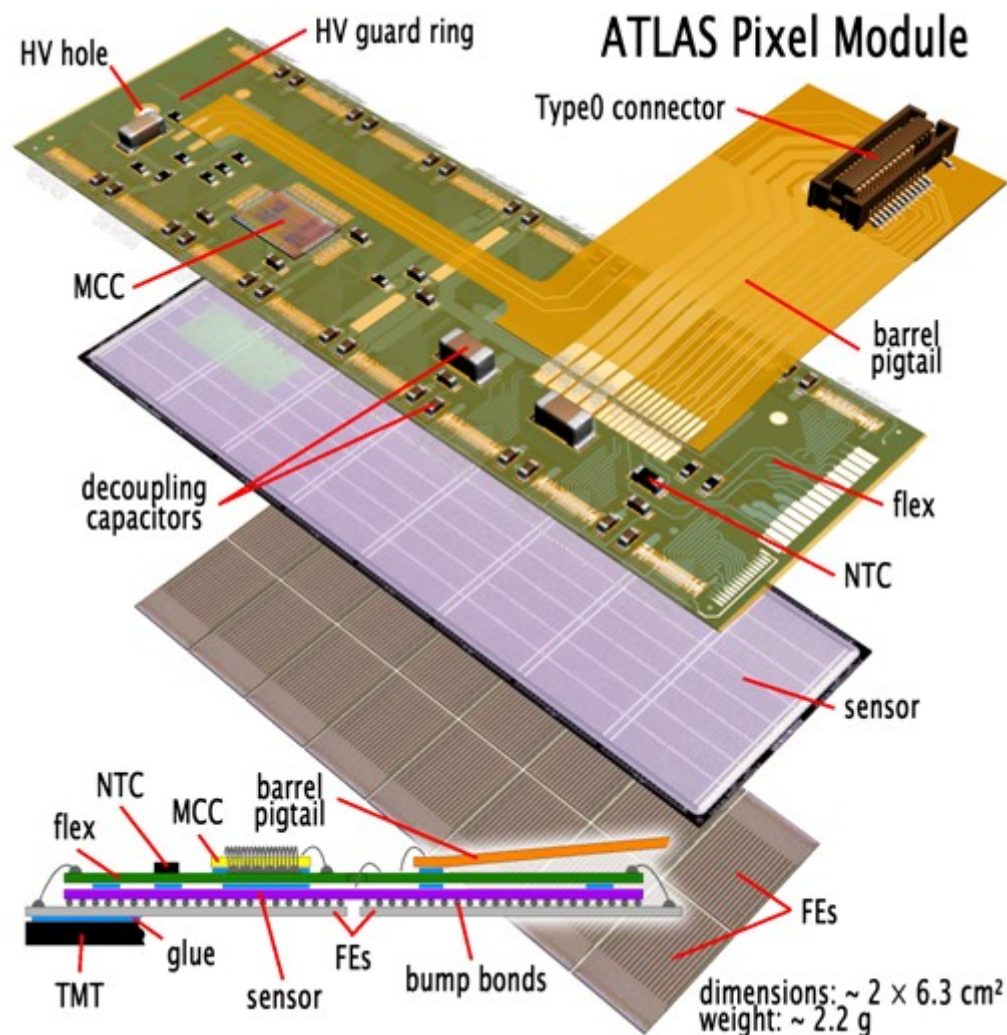


- Sensor signals are processed by several readout (front-end) chips
- FE-chips are controlled by on-detector controller chip
  - Controller chip can be on the module or on the ladder or similar
- Controller chip communicates with off-detector data acquisition
  - Typically via optical links (Additional interface-chips for electro-optical conversion on detector- and DAQ-side)

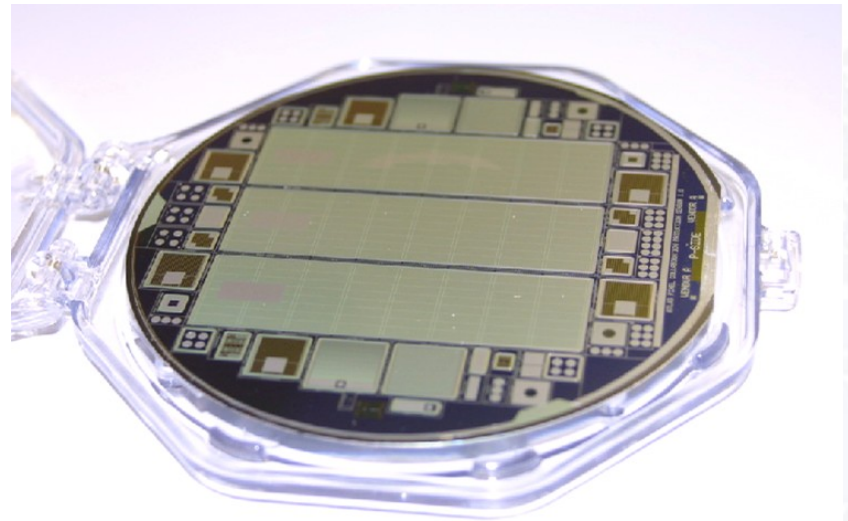




- Sensor is connected to FE-chips with bump bonds
  - Here: 1 sensor tile, 16 FE chips in 2 rows
- FE periphery with contact pads sticking out from underneath sensor
- Connected to flexible PCB with wire bonds
- Flexible PCB carries controller chip, passive components and connection to off-module electronics



# The Sensor



- The production of silicon sensor has profited from the developments in microelectronics; but there are also differences:
  - Sensor needs much purer, high-resistivity silicon (→ floatzone process)
  - In microelectronics everything happens in the upper few  $\mu\text{m}$  of the wafer – for the sensor the complete volume and in particular also the backplane is important
- Different possible choices for pixel and substrate material type

	N-type substrate	P-type substrate
N-type pixel	High radiation tolerance Double sided process → expensive	Single sided process No type inversion Less developed approach
P-type pixel	Single sided process Low radiation tolerance	Double sided process No advantage with respect to n-on-p

- The design of the pixel sensors has to take into account the requirements in terms of efficiency, stability and radiation hardness

- A polysilicon rod is mounted with a seed crystal in an inert atmosphere
- A small zone of the rod is melted by a movable RF-heater
- This floatzone is slowly moved through the crystal, at the end of this zone the silicon freezes to a single crystal
- Most impurities remain in the molten phase
- Produces very pure silicon as needed for sensors
- Ingots are cut into wafers, which are then lapped and polished

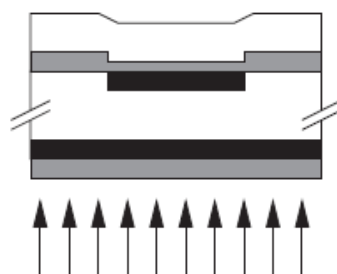




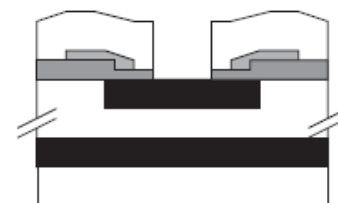
- Sensor processing is a sequence of
  - Thermal treatments (e.g. for thermal oxidation or annealing steps)
  - Photolithography
  - Etching
  - Doping (by diffusion or ion implantation)
  - Layer deposition of insulators (oxides, nitrides) or metals (Al)
- Spatial precision usually less critical than in microelectronics, but purity is much more important
- Double sided processing, cost depends on the number of structured masks



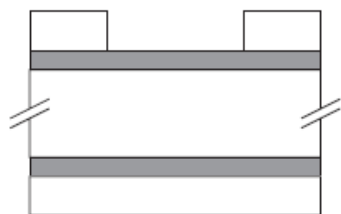
1. Thermal oxidation



5. Phosphorus implantation



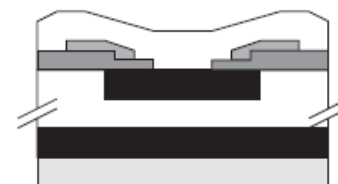
9. Etch oxide openings



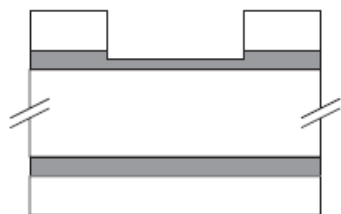
2. Photoresist for implant



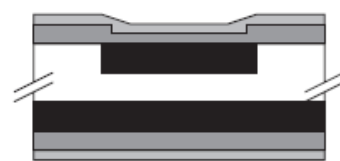
6. Annealing and drive-in



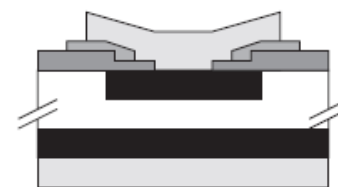
10. Back side aluminization



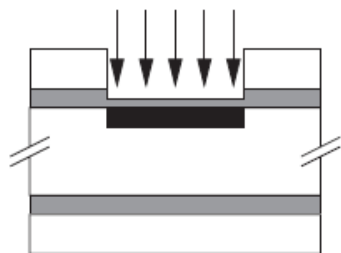
3. Etch oxide step for alignment



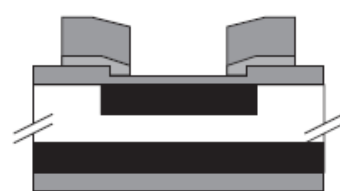
7. Nitride deposition



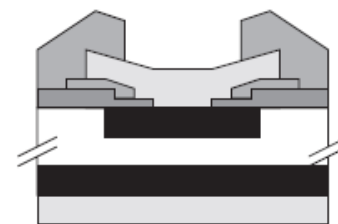
11. Front side aluminization



4. Boron implantation

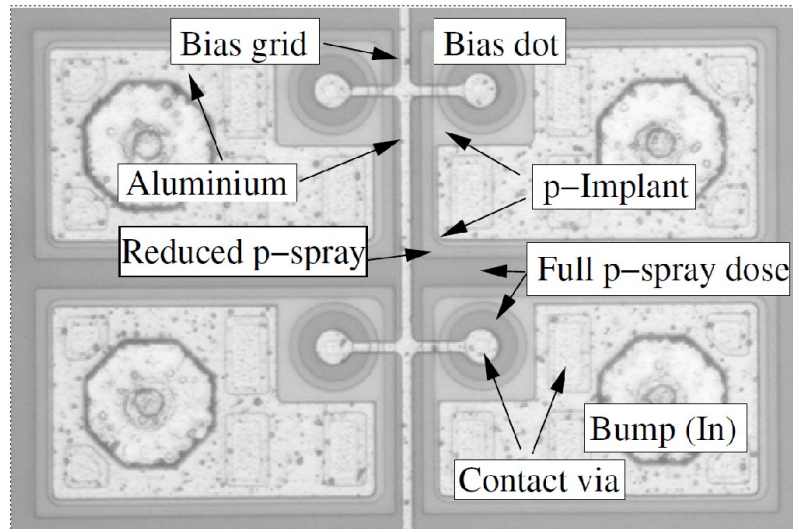
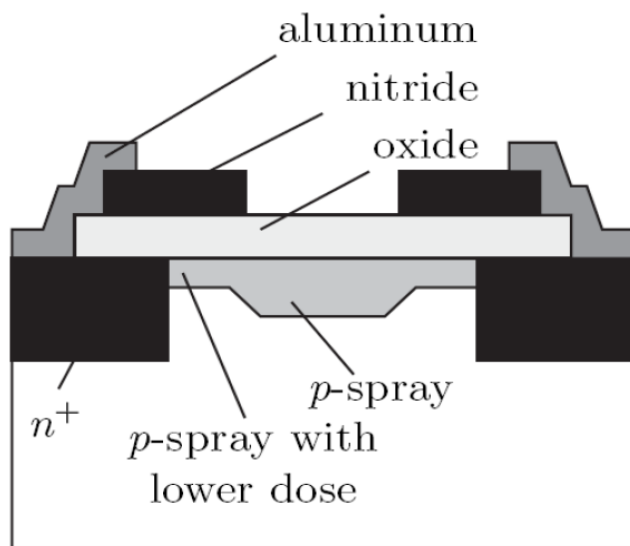


8. Etch nitride openings

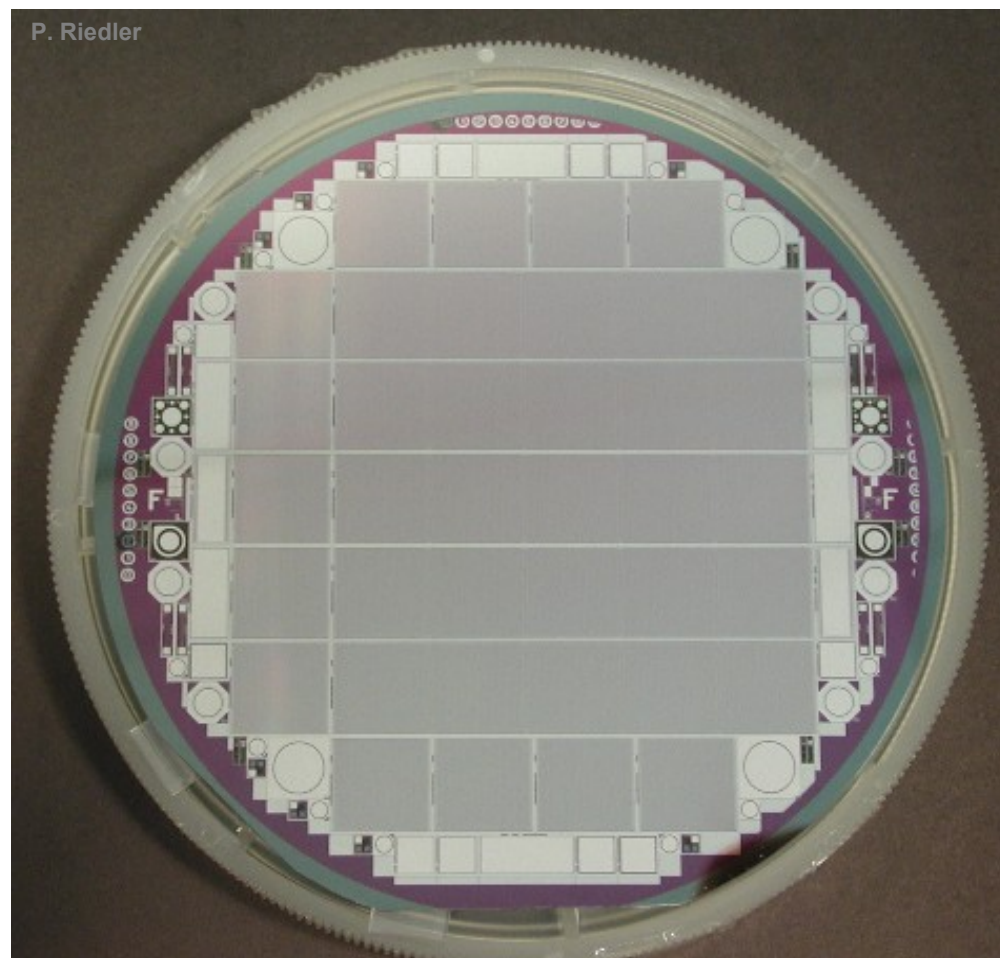


12. Passivation

From: Fischer, Rohe, Rossi, Wermes: Pixel Detectors

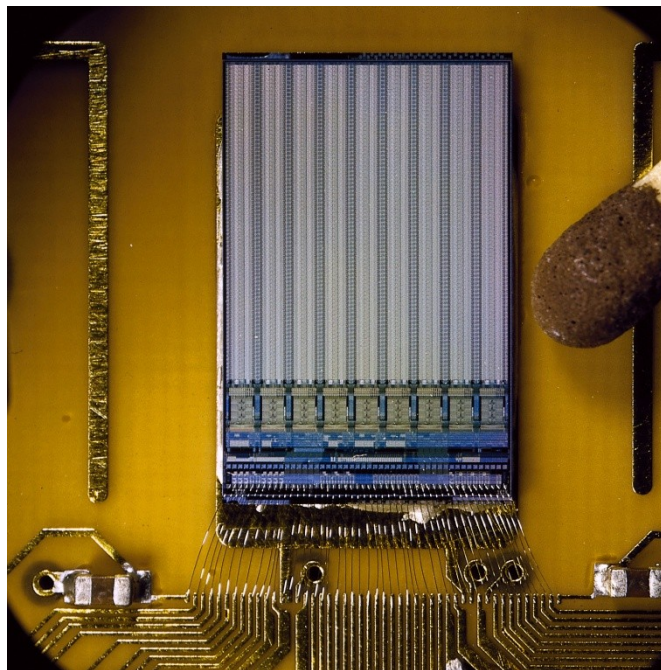


Four pixels of a CMS barrel pixel sensor



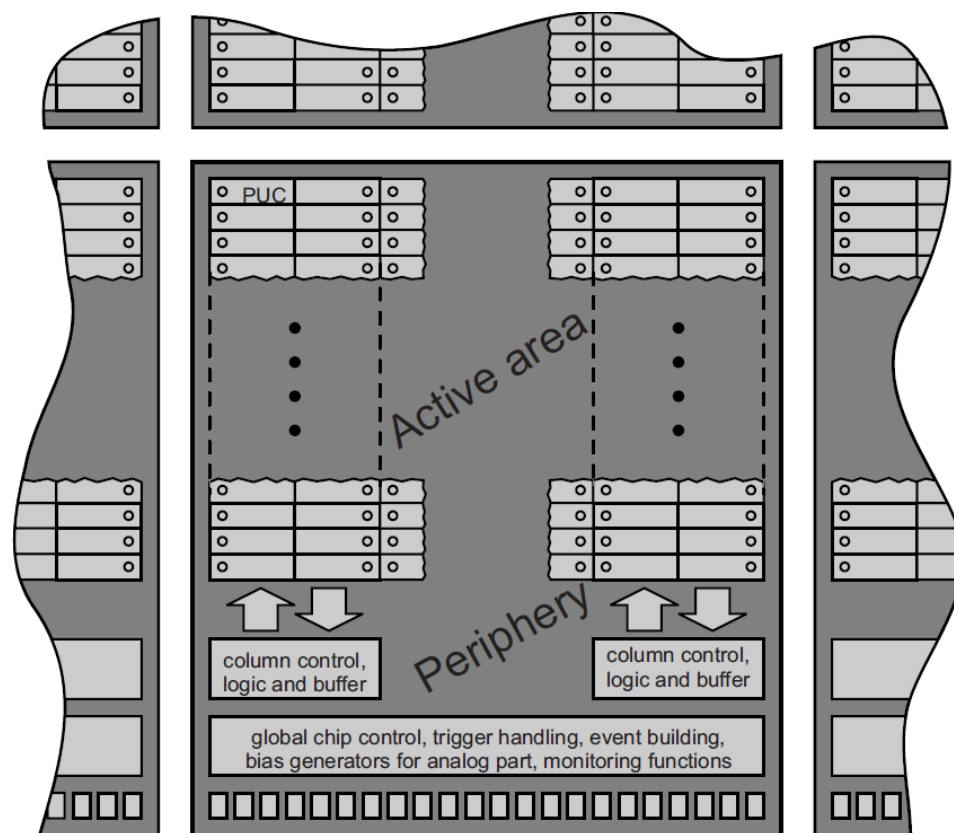
ALICE sensor wafer

# The Frontend Chip

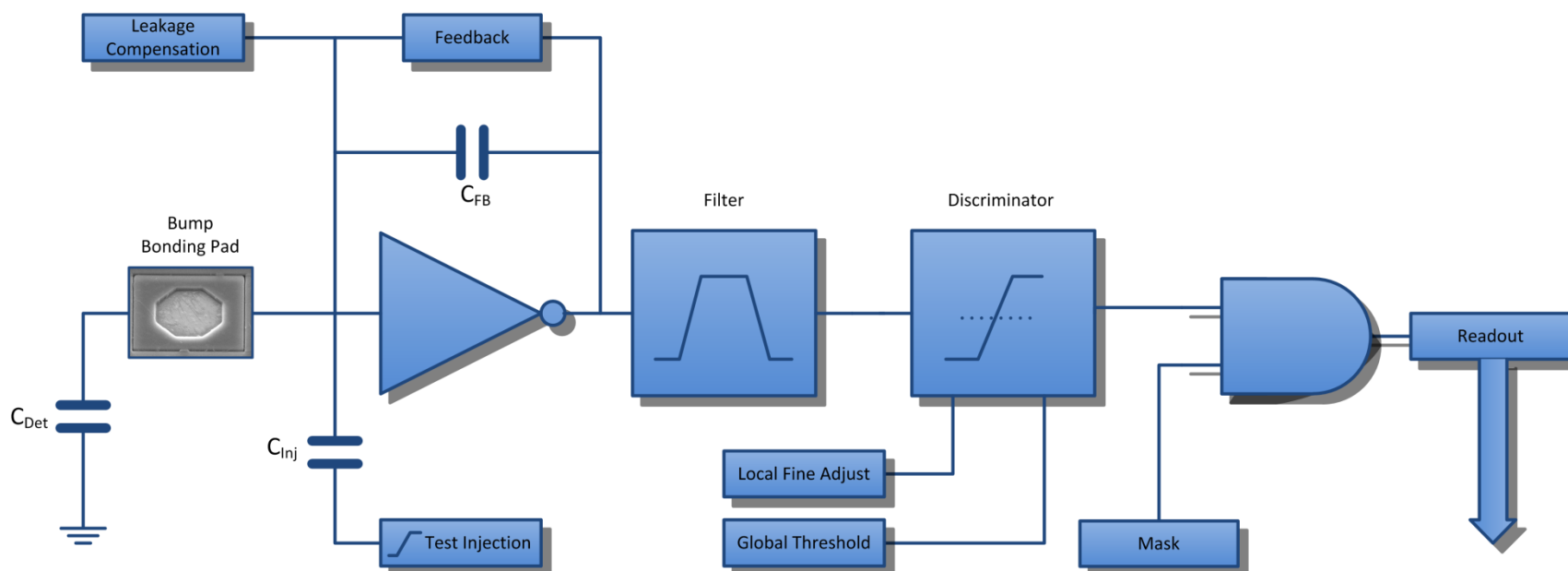




- Usually several smaller FE-chips read out one sensor tile
  - Sensor size is limited by wafer size and bump bonding requirements (flatness)
  - Electronics chip size limited by yield considerations (+process rules)
- Signal processing steps in the FE-chips:
  - Amplification of sensor signal
  - Hit decision
  - Hit storage
  - Trigger validation
  - Readout of triggered hits
- First two steps are always done in the pixel cell, in some designs more
  - Readout architecture depends on hit rate, trigger rate, trigger latency and geometric constraints

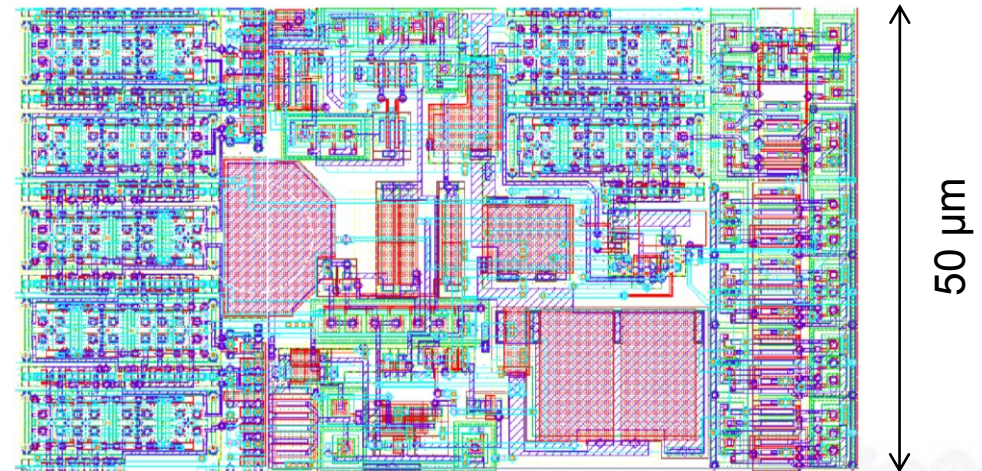


From: Fischer, Rohe, Rossi, Wermes: Pixel Detectors

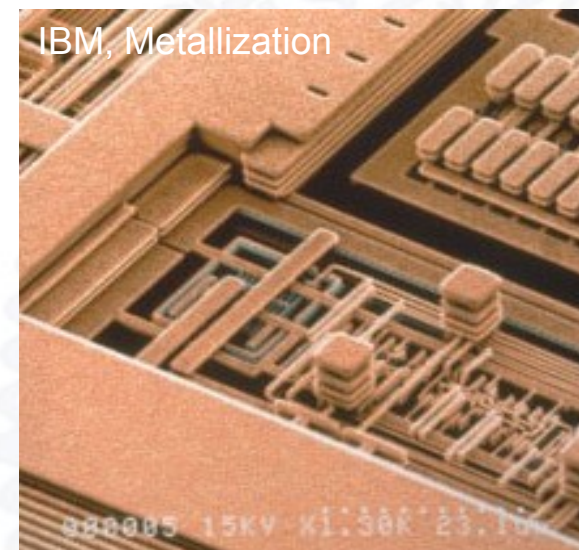


- Integration of signal charge
  - In 250  $\mu\text{m}$  Si: Most probable value 19000 e, but consider charge sharing between pixels, smaller charge depositions, radiation damage
- Hit decision
- Transfer of hit data to periphery
- Swiss army knife: many (conflicting) requirements: fast, low noise, low power consumption

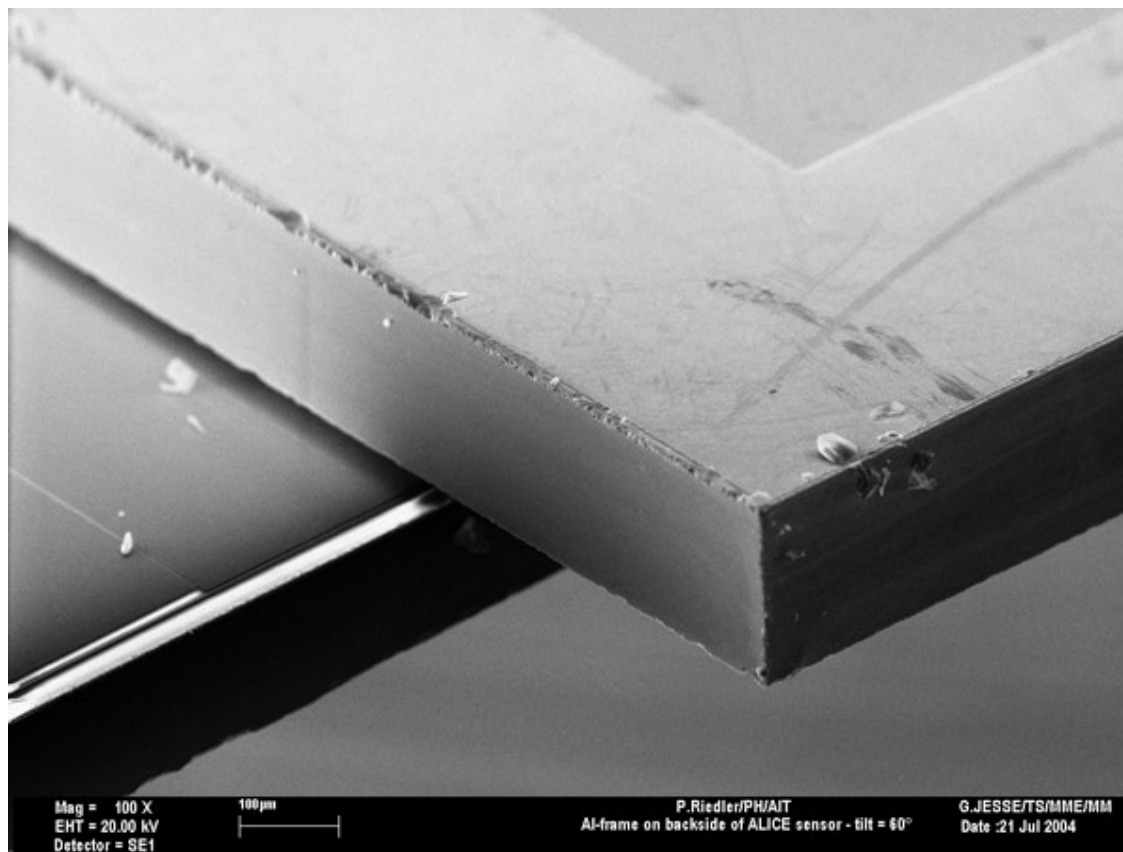
- Pixel chips use commercial microelectronics processes
- However the designs are “full-custom”
- Optimised for radiation hardness (non-standard design rules)
- Layout challenge: implement all necessary functionality in the area of a single pixel
  - LHC-type chips: 500 – 1000 transistors per pixel cell
- Mixed designs (analogue and digital)
  - Careful shielding necessary to avoid injection of noise



P. Fischer, CERN-2002-003, p.91



# Bump Bonding

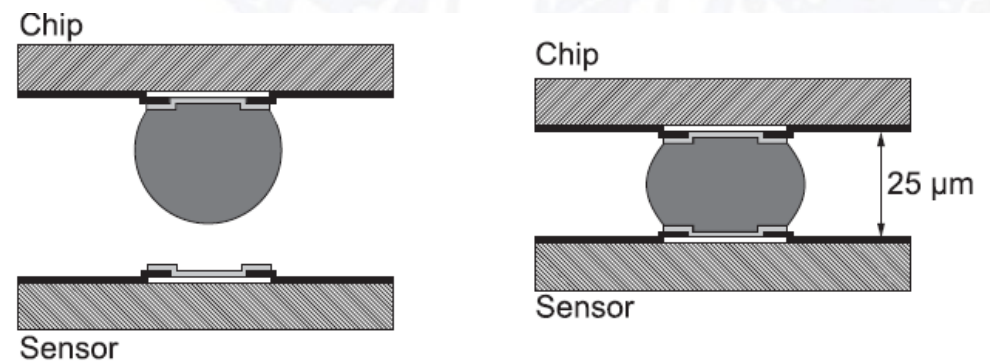
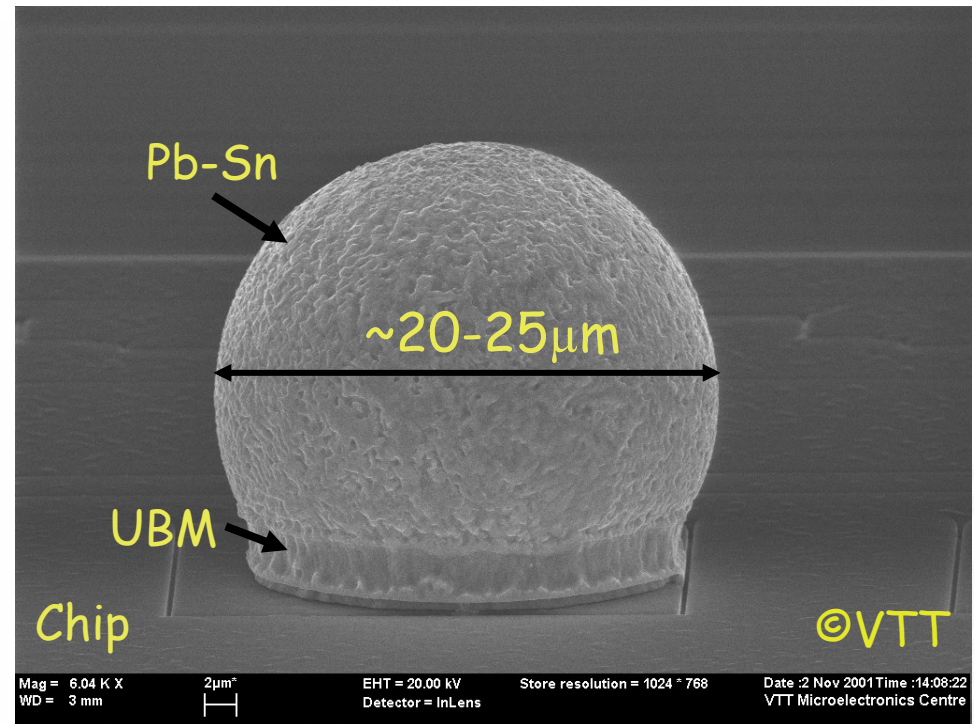
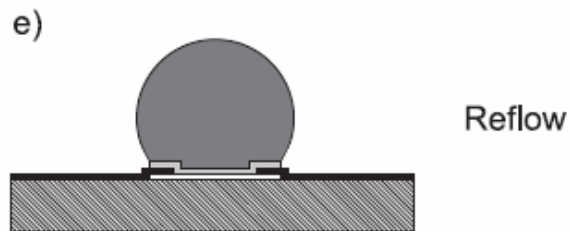
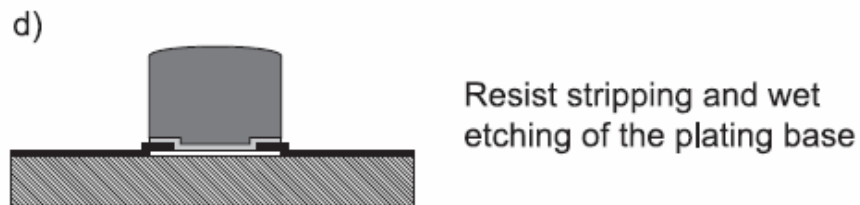
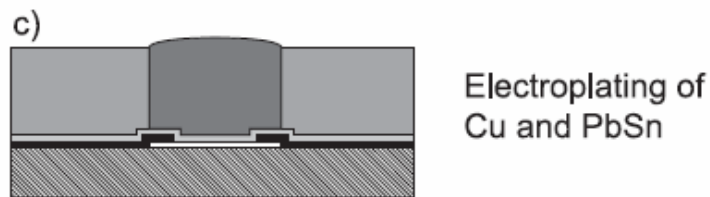




- Connection between chip and sensor is established with bump bonds
- Process used in industry, but pitches needed in HEP are typically smaller than industry standard
- Two main process parts:
  - Bump deposition
  - Flip-chip assembly
- Bump deposition usually done on wafer-level
- Electronics wafers are thinned after bump deposition (e.g.  $750\ \mu\text{m} \rightarrow 150\ \mu\text{m}$ )



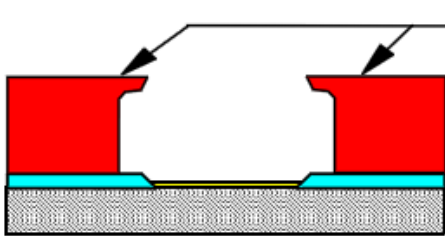
- Two main techniques in HEP:
  - Electroplated solder bumps
  - Indium bumps



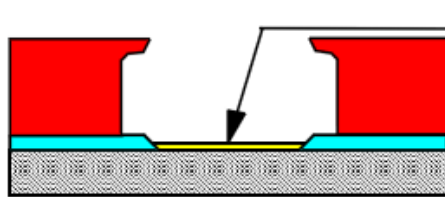
Fischer, Rohe, Rossi, Wermes: Pixel Detectors



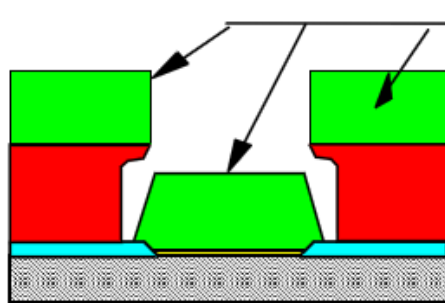
Wafer Cleaning



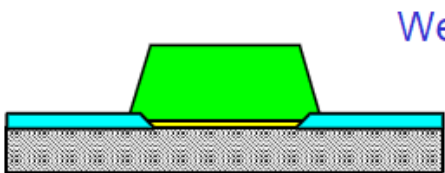
Photolithography



Plasma activator

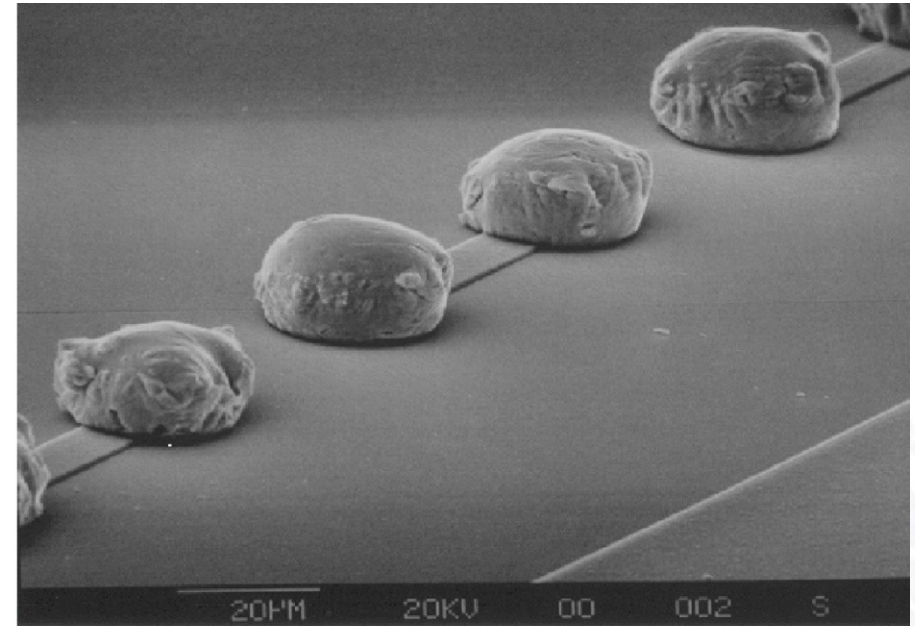


Evaporated Indium

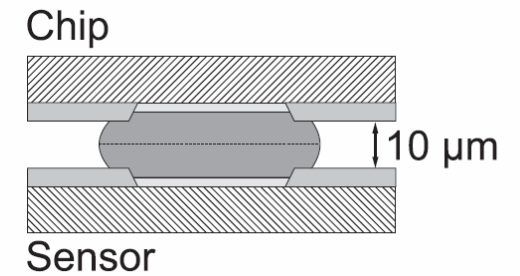
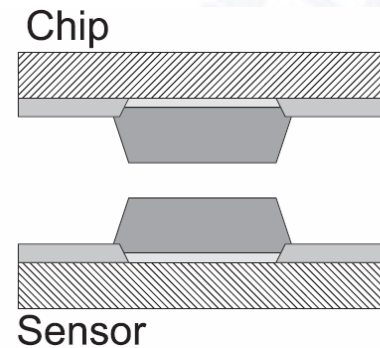


Wet Lift off process

Alenia Marconi Systems

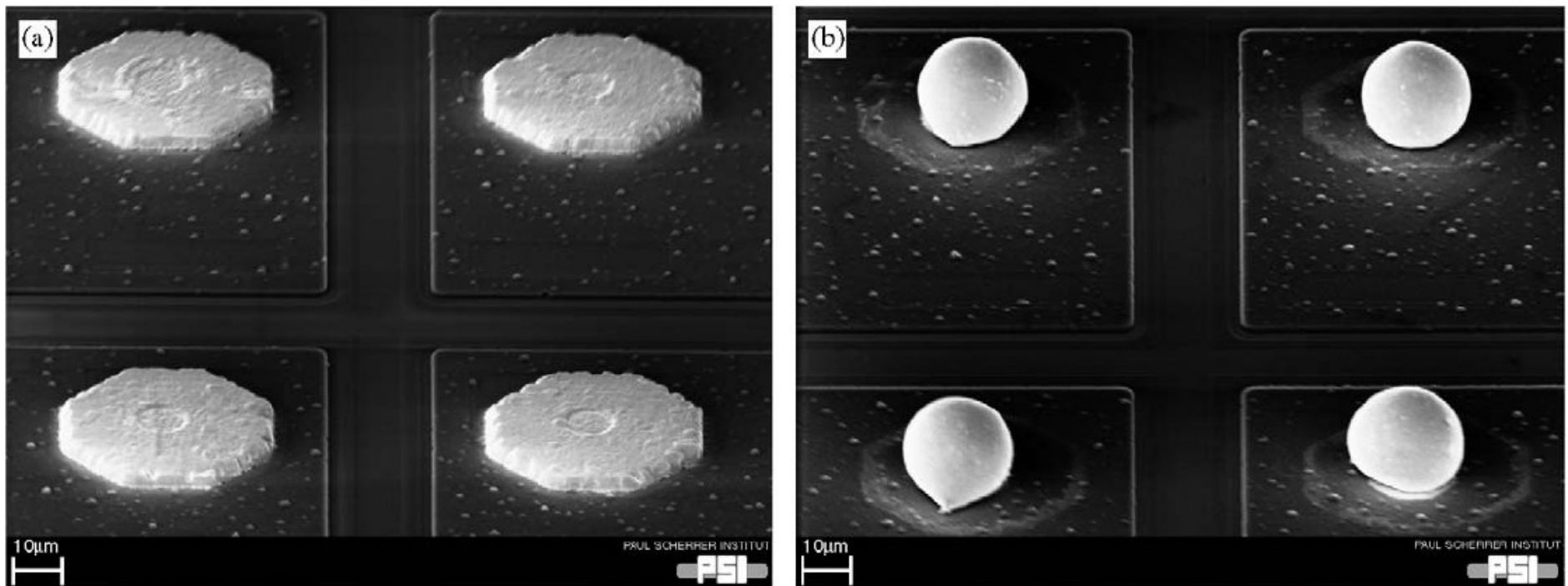


Alenia Marconi Systems, Rome





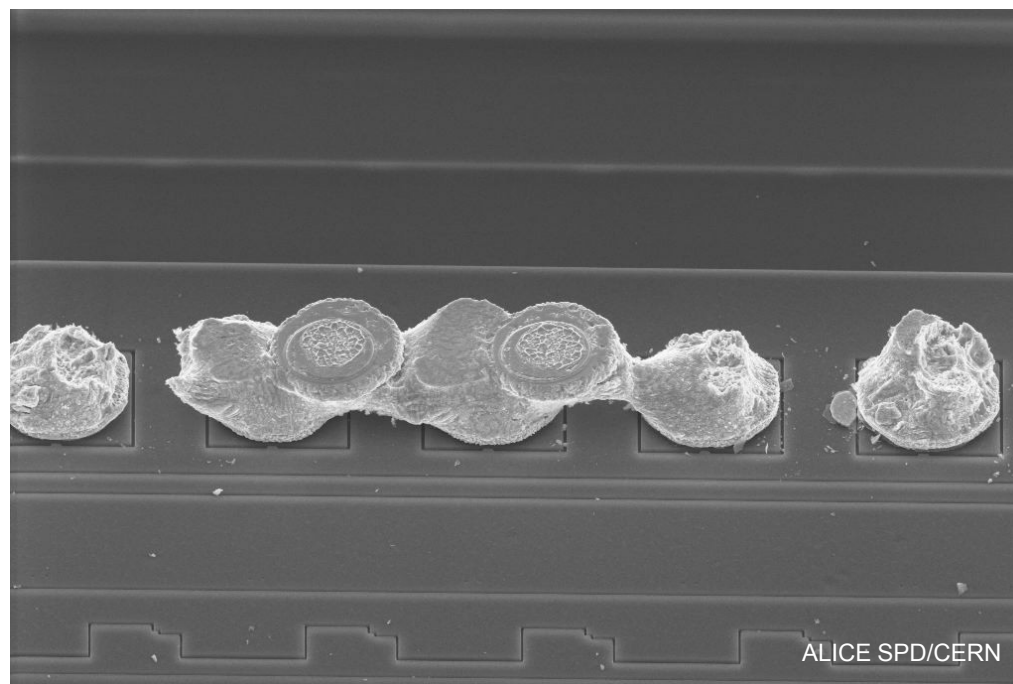
- The standard In process does not include a reflow step
- One worry: small distance between readout chip and sensor could lead to noise injection
- Process used in CMS (pitch 100  $\mu\text{m}$ ): Indium bumps with reflow  
→ distance sensor – readout chip approx. 15  $\mu\text{m}$



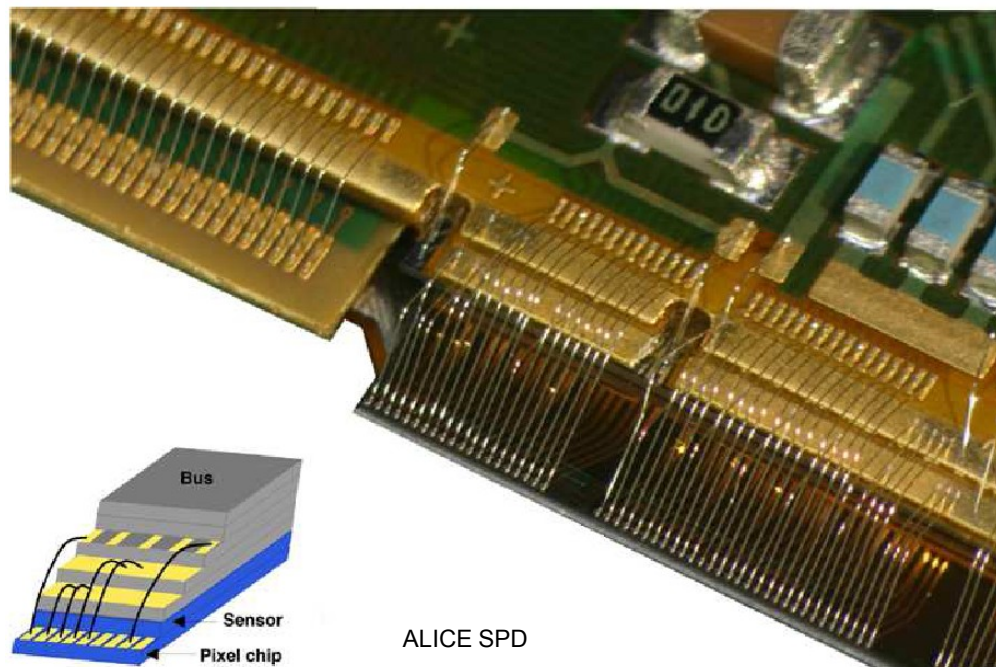
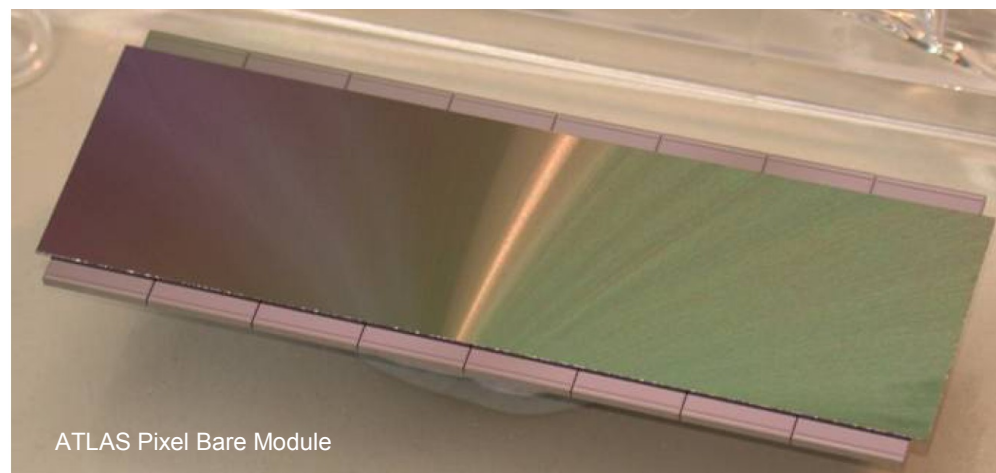
Ch. Broennimann et al., NIM A 565 (2006) 303 – 308



- Many possibilities for failures:
    - Missing or merged bumps  
(single dead pixels)
    - Mechanical defects, from chipped edges to broken wafers  
("best" case: increase of currents, worst case: complete chips lost)
    - Incomplete removal of photo resist  
(if on wire bond pads, no bonding possible)
    - ...
- Careful inspection and testing after all process steps



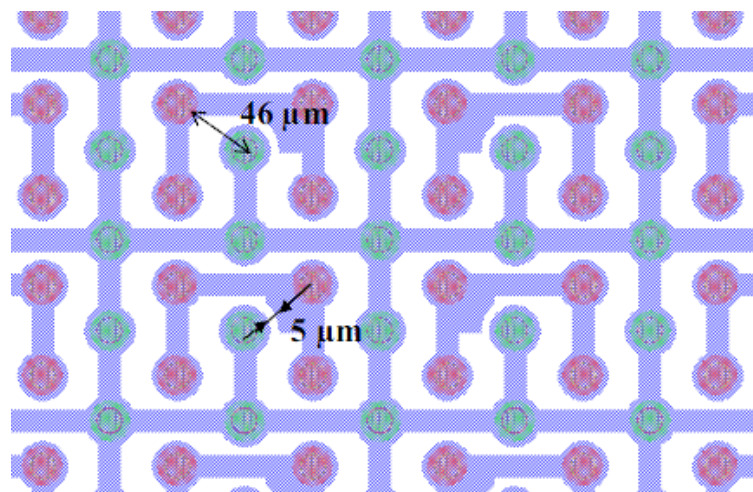
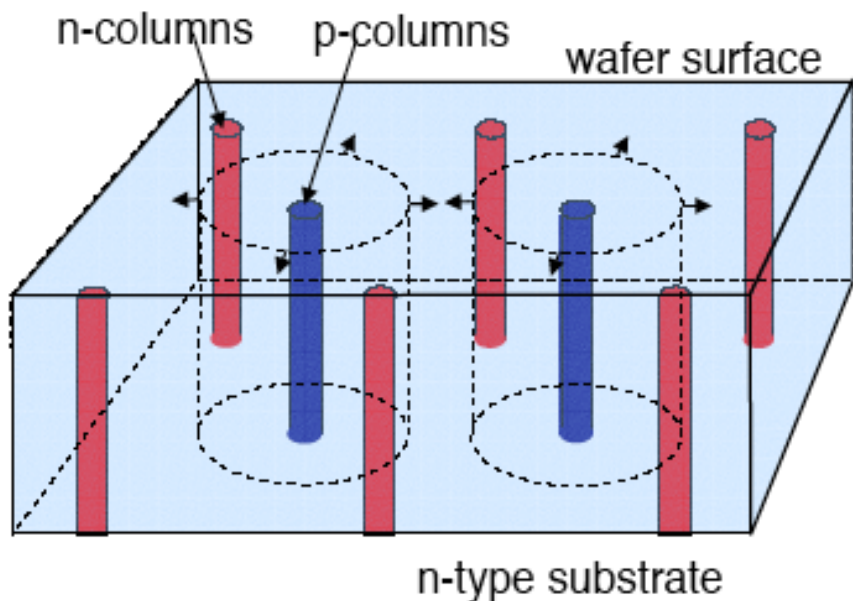
- In most cases signals and power are routed to the FE chip in a flexible PCB on top of the sensor
  - Problem: fast signals, low voltage drop with low material budget
- FE chips have contact pads at their periphery; these are connected with wire bonds to the PCB
  - Thin Al wires, contact is established by ultrasound welding



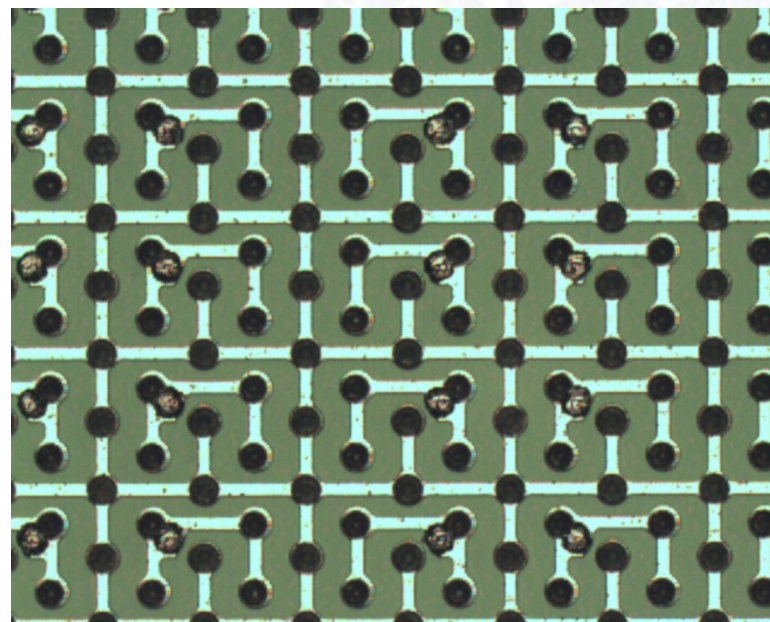
# Other sensors than planar silicon sensors...







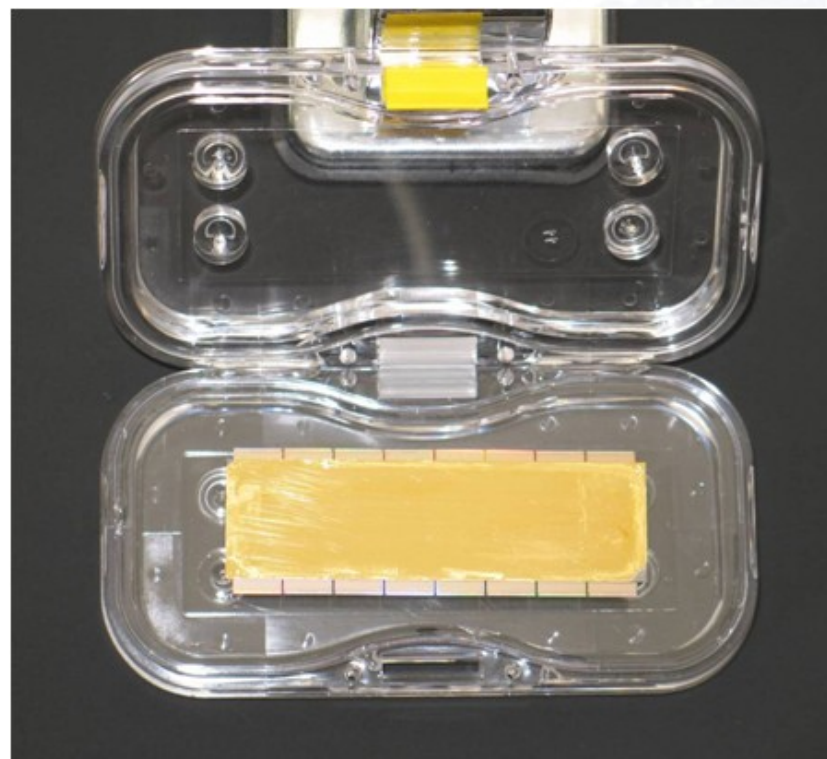
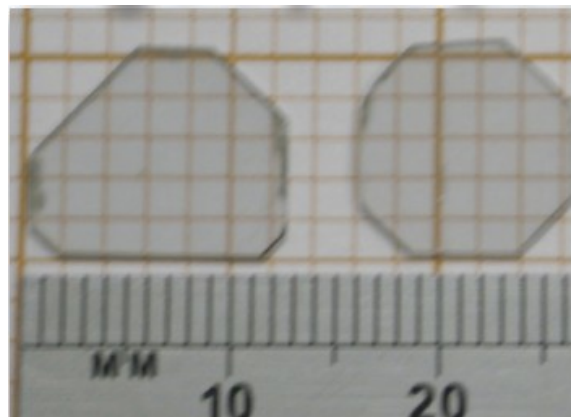
CMS 3D prototype sensor



- Lateral depletion ( $V_{\text{dep}} \leq 10 \text{ V}$ )
- Short charge collection distance
- Pixel metalisation connects several electrodes



- CVD Diamond: high resistivity  
→ no p-n-junction necessary
- Electrodes (pixels/strips/pads) defined by metallisation only
- Room-temperature operation, radiation hard, but signal height depends on diamond quality (charge collection)



# Now: Hands-on...

