Introduction to CMOS Pixel Sensors

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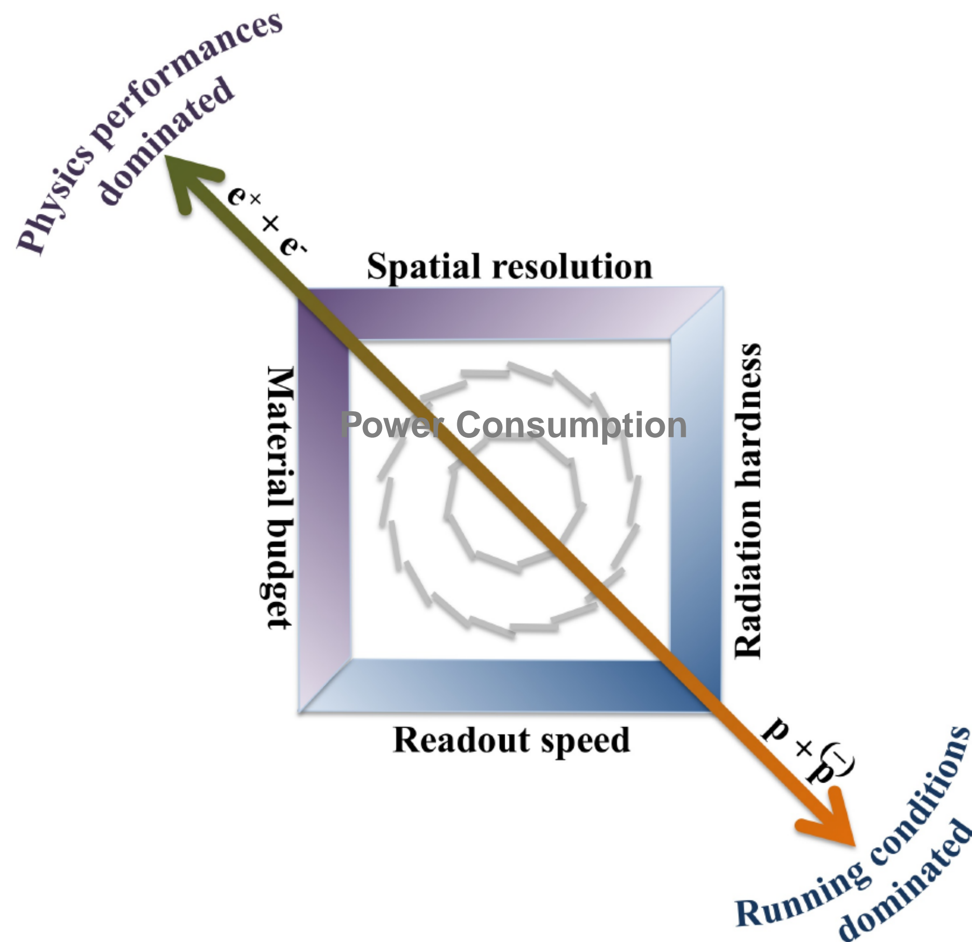
▷ **more information on IPHC Web site: http://www.iphc.cnrs.fr/-CMOS-ILC-.html**

OUTLINE

- Main features of CMOS pixel sensors
  - ▷ motivation ▷ principle: sensing & read-out ▷ limitations ▷ hit characteristics
- Achieved performances
  - ▷ means of evaluation ▷ beam test characterisation ▷ sources of performance deterioration
- Applications
  - ▷ system integration aspects ▷ subatomic physics apparatus
- Outlook
  - ▷ 2D sensors ▷ 3D sensors
- Summary

The Quadrature of the Vertex Detector

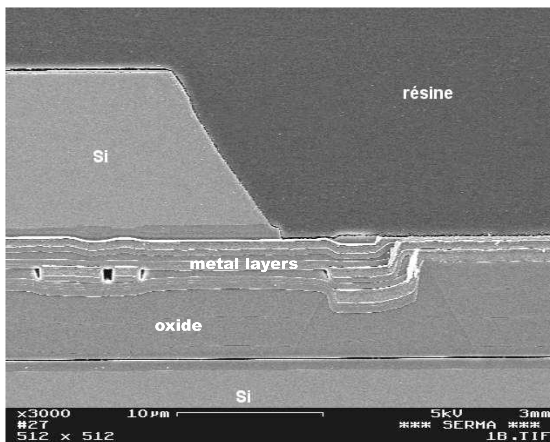


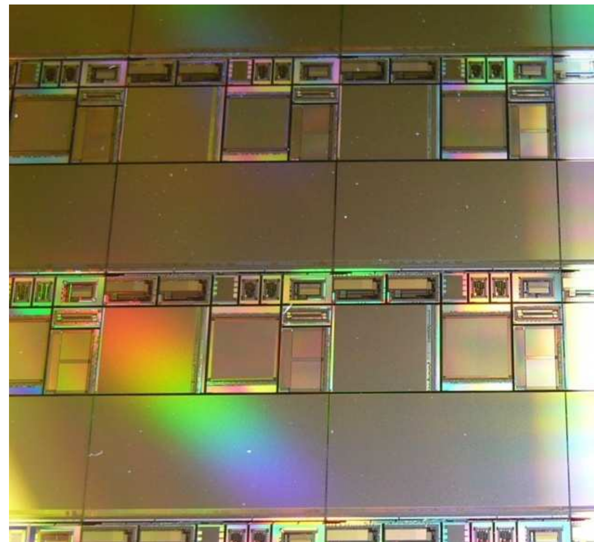
- CMOS pixel sensors offer the perspective of ”combining the extremes” (ultimately !)
- Several labs develop CMOS pixel sensors : Italy (INFN, Univ.), UK (RAL), CERN, France (IPHC, Saclay), USA, ...
- Several experiments chosed/envisage CMOS pixel sensors : STAR (construct), CBM (devt), ALICE (option), SuperB (option), ILC (option), ...

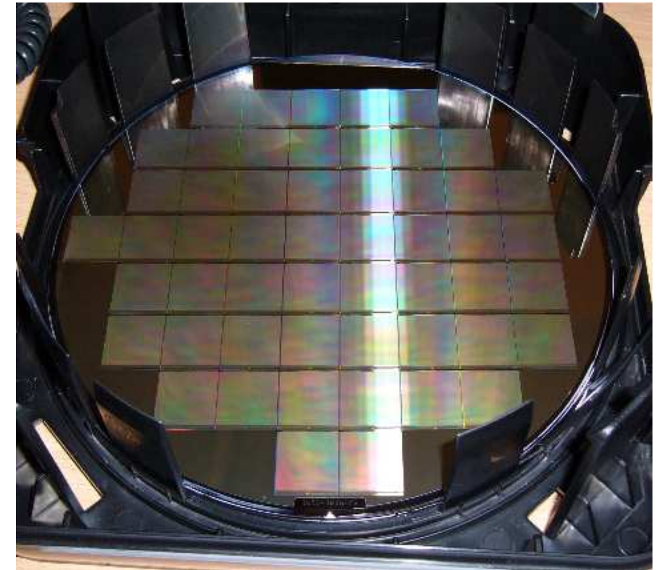
CMOS Technology

- C.M.O.S. $\equiv$ Complementary Metal-Oxide-Semiconductor
- CMOS pixel sensors exploit the fabrication processes used in industry for mass production of integrated circuits:
  - ⁕ micro-processors, micro-controler, RAM, ...
  - ⁕ cell phones, lap tops, cars, ...

- CMOS fabrication mode :
  - ⁕ μcircuit lithography on a substrate
  - ⁕ proceeds through reticules (2x2 cm^2) organised in wafers







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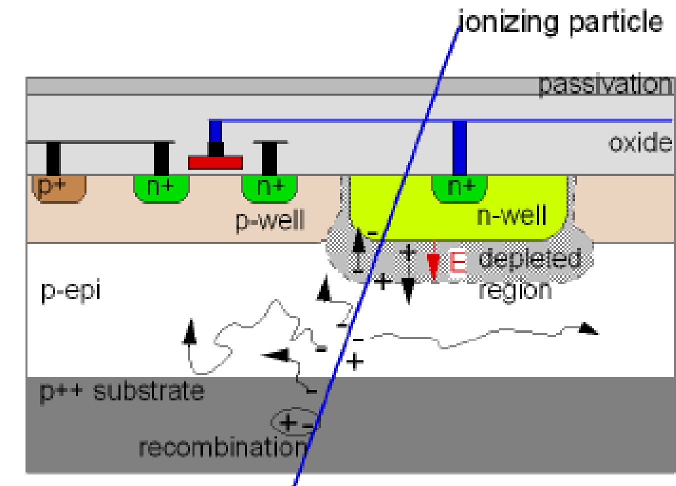
Main Features of CMOS Sensors

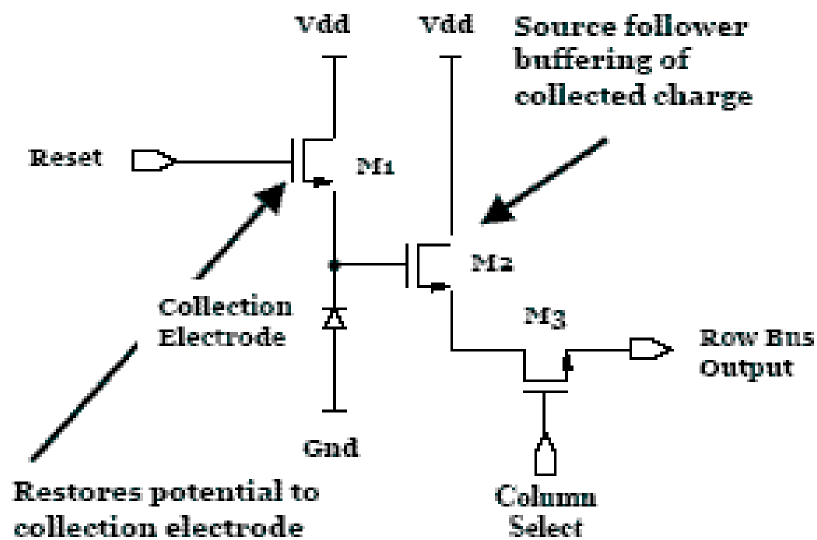


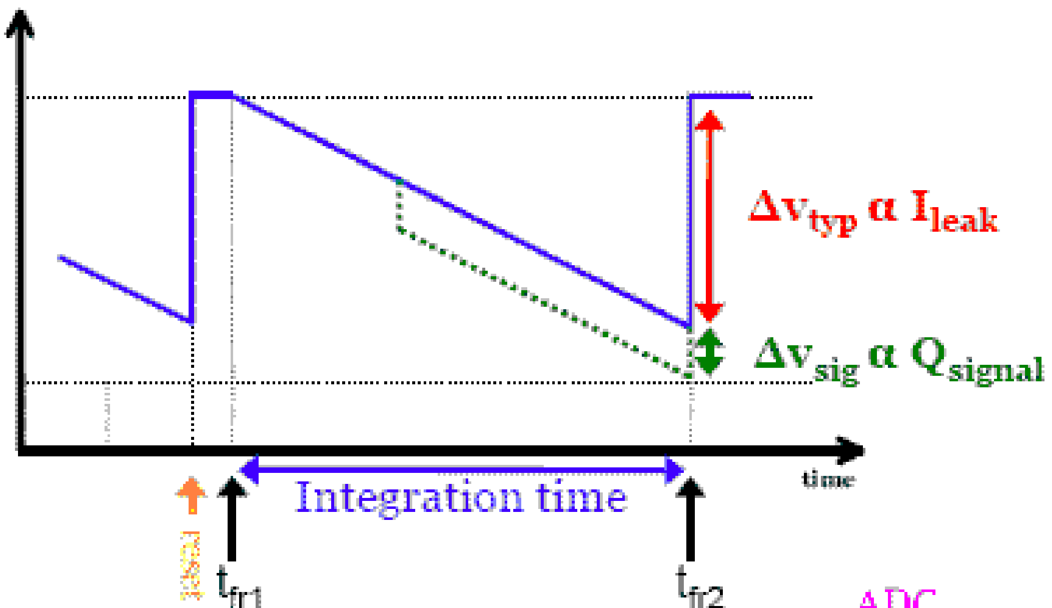
- P-type low-resistivity Si hosting n-type "charge collectors"
  - signal created in epitaxial layer (low doping):
    Q $\sim$ 80 e-h / $\mu m \mapsto$ signal $\lesssim$ 1000 e^-
  - charge sensing through n-well/p-epi junction
  - excess carriers propagate (thermally) to diode
    with help of reflection on boundaries
    with p-well and substrate (high doping)

- Prominent advantages of CMOS sensors:
  - ◇ granularity: pixels of $\lesssim 10 \times 10\ \mu m^2 \Rrightarrow$ high spatial resolution
  - ◇ low mat. budget: sensitive volume $\sim$ 10 - 20 $\mu m \Rrightarrow$ total thickness $\lesssim$ 50 μm
  - ◇ signal processing μcircuits integrated in the sensors $\Rrightarrow$ compacity, high data throughput, flexibility, etc.
  - ◇ other attractive aspects: T_{room} operation, cost, multi-project run frequency, industrial reliability,
    industrial technology devts & evolution, etc.

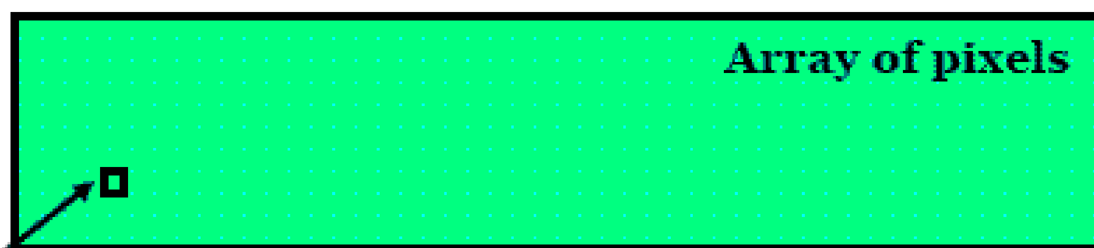
$\triangleright\triangleright\triangleright$ Thinning down to $\sim$ 30 μm permitted

Basic Read-Out Architecture

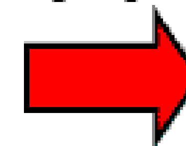




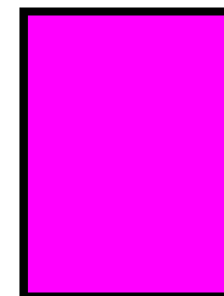
ADC



High-speed



Analog read-out



& storage

Pixel Array: Column select – ganged row read

Low power – only significant draw at readout edge

CMOS Pixel Sensors: Read-Out Architectures

- **Signal sensing and read-out are decoupled :**

  ⋇ signal sensing (charge collection) is continuous (no dead time)

  $\Rrightarrow$ signal read-out may be performed in various ways, independently of charge collection

- **Signal processing alternatives :**

  ⋇ self-triggered : only fired pixels are (randomly) read-out $\equiv$ hybrid pixels

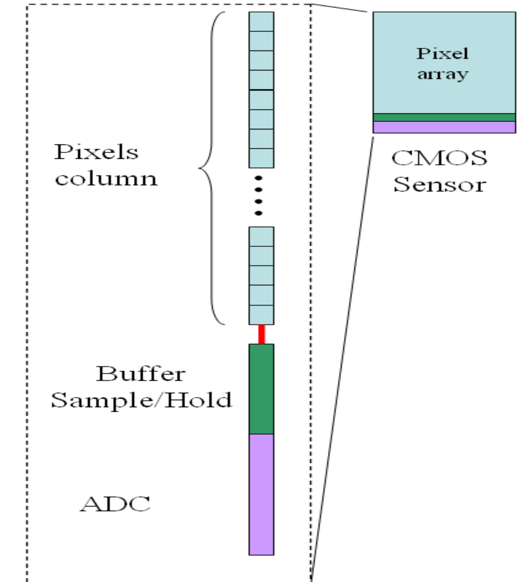
  ⋇ rolling shutter (less power consumption) : read-out of all pixels,

  followed by sparsification outside of sensitive area ▷▷▷▷

  ⋇ snap-shot : requires 2 consecutive read-outs,

  with 1 used for average noise subtraction

  (rather suited to light imaging due to $\sim$ 50 % dead time)

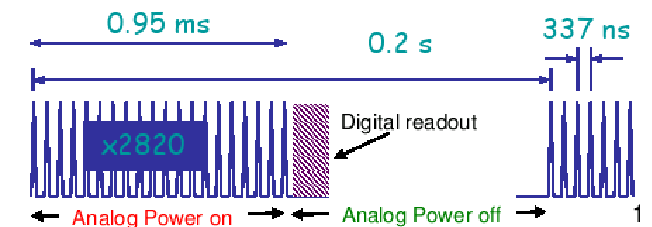


- **Signal transfer alternatives :**

  ⋇ continuous : permanent output to outside world

  ⋇ intermittent : signal stored on chip until read-out sign is provided

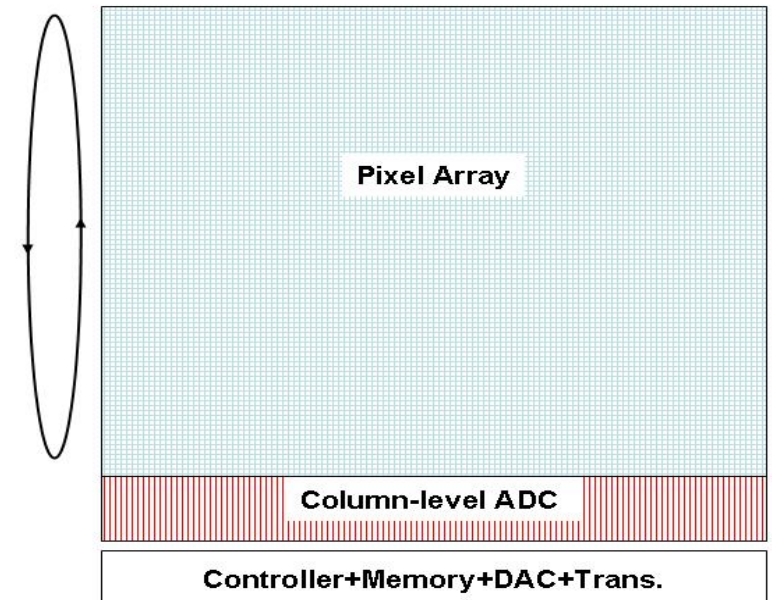
  $\hookrightarrow$ event based trigger or beam-time structure (ILC) ▷▷▷



Overview of Rolling Shutter Architecture

- **Sensor organisation:**
  - ⋇ Signal sensing and analog processing in pixel array
  - ⋇ Mixed and Digital circuitry integrated in chip periphery
  - ⋇ Read-out in rolling shutter mode

    (pixels grouped in columns read-out in //)



- **Main consequences:**
  - ⋇ **Read-out speed :**

    $\equiv$ integration time

    $\equiv$ nb of pixels $\times$ pixel read-out time (O(100 ns))

  - ⋇ **Power consumption :**

    limited inside the pixel array to the row being read out

  - ⋇ **Material budget :**

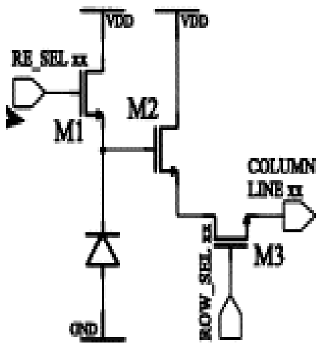
    peripheral band(s) for mixed+digital circuitry, insensitive to impinging particles ($\sim$ 10 % of chip surface)

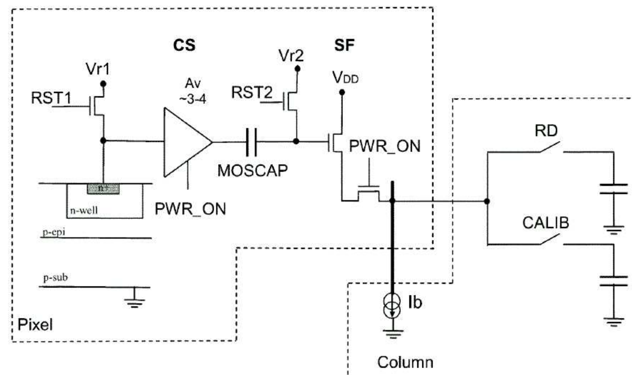
  - ⋇ **Time stamp :**

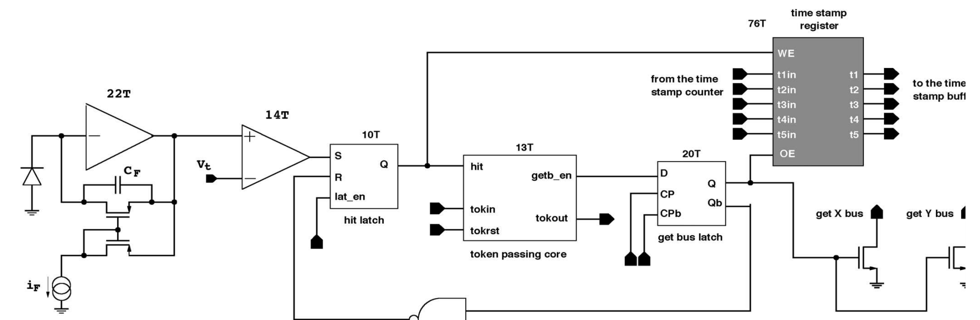
    each row corresponds to a specific time intervalle $\Rrightarrow$ adapt track reconstruction code

- **Main sensing and read-out micro-circuit elements**
  - ⋇ in-pixel conversion of charge into electrical signal (e.g. voltage) with average noise subtraction
  - ⋇ signal discrimination (in perspective of zero-suppression)
  - ⋇ discriminator output encoding (sparsification with charge encoding)
  - ⋇ data transmission logic $\rightarrowtail$ connection with the outside world

- **In-pixel μcircuitry :**







basic read-out — pre-amp + <noise> subtraction — pre-amp + shaper + discriminator

data reduction: outside chip — chip periphery — inside pixel

Limitations of the Technology

- **Very thin sensitive volume**
  - $\Rrightarrow$ impact on signal magnitude (mV !)
    - $\Rrightarrow$ very low noise FEE required

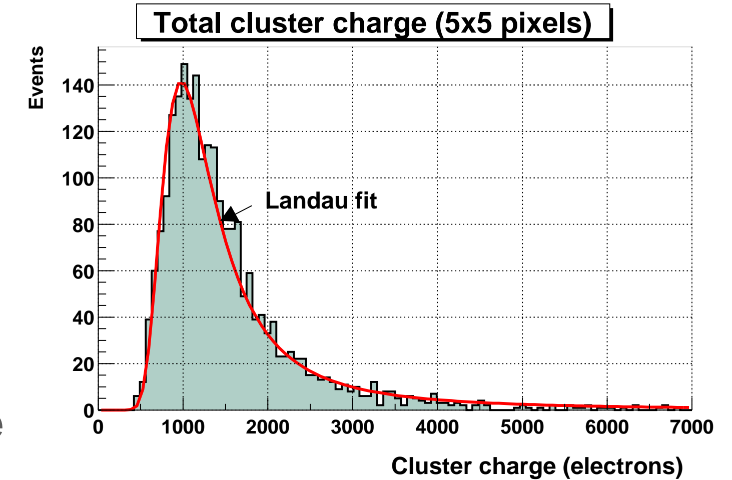
- **Sensitive volume almost undepleted**
  - $\Rrightarrow$ impact on radiation tolerance & speed
    - ▷ **tendency :** high-resistivity epitaxial layer $\Rrightarrow$ improved radiation tolerance

- **Commercial fabrication**
  - $\Rrightarrow$ fabrication parametres (doping profile $\longrightarrow$ epitaxial layer, number of metal layers, etc.) not optimal for charged particle detection :
    - ⋇ real potential of CMOS pixel sensors not exploited
    - ⋇ choice of process often driven by epitaxial layer characteristics, at the expense of the FEE circuitry parametres (feature size, nb of Metal Layers)

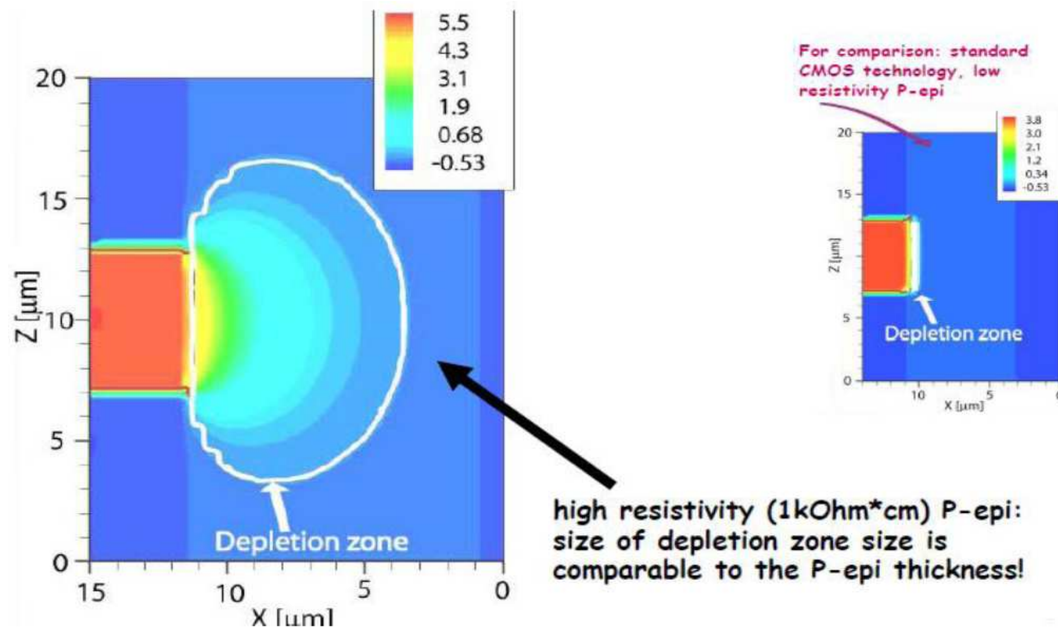
- **Use of P-MOS transistors inside pixel array restricted in most processes**
  - $\Rrightarrow$ limited signal processing functionnalities inside pixels (most performed on sensor periphery)
    - ▷ **tendency :** buried n-well techno. $\Rrightarrow$ allows use of P-MOS transistors (watch charge coll. eff. !)

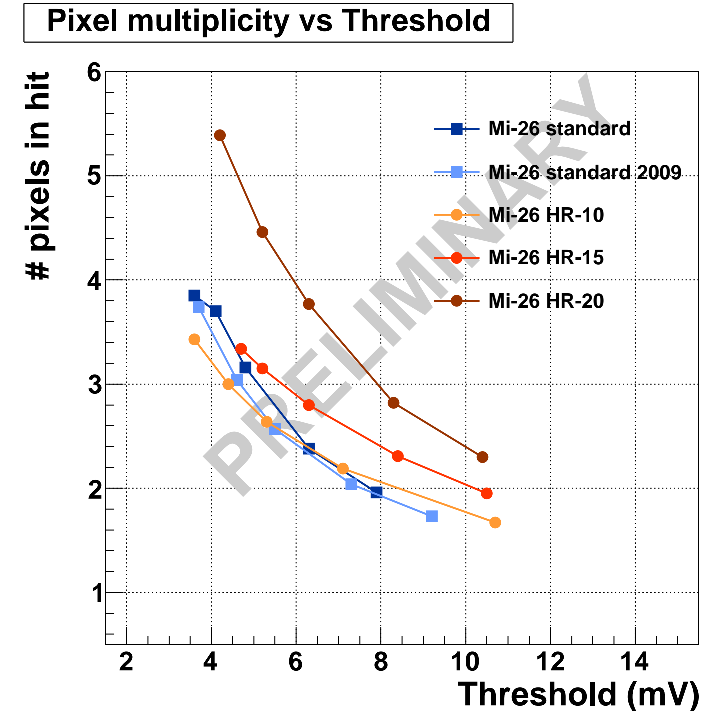
Hit Characteristics

- **Standard processes : charges diffuse thermally**
  - ⋇ $\lesssim 10^3$ e^- shared among $\sim$ 10-15 pixels per cluster
  - ⋇ typically $\lesssim$ 200/300 e^- on seed pixel



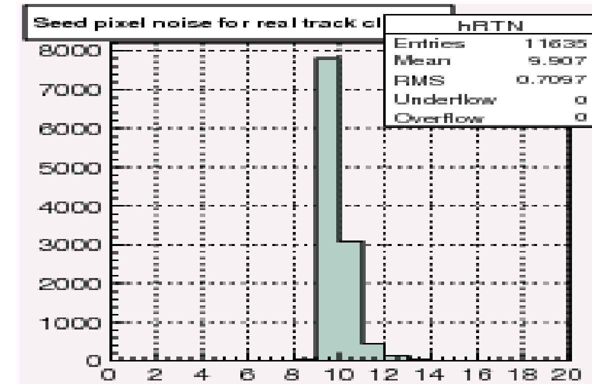
- **High-resistivity epitaxial layer : larger charge sensing volume**
  - ⋇ less diffusion $\Rrightarrow$ less pixels/cluster
  - ⋇ larger charge collected/pixel $\Rrightarrow$ higher SNR

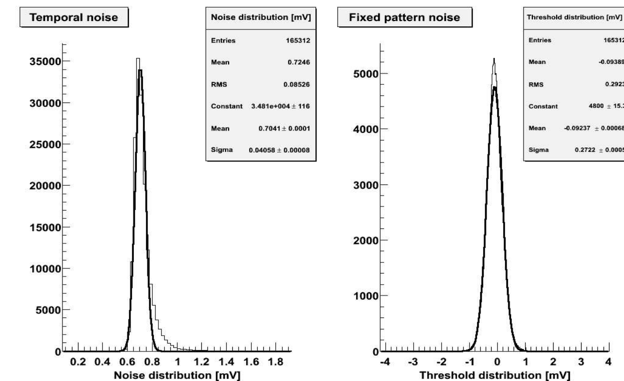




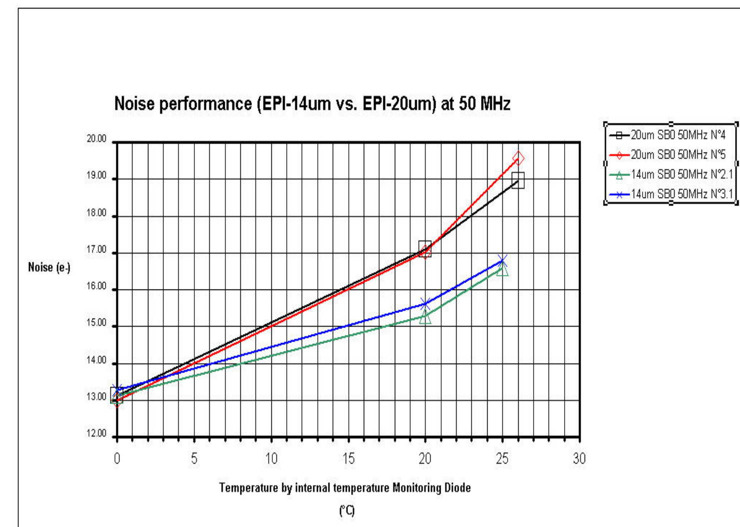
- # Sensor Noise: Sources, Reduction Strategies

- **Main Sources :**
  - ⁕ in pixel : sensing diode capacitance ▷▷▷
  - ⁕ in pixel : leakage current collected by sensing diode ▷▷
  - ⁕ outside pixel : signal processing micro-circuits



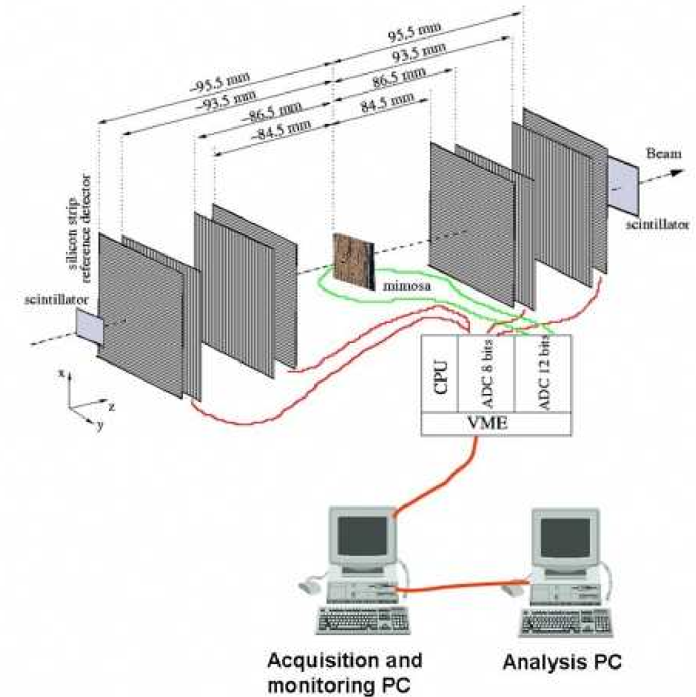


- **Tricks to minimise the noise :**
  - ⁕ maximal amplification inside pixel
    - ⇛ minimises the impact of the noise ▷▷▷ of the signal processing micro-circuits
  - ⁕ operate chip with short integration time
    - ⇛ minimises the integrated leakage current
  - ⁕ operate chip at low temperature ▷▷▷
    - ⇛ minimises the thermal noise

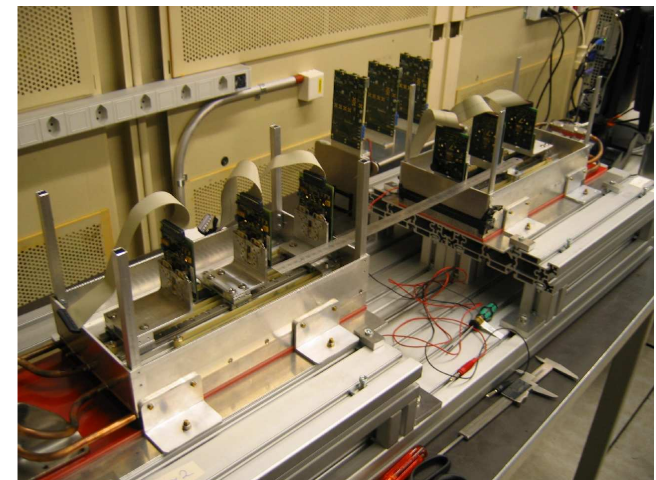


M.I.P. Detection Performance Evaluation

- **Laboratory :**
  - ⋇ test steering & read-out functionalities (e.g. pattern generator)
  - ⋇ evaluate charge collection efficiency & noise (^{55}Fe)
  - ⋇ assess charge-to-voltage conversion factor (^{55}Fe)
  - ⋇ estimate "m.i.p." detection efficiency with β (^{106}Ru)



- **M.I.P. beam :**
  - ⋇ typically $\sim$ 100 GeV/c π^- at CERN-SPS
    - $\Rrightarrow$ minimise multiple scattering
  - ⋇ install chip to test inside beam telescope (EUDET BT)
  - ⋇ determine :
    - ○ detection efficiency (and SNR)
    - ○ fake hit rate (and noise)
    - ○ single point resolution



CMOS Pixel Sensors: State of the Art

CMOS 0.35 µm OPTO technology
Chip size : 13.7 x 21.5 mm²

- Pixel array: 576 x 1152, pitch: 18.4 µm
- Active area: ~10.6 x 21.2 mm²
- In each pixel:
  - Amplification
  - CDS (Correlated Double Sampling)

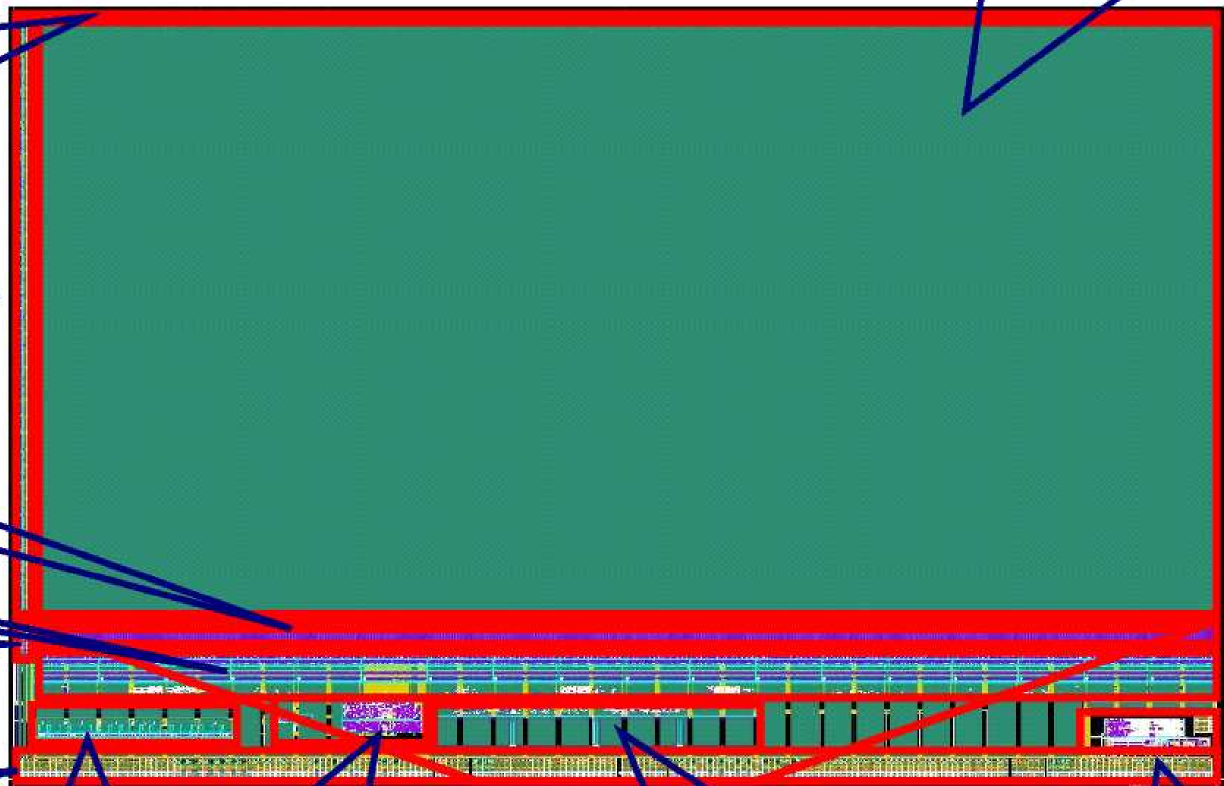
- Testability: several test points implemented all along readout path
  - Pixels out (analogue)
  - Discriminators
  - Zero suppression
  - Data transmission

- Row sequencer
- Width: ~350 µm

- 1152 column-level discriminators
  - offset compensated high gain preamplifier followed by latch

- Zero suppression logic

- Reference Voltages Buffering for 1152 discriminators



- I/O Pads
  Power supply Pads
  Circuit control Pads
  LVDS Tx & Rx

- Current Ref.
- Bias DACs

- Readout controller
- JTAG controller

- Memory management
- Memory IP blocks

- PLL, 8b/10b optional

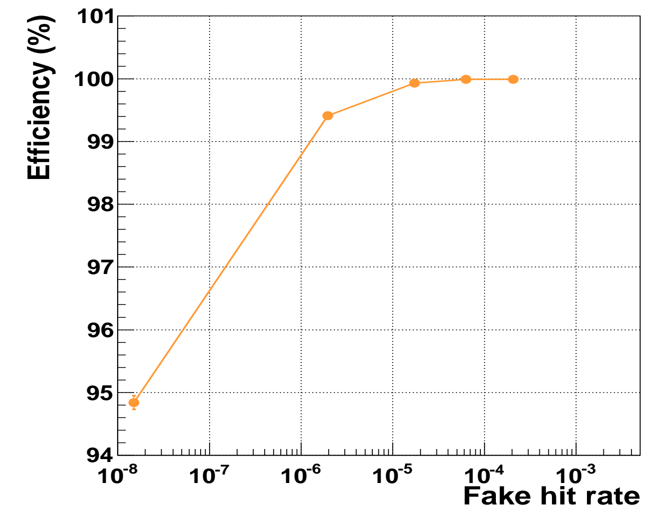
courtesy of Ch. Hu-Guo / TWEPP-2010

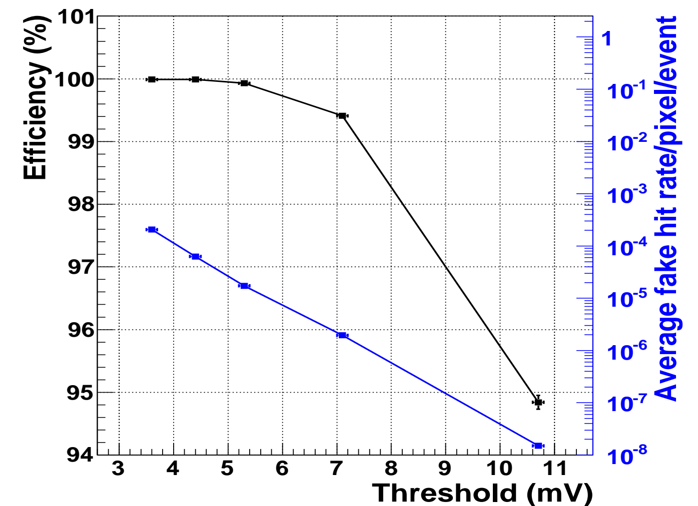
M.I.P. Detection Efficiency & Fake Hit Rate

- **Motivation :** find a sensor working point with high detection efficiency and marginal contamination by noise fluctuations (fake hits)

- **Detection efficiency**
  - ⋇ fraction of tracks reconstructed in telescope which are also reconstructed in the sensor
  - ⋇ study as function of discriminator threshold
  - ⋇ a high threshold may harm detection efficiency

- **Fake hit rate**
  - ⋇ fraction of noise fluctuations which pass the discriminator threshold
  - ⋇ study as a function of discriminator threshold
  - ⋇ a high threshold is best to keep fake rate marginal (typically $\lesssim 10^{-3/-4}$)



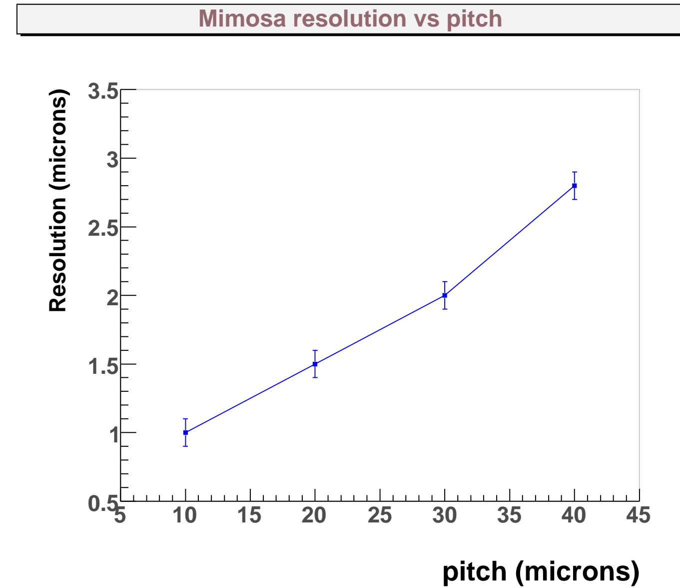


Spatial Resolution

- **Compare position of impact on sensor surface predicted with BT to hit reconstructed with sensor under test:**
  clusters reconstructed with eta-function,
  exploiting charge sharing between pixels

- **Impact of pixel pitch (analog output):**

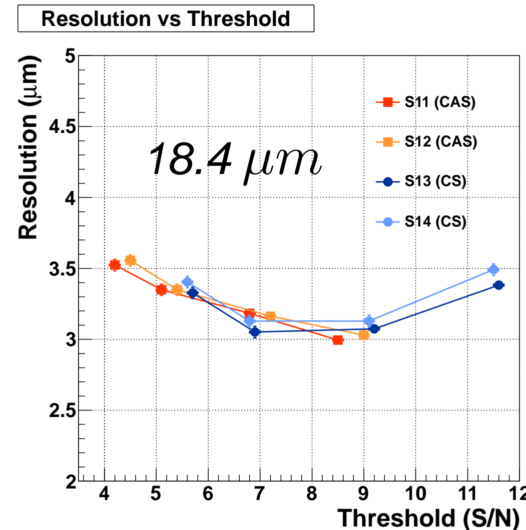
  $\sigma_{\mathbf{sp}} \sim \mathbf{1}\ \boldsymbol{\mu}\mathbf{m}$ (10 μm pitch) $\longmapsto \lesssim \mathbf{3}\ \boldsymbol{\mu}\mathbf{m}$ (40 μm pitch)

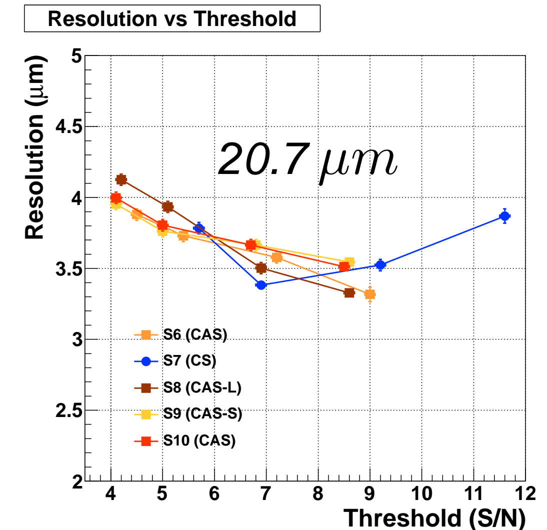


- **Impact of charge encoding resolution :**

  ▷ ex. of 20 μm pitch $\Rrightarrow$ σ_{sp}^{digi} = pitch/$\sqrt{12} \sim$ 5.7 μm

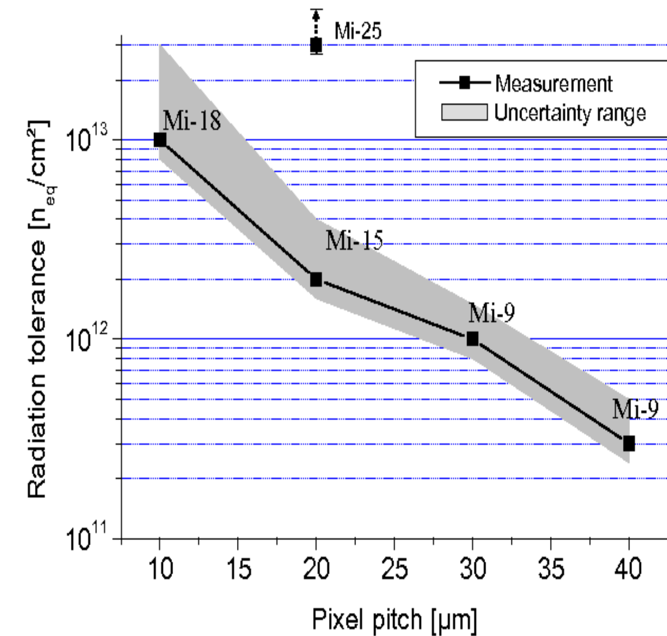
Nb of bits	12	3-4	1
Data	*measured*	*reprocessed*	*measured*
σ_{sp}	$\lesssim 1.5\mu m$	$\lesssim 2\mu m$	$\lesssim 3.5\mu m$

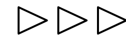


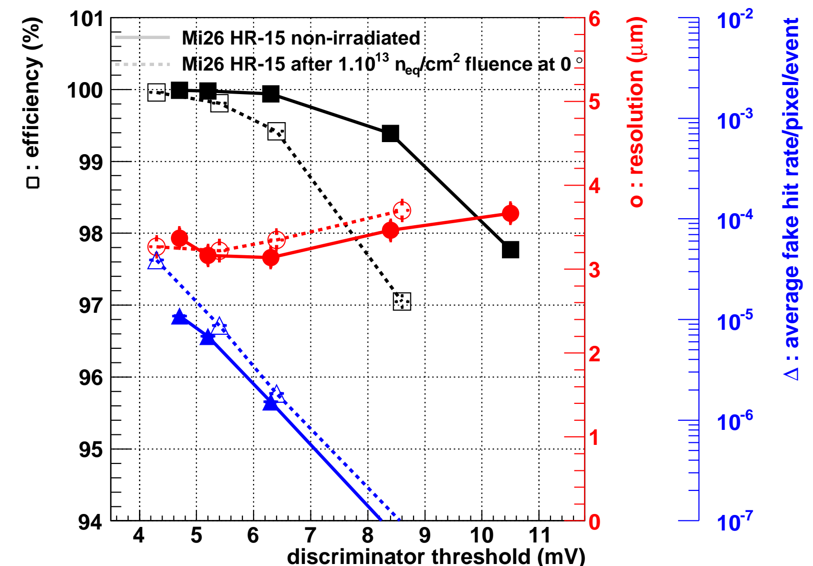


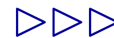
Radiation Tolerance

- **Introductory remarks :**
  - ⋇ still evolving (csq of CMOS industry process param. evolution)
  - ⋇ CMOS technology expected to tolerate high ionising radiation doses ($>>$ 10 MRad), in particular at $< 0^\circ$C and short t_{integ}
  - ⋇ main a priori concern : NON-ionising radiation (in absence of thick depleted sensitive volume)



- **Influence of pixel pitch :** 
  - ⋇ fig: all measts done with low resistivity epitaxial layer, but 1
  - $\Rrightarrow$ high density sensing diodes ($\equiv$ small pitch) improves non-ionising radiation tolerance



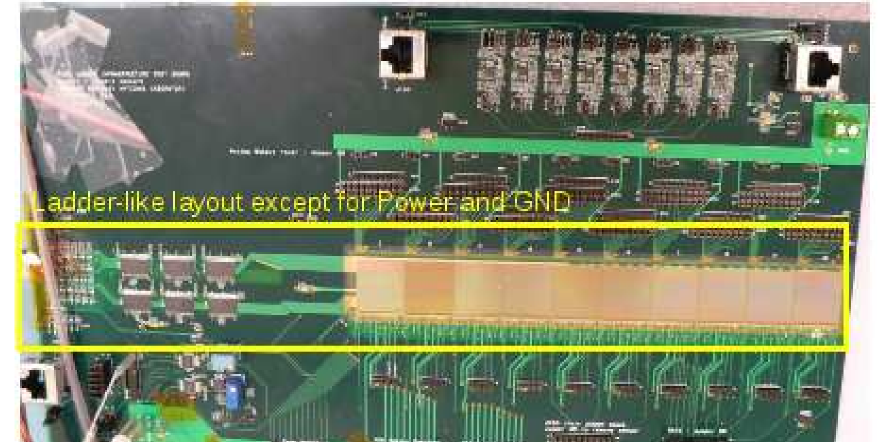
- **Influence of epitaxial layer resistivity :**
  - ⋇ ex: 400 $\Omega \cdot cm$ & O(1)V depletion voltage 
  - ⋇ trend : $\gtrsim$ 1 $k\Omega \cdot cm$ & $>>$ 10 V

$\Rrightarrow$ **tolerance to $\gtrsim 10^{14-15}$ n_{eq}/cm^2 not excluded**

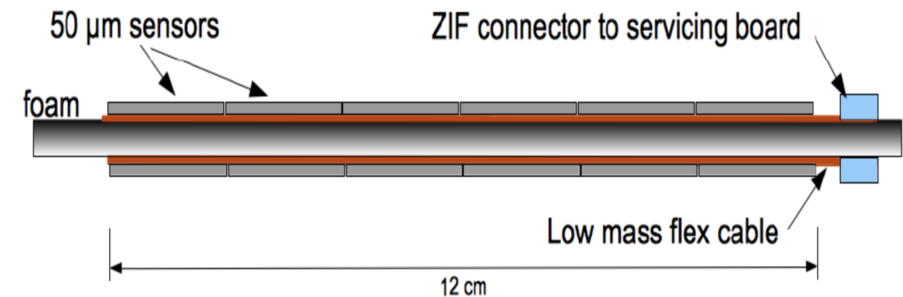
Sensor Integration in Ultra Light Devices

- **"Useful" sensor thickness $\lesssim$ 30 μm** $\Rightarrow$ *opens new possibilities w.r.t. thicker sensors*
  - ▷ *coarse thickness of sensors (e.g. EUDET BT) is 50 μm*

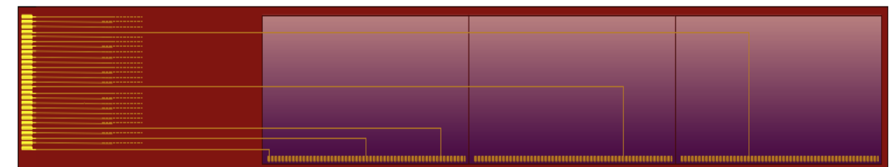
- **STAR-PXL ladder** (room temperature, single-end supported)**:**
  - ⋇ total material budget $\simeq$ 0.37 % X_0 :
    - 50 μm thin sensors $\simeq$ 0.05 % X_0
    - flexible cable $\simeq$ 0.07 % X_0
    - mechanical support $\simeq$ 0.2 % X_0
    - adhesive, etc. $\simeq$ 0.05 % X_0



- **Double-sided ladders with $\sim$ 0.2-0.3 % X_0 :**
  - $\Rrightarrow$ manifold bonus : compactness, alignment, redundancy, pointing accuracy (shallow angle), fake hit rejection, etc.

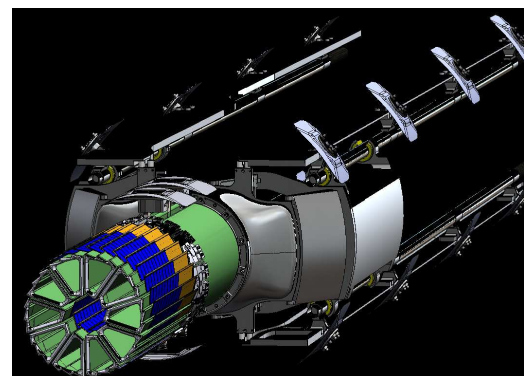


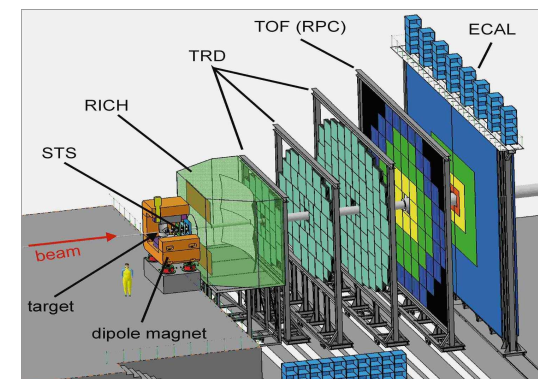
- **Unsupported & flexible ladders with $\lesssim$ 0.15 % X_0**
  - $\Rrightarrow$ 30 μm thin CMOS sensors mounted on thin cable & embedded in thin polyimide $\longrightarrow$ suited to beam pipe ?



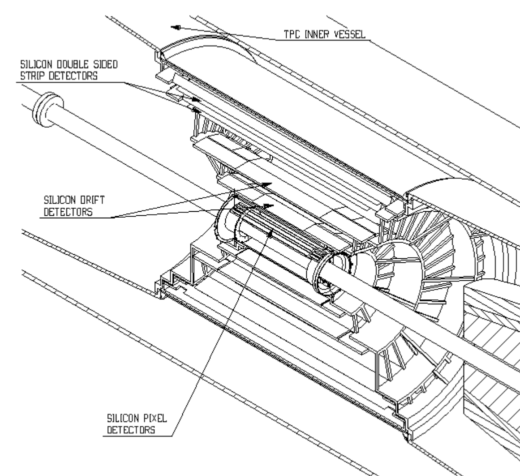
Applications in Subatomic Physics

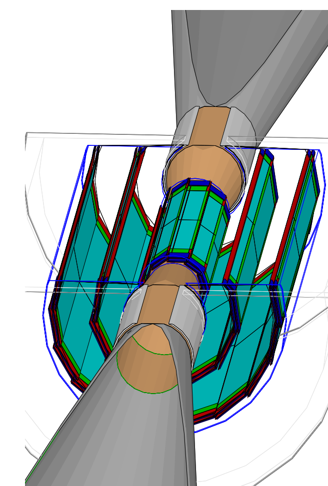
- **Beam telescopes :**
  - ⋇ EUDET (FP-6 / 2006-2010) : 6 planes with 1×2 cm^2 sensors
  - ⋇ AIDA (FP-7 / 2011-2015) : $\geq$ 3 planes with 5×5 cm^2 sensors





- **Vertex detectors :**
  - ⋇ STAR-PXL at RHIC : 2 layers
  - ⋇ CBM-MVD at FAIR/GSI : 2-3 stations
  - ⋇ option for ALICE-ITS at LHC: Layer-0 + ...
  - ⋇ option for Vertex detector at SuperB fact. : L0 + ...
  - ⋇ option for ILD-VTX at ILC : 3 double-layers





- **Trackers** ("large pitch") **:**
  - ⋇ BES-III at BEPC
  - ⋇ in general : trackers surrounding vertex detectors

- **EM calorimetres :** SiW calorimetre

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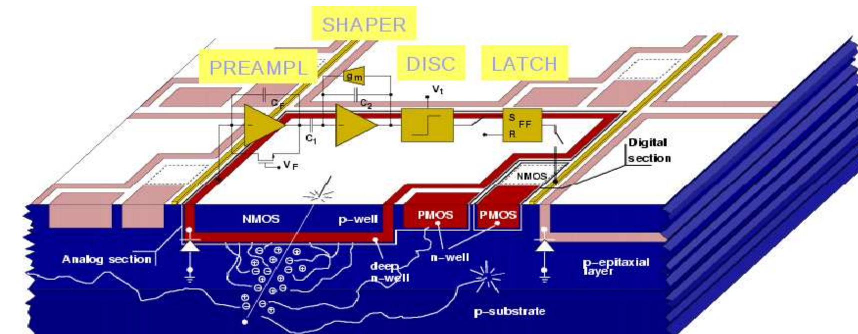
Perspectives: Fast 2D sensors

- **Evolve towards feature size $<<$ 0.35 μm :**
  - ⋇ μcircuits : smaller transistors, more Metal Layers, ...
  - ⋇ sensing : triple well, depleted sensitive volume, ...
- **Benefits :**
  - ⋇ faster read-out $\Rrightarrow$ improved time resolution
  - ⋇ higher μcircuit density $\Rrightarrow$ higher data reduction capability
  - ⋇ thinner gates, depletion $\Rrightarrow$ improved radiation tolerance
- **On-going R&D (examples) :**
  - ⋇ *APSEL* sensor (130nm) for SuperB & ILC Vx Det. :
    - ○ in-pixel pre-amp + shaping + discri. ▷▷▷
    - ○ sensing through buried n-well
    - ○ shallow n-well hosting P-MOS T
  - ⋇ *LePIX* project (90 nm) for sLHC trackers :
    - ○ large pixels connected individually to peripheral FEE (fast !)
    - ○ high-resistivity substrate, high depletion voltage



- **Main limitations :**
  - ⋇ VDSM technologies not optimised for analog μcircuits (low V !) $\Rrightarrow$ reliability
  - ⋇ conflict between speed (e.g. 10 ns) and granularity (e.g. 20$\times$20 μm^2 pixels)

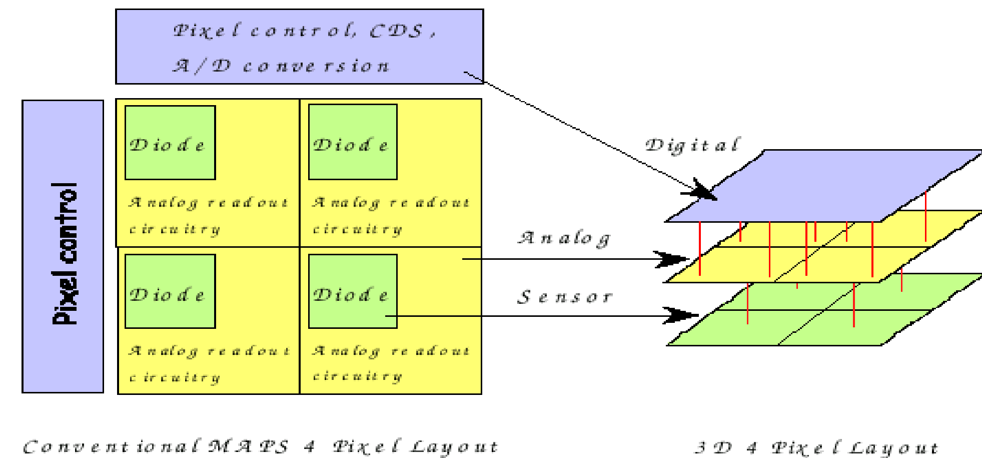
$\Rrightarrow$ **Natural trend : chip stacking**

Using 3DIT to reach Ultimate CMOS Sensor Performances

- **3D Integration Technologies** allow integrating high density signal processing μcircuits inside **small** pixels by stacking ($\sim$ 10 μm) thin tiers interconnected at pixel level

- **3DIT are expected to be particularly beneficial for CMOS sensors :**
  - ⋇ combine different fab. processes $\Rrightarrow$ chose best one for each tier/functionnality
  - ⋇ alleviate constraints on peripheral circuitry and on transistor type inside pixel, etc.

- **Split signal collection and processing functionnalities :**
  - ⋇ *Tier-1: charge sensing*
  - ⋇ *Tier-2: analog-mixed μcircuits*
  - ⋇ *Tier-3: digital μcircuits*



- **The path to nominal exploitation of CMOS pixel potential :**
  - ⋇ fully depleted 10-20 μm thick epitaxy $\Rrightarrow$ $\lesssim$ 5 ns collection time, rad. hardness $>$ Hybrid Pix. Sensors ???
  - ⋇ FEE with $\lesssim$ 10 ns time resolution $\rightarrowtail$ solution for CLIC & HL-LHC specifications ???

- **3DIC $\equiv$ consortium coordinated by FermiLab has already produced 1st generation of chips**

SUMMARY

- **CMOS sensor technology is becoming mature for high performance vertexing**
  - ⋇ most relevant for specifications governed by granularity, material budget, power consumption, ...
  - ⋇ excellent performance record with beam telescopes (e.g. EUDET project)
  - ⋇ 1st vertex detector experience will be gained with STAR-PXL, starting data taking in $\sim$ 2 years
  - ⋇ new generation of sensors under development for experiments $>$ 2015 (including trackers & calo.)
- **Technology full potential still far from being exploited**

  (despite improvement due to high-resistivity epitaxial layer processes)
- **Evolution of industry opens the door to 2 "natural" steps**

  towards the "ultimate" performances of the technology :
  - ⋇ fast 2D sensors based on VDSM CMOS technologies may allow for $\lesssim$ O(1) μs, $>>$ 10 MRad
  - ⋇ 3D chips are expected to "exhaust" the technology potential, but there is a long way to go

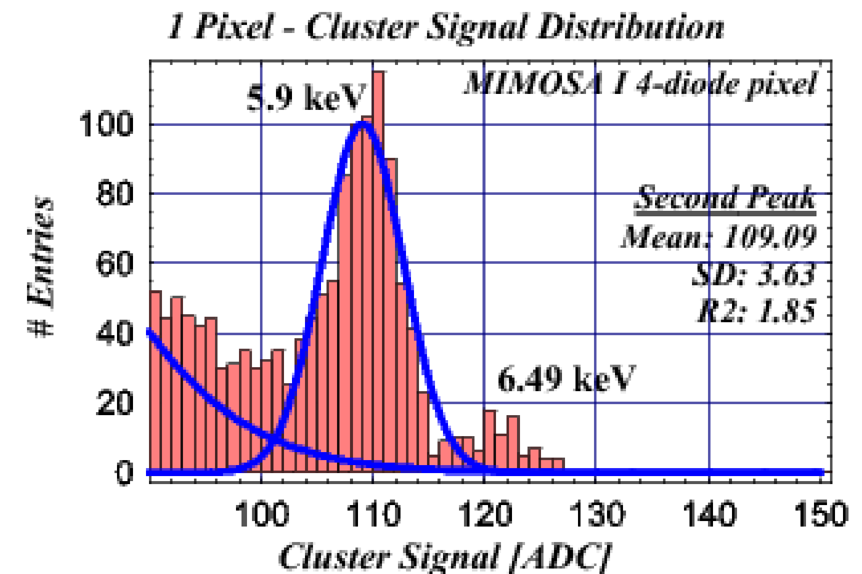
$\Rrightarrow$ may lead to fast & rad. hard devices suited to sLHC & CLIC

Calibration of Charge-to-Voltage Conversion Factor

- **Goal : establish a well defined correspondence between the measured sensor output voltages and the amplitude of the charge collected by each diode**

- **Mean :** use radioactive sources emitting particles with adapted and well defined energy

- **Ex: ^{55}Fe**
  - ⋇ emits X-Rays with 5.9 keV ($\sim$ 90%) or 6.49 keV ($\sim$ 10%)
  - ⋇ X-Rays interact with Si atoms through photo-electric effect
    $\Rrightarrow$ the ejected p.e. carries $\sim$ 100% of the X-Ray energy
    (e^{-} binding energy ...)
  - ⋇ the p.e. creates eh pairs at the expense of $\sim$ 3.6 eV per pair
    $\Rrightarrow$ 5900/3.6 $\simeq$ 1640 eh pairs (6490/3.6 $\simeq$ 1800 eh)



- **Calibration with ^{55}Fe X-Rays**
  - ⋇ a few % of X-Rays impinge sensor near sensing diode
    $\Rrightarrow$ nearly all e^{-} created get collected by nearby sensing diode
  - ⋇ the charge distribution observed on the ADC scale exhibits 2 peaks