Future Developments and Challenges

Simon Kwan
Fermilab

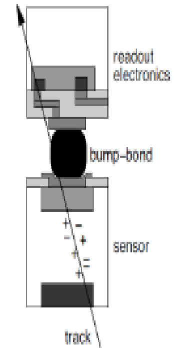
Presented at EDIT 2011 CERN Feb 10 2011

Scope

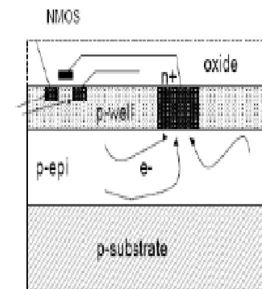
- Will focus on hybrid pixel detector and for the SLHC
- Current status
- Challenges
- R&D effort

Hybrid Pixel Detectors

→ all large detectors (i.e. LHC) so far



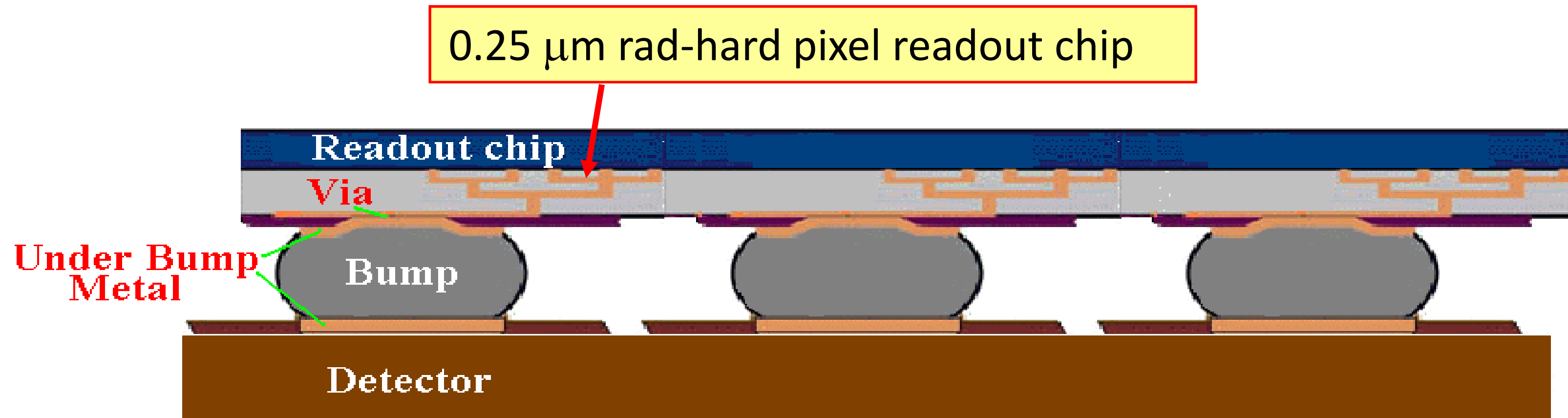
(Semi)-Monolithic Pixel Detectors



→ most new developments except for sLHC
MAPS (epi), MAPS (SOI), DEPFET, 3D-integration

Hybrid Silicon pixel devices

0.25 μm rad-hard pixel readout chip

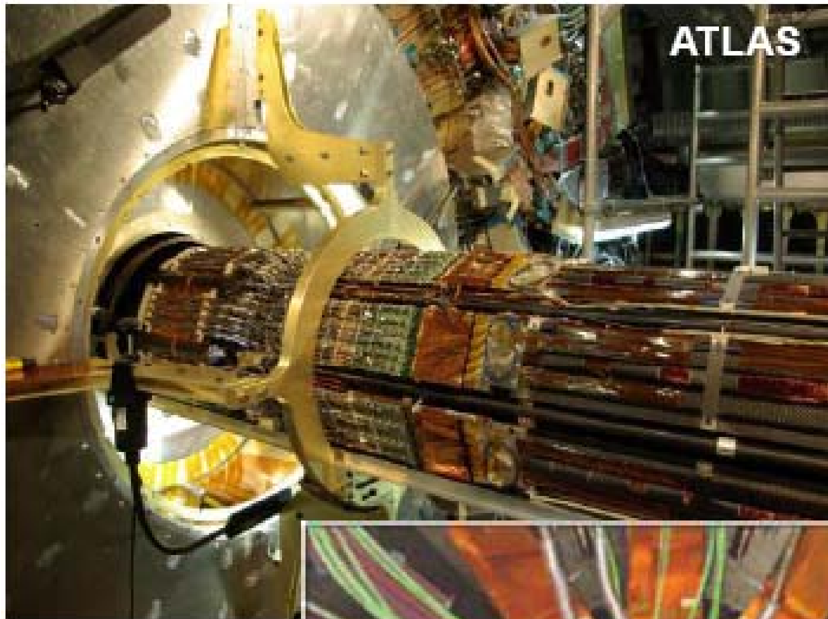


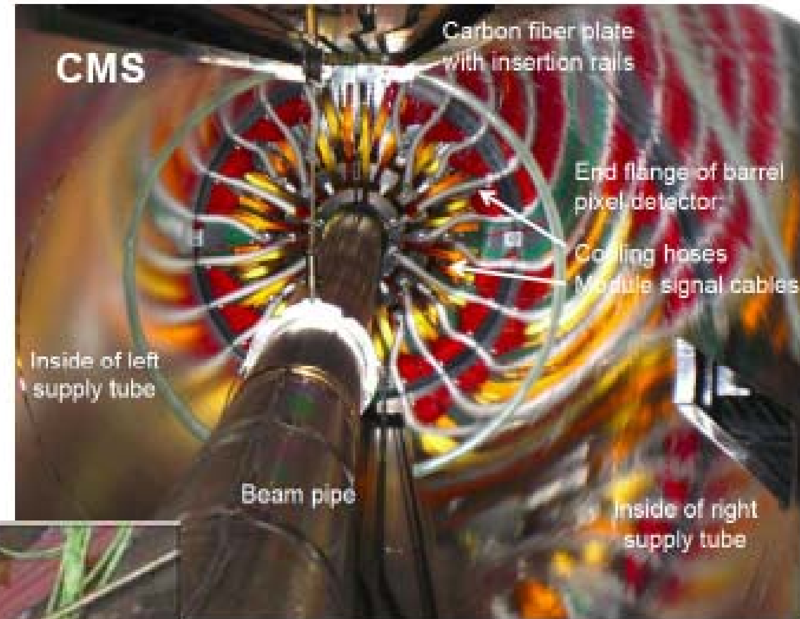
- Independent development and optimizations of readout chip and sensor
- Delivers unambiguous space point
  - Pattern recognition
  - Fine segmentation handles high track density
  - Excellent S/N
- n^+ pixels on n-type sensor used by ATLAS/CMS
- Bump-bonding : 2 technologies being used: Indium (In) and solder (Pb/Sn)

Pixel Detector at the LHC

Experiment	ALICE	ATLAS	CMS
Pixel Size	50 x 425 μm^2	50 x 400 μm^2	100 x 150 μm^2
Layers	2	3 layers + 2x3 disks	3 layers + 2 x2 disks
Radius (mm)	39 & 76	50.5, 88.5,122.5	43, 72, 110
Number of pixel chips	1200	27904	16000
Number of Pixels	9.83 x 10^6	80 x 10^6	66 x 10^6
Total Active Area	0.26 m^2	1.73 m^2	1.1 m^2
Material X_O per layer	1.1 %	~2.4 %	~ 2 %

Pixel Detectors at the LHC



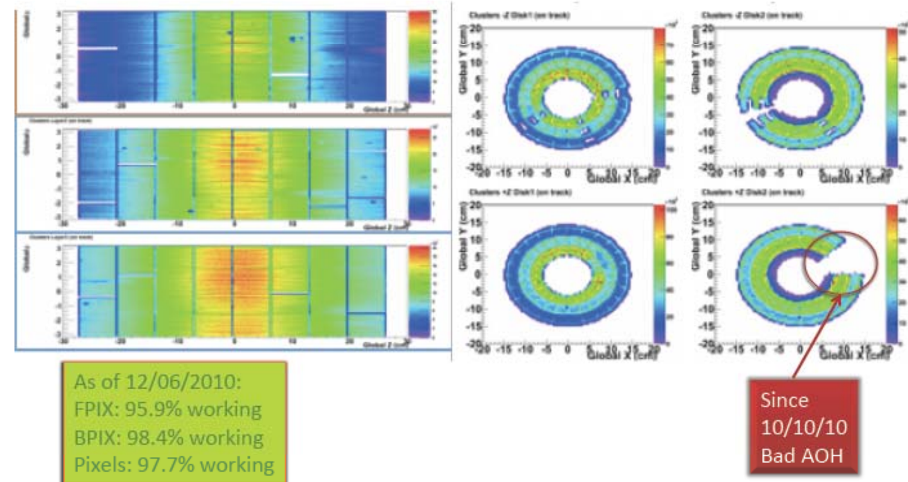


all based on

"Hybrid Pixel Detectors"

Operation experience of Pixel Detector at the LHC

- All work very well
- Easy and quick to switch on the detector
- >95% working pixels
- No radiation damage observed
- Suffered from LHC background of various flavors and need to come up with solution



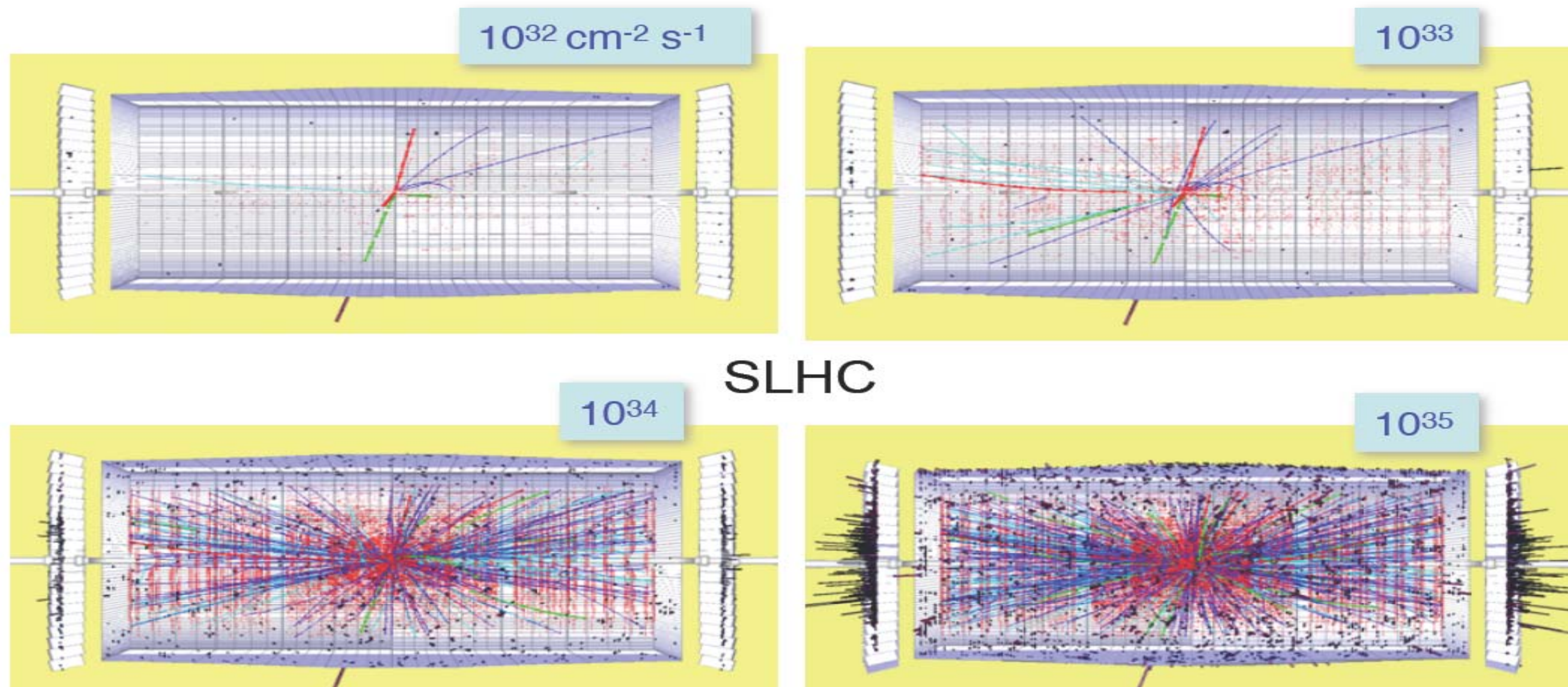
CMS Pixel Detector Status

Some Issues of Hybrid Pixel Detector

- Power consumption is high
  - e.g. ALICE pixel detector 1.5 kW, CMS 5 kW
- Needs active cooling
  - Cooling plant design and operation
  - Adds material
- Massive (relatively)
  - Sensor and readout chips
  - Dead region around edges (sensor guard ring; readout chips have digital circuit on periphery and wire bond pads)
- Bump bonding is expensive and is also the schedule driver

Tracking at the SLHC

- At the SLHC, with luminosities of 10^{35}, there will be ~400 interactions/ BCO



Challenges at the SLHC

- High particle rate, high bandwidth
- Radiation tolerance
- Less material
- Resolution as good or even better than the current detector
- Lower power
- More functionality, e.g. track trigger
- Practical consideration
  - Cost
  - Constraints of the existing experiment (cable plant, fiber plant, cooling lines, total power etc)

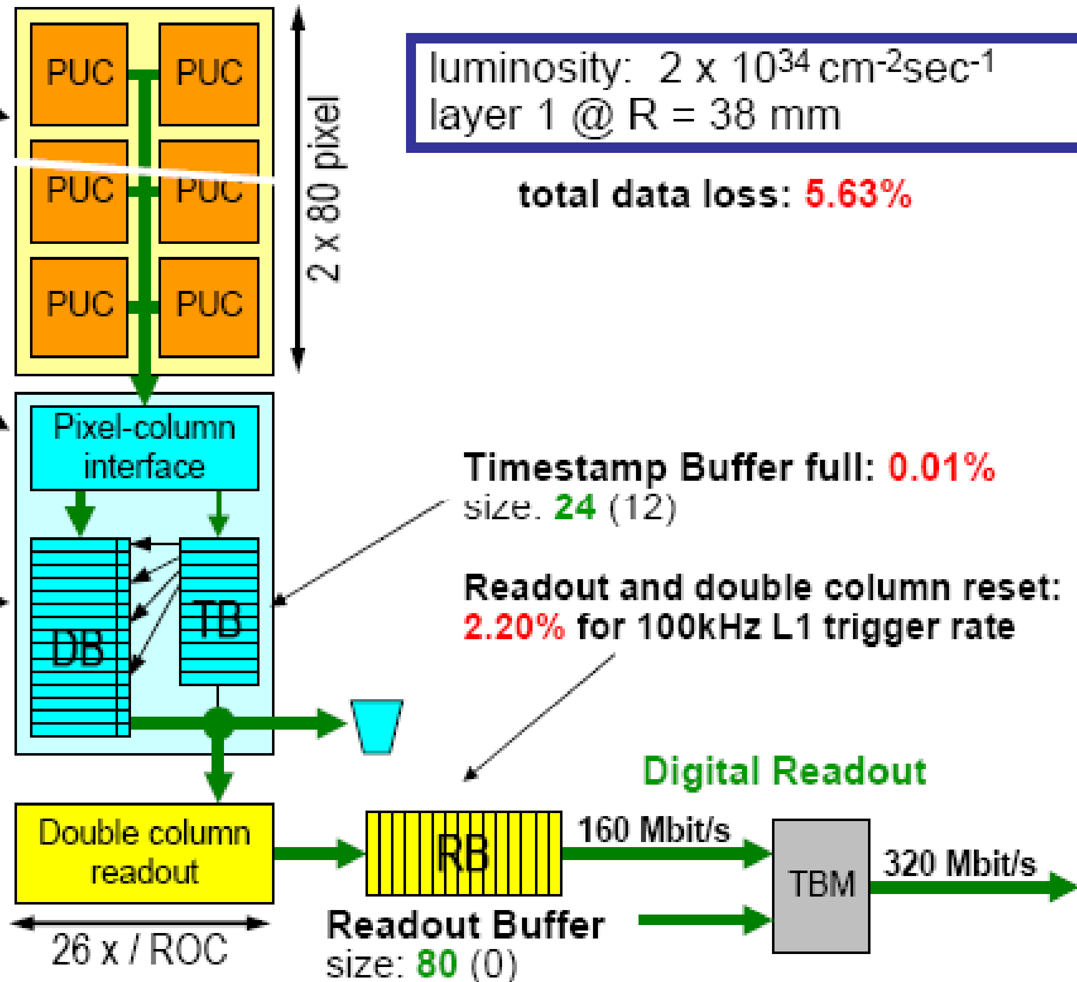
Data loss Mechanisms in ROC

Data losses dominated by finite buffer sizes !

Pixel busy: 0.72%
pixel insensitive until hit transferred to data buffer (column drain mechanism)

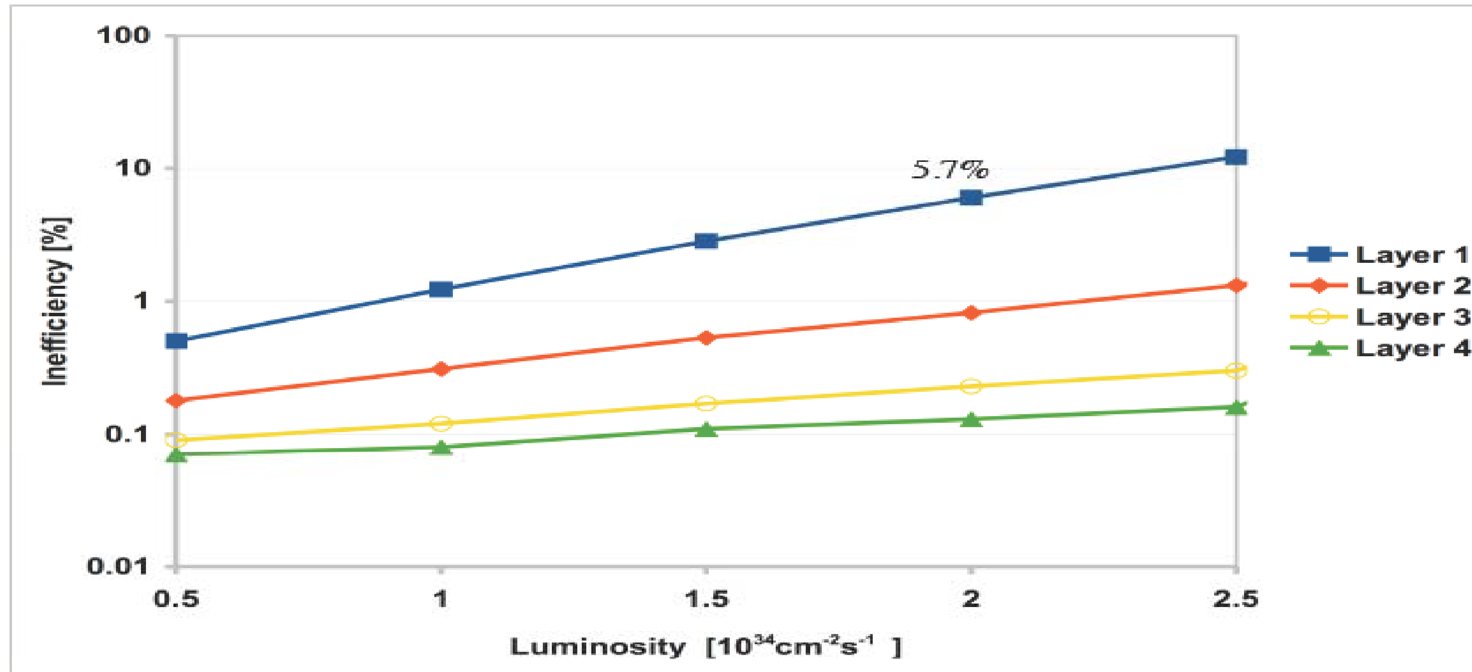
Double column busy: 2.03%
Column drain finds hitted pixels and transfers hits from pixel to data buffer. Maximum 3 pending column drains requests accepted

Data Buffer full: 0.68%
size: 80 (32)



simulation done by H.C. Kästli, PSI

Inefficiency vs luminosity



→Inefficiency depends exponentially on luminosity

Simulation has no safety factor
May be optimistic due to quality of simulation, typical events at 14 TeV;
Simulation should be repeated after we have some real data at 14 TeV
Limit of the technology and architecture

PSI ROC development Path

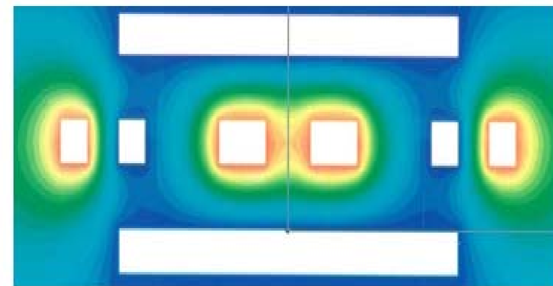
Readout Chip for Phase I

- Based on present readout chip
- Limitations of present ROC at Phase1:
  1. Buffers sizes for L1 latency (dominating)
     → **Increase number of buffers**
  2. Readout related dead-time at higher data volumes
     → **Additional readout buffer stage**
  3. Higher module count / same number of fibres
     → **Digital readout**
     - On chip ADC
     - New fast digital readout links
     - PLL to provide higher frequencies
     - Modification to control logic

130nm Chip for Phase II

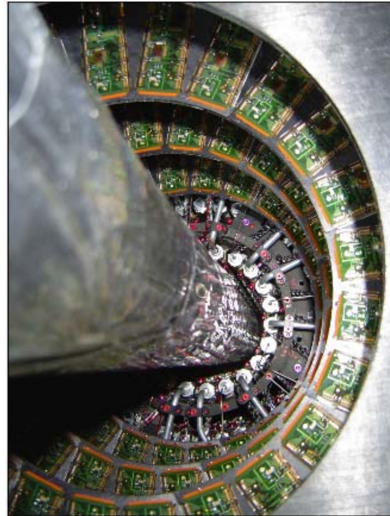
250 nm to 130 nm

- For a digital chip – no problem
- For a analog chip – more difficult (analog circuit simulations)
- For a mixed signal chip – very difficult (crosstalk problems, parasitic effects)
- PSI46 - ROC is a mixed signal chip
- Experience from PSI46 design needed, LHC run experience
- 8 years development time (my own estimation)

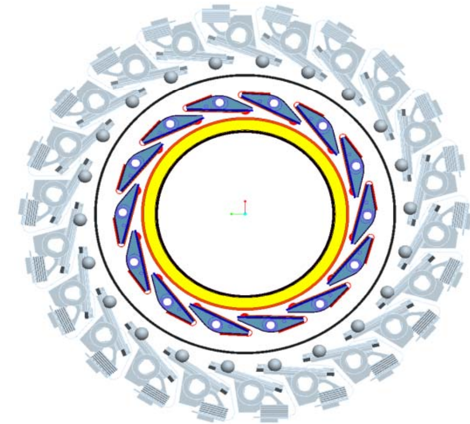


ATLAS: First Upgrade Insertable B Layer (IBL)

How it looks today.



IBL inside existing B-layer.



Project Goals:

Improve Physics performance of the present Pixel Detector:

- Reduce material budget to an "aggressive" 50% of the present inner most pixel layer, i.e. <1.5% X/X_0 at η=0.
- Have low R/O inefficiencies at LHC ultimate luminosity.
- Increase radiation hardness by a factor of five to $5x10^{15}$ 1MeV neutrons/cm^2

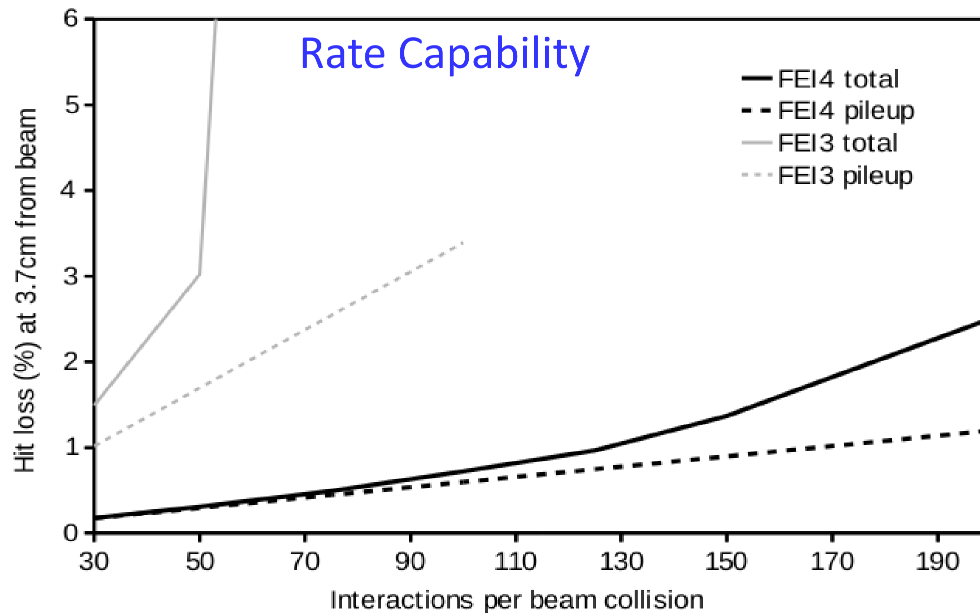
Installation schedule, 2013/14?

FE-I4 chip

- Largest chip in HEP to date
  - Will lower cost of future pixel detectors
- Ambitious step towards system-on-chip
  - Chip has full module functionality
  - Integrated power regulation including x2 DC-DC converter
- 16 Wafer fabrication submitted July 1
- Delivery last Fall; bench test results satisfactory
- Irradiation tests done up to 1e16 last December at LANL

FE-I4 Chip: Improve Performance and Lower Costs

Chip name	Width (cm)	Length (cm)	Active Area (cm^2)	Num. Pixels
FE-I4	2.0	1.9	3.36	26 880
Medipix [2]	1.4	1.7	1.94	65 536
ALICE1LHCb [3]	1.4	1.6	1.74	8 192
PSI46 [4] (CMS exp.)	0.8	1.0	0.63	4 160
FE-I3 [5] (ATLAS exp.)	0.7	1.1	0.58	2 880



Assembly Cost ~ inverse of the Chip Area

Design and verification done by large international team of engineers, students, and physicists.

Particle fluence at SLHC

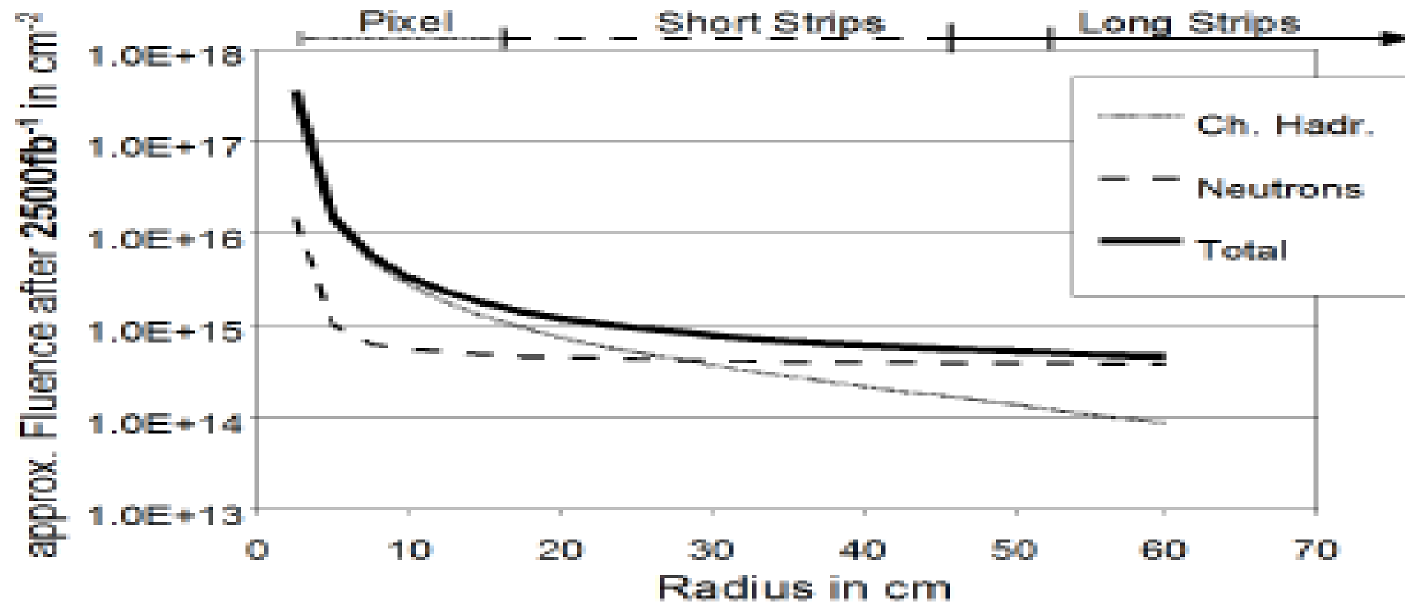


Figure 1: Estimated particle fluence at SLHC extrapolated from simulations for the CMS detector at LHC. [1]

For 2500 fb-1 of data

Radiation Damage

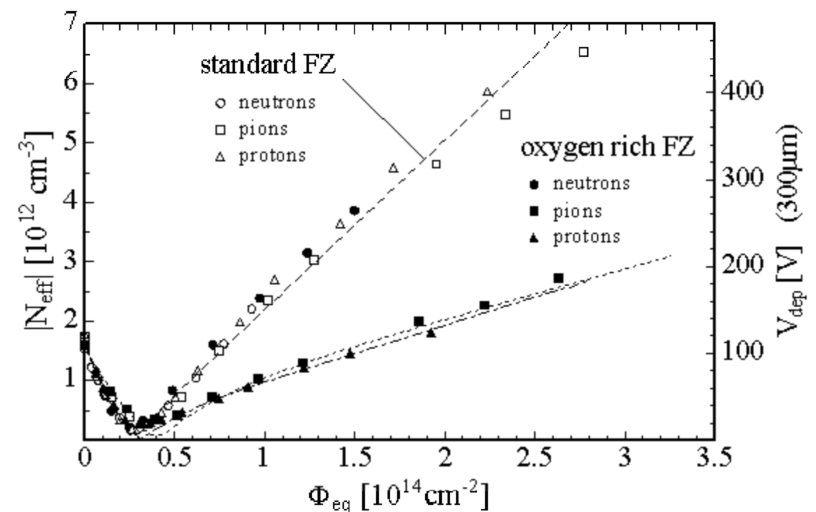
General alteration of the operational and detection properties of a device due to high doses of irradiation

Radiation induced effects:

- Electron-hole pair creation – particle detection
- Atomic displacement – dislocation of atoms from normal sites in the lattice -> long term effects on bulk properties
- Chemical bond rupture – surface effects, carrier's surface mobility decreases, oxide trapped etc -> surface damage

Radiation effects in Silicon detectors

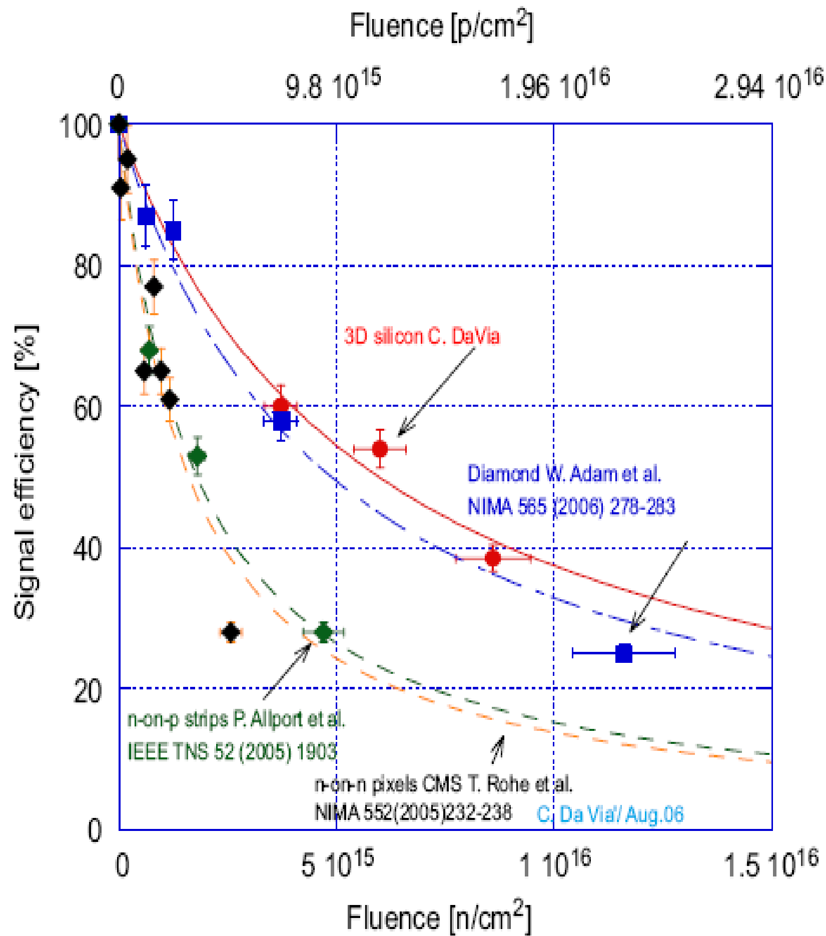
- Effects of displacements results in changes of the internal electric field, due to modified doping concentration
- For very high irradiations, conduction type will be inverted (type-inversion)
- Increase in leakage current
- Change in capacitance
- Charge collection losses

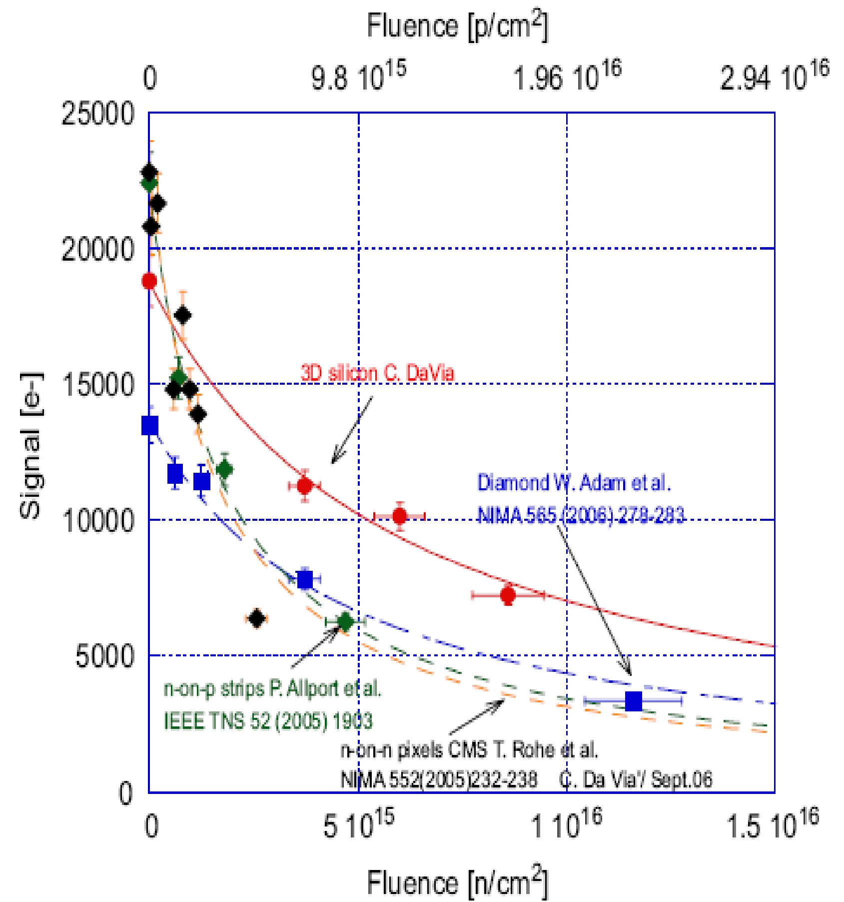


R&D on Sensor for the SLHC

- Big global effort on Sensor R&D for the SLHC
  - RD42 (diamond)
  - RD50 (rad-hard sensors, mostly on silicon)
  - 3d consortium (3d sensors)
  - ALICE, ATLAS, CMS, and LHCb effort

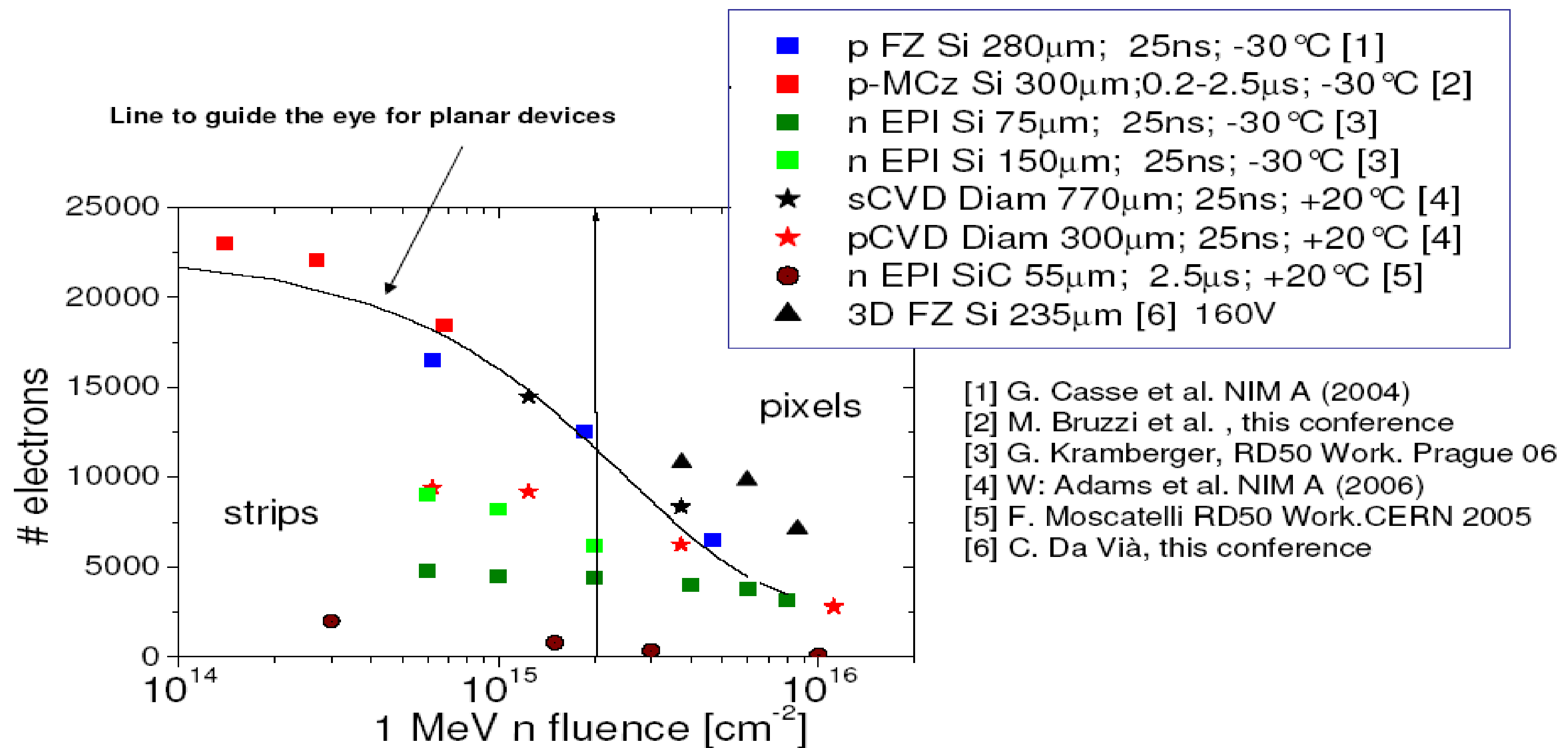
Radiation Hardness of Sensor





C. Da Viá et al. / Nuclear Instruments and Methods in Physics Research A 587 (2008) 243–249

Comparison of New Sensor Technologies



LHC-SLHC Comparison

LHC

- We can identify 3 different regions to match radiation damage and occupancy in the current LHC detector
- Radiation fluence increases by about a factor of 10 from one region to the other

R	Φ	Technology
>50 cm	10^{13}	p-on-n strip 500 μm thick, high resistivity (≈5 KΩ·cm), pitch ~ 200 μm
20-50 cm	10^{14}	p-on-n strips 320 μm thick, low resistivity (≈2 KΩ·cm), pitch ~80 μm
<20 cm	10^{15}	n-on-n pixels 270 μm thick sensors low resistivity (≈2 KΩ·cm) oxygenated

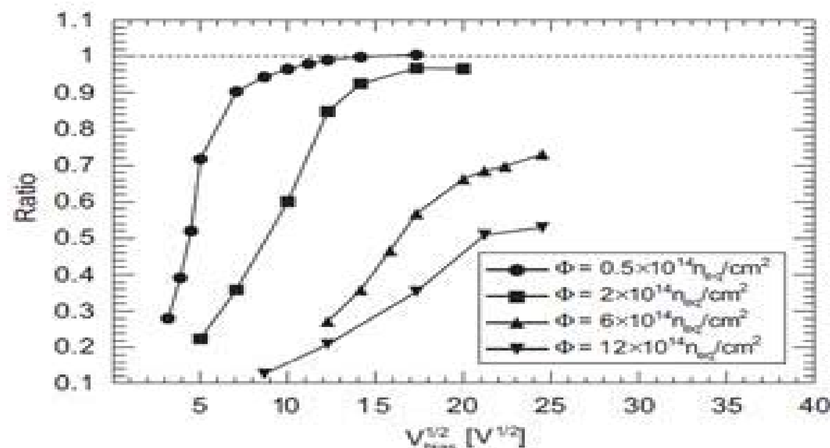
SLHC

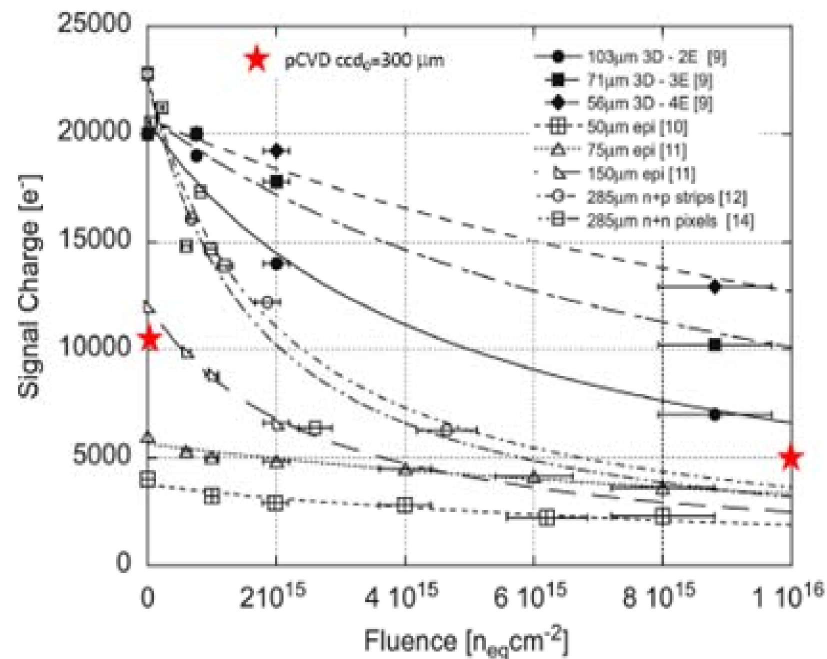
- Radiation fluence increases by a factor of 10 between LHC and SLHC.

R	Φ	CCE	Technology
>50 cm	10^{14}	20ke	Present rad-hard technology (or n-on-p)
20-50 cm	10^{15}	10ke	Present n+-n LHC pixel (or n-on-p)
<20 cm	10^{16}	>5Ke	RD needed

CMS Pixel Sensor Development

- Radii<20 cm
  - Better understanding of radiation performance of the current n-in-n pixel sensors
  - New ultra rad-hard sensor & material: 3D silicon and diamond
  - R&D on comparing planar Si (FZ, MCZ, epi, p-type etc) with 3D silicon and diamond before and after irradiation at Fermilab's MTEST
  - Understand cost, yield, fabrication and assembly issues
- Radii>20 cm
  - CMS has embarked on an ambitious planar Si R&D program with HPK

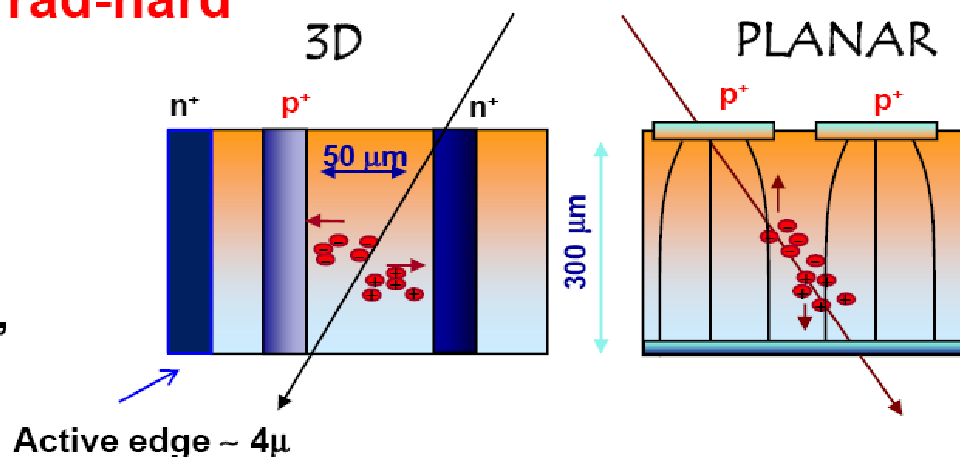


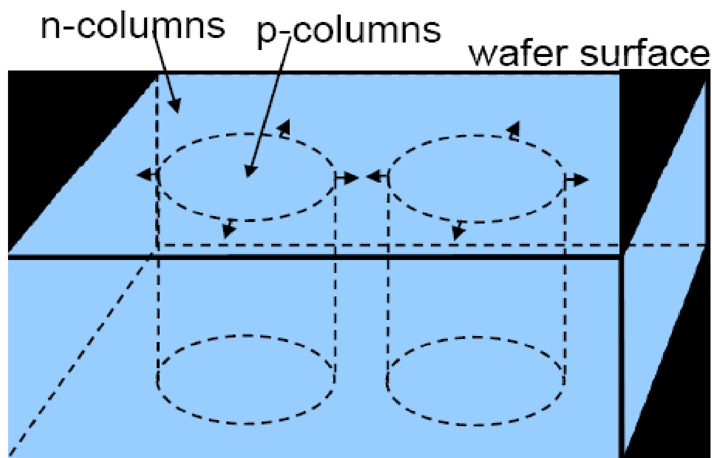


3D Sensors

First proposed by Sherwood Parker in the mid-90s;

- "3D" electrodes: **narrow columns along detector thickness,**
  - **diameter: 10µm, distance: 50 - 100µm**
- **Lateral depletion: great for rad-hard**
  - **Lower depletion voltage**
    - **Cooling**
    - **HV power distribution**
  - **Fast signal**
    - **Reduced bunch crossing, pileups, rate**

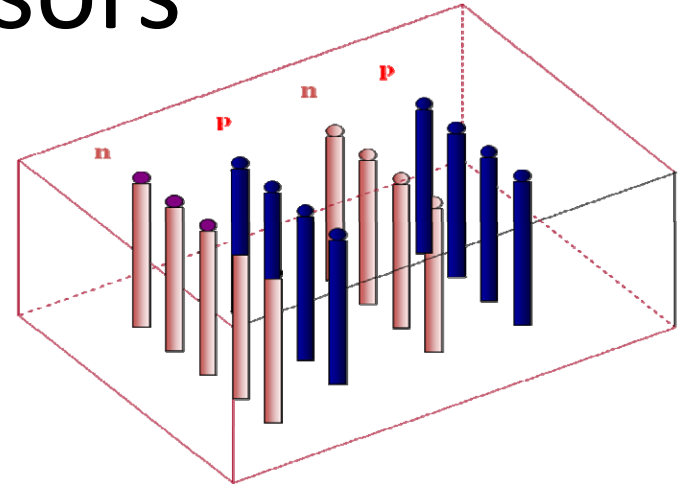




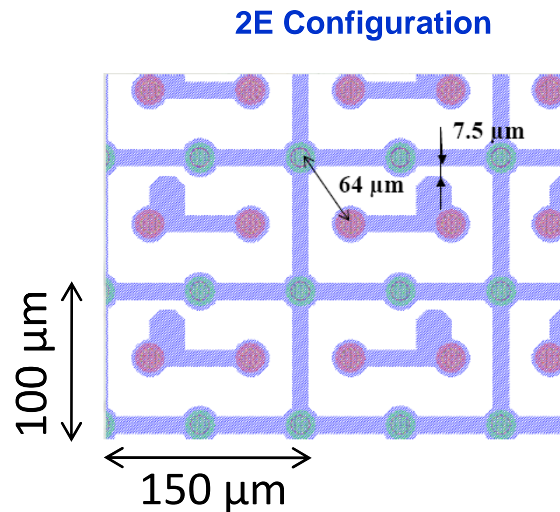
- 3D detectors also allow the implementation of the "Active Edge concept"
- Interest in the Forward physics community
- Active Edge concept can lead to Improving layout geometry which is of general interest

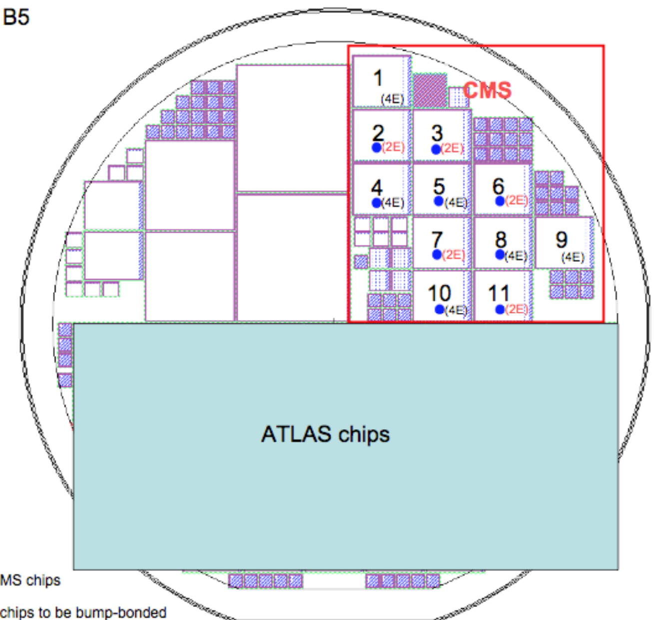
CMS 3D sensors

- As a part of “3D Collaboration” , fabrication transferred to SINTEF for small and medium scale production
- Two different 3D CMS layouts:
  - 4 readout electrodes per pixel (4E)
  - 2 readout electrodes per pixel (2E)
- More radiation hard:
  - Faster response
  - Lower depletion voltage
  - Less trapping
  - Lower noise
  - Larger active volume
- Devices were fabricated at SINTEF



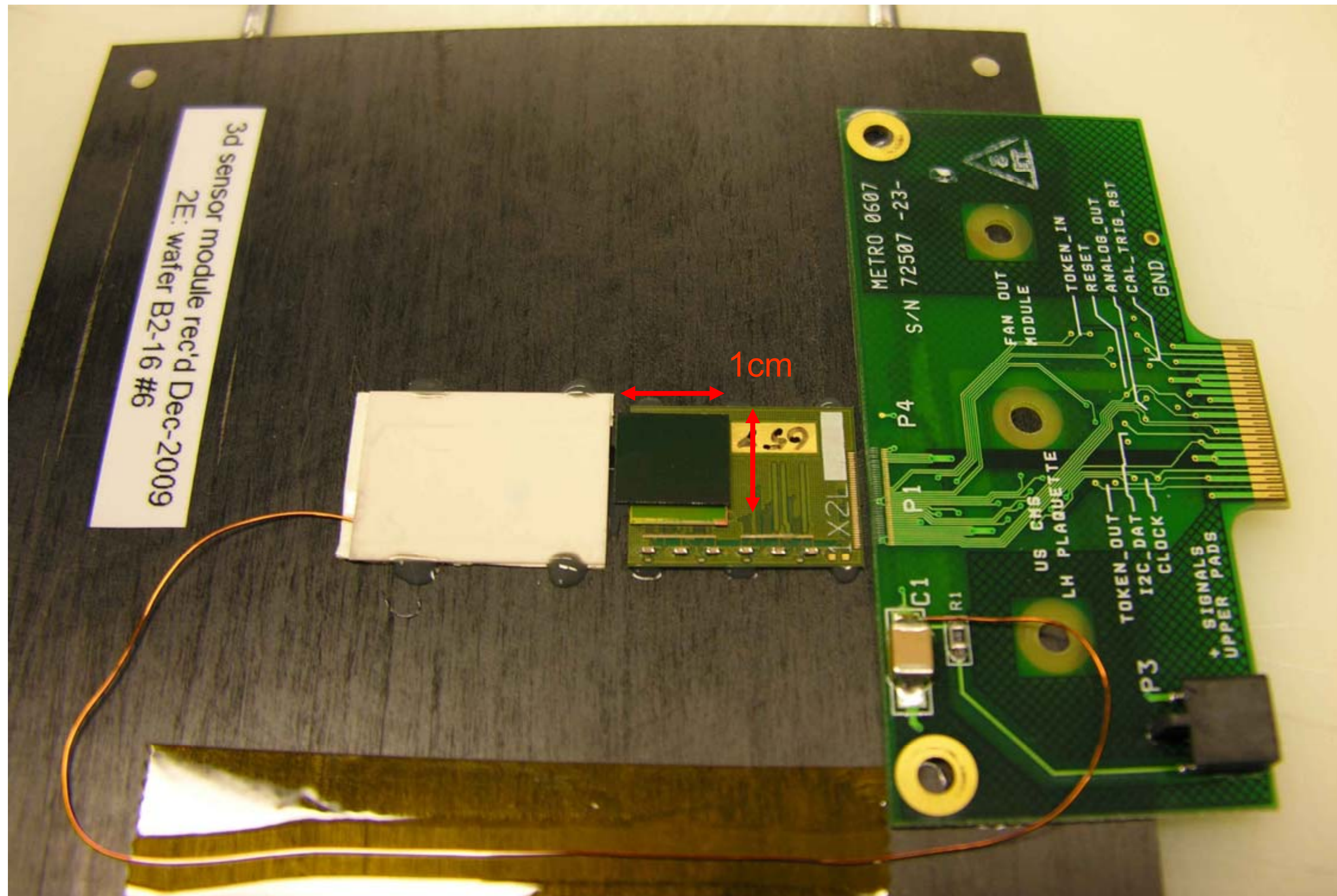
FNAL, Purdue + others collborators





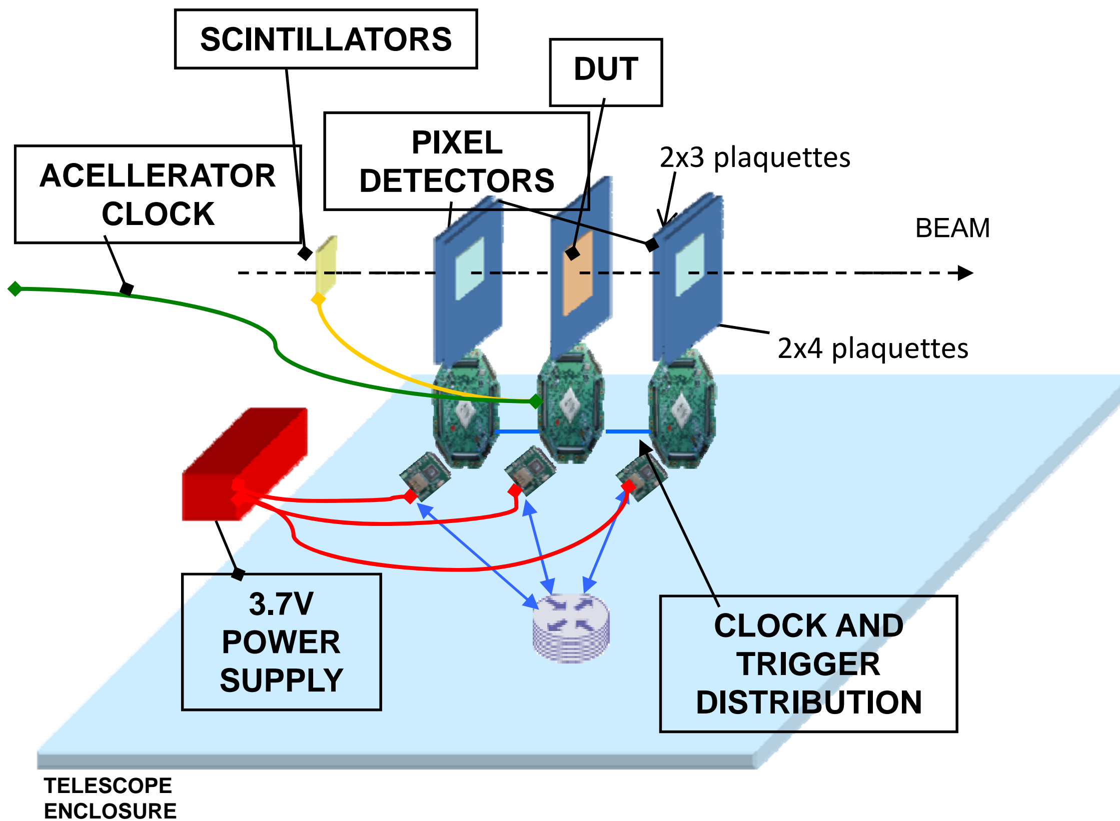
3D Detector

Cooling tubes

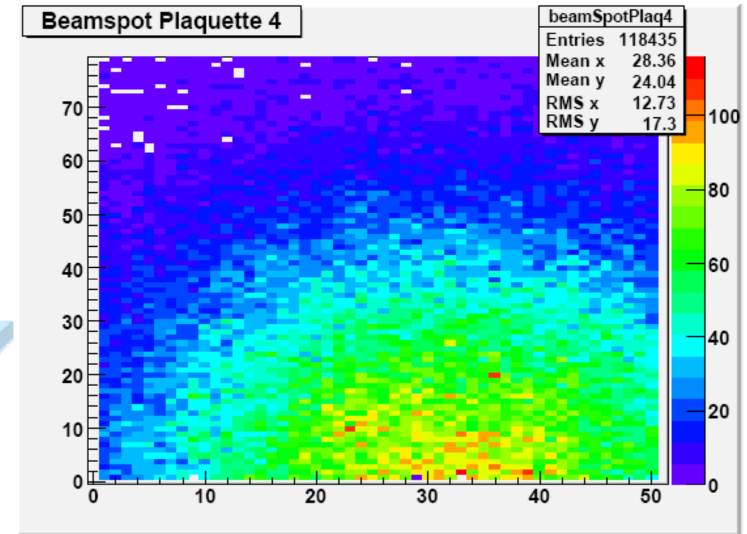


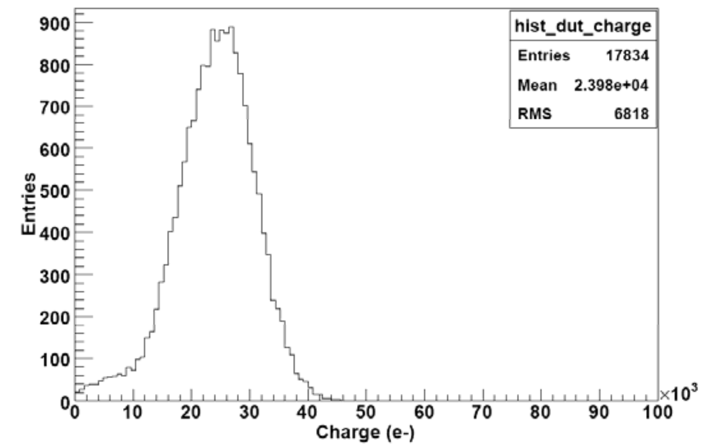
•Sensor produced at SINTEF (joint submission ATLAS, CMS, and Medipix). Bump bonded to a CMS pixel readout chip at IZM.

MTEST with 3D



Beam spot on 3D

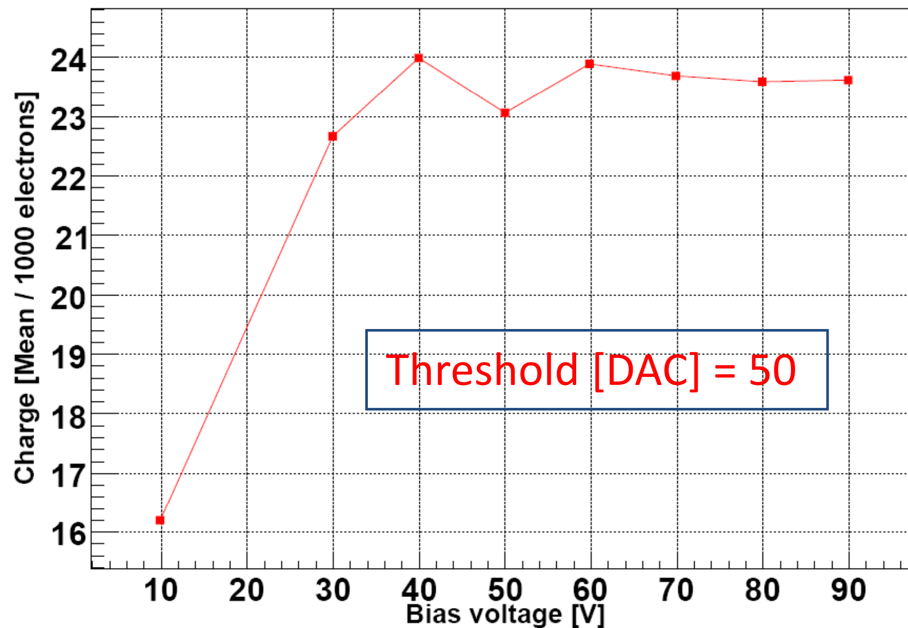


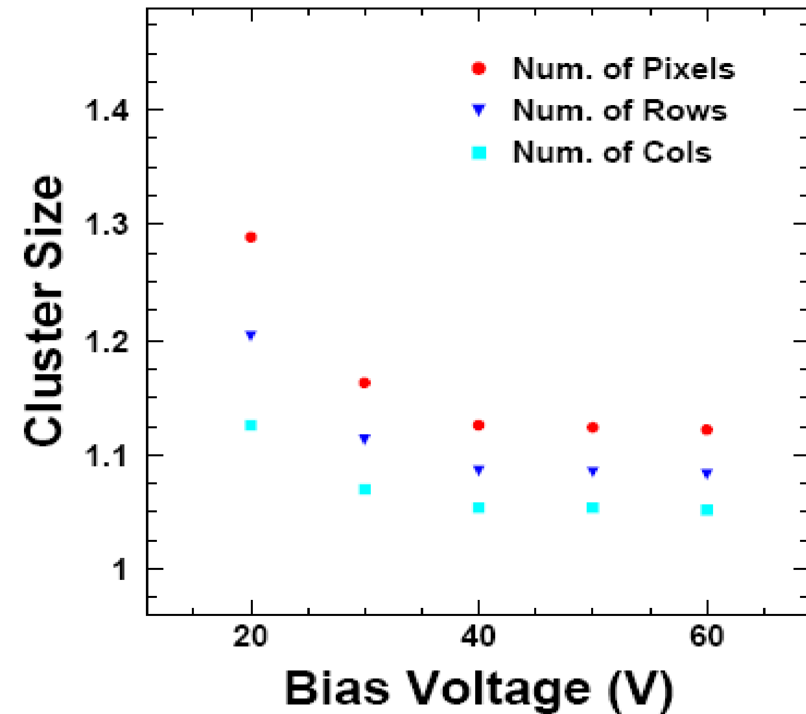


- 120 GeV protons beam
- No B field

FNAL, Purdue

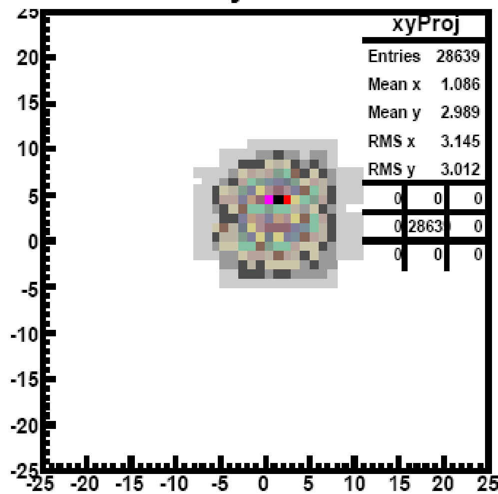
Prelim Results on 3d (2E)

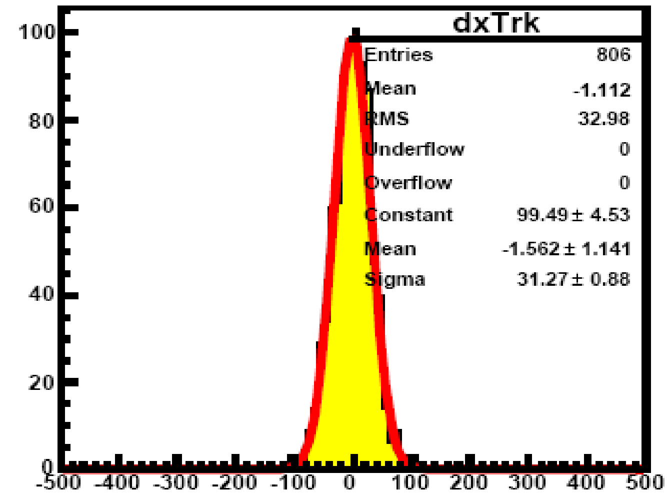


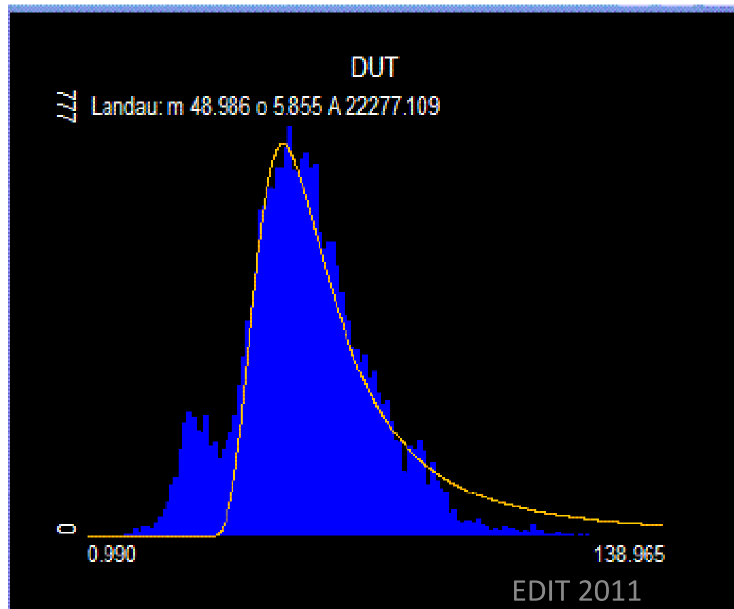


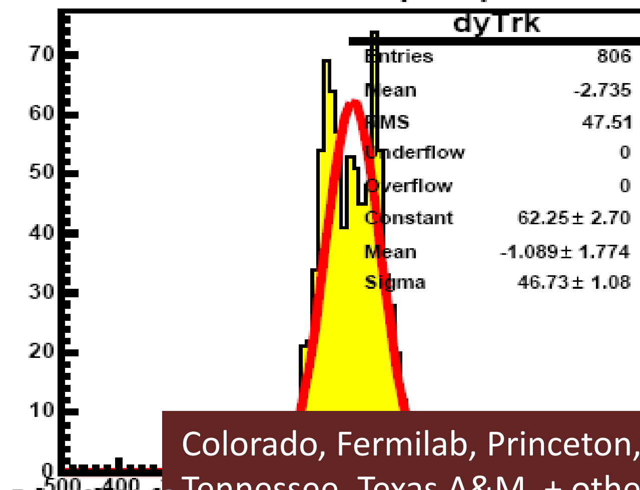
Not much charge sharing
Not much Lorentz drift
→Finer pitch readout required
Yield, cost, how big a module, assembly

MTEST Results: SC Diamond



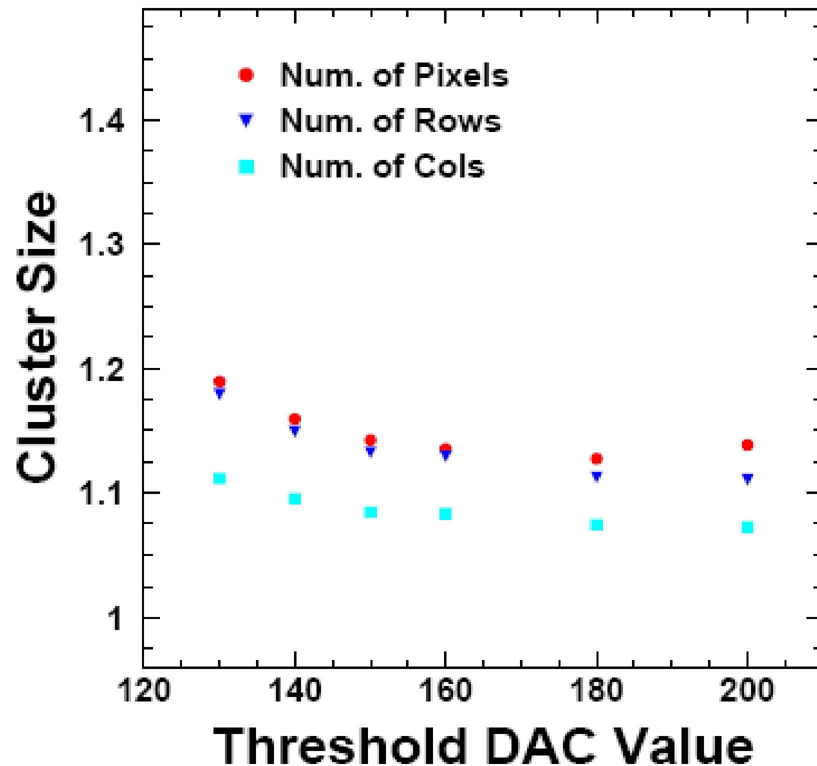


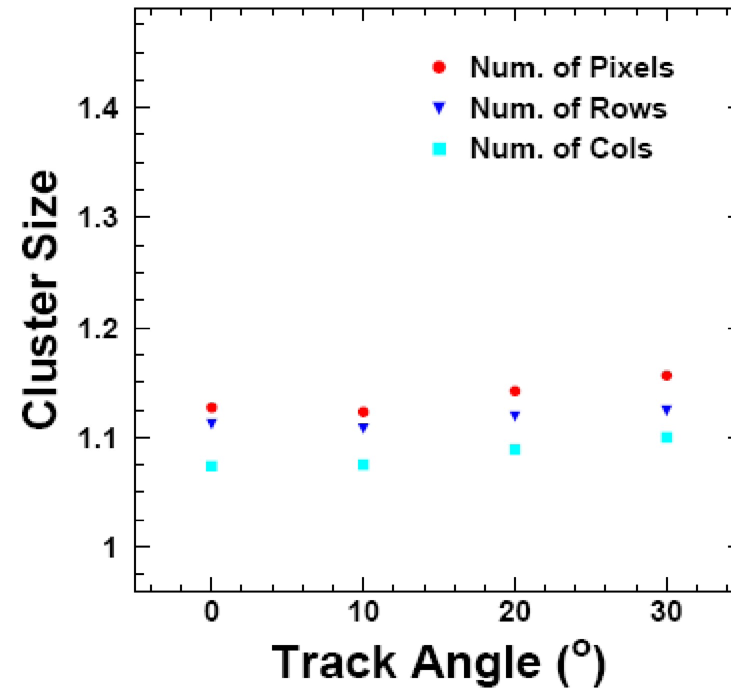




Colorado, Fermilab, Princeton, Rutgers, Tennessee, Texas A&M, + other CMS collaborators & LHCb (Syracuse)

Prelim Results on pCVD

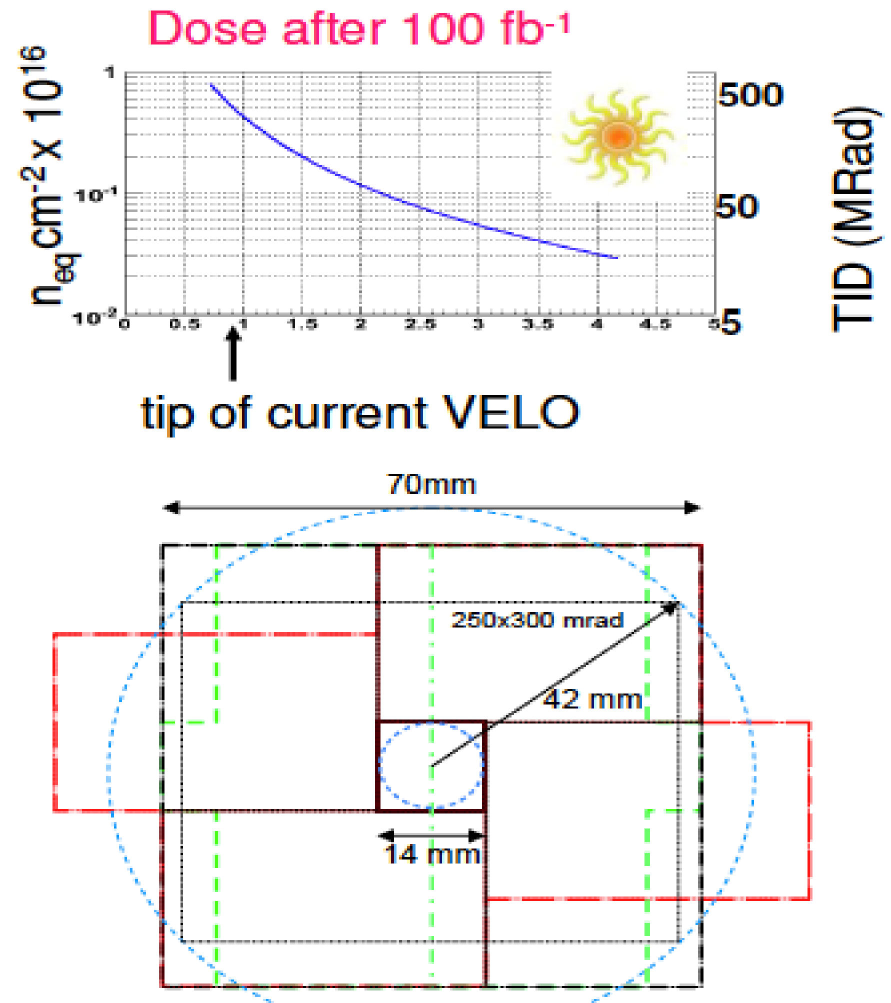




Small signal size; Low capacitance; fast drift
Needs an ASIC to match these properties
Cost, single vendor; small SC; pCVD

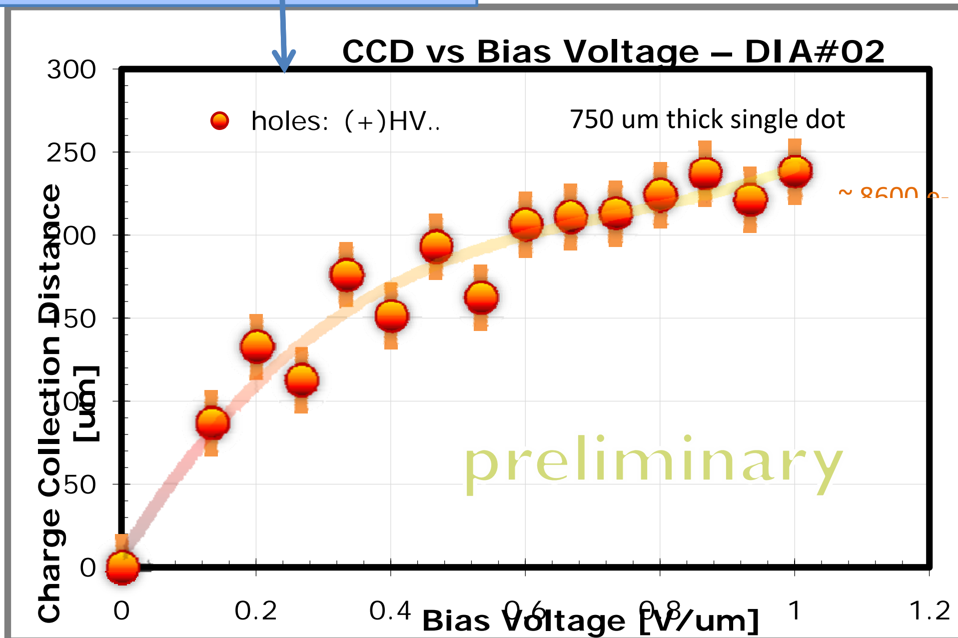
LHCb: Sensor R&D goals

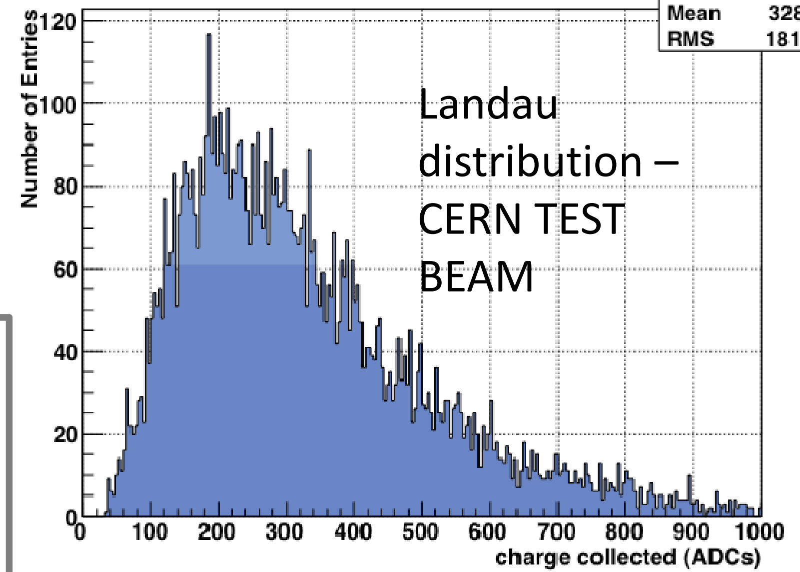
- ◆Produce viable solution which can withstand maximum radiation fluence expected for 100 fb^{-1}.
- ◆The contenders are planar Si (various technologies), 3d silicon (rd50 Glasgow-CNM), pcCVD diamonds (cost issues)
- ◆Our work is focused on pcCVD diamonds (within RD42), planar silicon (p-type sensors RD50), and may expand to 3d silicon in collaboration with Brookhaven (Z. Li)
- ◆Diamond advantages: low leakage current, even after considerable levels of irradiation, "self-cooling," low noise device
- ◆Silicon advantages: Higher charge collection, cost, ease of production



PRELIMINARY RESULTS

Laboratory studies with Sr^{90} source





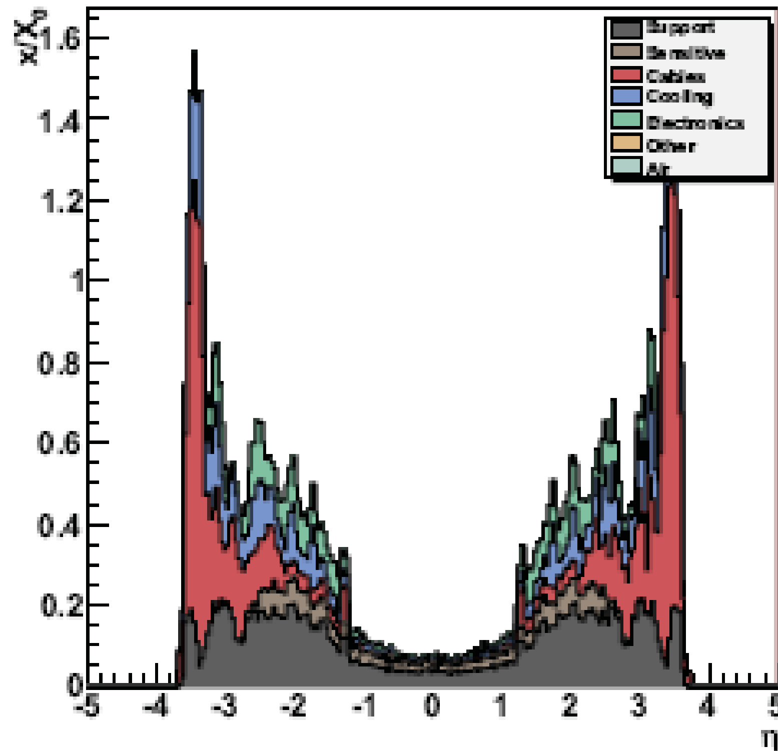
Landau distribution – CERN TEST BEAM

pcCVD diamond with strips with 50 μm pitch

Absolute charge calibration and resolution studies under way

Material Budget

Use CMS Pixel Detector as an example



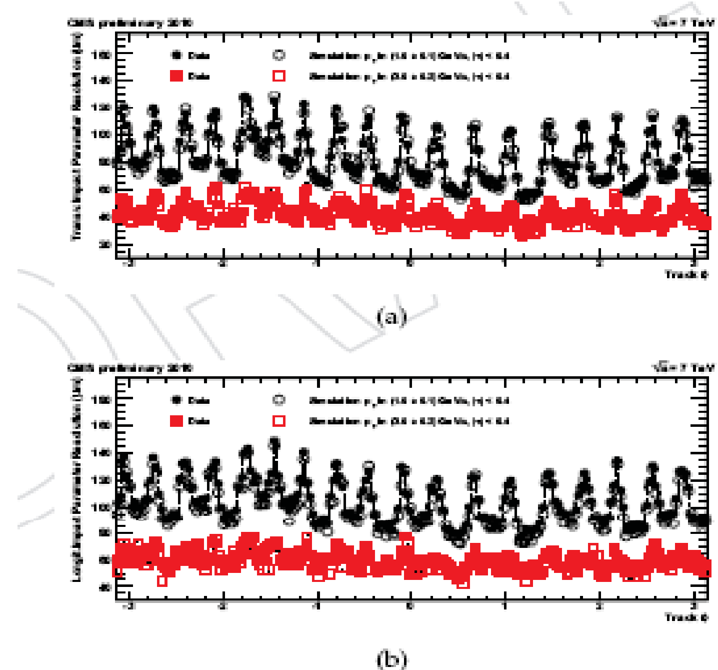


Figure 6.10: Measured resolution of the track transverse (a) and longitudinal (b) impact parameter as a function of the track ϕ for transverse momenta in $1.0 \pm 0.1\,\mathrm{GeV}/c$ (circles) and in $3.0 \pm 0.2\,\mathrm{GeV}/c$ (squares). Filled and open symbols correspond to results from data and simulation, respectively [7]. The 18 peaks correspond to the 18 cooling structures in the BPIX as

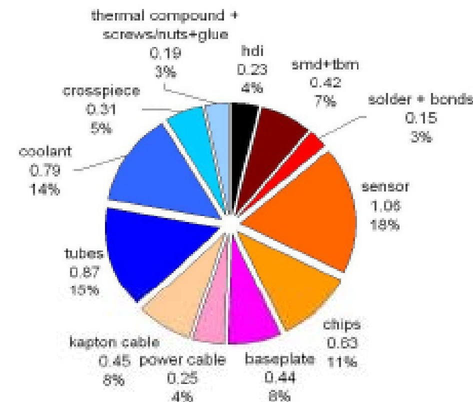
Material budget driver:

cooling and associated infrastructure –directly related to power dissipation;

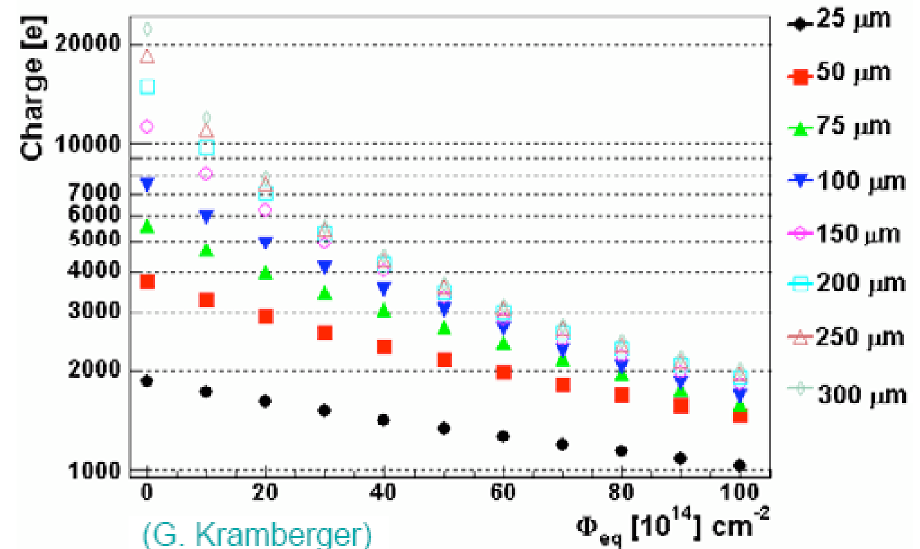
mechanical support;

Thinned Sensor

- At η=0, sensor contributes a significant fraction of the material budget
- Thinned detector almost collect the same charge as thicker ones after irradiation
- Depletion voltage (hence operation voltage is much lower) and hence lower leakage current
- Helps in reducing power



CMS Pixel

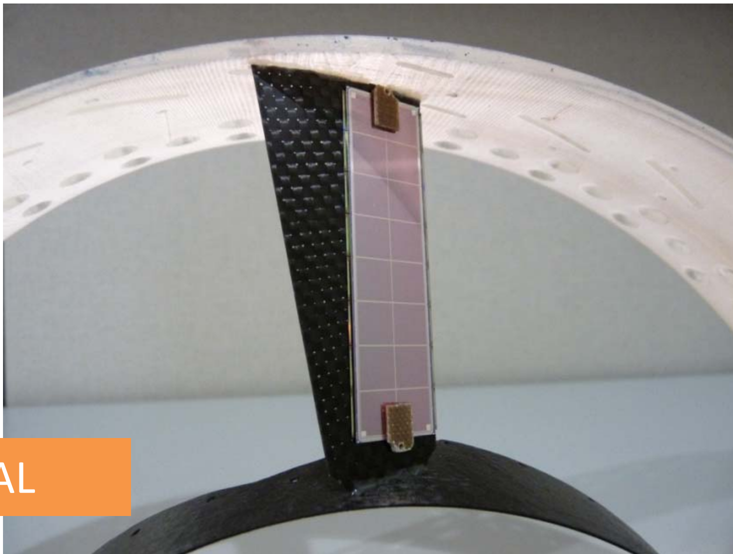


Light-weight Mechanical support Thermal Pyrolytic Graphite

- Pyrolytic graphite has a High thermal conductivity (in-plane k = up to 1700 W/m-K) and low density (2.26 g/cc)
- Need to stiffen TPG substrate since parts get damaged easily without adding a lot of material while keeping a reasonable thermal performance.

- Design of the CMS upgradeForward Pixel support
  - One ply of CFRP on TPG as facing sheet.
  - To reinforce the structure, perforated holes are drilled on TPG
  - CF encapsulation on both sides of TPG,

- Heat sink
  - Tiny tube for CO_2 cooling are embedded in Carbon-carbon (CC)
  - CC is fragile since it is made very thin and therefore there are some machining challenges.



FNAL

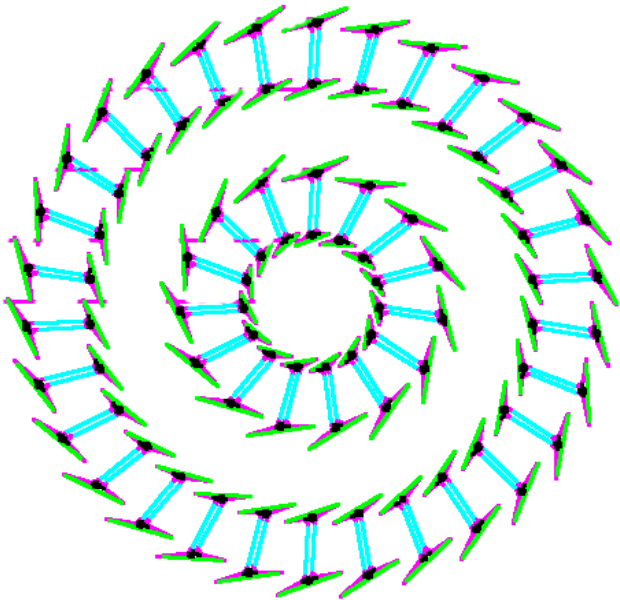
ATLAS: Develop New Materials for Support Structures

Developing <u>new material</u> – <u>all carbon foam</u> – in collaboration with US industry.

Material is machineable, has low-density, high thermal conductivity, and strong.

Currently basis for all future ATLAS pixel mechanics designs. Can be applied in other future experiments.

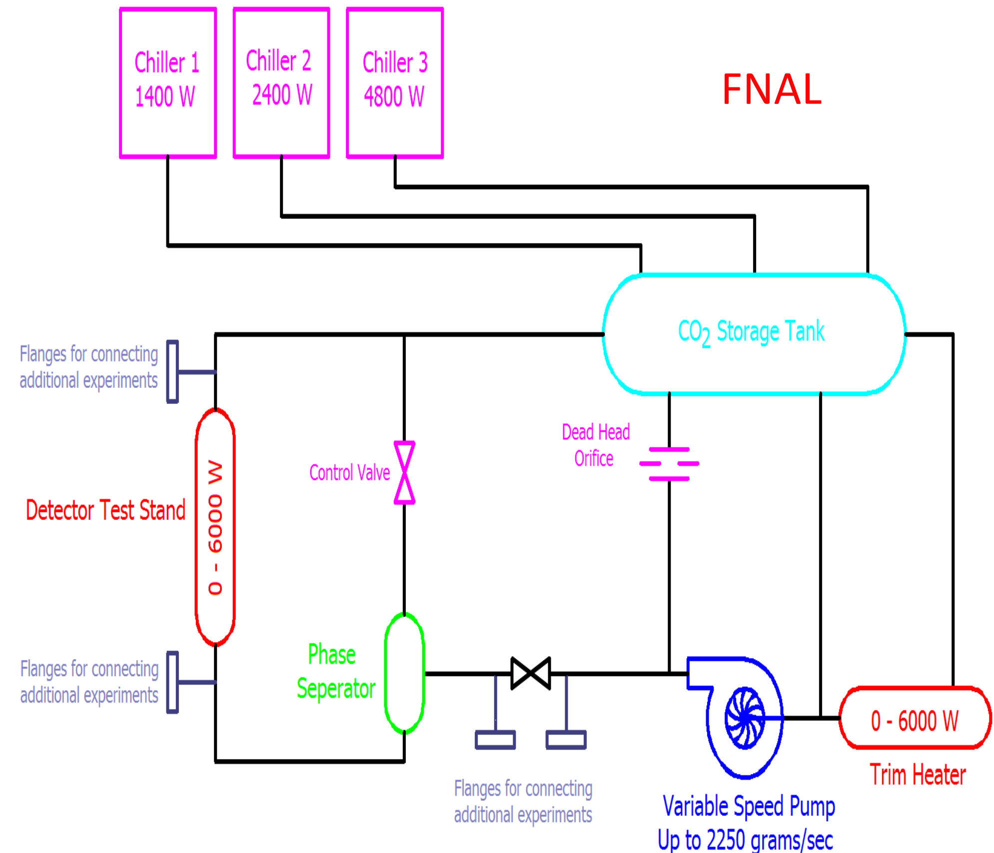
This is a highly successful, early prototype program involving LBNL and industry.



Double I-Beam concept for future pixel upgrade. Low mass because no support shell needed. Silicon mass equivalent of all mechanics: 2.8 kg versus 5.7 kg for present pixel detector plus IBL.

CO_2 Cooling for pixel and tracker upgrade

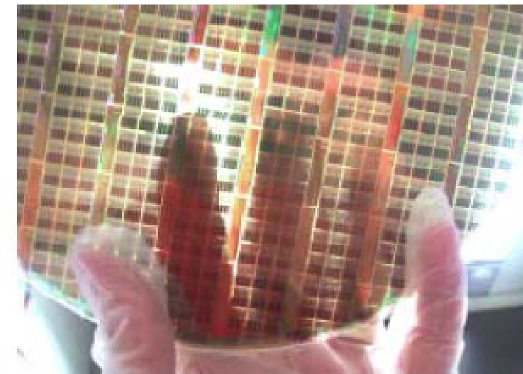
- Both ATLAS and CMS are interested in using bi-phase CO_2 cooling
- CERN group is working on a proto system based on LHCb experience
- CMS is planning to install CO_2 cooling for pixel phase 1 upgrade and tracker upgrade in phase2
  - Thin and light pipe inside the detector
  - Pipe connecting techniques
  - Existing pipe-work inside CMS detector
- A prototype CO_2 cooling system is also being assembled at Fermilab and is expected to be operational in March



Wafer Thinning

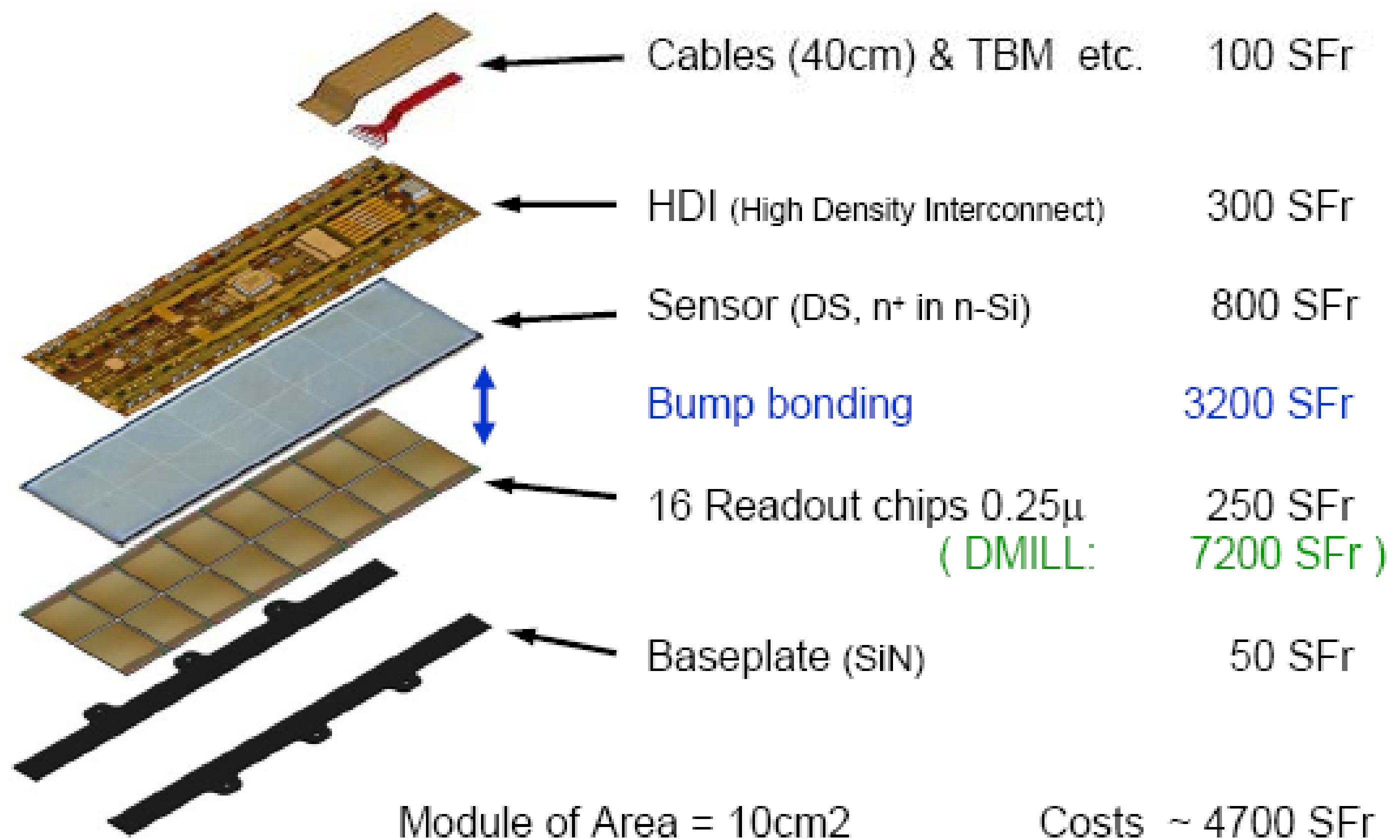
- Detectors and readout chips make a significant contribution to multiple scattering
  - Every 100 μ of silicon is 0.1% X_0
  - Hybrid pixels have 2 layers of silicon, each greater than 100 μ thick
- Take advantage of work being done in industry by major companies (IBM, INTEL, Toshiba, etc.) to reduce wafer thickness
- Thinning
  - Thinning to 50 microns is in production
  - State of the art – CMOS wafers thinned to 10-15 microns by lapping/grinding followed by wet or plasma etch and CMP. Thinner for SOI.
- Challenges
  - ***Handling/breakage***
  - ***Thickness uniformity on large wafers***
  - ***Circuit performance changes due to thinning***
    - *No change in Vt for 25u wafer (Fraunhofer, IZM)*
    - *No change in Idsat for 25 u wafers (IZM)*
    - *More tests needed*

Thinned IC wafer (J. Joly, LETI)



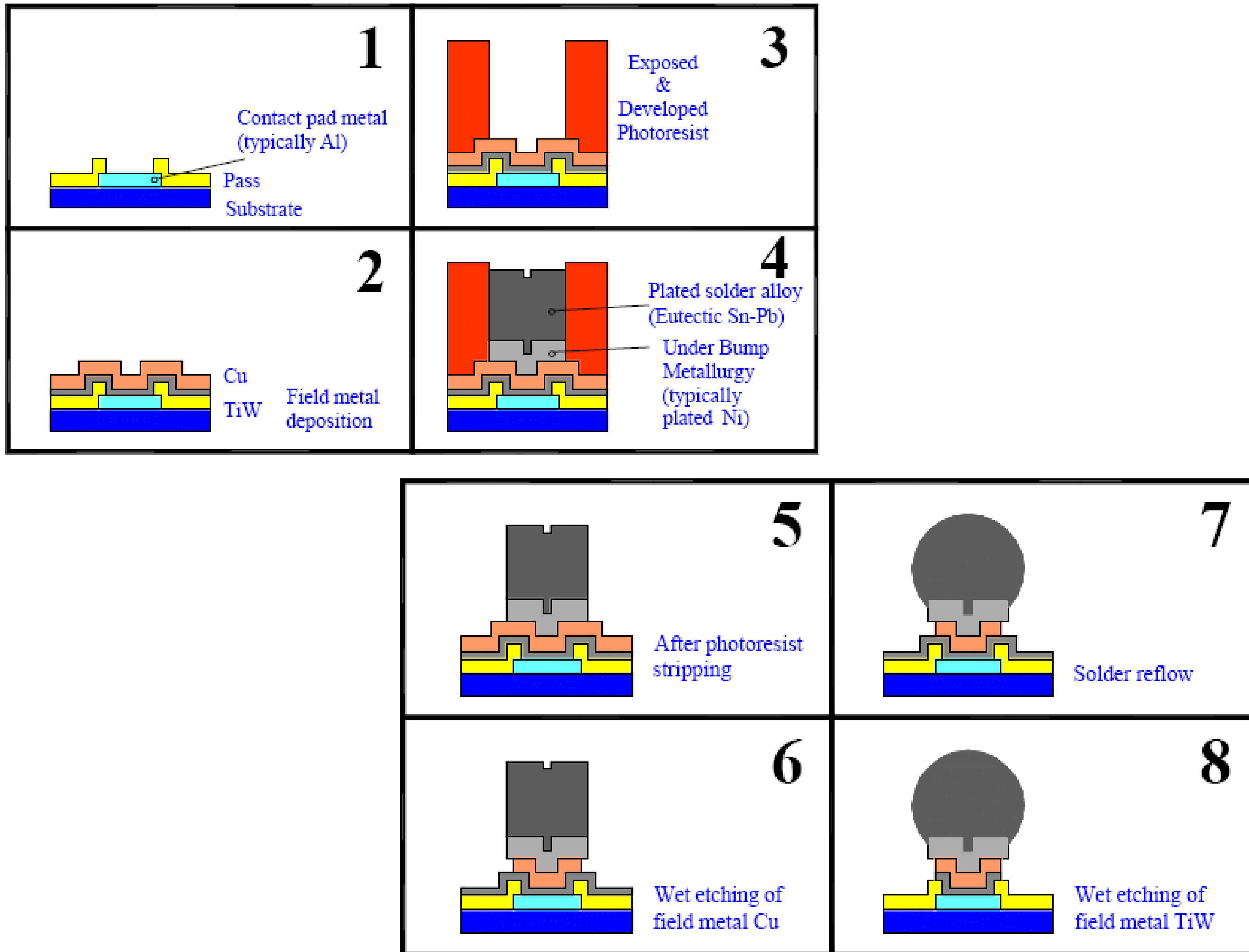
Thinned 200 mm wafer transferred on to glass handle wafer (A.Young, IBM)

Costs of a CMS Pixel Barrel Module



Optical links, FED , FEC, Power supplies add +15% → ~550 SFr/cm2

Bumping Process



Details of the steps

- Sensor wafers
- Design/finish of pad mask basing on GDS file supplied by us.
- Manufacturing of glass mask
- Sputter deposition of the plating-base
- Lithography of the resist layer
- Electroplating of the bond pads
- Stripping of resist and plating-base
- Dicing of wafers into sensor modules
- Cleaning, inspection and sorting

- ROC wafers
- Design/finish of pad mask basing on data supplied by the customer (GDSII format).
- Manufacturing of glass mask
- Sputter deposition of the plating-base
- Lithography of the resist layer
- Electroplating of the PbSn bumps
- Stripping of resist and plating-base
- Reflow of bumps
- Preparing for wafer thinning
- Wafer thinning to 180-200 μm
- Dicing of wafer into dies
- Cleaning, inspection and sorting

Flip Chip Bonding

Flip chip assembly is done in a Class-10 clean room.

Suss MicroTec FC150 Flip Chip Bonder with both Universal and Solder Reflow Bonding Arms.

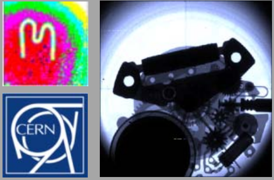
PROCESS STEPS

- Preliminary alignment.
- Detector and readout chips are adjusted exactly parallel using a laser autocollimator.
- Lateral alignment (x,y, θ).
- Pre-bonding compression of softened bumps.
- Reflow bonding.
- Cooling.

NOTES

- Chips are heated through custom SiC vacuum tools using infrared halogen lamps.
- Alignment accuracy: < 3 µm.
- Throughput: 3-4 bondings/hour.

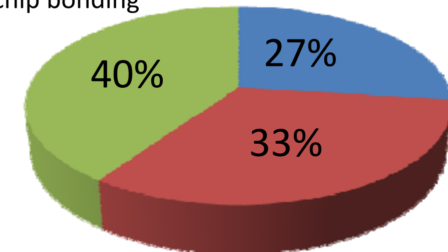
J. Salonen *et al.*, "Flip Chip Hybridization…", PIXEL2002 Workshop, Carmel, CA, September 9-12, 2002



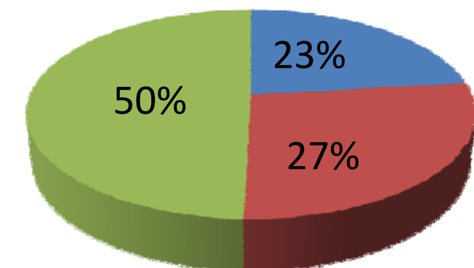
Low-Cost µ-Bump Bonding -

- Bump bonding (BB) costs for a single pixel detector unit have been € 200 – € 300.
  - ReadOut Chip (ROC) : Sensor Chip (SC) : BB (cost ratio) = 1:2:7!
- Increase in pixel detector area in the LHC upgrade – coverage of ten(s) of square meters?
  - BB is a major cost issues and a motivation for the low-cost study
- Studied low-cost BB technologies have to exist still after 10 years and have to be compatible with 300 mm wafers.
- Development has to be done on all fields of the pie diagrams for getting to ultimate low-cost BB solution.

Cost structure 2008 - bump bonding of single detector (estimate)

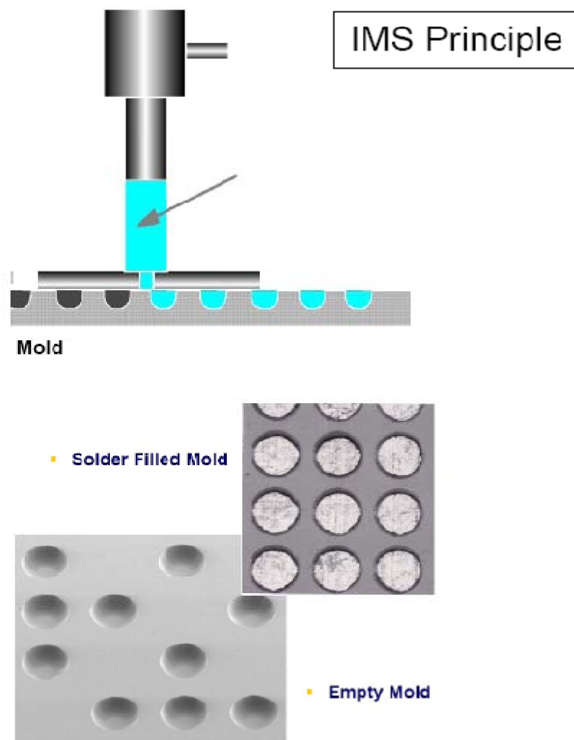


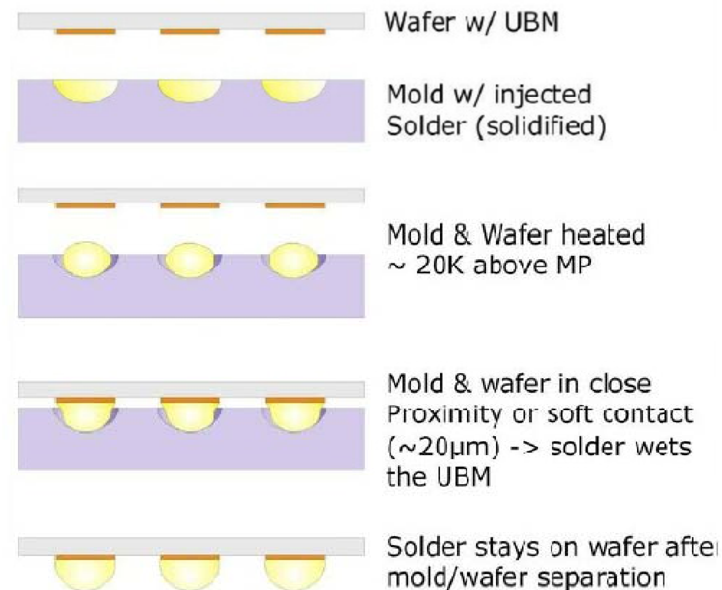
Cost structure 2010 - bump bonding of single detector (estimate)



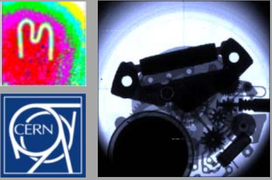
Lost Cost Bumping

C4NP Low Cost Bumping **Injection Molded Solder** (IBM & Süss)





- IMS allows bump 75µ size and pitch of 150µ
- 200µ thick wafers processed so far
- Wafer costs (300mm) ~ 150 $

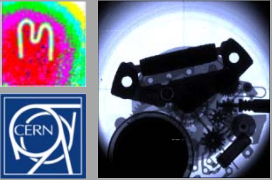


UBM Deposition

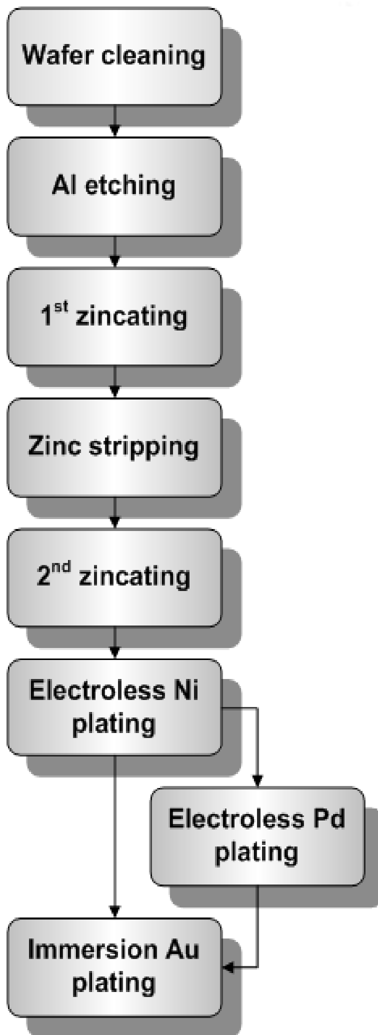
- Electroplating has typically been used for solder bumping pixel of wafers.
  - Well characterized and reliable technology, but rather expensive in small-scale production.

- Electroless Nickel (EN) under bump metallization (UBM) is studied as a corner stone for low-cost BB in this presentation because:
  - EN is suitable for various flip chip scenarios
  - EN can be processed without lithography
  - Batch processing - high-volume capability and affordable price
  - Reliable UBM – thick Ni as diffusion barrier for solder

- Electroless technology could substitute traditional electroplating processes *in certain bump size/pitch window* in combination with complementary solder deposition techniques.
  - Solder ball placement solutions are also studied for low-cost solder deposition.
  - Anisotropic conductive films (ACF) could be used, but there aren't many suitable films available for area array type fine-pitch applications (issues with small pad area).
- This presentation focuses on the testing of EN UBM's.



Electroless Nickel (EN) Process Flow



Electroless Ni/Au Process Flow

Silicon, Organics

Incoming

1) Pass Clean

Al_2O_3

2) Al Etch

3) Zincate

Zn

Zn - Al Replacement

4) Zn Strip

5) Zincate II

6) Ni Plate

Ni

Ni – Zn Replacement

6) Ni Plate Cont.

Ni

P

Ni/P Autocatalytic Reaction

6) Ni Plate Cont.

7) Gold Plate

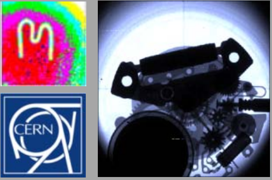
Au

Au/Ni replacement reaction

Source: Pac Tech publications, ref #62:
http://www.pactech.com/index.php?option=com_content&view=article&id=154&Itemid=21

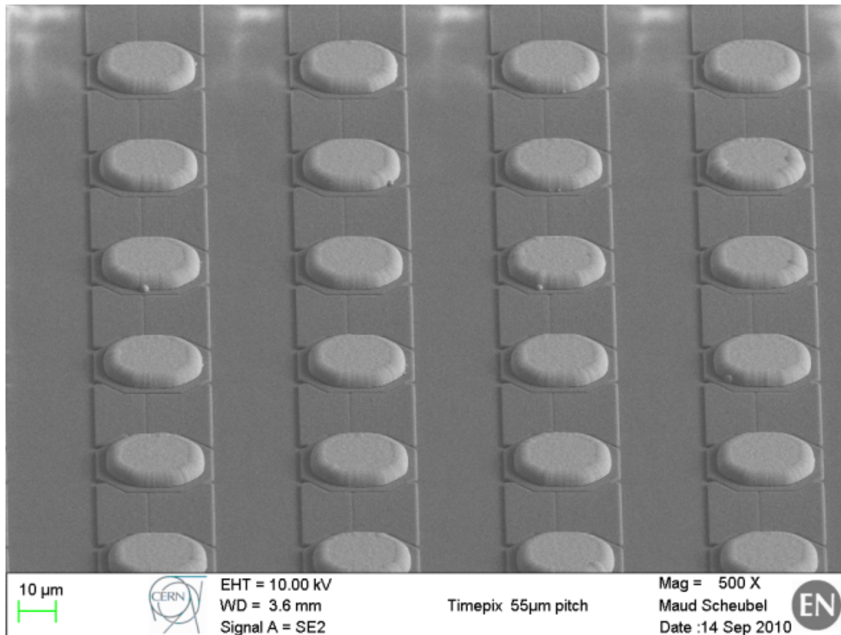
PAC TECH
PACKAGING TECHNOLOGIES

CERTIFIED ISO 9001: 2000 & ISO TS 16949 CONFIDENTIAL

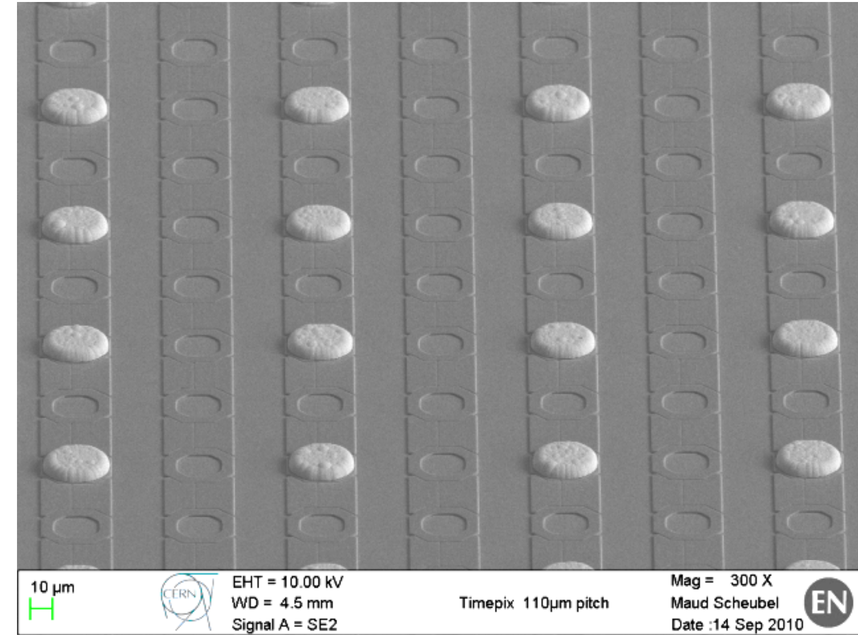


ENEPIG UBM Tests with Timepix Wafers

- Test vehicle wafers were used for gathering statistics from FC assemblies.
- Real CMOS wafers were processed with ENEPIG to see if the EN UBM process is feasible on real pixel wafers.
- ENEPIG UBM was grown on Timepix wafers with two different pitches
  - 55 µm – without photoresist mask
  - 110 µm – with photoresist masking. Chips were electrically measured after EN process – no degradation in electrical performance.

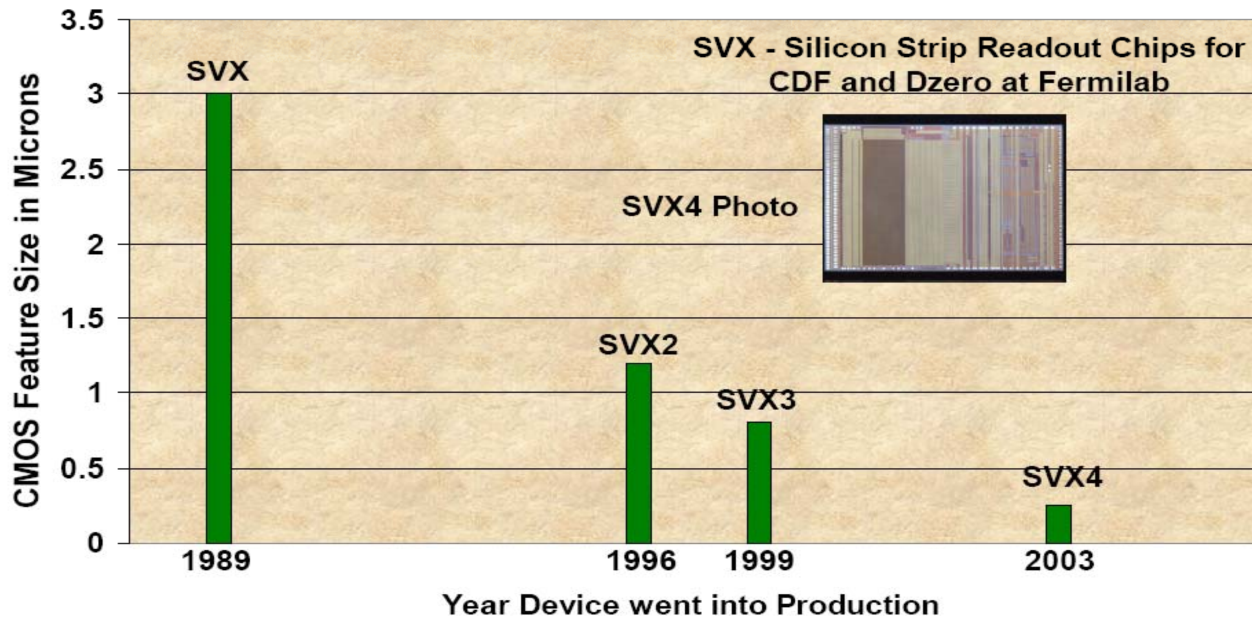


ENEPIG UBM pads on Timepix chip (55 µm pitch)

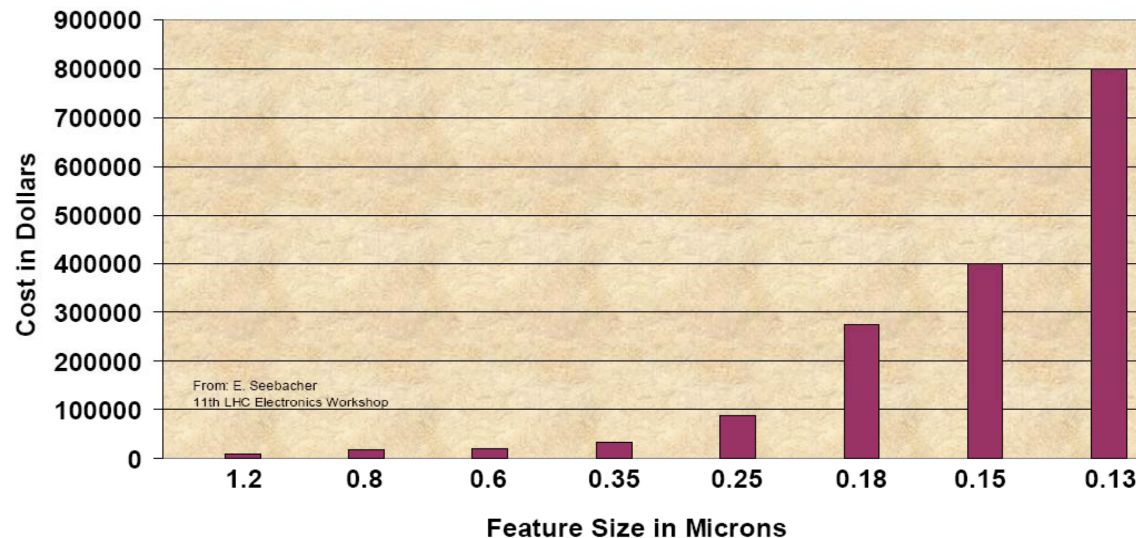


ENEPIG UBM pads on Timepix chip (110 µm pitch)

ASIC Fabrication



ASIC Fabrication Cost



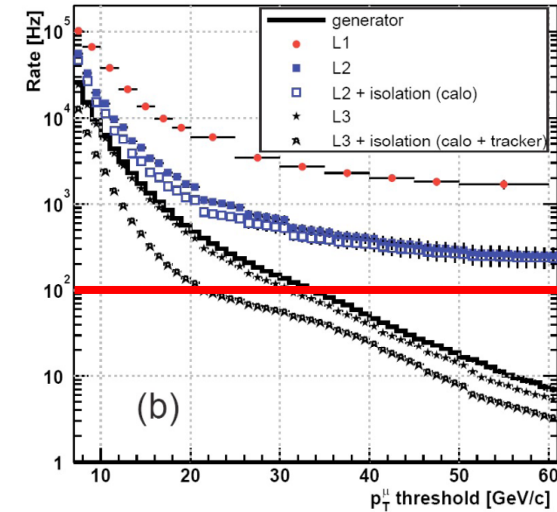
Can the HEP community afford the high cost of 0.13um and DSM for lower power, more functionality, more radiation tolerant, higher speed?
Wafer production isn't the issue; Mask cost is the major issue.
Share cost; work together; minimize number of iterations

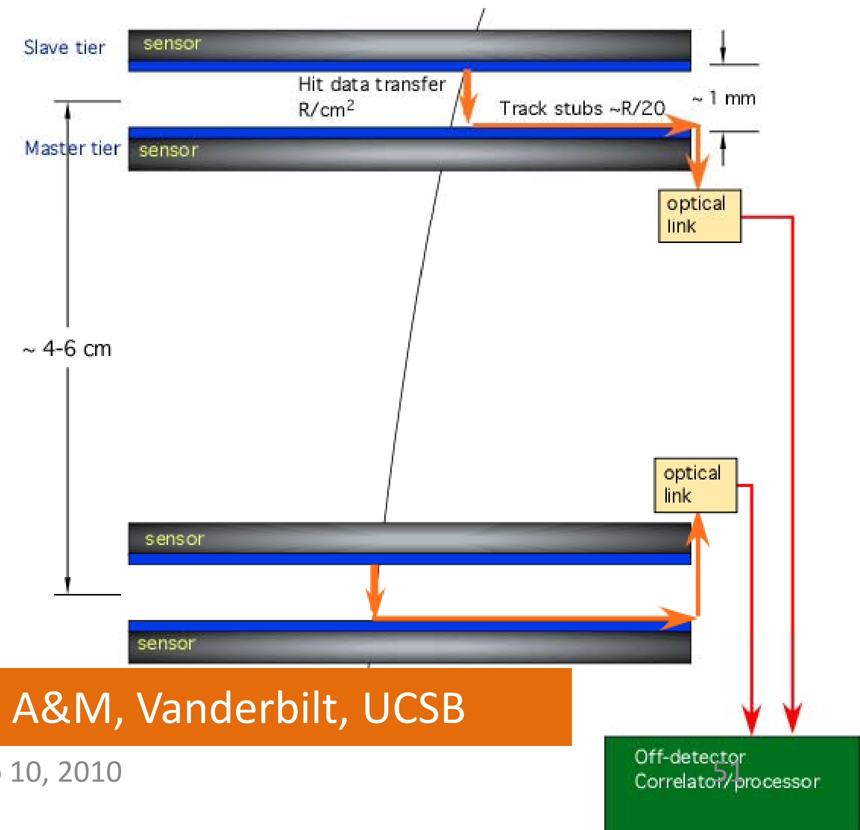
Impact of Triggering

- A track-based trigger for the SLHC is required
- The track based trigger could imply a big change in the way we think modules/pixel chip layout and readout architecture
- Will also have a big impact on cooling, data link, cabling, mechanical support, alignment, assembly

Track Trigger

- CMS L1 trigger will saturate at sLHC luminosities
- Tracker information at L1 trigger can maintain acceptable thresholds for μ, e and τ
- Requires the transmission of a huge data volume
- Use a vertically integrated design to filter out low Pt tracks and reduce data flow by >20. Curvature information can be analyzed locally $\Rightarrow$ minimize data transfer and power.
  - Stacked layers ~ 1mm apart provides Pt resolution
  - Local processing and local hit correlation



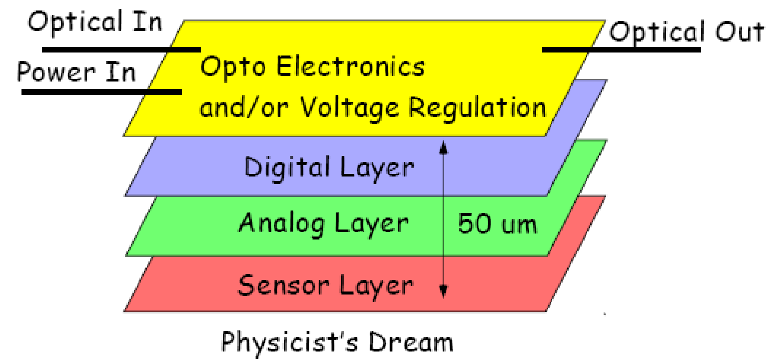


Brown, Cornell, Fermilab, UC Davis, Rochester , Texas A&M, Vanderbilt, UCSB

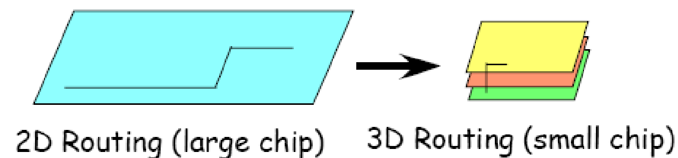
3D – Vertical Integration

3D Integrated Circuit Development

- A 3D chip is generally referred to as a chip comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded and interconnected to form a "monolithic" circuit.
- Often the layers (sometimes called tiers) are fabricated in different processes.
- Industry is moving toward 3D to improve circuit performance.
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power and crosstalk



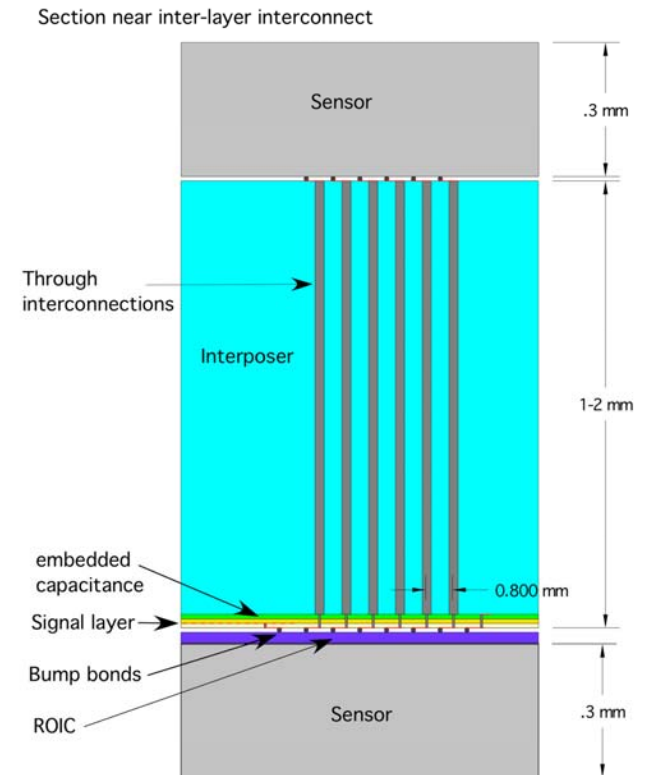
Physicist's Dream

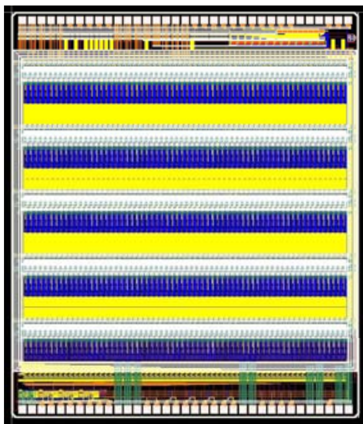


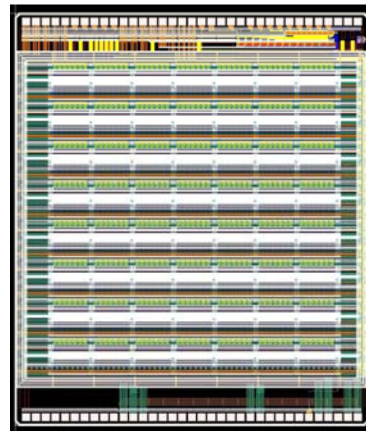
Cornell

3D Interconnection

- A single chip on the bottom tier can connect to both top and bottom sensors ⇒locally correlate information
- Enabled by "vertical interconnected" (3D) technology.
- Analog information from the top sensor is passed to ROIC through the interposer
- **VICTR Chip** intended to demonstrate the ingredients of a 3D-based track trigger







- One layer of chips ⇒No "horizontal" data transfer ⇒ lower noise and power
- Fine Z information is not necessary on the top sensor (~1 cm vs ~1-2 mm) strips can be used to minimize via density in the interposer

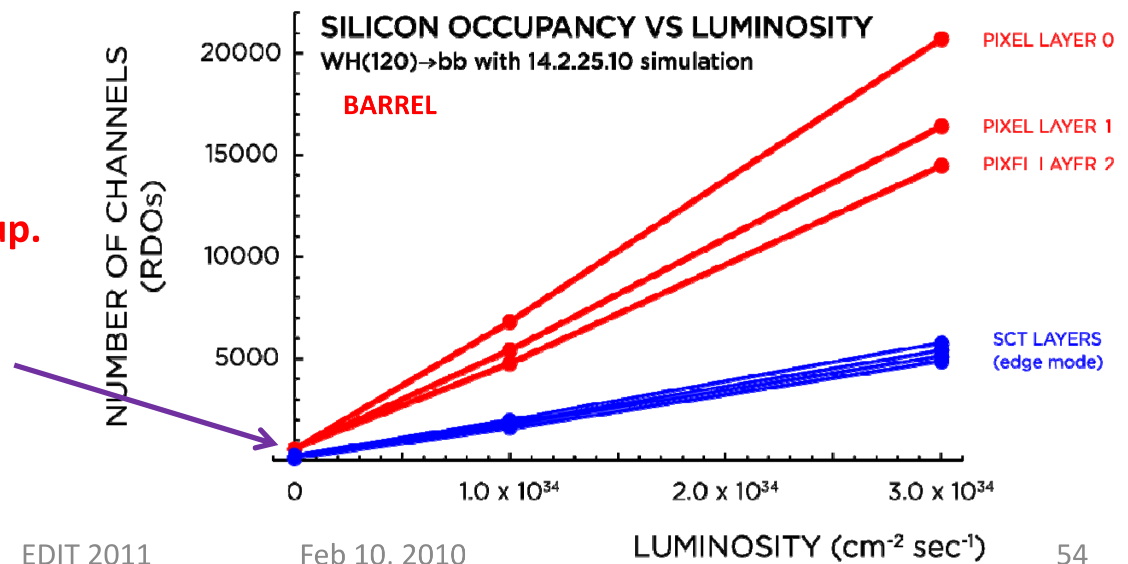
FNAL

ATLAS: Tracking in the Trigger at high $\mathcal{L}$: FastTracKer (FTK)

- Many/most new physics scenarios: final state with heavy flavor
  - Select *b*-jets and τ-jets from enormous QCD background $\Rightarrow$ tracking
  - FTK also provides significant improvement in ability to impose isolation requirement for leptons even at design luminosity.
- Baseline for $\leq 1\times10^{34}$: tracking in level-2 farm; uses 50-100% of mean L2 time/jet-cone, leaving little time for other needed event selection algorithms.
- FTK completes global tracking in 25 μsec at 3×10^{34}.
- Based on new Associative Memories (look simultaneously at an enormous number of track patterns stored in custom content-addressable memory). R&D is pursuing 3D silicon chip techniques.

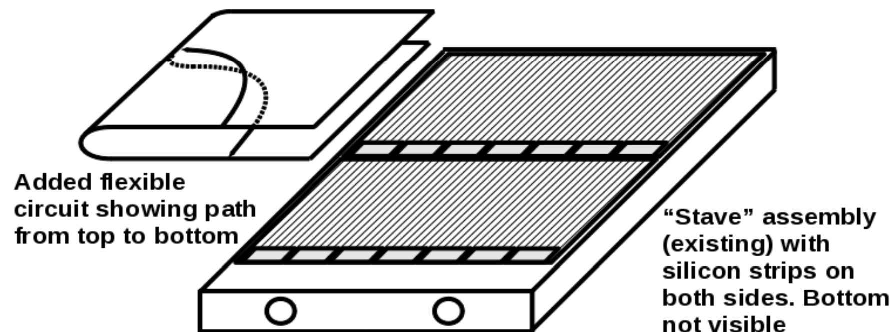
Tracking at high $\mathcal{L}$ is greatly complicated by enormous pile-up.

y intercept: all hits from the hard scattering interaction!!



Intelligent Trackers

- Community wide interest in increased functionality tracking layers for improving triggers in very dense high rate events.
- "Workshop on Intelligent Trackers" held at LBNL in Feb. 2010.
- 50 participants to from LHC experiments and beyond
- Proceedings to appear on JINST
- LBNL Plans: continue work on coupled layer design in collaboration with Uppsala



Continue development of Si + C-foam interposer wafers

Conclusions

- Hybrid Pixel detectors work well at the LHC
- Space point information opens up new possibilities in tracking and vertexing
- SLHC poses enormous technical challenges which would require a coordinated R&D effort in the community