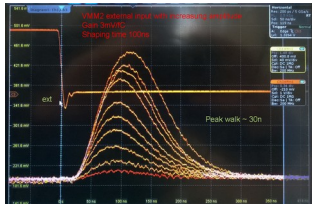# DRD1 Community Meeting WG5 Electronics

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Topics discussed in the Survey

- Analog/Digital Electronics
- Discrete Readout Front End Electronics and ASICs (strips/pixels)
- Charge/Photon readout
- FE input protection & spark quenching
- Waveforms and Digitizer
- Cluster Counting
- Signal Processing
- Specific needs: Timing, High rate, Low noise, Wide Dynamic Range,...)
- Grounding and shielding
- Calibration
- SoC based sensor readout
- General purpose DAQ, FPGA based readout/trigger and Trigger-less systems
- High Voltage Systems and High Voltage distribution schemes
- LV Powering
- Cooling
- Laboratory instrumentation (High resolution floating ammeters, Monitoring and control systems)

General view on the readout

Electronics Development

A. Yes: 33 (47.83%)

B. No: 36 (52.17%)

Yes
No

Do you have access at your institute to experts and services that can support common activities in the collaboration?

A. Yes: 39 (56.52%)

B. No: 30 (43.48%)

Yes
No

Would you be willing to contribute or support common developments in the context of the DRD1 collaboration?

A. Yes: 41 (59.42%)

B. No: 28 (40.58%)

Yes
No

Do you have experience and industrial contacts for custom made electronics production?

A. Yes: 30 (43.48%)

B. No: 39 (56.52%)

Yes
No

- ½ of the projects involved into electronics R&D. This coincides more or less with number of teams who have access to the electronic expertise in their labs, and are willing to contribute to electronic R&D.

- A bit less than ½ of the teams interact with industry to produce their electronics.

Readout type

A. Analog Electronics: 39 (6.21%)

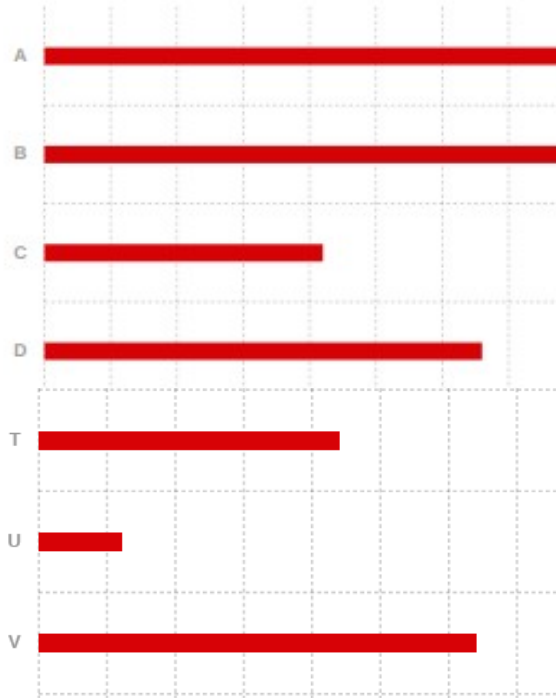B. Digital Electronics: 40 (6.37%)

C. Discrete Readout Front End Electronics: 21 (3.34%)

D. Multichannel Integrated (ASIC) Readout Front End Electronics: 33 (5.25%)

T. General purpose Data Acquisition systems: 22 (3.50%)

U. SoC based sensor readout: 6 (0.96%)

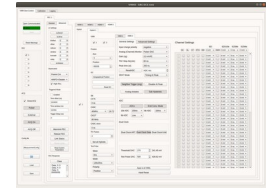V. FPGA based readout/trigger: 32 (5.10%)

example discrete electronics
preamp-shaper-pulser-trigger

example ASICs and
FPGA on one hybrid

SoCs for monitoring and
environmental sensing

General purpose DAQ

- A and B are basically clear everybody needs this
- Discrete electronics, intrinsically not scalable, however 21% interest means it is important
- ASICs and FPGAs shared equally, in practise probably one needs a combination of both
- Interest in a general purpose DAQ surprisingly low, shouldn't a standard DAQ be a common goal ?
- SoC have a small share of applications, though SoC (Arduino's etc) for sensing and IoT very common

Readout type

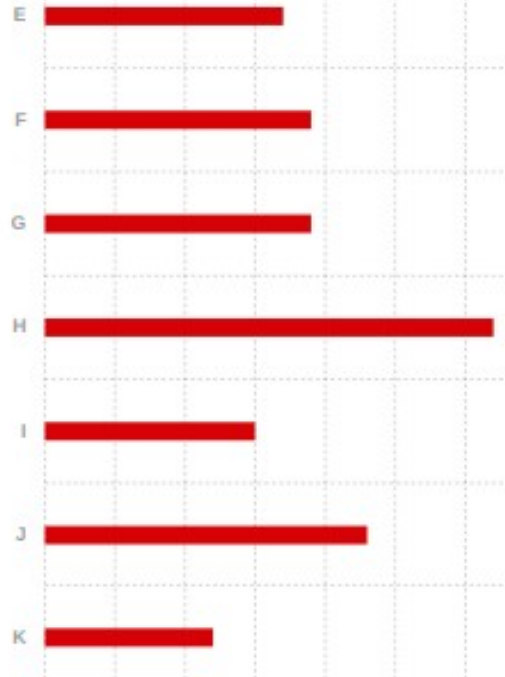E. Pixels: 17 (2.71%)

F. FE input protection: 19 (3.03%)

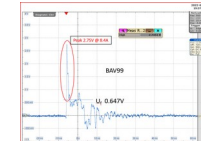G. Spark Quenching: 19 (3.03%)

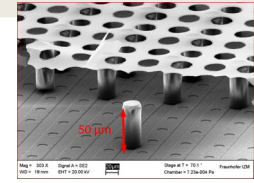H. Charge readout: 32 (5.10%)

I. Photon readout: 15 (2.39%)

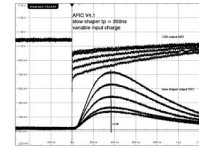J. Waveforms and Digitizer: 23 (3.66%)
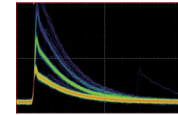
K. Cluster Counting: 12 (1.91%)

Gridpix

classic Diode protection

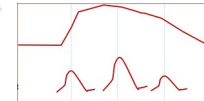CSA->shaper chain low noise charge conversion

SI-PM single photon resolution

ASIC	Year	Node	Time res.	Max sample/ch.	Channels
LABRADOR3	2005	250 nm	16 ps	260	8
BLAB	2009	250 nm	< 5 ps	65536	1
DRS4	2014	250 nm	≈ 1 ps	1024	8
PSEC4	2014	130 nm	≈ 1 ps	256	6
SamPic	2014	180 nm	≈ 3ps	64	16

waveform samplers

Charge cluster conversion: time resolution

Cluster counting more physics topic, electronics-wise covered by pixels with very high BW FADC readout
Pixels understood as GridPix, or are small pads are counted as pixels?
input protection & spark quenching unless already contained in ASICs, an issue for most gas detectors
charge / photon RO: 2 complementary paradigms of electronic amplifier and optics sensor or SiPMs.
Waveform digitizers: a.) TPC & cluster counting b.) ASICs with digitizer / shaper like SAMPA, c.) waveform samplers for R&D on pSEC
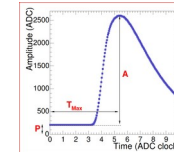
External requirements

L. Signal Processing: 21 (3.34%)
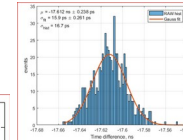
M. Timing: 31 (4.94%)

N. High rate: 31 (4.94%)

O. Low noise: 33 (5.25%)

P. Wide Dynamic Range: 25 (3.98%)

100ps resolution from 100 ns semi-gauss peak via offline signal processing CMS EMCal)
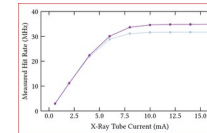
17 ps SAT time with pSEC, RD51 GDD lab

High rate hit at X-ray source (GDD VMM)
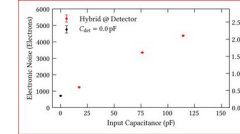
ENC noise vs Cdet (VMM)
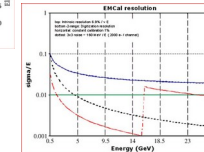
Large (14 bit) dynamic range via 2- gain readout (ALICE EMCal)

diverse electronics requirements more or less equally distributed for different types of detectors, optimizations like time resolution, space resolution, high rate, low noise or large dyn range. May not necessarily exclude each other and can partially be implemented with same ASICs, example: large dyn range can be implemented by sacrificing every 2nd channel of a standard ASIC for High + Low gain, If not possible, new specific ASICs may be required: keep an eye on new ASIC developments

Q. Grounding and shielding: 25 (3.98%)

R. Calibration : 23 (3.66%)

S. Triggerless systems: 25 (3.98%)
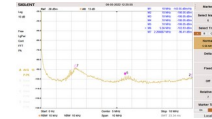
noise spectrum in GDD lab

Calibration

Peak ratio not 2:1

3000:1100
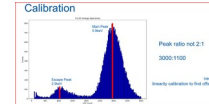
standard Fe-55 calibration

Pro Triggerless	Contra Triggerless
1. No external trigger HW	1. Higher threshold levels needed
2. high readout efficiency	2. Higher accidental events
3. full angular coverage	3. Noisy channel mask mandatory
4. high trigger rates*	4. More SW overhead for eventbuilding
5. Pattern injection (event, time)**	5. Runtime limit*= timestamp overflow

- Q and R are a standard for every laboratory or experimental setup. Noise optimization strategies exists but also depends on environment. Calibration methods span from simple detector calibration methods (Fe55 peaks) to advanced methods using testbeams with particles
- S triggerless requirement for either high rate but also rare event detectors. Triggerless has pros and cons' Example triggerless require higher threshold above baseline. ASICs with both
- triggerless and triggered exist (example VMM)

Services and monitoring

W. High Voltage Systems and High Voltage distribution schemes: 22 (3.50%)

X. High resolution floating ammeters: 7 (1.11%)

Y. Monitoring and control systems: 21 (3.34%)

Z. Dedicated lab instrumentation: 15 (2.39%)

AA. LV Powering: 7 (1.11%)

BB. Cooling: 12 (1.91%)

active voltage divider proto NIM module 2016

Femtometer 10 fA-1uA log. readout 2014

VMM monitoring and control panels 2022

280nm LED pulser 12V@ 500ps, 2022

2023 power box VMM frontend 40W from 12-33V input

2019 multipurpose cooler for VMM: convection and water
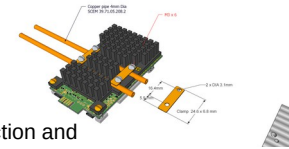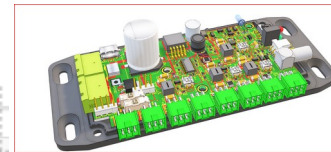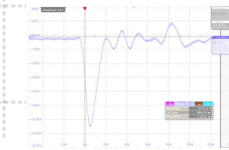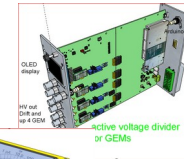
W…BB looks like many of these could be purchased ? If not, many special developments have been prototyped over years. Some examples shown.
Should we make a survey to see what is available, which methods have been used and which developments should be prioritized for the community?

Summary 69 teams: expressed preferences electronics

high rate – low noise –high Cd -large dyn range- multichannel –low power (7)
future SRS : low noise@ 1fC, optical RO links, neg. Ion TPC, selective trigger in FPGA , opt. camera RO
plug&play, longterm support, triggerless and triggered RO, user friendliness, configurable,
better quality assurance, guaranteed ASIC access (8)
SRS frontends (APV, VMM, Timepix, SAMPA, + gen purpose, + very high Cd detector) (4)
HV instrumentation and HV distribution (2)
WeROC-based systems , OMEGA ASICs (2)
RO systems Radhard – low power – high speed ASIC (2)
Analogue FE with spark protection (AVP) (1)
Fast timing support (1)
Photon detector SiPMs with bias Gen. (1)
Mux'ed readout MM and TPC's (1)
Fast FE ASICs for RPC and Drift (1)
GET based electronics (1)
FPGA based RO of Drift tubes (1)

Some citations in comments

*"We are **willing to collaborate on a joint initiative that makes use of all of our resources**. Possible projects with DRD collaborators will help us to take responsibility and give more contributions"*

*"We are intersted in having electronics like **APVs and VMM with SRS like system or equivalent**. For **RPCs we are intersted in WeROCK based systems.** We are also considering to **explore in future possible fast electronics (~50 ps)** for possible fast timing detectors"*

*"..Tried to explore different approaches (VMM, tiger, based, etc..) imply full time resources. Appreciated the effort to establish new standard based on VMM. **We see that several groups are designing new "optimal chips for mpgd", likely in a sort of disconnected way.** An effort should probably be made within the community **towards a new standard of front-end electronics + DAQ for MPGD operation at high rates, with low noise and high dynamic range"***

2022: SRS: from detector to Online

The Scalable Readout System SRS with VMM frontend, so far implemented as a triggerless, multichannel readout system for gas and photon detectors. Triggered readout planned for 2023.

SRS crates
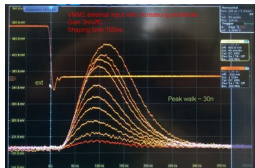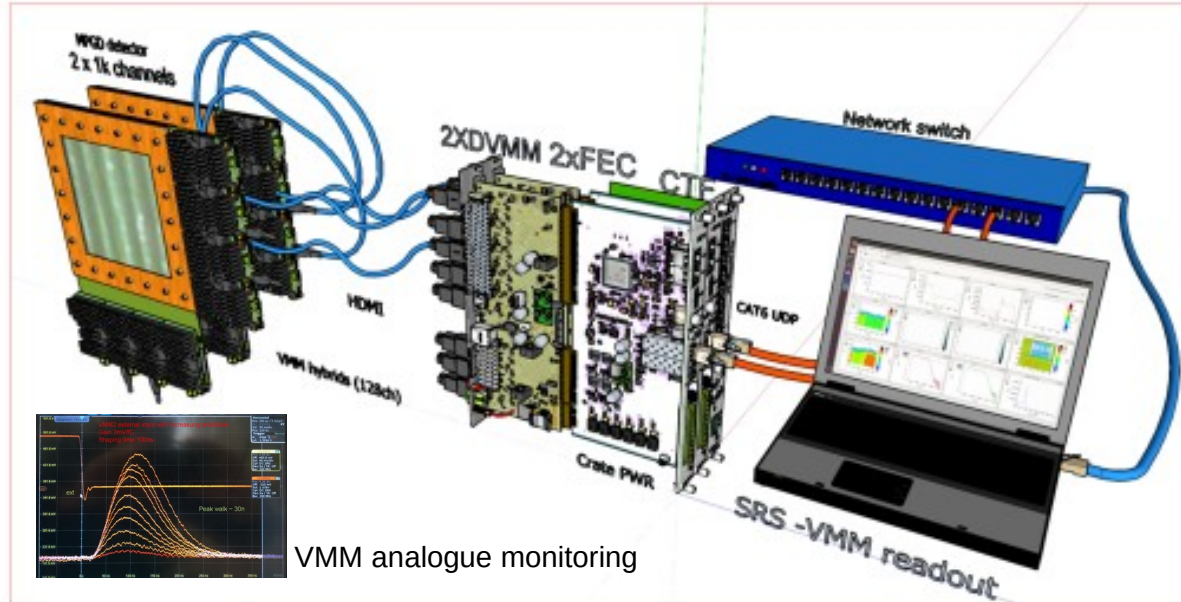
VMM analogue monitoring

DAQ and slow controls

1 FEC for 8 VMM hybrids / 1024 detector channels connected via HMDI AD cables to DVMM. 2 FEC's with CTF (common clock) for 16 hybrids , 2048 ch. DVMM cards with octal HDMI connector including 70 W power for 16 VMM hybrids. Power / housing for 2 FECs and CTF via 1 Minicrate (not shown). 1 GB Ethernet /UDP uplink from FEC to Network via SFP+ jack, fiber or optical 1 GBE for network with Jumbo packet support. ESS DAQ Software with Vmm Controls tb. installed under Linux.

3
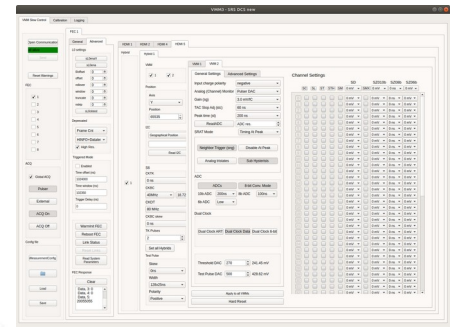
eFEC , future backend of a scalable RO architecture

New features:

1 eFEC: max 64 FE- hybrids @ 128ch (8k ch) with 8 x FE uAssister cards and 8 powerboxes

FE links to uAssister fibre or copper

Backwards compatible with FEC with 8 HDMI link (legacy)

Horizontal + Vertical RO architectures

Sync and Xrosslink buses

SoC plugin for development and diagnostics

1 Single card to fit in SRS crates
Minicrate : 2 x eFEC
Eurocrate : 8 x eFEC
Power: SATA only

Output up 40 Gbps to network switch

realtime triggers over all channels (custom Firmware)

8x copper FE HDMI links (legacy HDMI links)

P1 P2 power

USB (to SoC)

NIM-In/Out

CTF clk RG45

1x SFP 5/10 Gbit vertical architecture option

SYNC-bus 2 x 8pin

Opt fibre

SFP plugin 6 x 5/10 Gbit
6x FE links

Up to 4 x SFP plugin 4x 10Gbase UDP to Online

1 x 1000Base SFP Ethernet:
Controls or embedded cores

XCZU7CG Ultrascale Zync

X-link 2x RG45
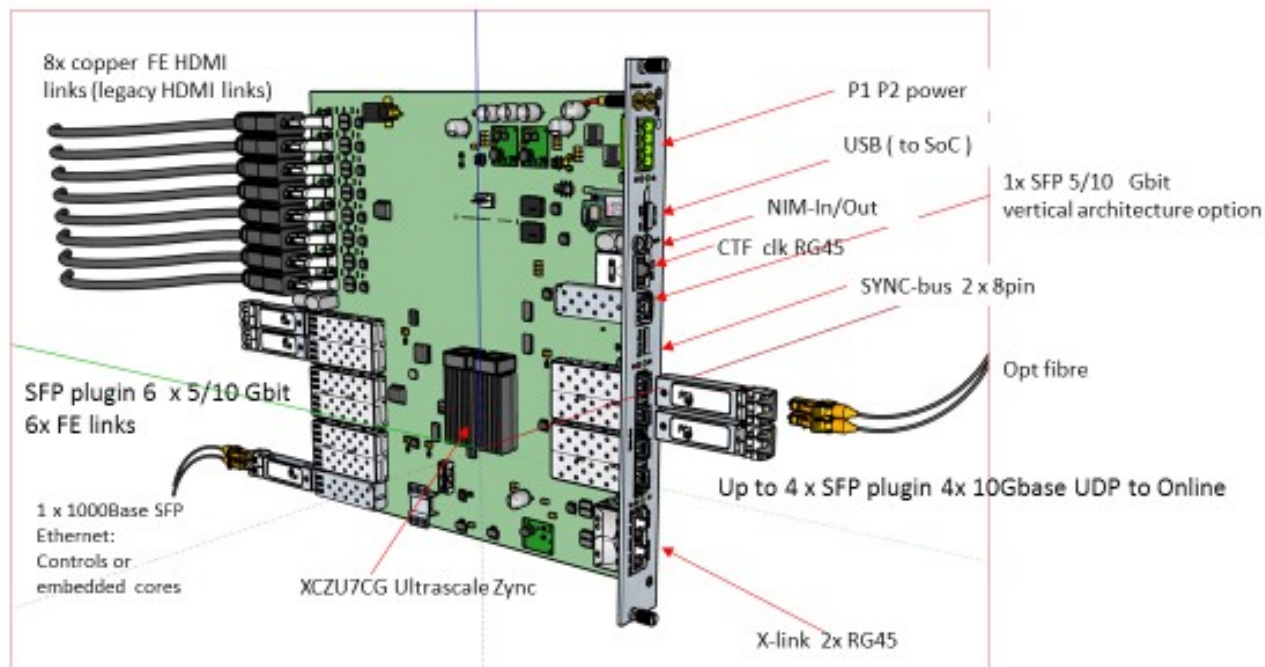
OMEGA ASICS

- French OMEGA laboratory ASICS distributed by WEEROC under the CAEN umbrella.

  Few chips availables for gas detectors are described below:

  GEMROC: for GEM/MICROMEGAS

  dynamic range 1-500 fC, semi-digital with 3 thresholds.

  64 channels. Time stamping 200ns.

  PETIROC2C (iRPCROC): for RPC

  20 fC - 3 pC, 32 channels (used with 16 channels to reduce X-talk). Fast preamp for time stamping with 30 ps resolution.

  Other chips are for calorimetry (HARDROC, HGCROC), SiPM (CITIROC) etc…

  Some publicly available

  https://www.weeroc.com/products/see-catalogue

  Some under development

  https://portail.polytechnique.edu/omega/fr

  Many chips are AMS 0.35 µm technology.

  Recent chips from 2019 are TSMC 130nm

  (LIROC improved version of PETIROC2C)

Electronics in RPC

Various custom systems are used for RPC projects:

ALICE Multigap GRPC:

    CERN developed ASIC NINO + readout board with Xilinx FPGA for T

https://kt.cern/sites/default/files/technology/nino/tech-brief/ninonew.pdf

10 ps time jitter; input signal 30 fC - 2 pC; LVDS signal

Used also for EEE project, prospected for NIKA

CMS iRPC:

Petiroc2C ASIC + readout board with Cyclone V FPGA with TDC. Optical readout.

https://indico.cern.ch/event/1123140/contributions/5002734/attachments/2518292/4329952/CMS%20iRPC%20FEB%20development%20and%20Validation.pdf

ATLAS RPC: custom pre-amplifie, discriminator TDC based on SIGE 130 nm technology.

Directly soldered on the strip PCB. Threshold sensitivity down to 1 fC.

https://indico.cern.ch/event/1123140/contributions/4994337/attachments/2518449/4330185/RPC2022_LP.pdf

Many more: CMS RPC, KODEL, ILC SD-HCAL
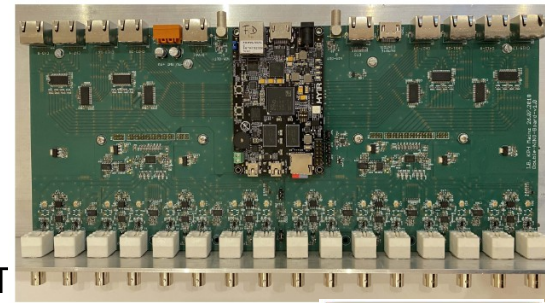
A. Detector Characterization Laboratory: 57 (12.87%)

B. Manufacturing and Production Workshop: 27 (6.09%)

C. Assembly Facilities: 35 (7.90%)

D. Clean Rooms: 57 (12.87%)

E. Gas system design and production: 30 (6.77%)

F. Mechanical Workshop: 52 (11.74%)

G. Electronics Workshop: 45 (10.16%)

H. Analysis Laboratory: 18 (4.06%)

I. Metrology Laboratory: 12 (2.71%)

J. Radioactive Sources (active, passive): 56 (12.64%)

K. Irradiation Facilities: 25 (5.64%)

L. Test Beam: 19 (4.29%)

M. Other: 10 (2.26%)
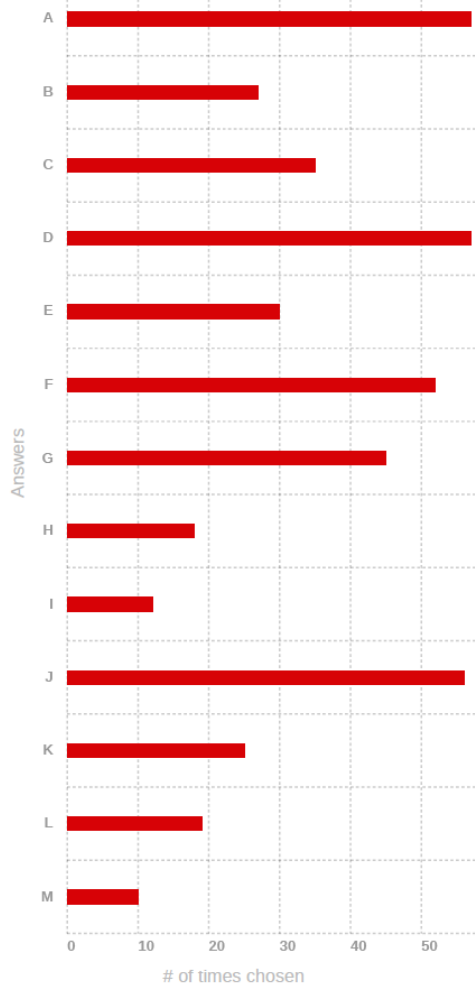
G. Electronics Workshop: 45 (10.16%)

- community has a rich offer of possibilities which can be exploited for
- development of a common electronics
- irradiation facilities and testbeam possibilities for electronics qualification
-

Answers

# of times chosen

Taking a look at the ECFA - matrix

electronics:
 R&D roadmap symposium
 https://indico.cern.ch/event/1001692/

Task force 1 Gas detectors April 29 2021
https://indico.cern.ch/event/999799/

What can we extract from this for electronics?
Does it cover the needs of the gas community
What has to be added
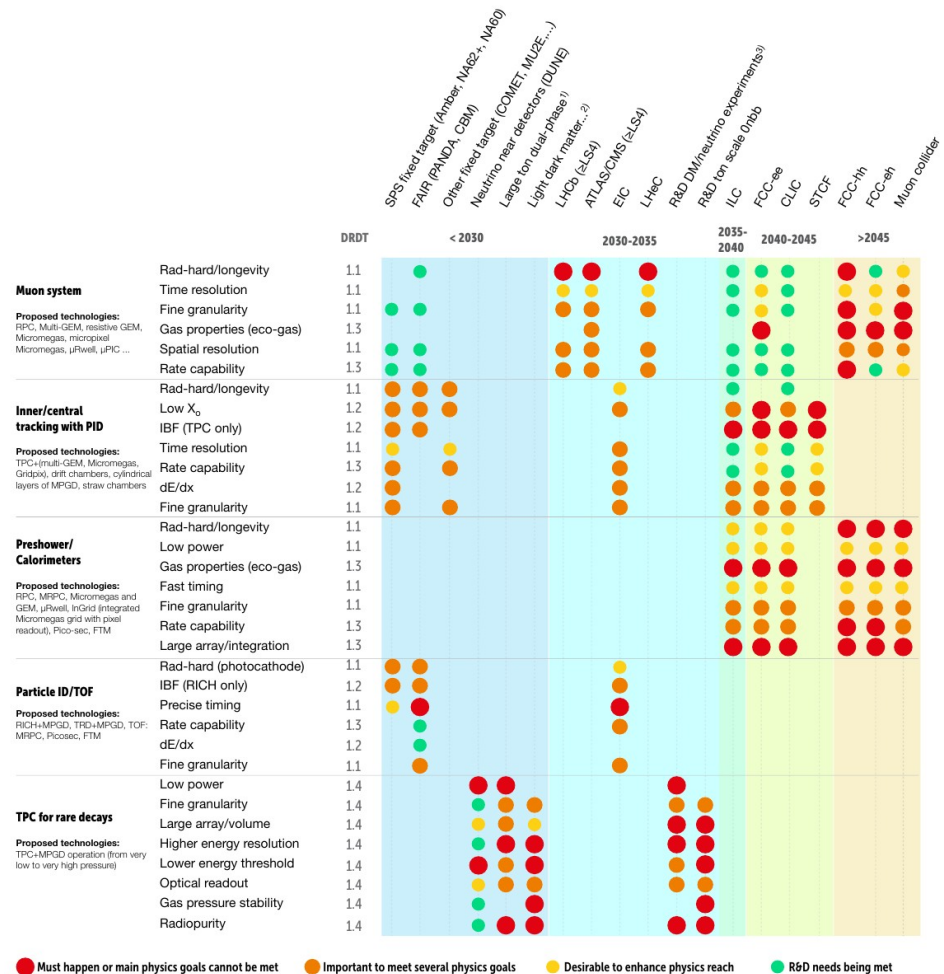
ECFA priorities electronics

Gas detectors:

Low noise @ high detector capacitance [*RICH, PICOSEC, TP*C]

Ultra low noise [*TPC rare events*]

High data and trigger rates [*ALICE , LHCb*]

Low noise (< 400 e-) [*RPC, ATLAS Muons*]

Cluster counting 4D (in t and x => higher dE/dx) [*future e+e- colliders*)

Time resolution (15-20 ps) [*TOF, Cerenkov, MRPCs*]

Continuous readout [*FTM or PICOSEC*]

IBF minimization [*RICH and PICOSEC*] *both in detector and electronic filters*

Input protection [*all gas detectors*]

General focus:

Dedicated FE electronics, connectivity, cooling, accessibility, replacability [all compact detectors]

items in red: where does this fit with listed activities in DRD1 electronics

ECFA electronics in general (all detectors)

ASICs status 2022: ca 40 dedicated ASICs 65 and 130 nm -> can we get a summary of these

  => next gen. ASICs 28 nm CMOS

• Higher data rates, fibre readout links, power management -> SRS upgrade, eFEC and new frontends

• Higher readout efficiency, advanced data reduction (ML in FPGA) -> eFEC's major issue: trigger processing in FPGA

• Flexible frontends (programmable FPGA cores in RO ASIC) -> so far we have ASIC + FPGA in the frontend

• 50 ps timing resolution to become standard -> look for ASICs with this feature , integrate in frontend

• Larger dyn range @ higher linearity -> 8..10 bit standard with 1.2V Vcc, extension to 12 bit by sacrificing 50% of channels

FE Power: 2022 LHC hundreds of kW

• New DCDC conversion techniques, coils don't work in B field, capacitor based ?

                             -> new high eff. buck converters with integrated coils in VMM powerbox, B-field be tested

• Better power management, serial power, dynamic power etc

    -> gas detectors ? so no known activity in this domain

Chip matrix MPGD's 2021 (https://indico.cern.ch/event/1040996/timetable/#20210614)

Name	Exp	Detectors	£Ch	Shaping	Noise	Range [ke]	Input signal	Pol.	ADC [#bits]	fs [MHz]	P/ch [mW]	Feature	Technology	Radhard
AFTER	T2K; T2K upgrade	TPC, micromegas end-plate	72	50-1000	(350-1800)e +(22-1.8)e/pF	4 ranges: 750/1500/2250/3800	current	both	external 12-bit ADC	1 to 50 SCA sampling	8	SCA	0.35 μm CMOS	N.D.
AGET	ACTAR, AT-TPC, SπRIT	MGPD+DSSD	64	25-500	(435-34000)e +(19-7.4)e/pF	4 ranges: 750/1500/6240/62400	current	both	external 12-bit ADC	1 to 100 SCA sampling	10	SCA; Triggerless; selective readout	0.35 μm CMOS	N.D.
DREAM	CLAS12	MGPD	64	25-450	(394-2140)e + (10-0.34)e/pF	4 ranges: 312/624/1248/3744	current	both	external 12-bit ADC	1 to 50 SCA sampling	10	SCA; Trigger	0.35 μm CMOS	N.D.
GEMROC	(Client under NDA)	GEMs	64	30-200	N.D.	1fC -> 500fC	charge	negative	N.D.	40MHz	1mW	//	0.35 SiGe	N.D.
HARDROC3	ILC CALICE sDHCAL	RPC	64	50-150 (Q) 20 (T)	N.D.	10fC -> 50pC	current	negative	N.D.	50MHz	1mW	Zero Suppression	0.35 SiGe	N.D.
PADI-X	CBM	RPC, Diamond, Straw Tubes, Silicon, Micro-Channel Plates, Channel Electron Multiplier, Scintilation, PMT	8	0	N.D.	1 fC - 2 pC	current	pos/neg	external	//	16.8	Setable Input impedance: 50 - 400 Ω	CMOS UMC-180 nm	2.4
PADI-XI	CBM	//	8	2.5-17	N.D.	1 fC - 2 pC	current	pos/neg	external	//	22	Setable Input impedance: 18 - 250 Ω	CMOS UMC-180 nm	2.4
PADI-XII	for future experiments	//	8 or 4 channels	2.5-17	N.D.	1 fC - 2 pC	current	pos/neg	external	//	24 for LED / 32 for PSA	Setable Input impedance: 18 - 250 Ω	CMOS UMC-180 nm	2.4
PETIROC2	CMS Muon	RPC (was designed for SiPM)	32	25-100 (Q)	N.D.	1mV (~1pe)	voltage	both	10 bits	N.D.	6mW	//	0.35 SiGe	N.D.
SAMPA_v4	ALICE	TPC-GEM / MCH-MWPC	32	160/320	550e+25e/pF	400/600 (@160ns) 3100 (@300ns)	charge	pos/neg	10 bits	10 MHz	20	Z.S. Baseline correction. Huffman.	130 nm	N.D.
SAMPA_V5	sPHENIX	TPC-GEM	32	80/160	550e+25e/pF	400/600	charge	pos/neg	10 bits	10/20 MHz	20	Z.S. Baseline correction. Huffman.	130 nm	N.D.
STAGE	HARPO	MGPD+DSSD	64	25-4000	(435-34000)e +(19-7.4)e/pF	4 ranges: 750/1500/6240/62400	current	both	external 12-bit ADC	1 to 100 SCA sampling	10	SCA; Triggerless; selective readout	0.35 μm CMOS	N.D.
STS/MUCH-XYTER2.2	CBM Experiment at FAIR	Microstrip silicon detectors at Silicon Tracking System, GEM detectors at Muon Chamber	128	90-260	550e+25e/pF	624ke with for GEM, 75ke for Silicon	charge	pos/neg	5	continuous-time	10	BaselineCorrection / PeakFinding	UMC 180 nm CMOS	N.D.
VMM3a	ATLAS	New small wheel, sTGC, Micromegas	64	25-200	depends configuration	2pC at 0.5mV/FC, in linear range	charge		3 ADCs per channel, 10b, 8b, 6b	200ns conv. time	~11mW	data driven, Baseline stabilization, neighbouring logic, fast digitisation, Peak Finding, timing information, and many more	130nm GF	>300kRad
WASA	CEPC	TPC, GEM	16	160	533e +9.1e/pF	748.8	charge	negative	10	100M max.	2.33	direct waveform output	65nm CMOS	N.D.

Our Idea of 'Assets'

Collaboration:

   Provide the platform and long term experience for developing common electronics (tools)

   Everyone is adding some parts and can profit from the efforts of all

   Collaboration could provide resources for the development

Institutes: Provide tools, knowhow, work power and small amounts of funding for realizing the plans

Start: Collecting the requirements and lay out a plan for covering (most of) them

   Need a collection of different ASICs

   Feedback of our community to the ASIC designs to take care of gaseous detectors

Funding / Financial support

=> Same challenge as in many other topics (e.g. simulation):

funding for detector electronics is difficult to get, if it's not for a big experiment

Sofar, SRS has been funded by common fund and groups, that needed specific parts first.

There are some general ideas:

- European grant programs
- Create work packages
- Income from royalties
- Sufficient 'in collaboration' resources to build prototypes with minimum funding?

Summary

- We have a wide field to cover - not only readout electronics, but also more standalone application like HV, current monitoring and other electronic interfaces
- Survey was somewhat inconclusive: No strong demands for any specific developments, but many diverse requests / suggestions
- Interest in a more advanced common readout system seems largest denominator.
- Survey shows a strong interest in participation of many institutes in development and many 'in house' possibilities for production and testing
- Still merging of communities has only started, common needs and requirements are still to be evaluated and identified
- Still need your input: Any comments?