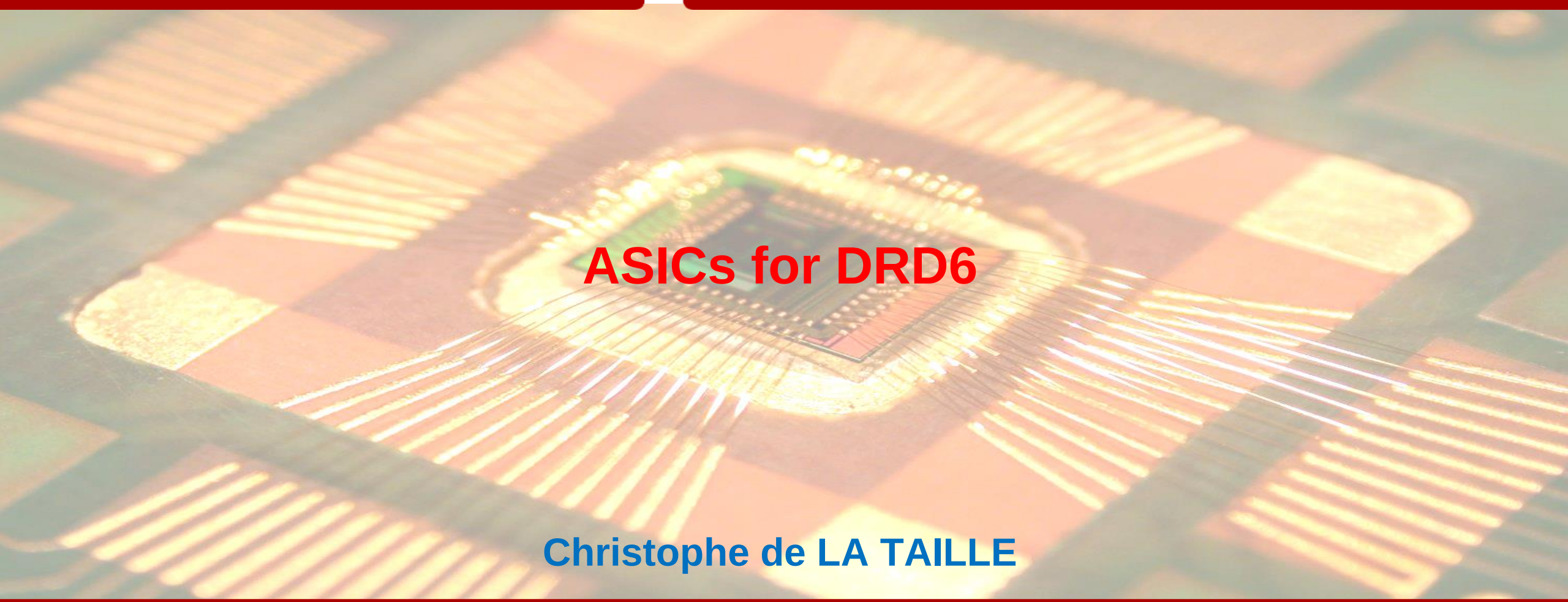

ASICs for DRD6

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DRD6 readout schemes

Name	Track	Active media	readout
LAr	2	LAr	cold/warm elx"HGCROC/CALICElike ASICs"
ScintCal	3	several	SiPM
Cryogenic DBD	3	several	TES/KID/NTL
HGCC	3	Crystal	SiPM
MaxInfo	3	Crystals	SIPM
Crilin	3	PbF2	UV-SiPM
DSC	3	PBbGlass+PbW04	SiPM
ADRIANO3	3	Heavy Glass, Plastic Scint, RPC	SIPM
FiberDR	3	Scint+Cher Fibres	PMT/SiPM,timing via CAENFERS, AARDVARC-v3,DRS
SpaCal	3	scint fibres	PMT/SiPMSPIDER ASIC for timing
Radical	3	Lyso:CE, WLS	SiPM
Grainita	3	BGO, ZnWO4	SiPM
TileHCal	3	organic scnt. tiles	SiPM
GlassScintTile	1	SciGlass	SiPM
Scint-Strip	1	Scint.Strips	SiPM
T-SDHCAL	1	GRPC	pad boards
MPGD-Calo	1	muRWELL,MMegas	pad boards(FATIC ASIC/MOSAIC)
Si-W ECAL	1	Silicon sensors	direct withdedicated ASICS (SKIROCN)
Si/GaAS-W ECAL	1	Silicon/GaAS	direct withdedicated ASICS (FLAME, FLAXE)
DECAL	1	CMOS/MAPS	Sensor=ASIC
AHCAL	1	Scint. Tiles	SiPM
MODE	4	-	-
Common RO ASIC	4	-	common R/O ASIC Si/SiPM/Lar

Trends for calorimeter readout

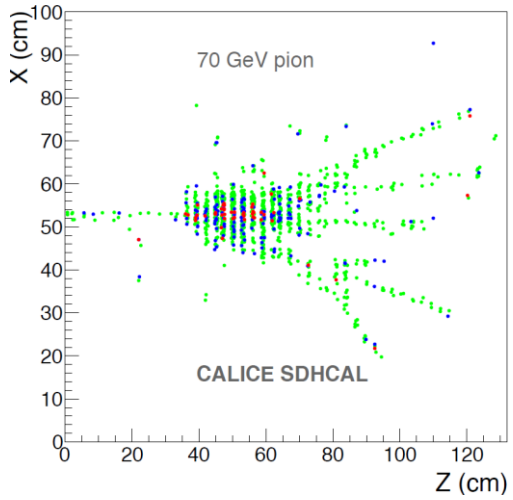
- On-detector embedded electronics, low-power multi-channel ASICs
  - CALICE SKI/SPI/HARDROC, FLAME, CMS HGCROC, FCC Lar, FATIC…
  - Challenges : #channels, low power, digital noise, data reduction

- Off-detector electronics : fiber/crystal readout
  - Wavefrom samplers : DRS, Nalu AARD, LHCb spider…
  - Challenges : low power, data reduction

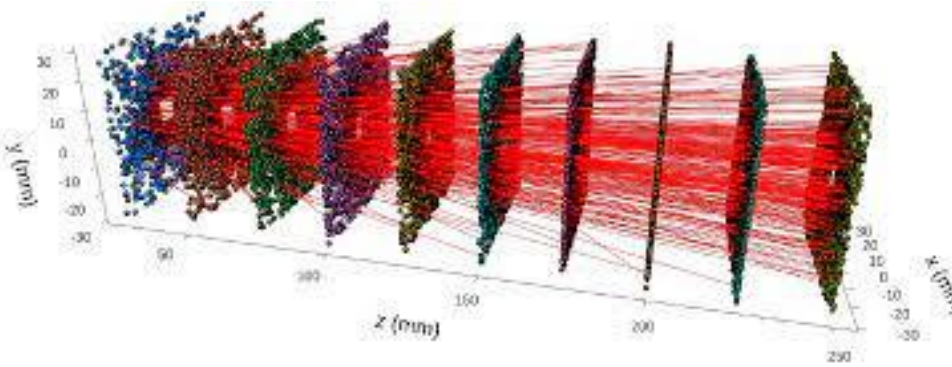
- Digital calorimetry : MAPs, RPCs…
  - DECAL, ALICE FOCAL, CALICE SDHCAL
  - MAPS for em CAL : eg ALPIDE ASIC for FOCAL, DECAL…
  - Challenges : #channels, low power, data reduction

Digital calorimetry

- Hadronic : e.g. CALICE RPCs or µmegas
  - ~1 cm² pixels, low occupancy, ~1 mW/cm²
  - Performance improvement with semi-digital architecture
  - Timing capability can be added



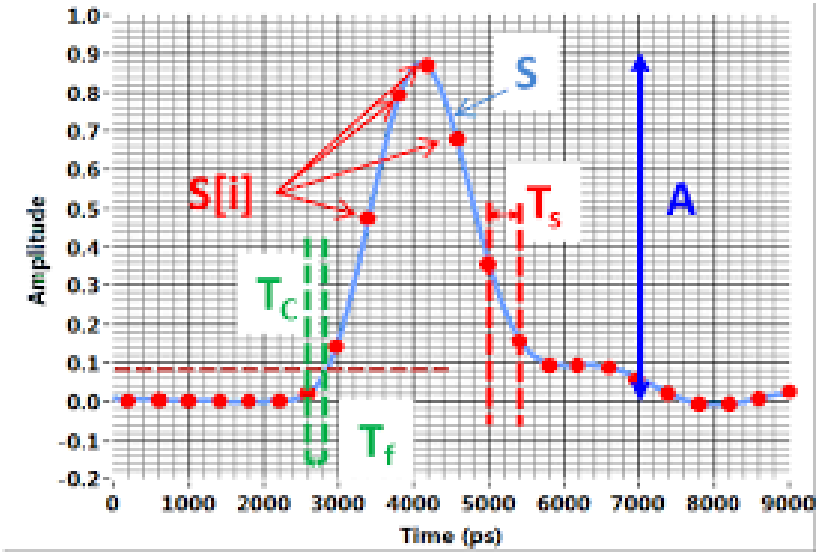
- Electromagnetic : e.g. DECAL, ALICE FOCAL…
  - Based on ALPIDE : (50µm)² pixels, high occupancy, ~ few 100mW/cm², slow
  - To be compared with embedded electronics ~10 mW/cm²
  - Most power in digital processing => would benefit a lot from ≤ 28 nm node
  - Semi-digital and/or larger pixels coudl be an interesting study

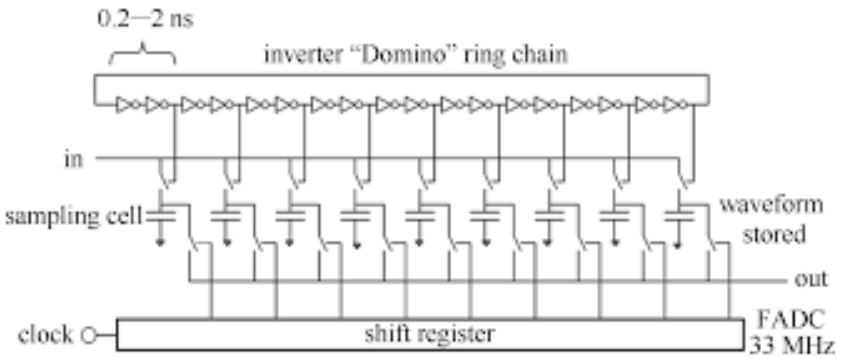


Waveform sampling

- Switched capacitor arrays (DRS4, Nalu, SAMPIC…)
  - Pulse shape analysis
  - High accurcay timing, digital CFD
  - Sizeable power to provide GHz BW on large capacitance
  - large data volume

- Often used in off-detector electronics
  - Space and cooling available
  - Small/medium size detector readout and/or characterization





Common readout ASICs proposal [AGH, Omega, Saclay]

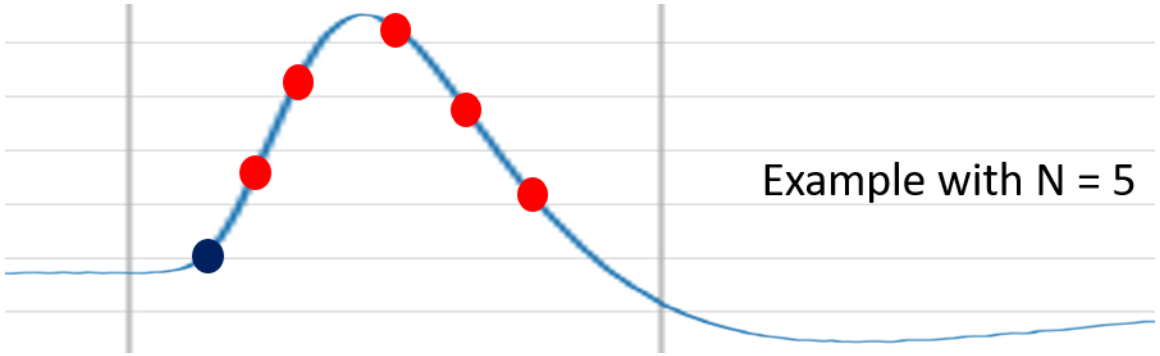
- Develop readout ASIC family for DRD6 prototype characterization
  - Inspired from CALICE SKIROC/SPIROC/HARDROC/MICROROC family
  - Targeting future experiments as mentionned in ICFA document (EIC, FCC, ILC, CEPC…)
  - Addressing embedded electronics and detector/electronics coexistence + joint optimization
  - Detector specific front-end but common backend

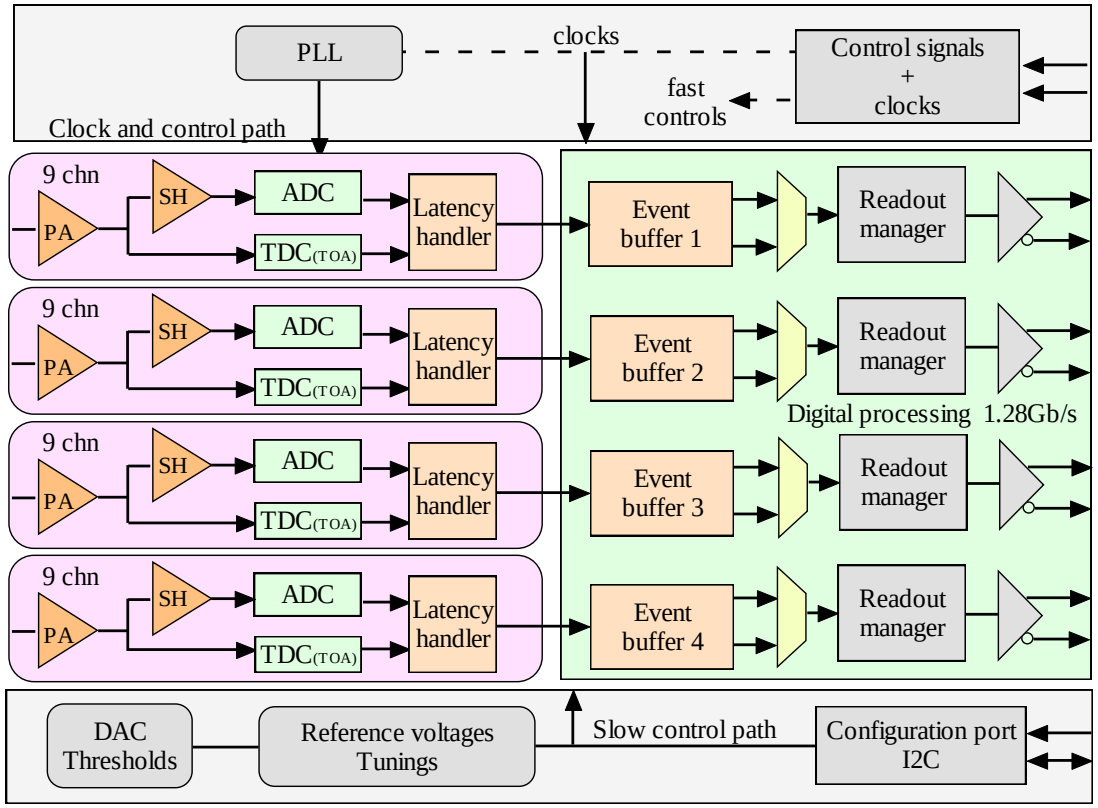
  $\Rightarrow$ allows common DAQ and facilitates combined testbeam

- Start from HGCROC / HKROC : Si and SiPM
  - Reduce power from 15 mW/ch to few mW/ch
  - Allows better granularity or LAr operation
  - Extend to LAr (cryogenic operation) and MCPs (PID)
  - Remove HL-LHC-specific digital part and provide flexible auto-triggered data payload
  - Several improvements foreseen in the VFE and digitization parts

HKROC : starting chip

- HKROC is 36 channels: 12 PMTs with High, Medium and Low gain
  - Or 36 PMTs with one gain
  - Charge measurement with 10 bit ADC
  - Time measurement with 25 ps binning
  - Readout with high speed links (1,28 Gb/s)
  - Hit rate ~400-1000 kHz/ch in average
  - Up to 20 consecutive events possible
  - Low power : 10 mW/ch
  - BGA package
  - HKROC is a waveform digitizer with auto-trigger and ps timing





Electronics for DRD6

- Common ASIC for time/charge measurement
  - Proposed as a service to allow detector characterization rather than electronics debugging
  - Common DAQ and easy combined tests

- Several other ASICs R/Os also developed and it is good !
  - FLAME/FLAXE, FATIC…
  - Waveform samplers : commercial or specific (SPIDER et al.)
  - DECAL

- Exchange on performance/issues inside DRD6 and DRD7

- Target (if possible) compatible I/Os : 40 MHz CK, I2C slow control, output levels…

c4. Interface with other DRDs

DRAFT, under discussion

- R&D in electronics is not carried out in isolation
  - Many engineers will be active in both DRD-specific projects and DRD7 generic R&D
  - DRD-specific projects will take care of
    - Determination of system parameters and specifications
    - Planning and costing of prototype development and production
    - Production, verification, and integration of ASICs and other project-specific components
    - Testing and operation of large-scale prototypes
  - DRD7 projects will
    - Review system specifications and design as requested, possibly also on a rolling basis during the course of the project, and including analysis of engineering effort and specialised skills requirements
    - Provision access to tools and vendors
    - Develop and provision common IP, components, and subsystems, encompassing hardware, firmware and software
    - Develop common, generic, complete components or systems, when too big or too complex to be designed in one single DRD
    - Provision specialised or large-scale facilities for electronic development and testing

Summary

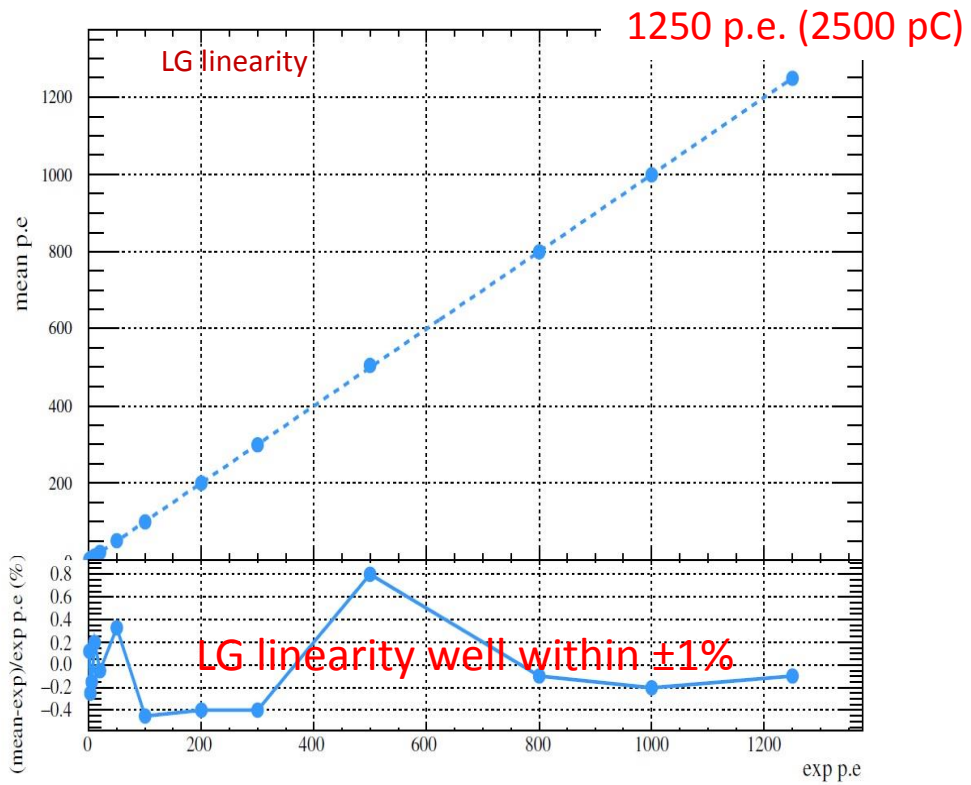
- Importance of joint optimization detector/readout electronics
- Trend to reduce power and data volume
  - Pileup will be less of an issue
- Keep open all the different R/O options
- Provide common R/O ASICs when no specific development is required

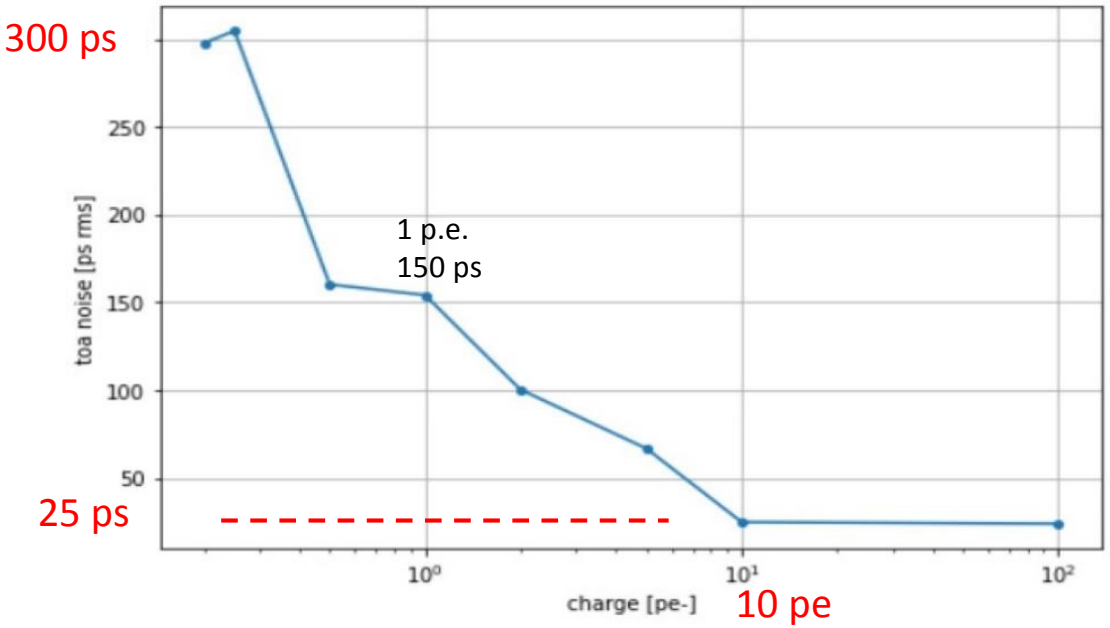
summary

backup

Main experimental results with HKROC0 – Charge and Time

- Measurement with the full chain (analog + digital and reconstruction)
  - Signal auto-triggered with threshold





Charge resolution :

< **0.1 p.e (200 fC)** at ≤ 10 p.e

< 1 % otherwise

Charge linearity < **±1%** from 1 to **1250 p.e. (2500 pC) across the 3 gains**

TDC characterization with **1/6 p.e. threshold**

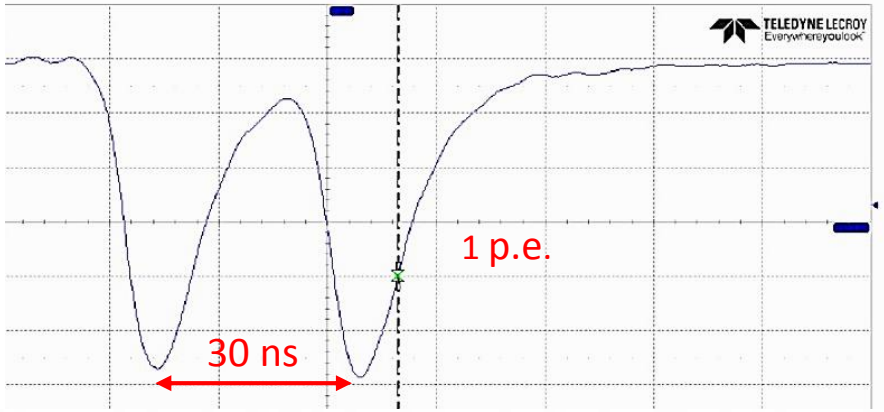
TDC resolution :

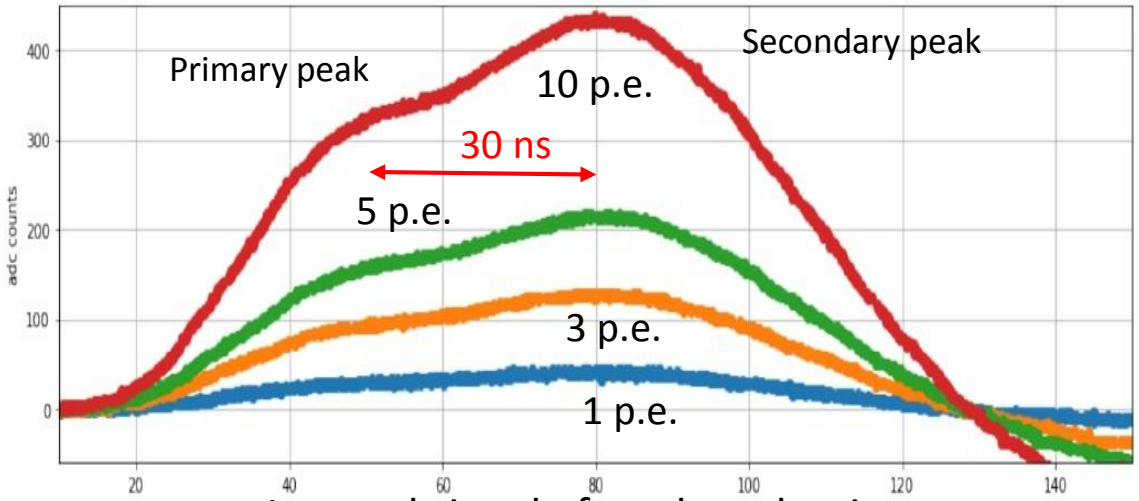
150 ps rms @ 1 p.e

≤ 25 ps rms @ 10 p.e

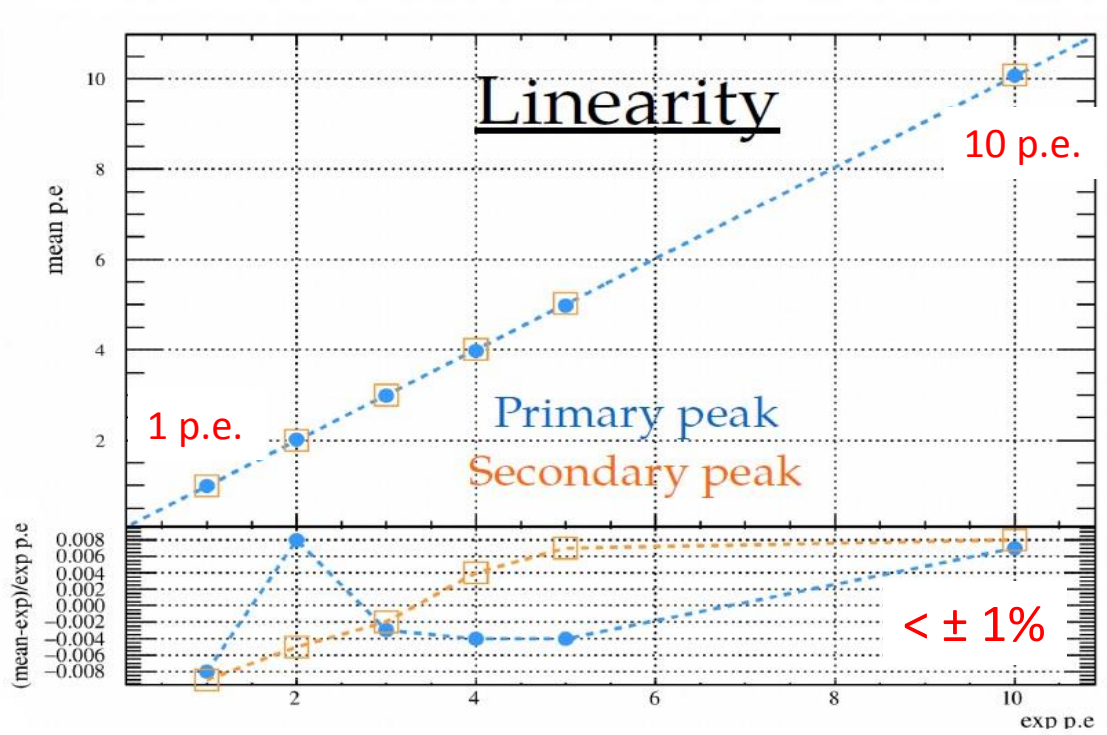
Main experimental results with HKROC0 - Pile-up

- Measurement with 2 events separated by ~30 ns (full chain: analog, digital and reconstruction)
  - Signals auto-triggered (internal prommagble threshold)





Internal signal after slow shaping

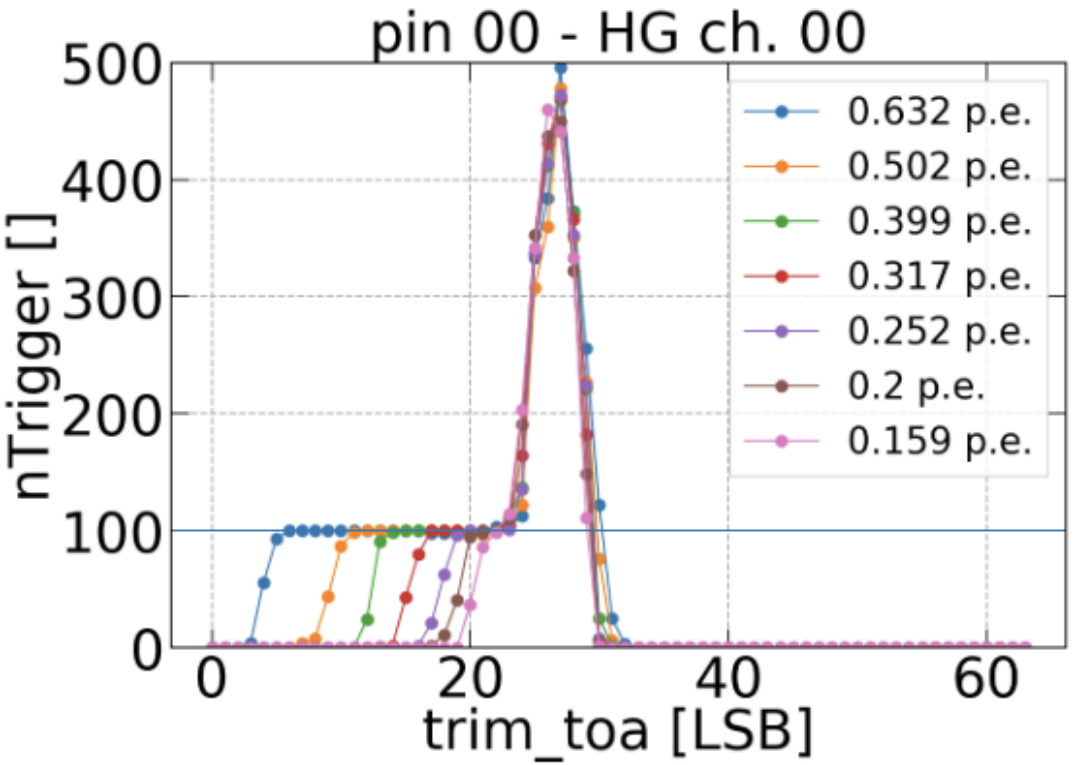


Charge reconstruction algorithm of the two peaks

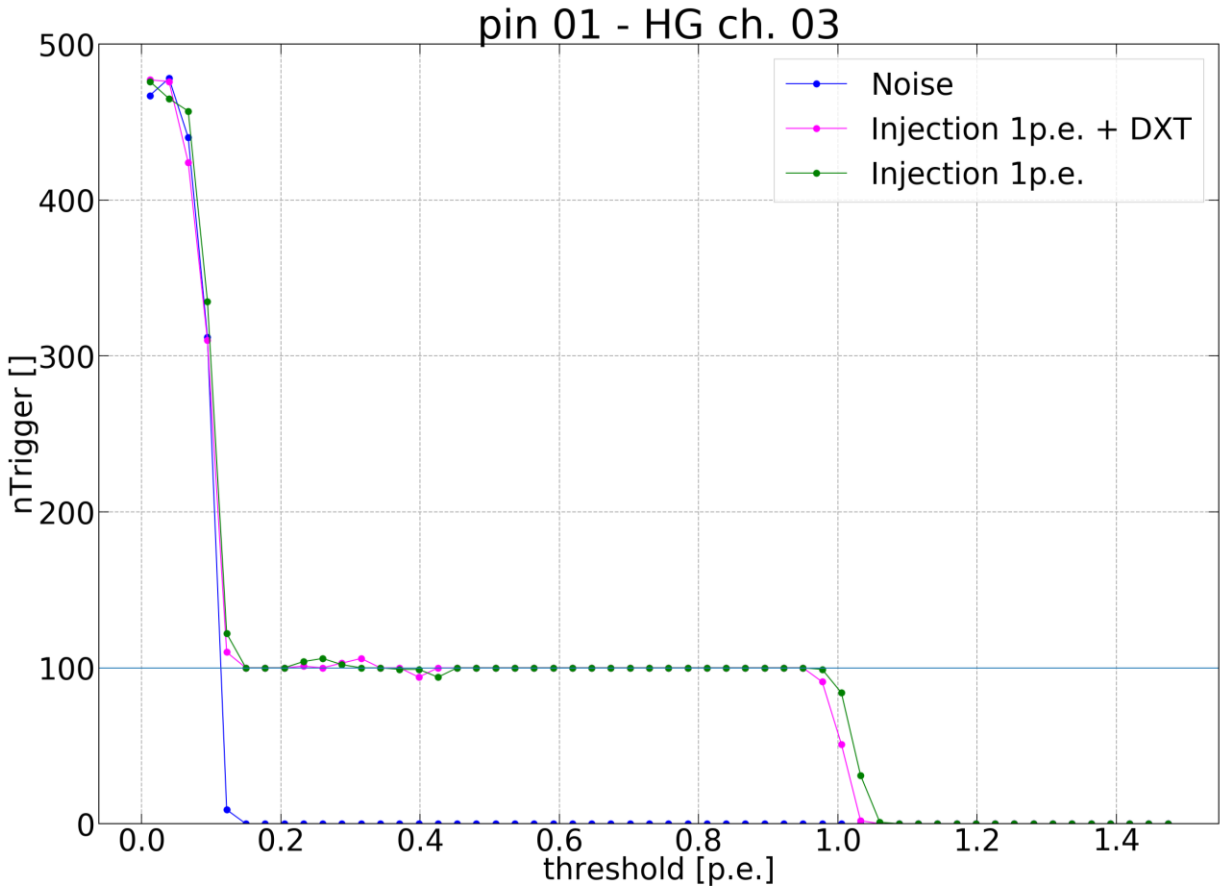
Good linearity of reconstructed pile-up events

We can reconstruct both peaks properly !

Threshold measurements with HKROC1b



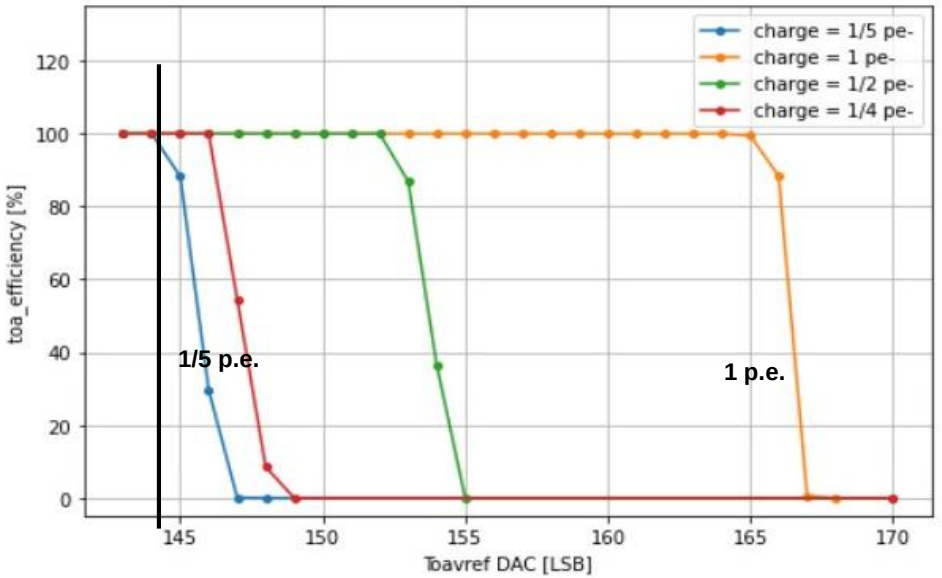
Minimum threshold of 1/6 pe



1 pe trigger efficiency with 1000 pe in another channel

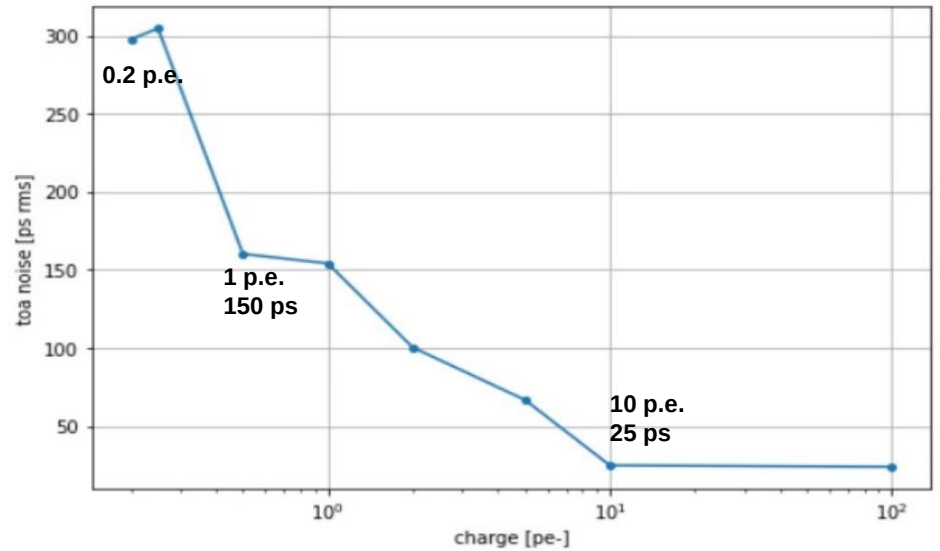
HKROC0 Trigger measurements

The HyperK specifications require the trigger **threshold** to be set at **1/6 p.e (330 fC)**



- **Hit efficiency : 90 % for 1/5 p.e events (400fC)**

  ~100 % if ≥ 1/4 p.e
- Extracted **threshold** value corresponding at **1/6 p.e**
- **Very low noise** : < 1 Hz **(0 noise hit in 10s @ 1/6 of p.e.)**



TDC characterization with **1/6 p.e. threshold**

TDC resolution :

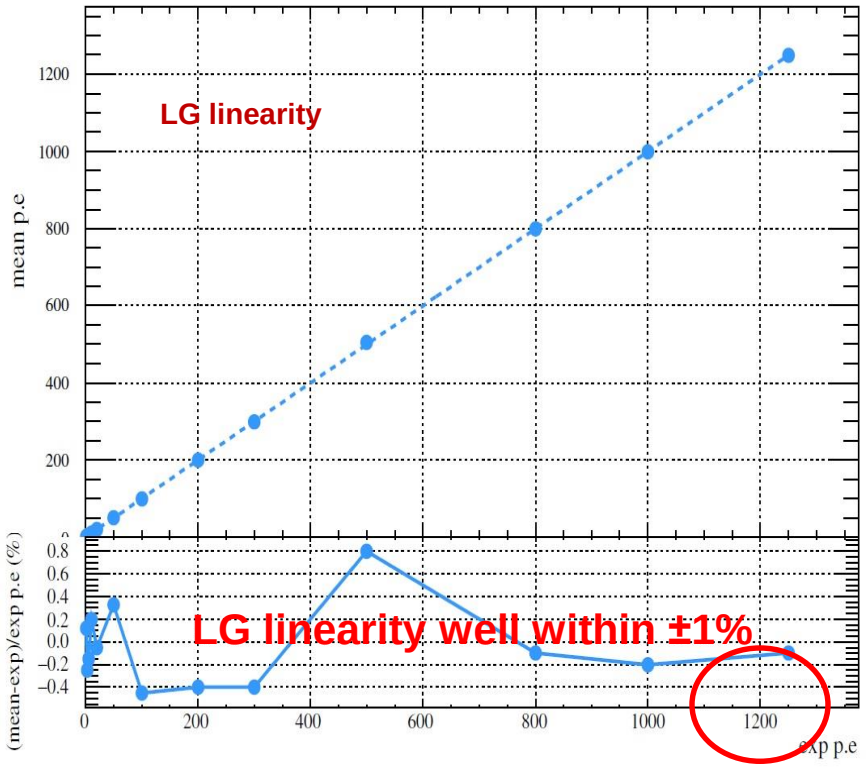
150 ps rms @ 1 p.e [300 ps required]

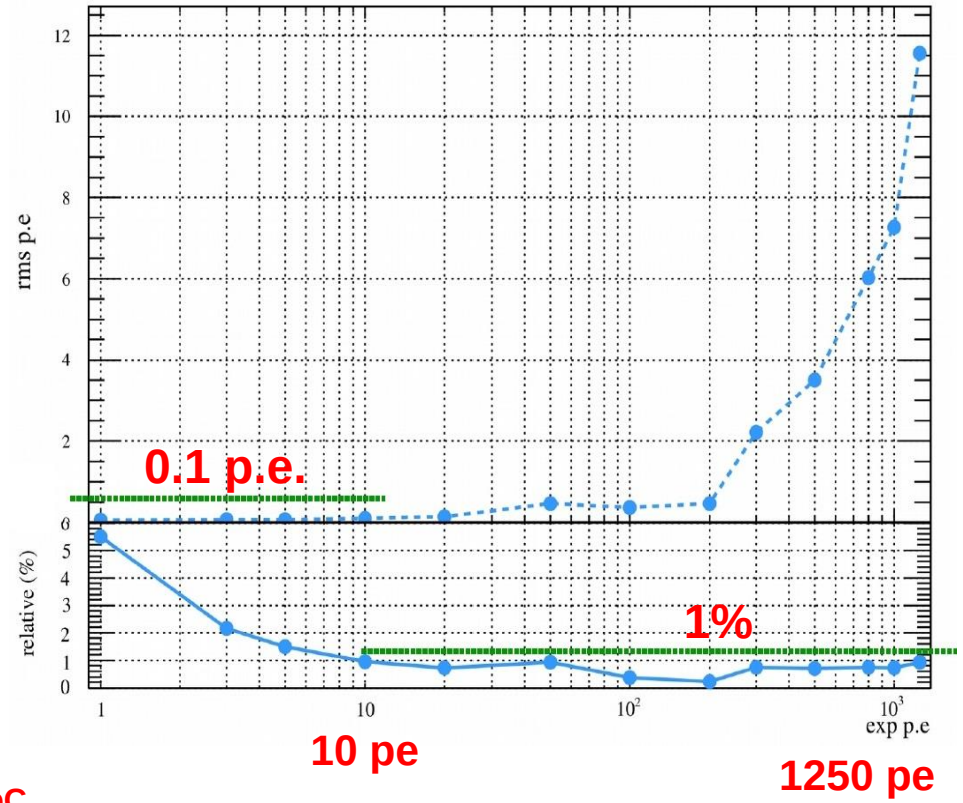
≤ 25 ps rms @ 10 p.e [200 ps required]

- Excellent agreement with HK requirements

HKROC0 Charge measurements

The **whole** acquisition **chain** is tested:
The signal is **amplified**, **auto-triggered** and **converted** by the internal **ADC**.





HG, MG and LG tested!!

Charge linearity < **±1%** from 1 to **1250 p.e. (2500 pC)**

The charge measurements Fulfill the HK requirements!!!

Charge resolution :

< **0.1 p.e (200 fC)** at ≤ 10 p.e

< 1 % otherwise