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ePixUHR-35kHz: a read-out ASIC for tender X-ray imaging at LCLS-II with 35 kHz frame-rate

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The ePixUHR-35kHz is a novel Application Specific Integrated Circuit (ASIC) developed at the SLAC National Accelerator Laboratory to meet the demanding requirements of the Linac Coherent Light Source II (LCLS-II) X-ray laser facility. The ASIC consists of an array of pixels with a pitch of 100 μm, organized into clusters of 72 pixels each. Each cluster includes a Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) operating at 8 MSPS, with digital logic to synchronize the analog and digital sections. By distributing 448 ADCs throughout the pixel array and pipelining the integration and conversion processes, the ePixUHR-35kHz achieves high frame-rates. The pixel front-end incorporates an automatic gain-switching charge integrating amplifier in each pixel, extending the dynamic range up to 104/photons/pixels/frame.

In the first prototype of the ASIC, the full-frame readout speed is constrained to 35 kHz due to the limited bandwidth of Low-Voltage Differential Signaling (total data throughput is 16 Gb/s). However, the pixel front-end and the ADCs have been designed to achieve up to a frame-rate of 100 kHz, which is the goal of the next development phase. A Region-of-Interest (ROI) logic enables characterization of such blocks at the maximum frame-rate.

ePixUHR-35kHz has been designed on a 130 nm CMOS technology and the first full-reticle size prototype with a matrix size of 192×168 pixels has been fabricated. In this presentation, we will discuss the design of the various blocks and the overall ASIC architecture. Testing of the ASIC has started in April and preliminary characterization results will be discussed. ePixUHR-35kHz represents a first significant milestone towards the development of the next generation of full-frame readout X-ray detectors for LCLS-II.

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