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P1.10: A 20 Gbps PAM4 Receiver ASIC in 55 nm for Detector Front-end Readout

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High speed optical links with high bandwidth and large data capacity have been widely used in detector front-end readout. There are NRZ (Non Return to Zero) and PAM4 (4-level Pulse-Amplitude Modulation) signal modulation formats in optical link, the NRZ also known as PAM2 has been used for decades, but PAM4 is attracting more and more attention for its doubled bandwidth efficiency compared with NRZ with the increase of data rate. The optical receiver based NRZ and PAM4 modulation formats is a key component of the optical link for converting optical signals into electrical signals. Some receivers using NRZ format have been reported, such as GBTIA[1], a 5 Gbps optical receiver has been used in high-energy physics experimental detectors, and QTIA[2], a 2.5 or 10 Gbps 4 channel array optical receiver.
As a further study, this paper presents the design and simulation results of a 20 Gbps PAM4 receiver ASIC fabricated in 55 nm CMOS technology for detector front-end readout. The 20 Gbps PAM4 receiver ASIC mainly consists of an equalizer stage, voltage shifter, 3 hysteresis amplifiers, decoder and CDR (Clock and Data Recovery). A 20 Gbps PAM4 signal will be input to the equalizer stage with CTLE (Continuous Time Linear Equalizer) structure for high frequency signal attenuation caused by PCB transmission line and parasitic parameter from bonding wires and input pads. The voltage shifter provides a voltage shift by removing common mode voltage, then the central voltage of each eye of PAM4 will be removed to zero. The 3 PAM4 signals output by the voltage shifter will be further amplified by 3 hysteresis amplifiers respectively. Three MSDFFs (Master Slave DFFs) after the 3 hysteresis amplifiers will resample the three signals and the sampling clock will be provided by the 10 GHz clock recovered by CDR. The sampled signals will be sent to decoder for processing to obtain two NRZ signals (MSB and LSB). In order to improve the quality of the output NRZ signal, the decoded signal will be resampled by the clock signal recovered by CDR.
The 20 Gbps PAM4 Receiver ASIC has been designed in 55 nm CMOS technology with the chip area of 2.2 mm × 1.6 mm. The simulation results show that two logically NRZ (MSB and LSB) data can be obtain and the jitter of eye diagram of MSB and LSB are 1.67 ps and 1.73 ps, respectively. And the jitter of clock recovered by CDR is around 1.46 ps. The chip has been taped out and the tests are planned to be conducted in this June.

[1] Menouni M . The GBTIA, a 5 Gbit/s radiation-hard optical receiver for the SLHC upgrades[J]. Twepp Topical Workshop on Electronics for Particle Physics, 2009.
[2] Sun H , Huang X , Chao C P , et al. QTIA, a 2.5 or 10 Gbps 4-Channel Array Optical Receiver ASIC in a 65 nm CMOS Technology[J]. 2021.

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