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P1.32: System for Fast Readout and Tests of Pixel IC Operating in Single Photon Counting Mode using PCIe-based FPGA

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Hybrid pixel detectors become popular in particle and photon detection techniques for many years [1]. A hybrid detector consists of two parts: a pixelated sensor (based on Si, Ge, GaAs, CZT, etc) and a readout Integrated Circuit (IC) usually containing a few tens of thousands of pixels and millions of transistors. Integrated circuits suffer from the inaccuracies of manufacturing processes and therefore they should be thoroughly tested before the bump-bonding process with the sensor.

The paper presents a highly efficient system for automated testing of IC of pixel architecture using PCI-based FPGA. Our solution is based on the Intel Arria 10 GX development kit and a Linux-powered PC connected via PCIe 8x Gen 3 interface. It has been built of well-thought-out modules connected through a set of precisely defined interconnects. This approach enabled development of an architecture that may be easily implemented in both PCIe-based systems and System-on-Chip devices such as Intel Agilex SoC. The overall architecture of the developed system is shown in Fig. 1. The presented architecture has been tested with both a manufactured integrated circuit and an FPGA RTL model [2].

During the tests with IC, we used a readout integrated circuit of pixel architecture, designed for CdTe pixel detectors used in X-ray imaging applications with moving objects. The IC core is a matrix of 192 x 64 square-shaped pixels of 100 µm pitch operating in single photon counting mode (see Fig. 2 and 3). Each pixel contains a fast analog front-end followed by 3 independently working discriminators and 3 ripple counters. Such pixel architecture allows photon processing one by one and selecting the X-ray photons according to their energy. During the data readout phase, the counter in each column forms a shift register. The data from the register is loaded, bit by bit, into the peripheral fast 192-bits registers and shifted out of the chip via 4 fast LVDS parallel lines. The peripheral area located at the bottom of the integrated circuit also contains a bandgap reference source, bias DACs, an I/O control logic, a slow control for settings the register configuration in each pixel, as well as LVDS drivers and receivers.

The test system based on FPGA allows a wide range of tests of different integrated circuits of pixel architecture (e.g. registers tests, counter tests, DAC tests, threshold scans with calibration pulses, DC offset correction, gain, and noise extraction, etc). The communication with IC can be performed with a controlled clock up to 0.8 GHz, which allows also testing the new generation of ICs equipped with SerDes interfaces operating in Gbps range. The authors acknowledge funding from the National Science for Research and Development, Poland, contract No. MAZOWSZE/0099/19.

[1] R. Ballabriga, et al., Photon Counting Detectors for X-Ray Imaging With Emphasis on CT, IEEE Trans. on Radiation and Plasma Medical Sciences, vol. 5, no. 4, pp. 422-440, July 2021.
[2] P. Skrzypiec and R. Szczygieł, Readout chip with RISC-V microprocessor for hybrid pixel detectors, Journal of Instrumentation, vol. 18, no. 1, p. C01030, Jan. 2023.

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